VIT

School of Computer Science and Engineering

Winter Semester 2023-24

Continuous Assessment Test – II

SLOT: D2+TD2

Programme Name & Branch: BCB, BCE, BCI, BCT, BDS, BKT

Course Name & Code: Computer Architecture and Organization- BCSE205L

Class Number (s): Common to all

Exam Duration: 90 Min.

Maximum Marks: 50

General instruction(s): Answer all five questions

Q. No.	Question	Max Marks
1.	A program runs in 10 seconds on computer X with 2 GHz clock. Assume that the Computer Y runs the same program in 6 seconds, then compute the following: i)What is the number of CPU cycles on computer X ? ii) If computer Y requires 10% more cycles to execute program when compared to computer X, then what is the clock rate for computer Y? iii) Assume the computer Z is running with clock rate of Y and the number of clock cycles as X, then find the CPU time of Computer Z. iv) Identify the fastest and slowest machine among X, Y and Z. v) Assume that the computer A executes 3 million instructions in the CPU time of the fastest Computer among X, Y and Z, determine MIPS.	10
2.	A computer employs RAM chips of 1024 x 8 and ROM chips of 1024 x 8. The computer system needs 2k *8 bytes of RAM, 2k *8 bytes of ROM, and four interface units with four registers in each. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers. a. How many RAM and ROM chips are needed? b. Draw a memory-address map for the system. c. Give the address range in hexadecimal for RAM, ROM, and interface. d. Develop a chip layout for the above said specifications.	10
3.	Consider a 2-way set associative cache memory with total 8 cache lines and a main memory with 128 blocks. Assume that the cache is initially empty. Which memory references will be present in the cache if optimal cache block replacement policy is used with the following sequence of memory references? Compute the Hit ratio (H) and Miss ratio (M). Memory references are: 5, 2, 3, 7, 3, 15, 14, 2, 1, 21, 13, 72, 12, 5, 19, 3, 2, 1, 22, 9, 26, 10, 5, 1, 7, 26, 14, 9, 19, and 26.	10
4.	a) A hard disk with a transfer rate of 10 Mbytes/seconds is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation? b) Discuss the functionality of interfaces in I/O subsystem with neat diagram.	10 (5+5)
5.	a) Consider a byte addressable memory of 64 Bytes with 4 way high-order interleaved. Identify the following i) If the CPU generates 101100 main memory address, then identify the bits required to select the module and the bits required to select the specific location in the selected module. Also mention the selected module and specific location in the selected module for the above mentioned address. ii) Sketch the structure of the above interleaved main memory. b) Explain different phases of instruction cycle with neat sketch. Describe the various CPU registers involved for the completion of each instruction execution.	10 (5+5)

Course name & code : BITE301L & Computer Architecture and Organization

Class Number (s) : VL2023240503717, VL2023240503759, VL2023240503768

Faculty Name (s) : Dr.Meenatchi S, Dr.Praveen kumar Reddy, Dr.Balasubramani M

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):-

Q. No.	Questions	Max Marks
1.	A computer employs RAM chips of 512 x 8 and ROM chips of 1024 x 8. The computer system needs 1024 x 16 of RAM, 1024 x 16 of ROM and two interface units with 256 registers each. a) Calculate the design parameters. [3 marks] b) Design a memory-address map for the above system. [3 marks] c) Show the chip layout for the above design. [4 marks]	10
2.	Design a cache with the following properties: • Size of Data words is 32 bits • A cache block will contain 2048 bits of data • The address supplied from the CPU is 32 bits long • There are 2048 blocks in the cache. Represent the number of bits in offset, index and tag, if we make our cache Direct mapped, 2-way set-associative and 4-way set-associative. [3+3+4 Marks]	10
3.	(i) Consider a system with 8-bit addresses and 16-byte pages. A process in this system has 4 logical pages, which are mapped to 3 physical frames in the following manner: logical page 0 maps to physical frame 2, page 1 maps to frame 0, page 2 maps to frame 1, and page 3 is not mapped to any physical frame. The process may not use more than 3 physical frames. On a page fault, the demand paging system uses the LRU policy to evict a page. The MMU has a TLB cache that can store 2 entries. The TLB cache also uses the Optimal policy to store the most recently used mappings in cache. Now, the process accesses the following logical addresses in order: 7, 17, 37, 20, 40, 60. a) Indicate whether the above accesses would result in a page fault. Assume that the TLB cache is empty before the access begin. [3 marks] b) Give the page number associated with the memory access that leads to page fault. [1 mark] c) Which page under LRU would be replaced with the page which caused the page fault? [1 mark] (ii) Represent -13.275_{10} and 12.48_{10} in double precision IEEE-754 format.	5 5
4.	A computer program involves multiplying two signed numbers (stored as 8 bit) -21 and +17. Illustrate how this operation would be handled by Booth's algorithm.	10
5.	Perform division operation on the operands: dividend = -27 and divisor = + 22 using restoring division algorithm. Show the contents of the quotient and remainder registers during the operations.	10

VIT

Vellore Institute of Technology

School of Computer Science and Engineering

Winter Semester 2023-2024 Continuous Assessment Test – I

Program Name & Branch: BCB, BCE, BCI, BCT, BDS, BKT **SLOT: D2+TD2**

Course Name & code: Computer Architecture and Organization- BCSE205L

Class Number (s): Common to all

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Answer all five questions

Q.No.	Question	Max Marks
1.	List out the various registers of IAS machine and write the significance of each register. Also demonstrate an assembly code using IAS instructions for the following expression: C=(A+B)/D Assume the inputs are available in the memory locations 101 onwards. Store the result in memory location 104 onwards.	10 [5+5]
2.	a. Draw the flowchart for Booth's algorithm. b. Perform Booth's multiplication for the given numbers -15 and 6 (i.e. -15×6). Description of each step is expected.	10 [4+6]
3.	a. Explain the IEEE 754 floating-point representation. b. Perform the division for the given numbers 21 and 4 (*i.e.* 21/4,) using non-restoring algorithm. Description of each step is expected.	10 [4+6]
4.	a. Discuss the instruction types of IAS machine with suitable example? b. Describe the functional components of a computer with a neat diagram?	10 [5+5]
5.	Write the assembly code for the given arithmetic statement. A= (B+C) *D using 0,1,2 and 3 address instructions and compute memory traffic for 0,1,2 and 3 address machines. Assuming the following fields: addresses - 2 bytes, data values -2 bytes, opcode -8-bits and word length -1 byte.	10 [5+5]

VIT

Vellore Institute of Technology

School of Computer Science and Engineering

Winter Semester 2023-2024 Continuous Assessment Test – I

Program Name &Branch: BCB, BCE, BCI, BCT, BDS, BKT Slot: S1+TD1

Course Name & code: Computer Architecture and Organization- BCSE205L

Class Number (s): Common to all

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Answer all five questions

Q.No.	Question	Max Marks
1.	Write an Assembly language programming for the following expression using the IAS computer Instruction set and interpret the flow of the IAS computer (Register flow of operations) R = P – Q Assume the memory locations 800, 801, and 802 for P, Q, and R respectively.	10
2.	a. Show the bit pair recoded table for three-bit combinations. (3 Marks) b. Perform the multiplication with the numbers -12 and 6(i.e.-12*6) using the Modified Booth's algorithm. (7 Marks) Description of each step is required.	10
3.	a. Identify the most widely used signed number representation among the available representations. Justify your answer. (3 Marks) b. Perform the division with the numbers 14 and 6 (ie. 14/6,) using the restoring algorithm. (7 Marks) Description of each step is required.	10
4.	a. Compare and Contrast RISC with CISC (5 Marks) b. Perform arithmetic shift right operations one time on the following decimal number. (i) 13 (ii) 27 (5 Marks) Represent the above numbers in 8-bit binary form	10
5.	a. Evaluate the following expression in 3-address and 2-address instruction formats. (4 Marks) A = (B * C) + (D * E) b. Elucidate various addressing modes with examples. (6 Marks)	10