Design of an Analog LDO Regulator in SCL 180nm CMOS Technology

EE: 660 Power Management IC Design | Prof. Madhav Pathak

Sushant Gudmewar | 22110264

This report presents the design and analysis of a Low Dropout (LDO) Voltage Regulator implemented in SCL 180nm CMOS technology for power management applications. The regulator operates with an input voltage (Vin) of 1.8V and delivers a regulated output voltage (Vout) of 1.6V, supporting a load current range of 20 mA (light load) to 100 mA (full load) with a nominal load of 50 mA. The design is optimized for high efficiency, low DC error, and robust transient response, ensuring minimal overshoot, undershoot and fast settling time. The regulator operates with a 1.8V supply voltage, a 1V reference voltage, and utilizes a 1µA current source for biasing.

Miller compensation is employed to maintain stability across different operating conditions. This technique improves phase margin and enhances frequency response by introducing a compensation capacitor (Cc) between the output of the error amplifier and its input, thereby extending the bandwidth and increasing the phase margin. The regulator consists of a pass transistor, an error amplifier (OTA), and a feedback network.

Circuit Diagram

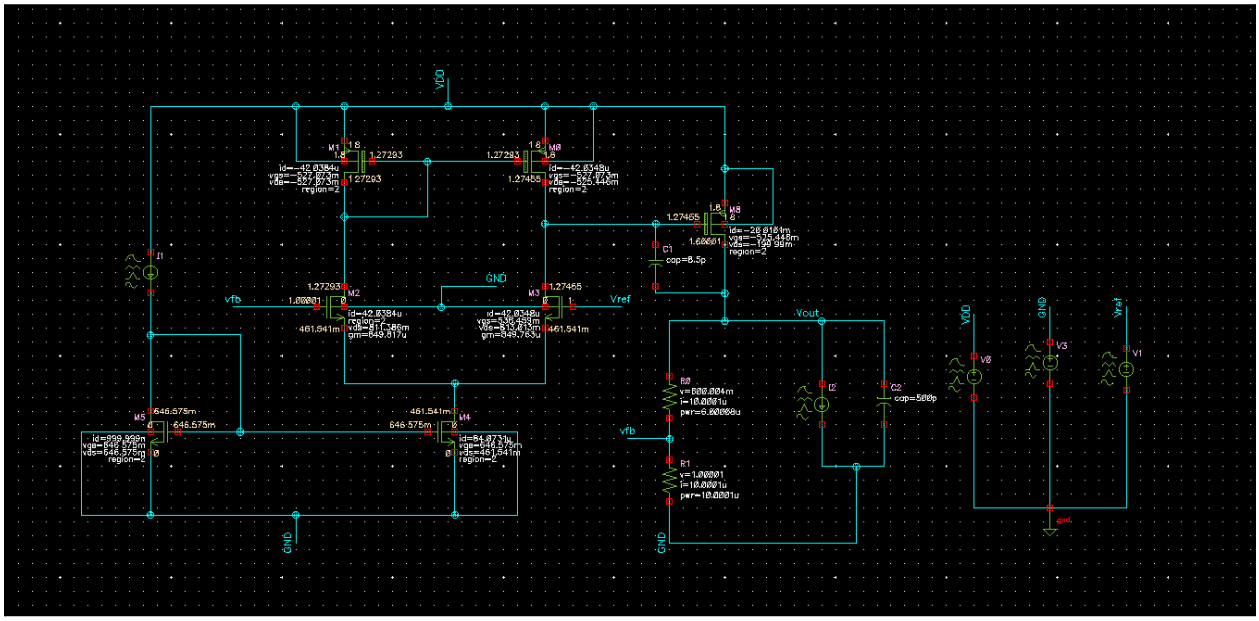

Fig 1. Schematic of LDO

Sr. No	Transistor	W (µm)	L (µm)	m	V_{ov} (mV) (At 50mA)	gm (µS) (At 50mA)
1	Pass (M8)	100	0.18	200	66	701.09×10^{3}
2	M2	8	1	10	17.427	848.79
3	M3	8	1	10	17.644	850.539
4	M0	8	1	12	114.774	555.318
5	M1	8	1	12	114.77	553.743
6	M4	6	5	7	269.192	584.293
7	M5	0.525	5	1	283.814	6.632

Table 1. W/L ratios of Transistors

Components Used

Sr. No.	Component	Value
1	R0	60 KΩ
2	R1	100 KΩ
3	I1	1 µA
4	C1	8.5 pF
5	C2	500 pF
6	V1	1 V
7	V3	1.8 V

Table 2. Component Parameters

Sizing of Transistors

a. For Pass Transistor (PMOS) Sizing

$$I_D = \frac{1}{2} k_p \frac{W}{L} (V_{SG} - V_{th})^2 = \frac{1}{2} k_p \frac{W}{L} (V_{ov})^2$$

$$k_p \approx 50\ \mu \frac{A}{V^2}, V_{ov} = 0.2\ V, I_D = 100\ mA$$

$$\frac{W}{L} = 100,000$$

$$L = 0.18\ \mu m,\ W = 18,000\ \mu m$$

b. Settling time should be less than 1 μs

$5 * \tau = settling\ time, \therefore \tau = 0.2\ \mu s$

$\therefore BW = 5\ MHz \quad (\because \tau = \frac{1}{BW})$

$\omega_{ugb} = gm_1/(Cc + Cgg)$

$Using\ Cc = 5\ pF,\ Cgg \approx 25pF$

$\therefore gm_1 = 942.47\ \mu S$

Here gm_1 is the transconductance of M2

c. Efficiency at Full Load should be greater than 88.78%

$\eta = Pout/Pin = (Vout * Iout)/(Vin * (Iout + Iq))$

$Iq = 122\ \mu A$

- Sizing of NMOS differential Input Pair

$gm_1 = \frac{2 * I_D}{Vov}$

$Using\ I_D = 50\ \mu A;\ Vov \approx 0.15\ V$

$k_n \approx 270\ \mu \frac{A}{V^2}$

$I_D = \frac{1}{2} k_n \frac{W}{L} (V_{ov})^2$

$\frac{W}{L} = 16$

- Sizing of PMOS current mirror

$I_D = \frac{1}{2} k_p \frac{W}{L} (V_{ov})^2$

$Using\ I_D = 50\ \mu A;\ Vov = 0.2\ V$

$\frac{W}{L} = 50$

- Sizing of Current Mirror

$1\ \mu A\ to\ 100 \mu A.\ W/L\ of\ tail\ transistor\ should\ be\ approximately\ 100\ times\ that\ of\ M5.$

$For\ tail\ transistor,$

$I_D = \frac{1}{2} k_n \frac{W}{L} (V_{ov})^2$

$Using\ V_{ov} = 0.3V,\ \therefore \frac{W}{L} = 8.23$

$\therefore (\frac{W}{L})_{M5} = 0.0823,\ but\ Minimum\ W = 0.22\ \mu m, so\ L = 5\ for\ both\ M5\ and\ M4$

Frequency Response Summary

Load (mA)	Gain Margin (dB)	Phase Margin (Deg)	f_{ugb} (MHz)	Loop Gain (dB)
20 *(Light Load)*	17.2009	60.3341	5.18212	72.54
50 *(Nominal Load)*	20.8103	64.4024	5.02683	70.24
100 *(Full Load)*	23.616	67.4071	4.64076	65.92

Table 3. GM, PM, Bandwidth and Loop Gain

Frequency Response Plots

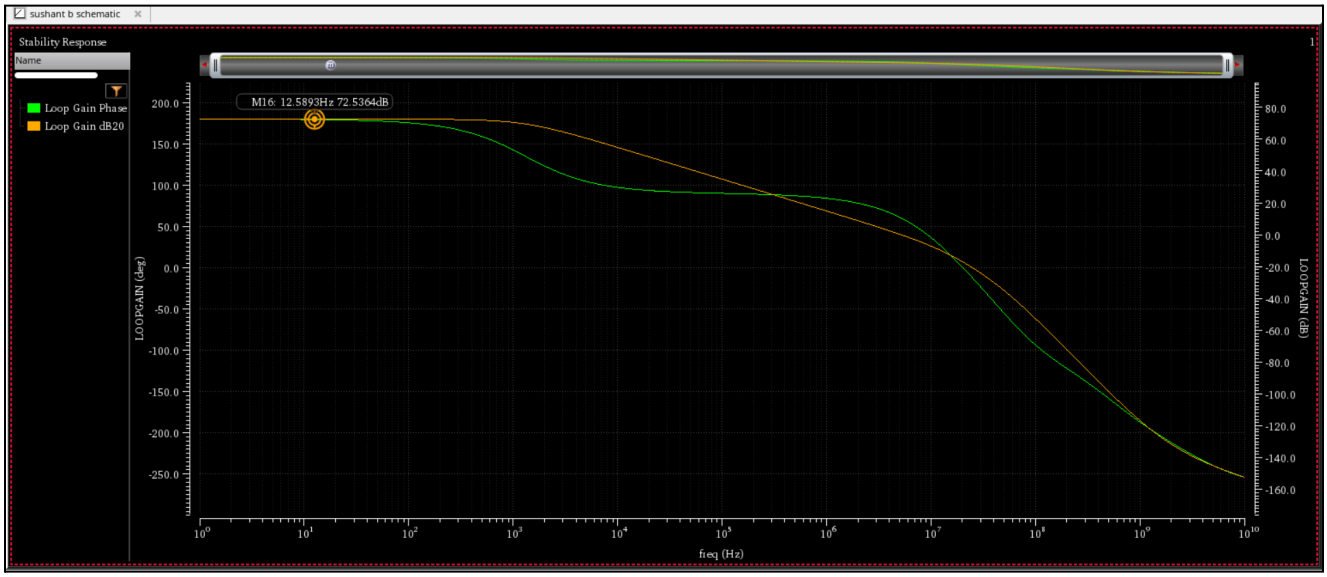

Fig 2. Stability Response at Light Load Condition

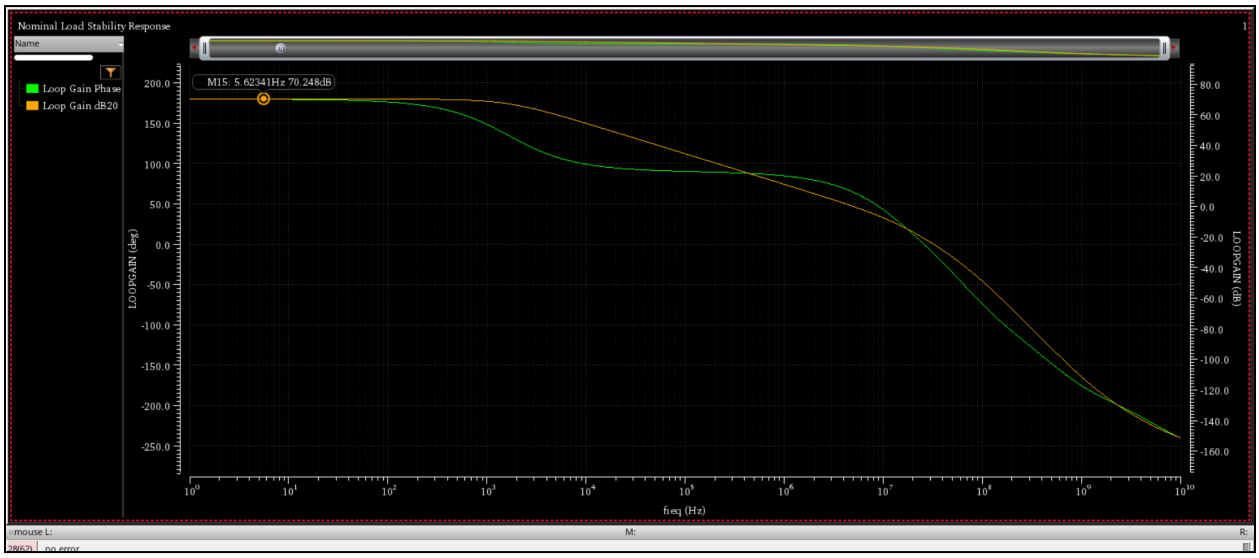

Fig 3. Stability Response at Nominal Load Condition

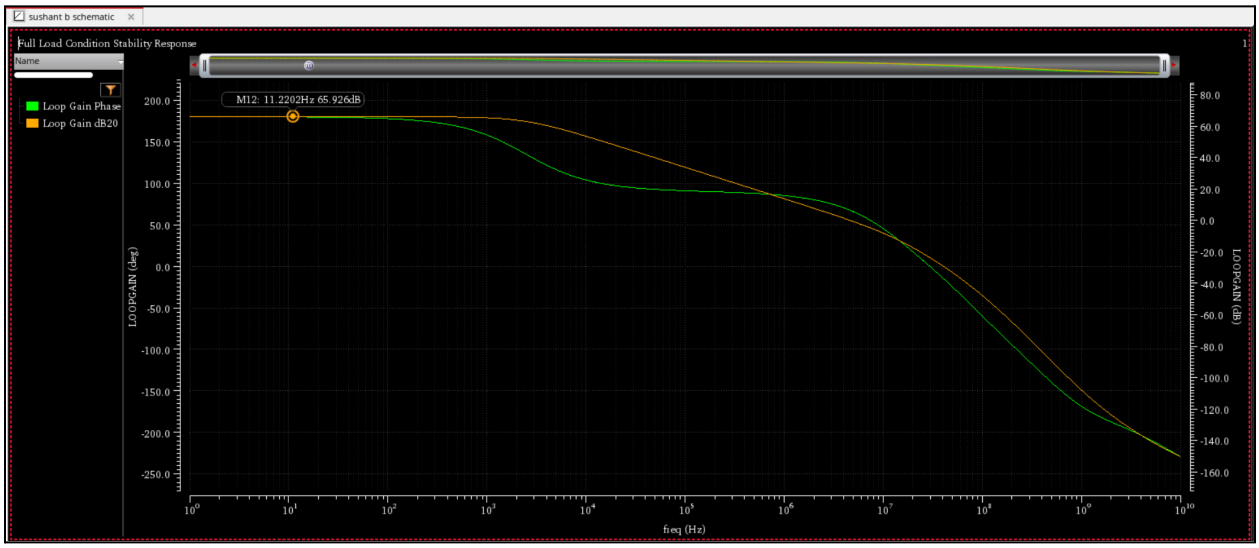

Fig 4. Stability Response at Full Load Condition

Transient Response

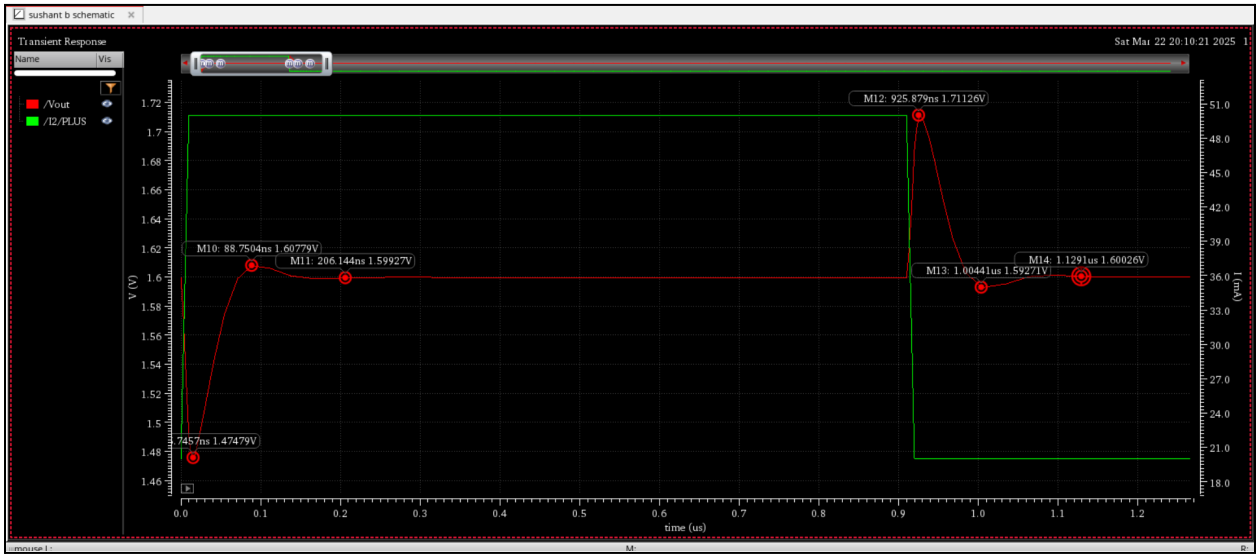

Figure 4: Transient Response to a Step Change in Load Current

Transition	Overshoot	Undershoot	Settling Time
20 $mA \rightarrow$ 50 mA	-	125.21 mV	0.2 μs
50 $mA \rightarrow$ 20 mA	111.26 mV	-	0.2 μs

Table 4. Transient Response Parameters for Load Current Step Change

Power Consumption

Block	Power Consumption (μW)		
	Nominal Load	**Light Load**	**Full Load**
Feedback	15.99	16	15.98
OTA	152.20	151.98	151.97
Pass Transistor	10.02×10^3	4.00×10^3	20.07×10^3

Table 5. Block-wise Power Consumption Under Different Load Conditions

Efficiency

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}\ I_{out}}{V_{in}\ I_{in}}$$

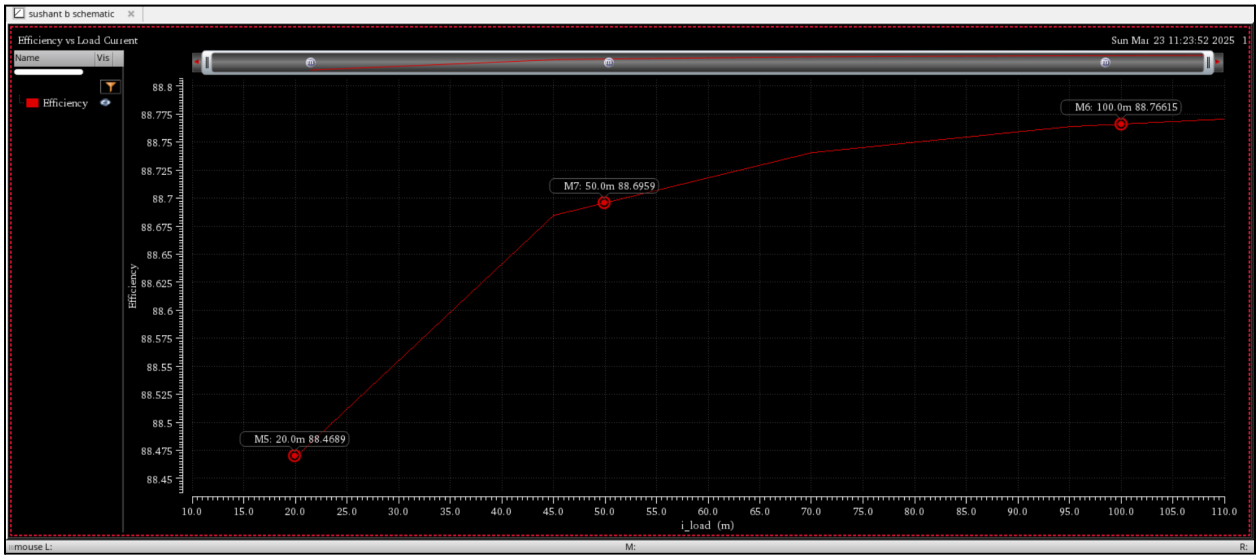

Figure 5: Efficiency across load range

Load Regulation

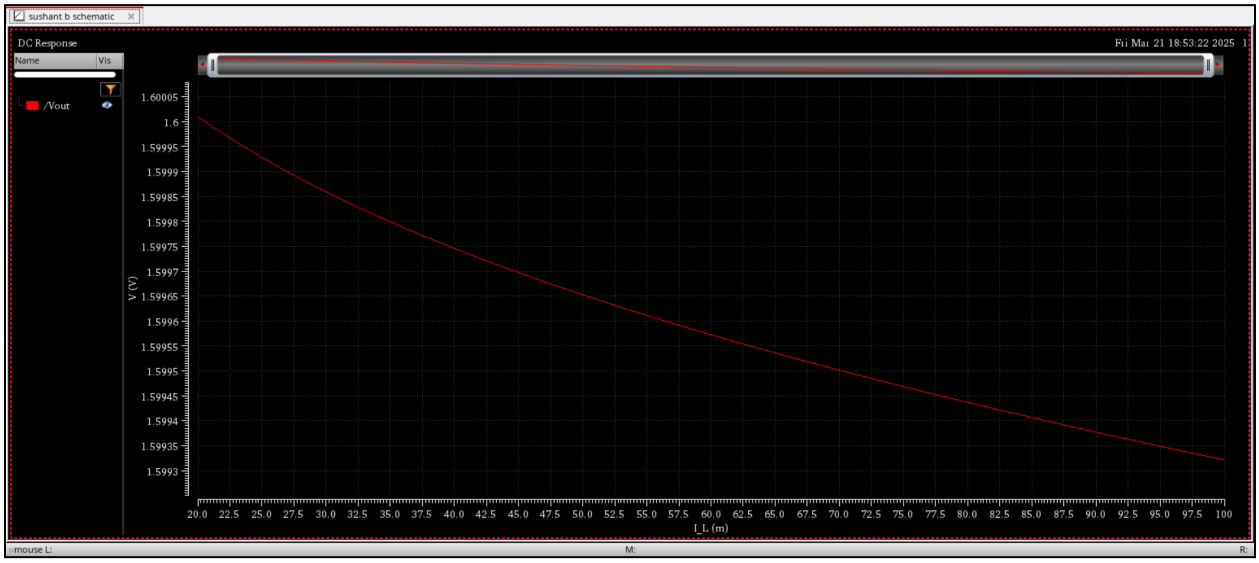

Figure 6: Load Regulation from Light Load to Full Load

– $Load\ Regulation \leq 0.045\%\ of\ Vout$

Line Regulation

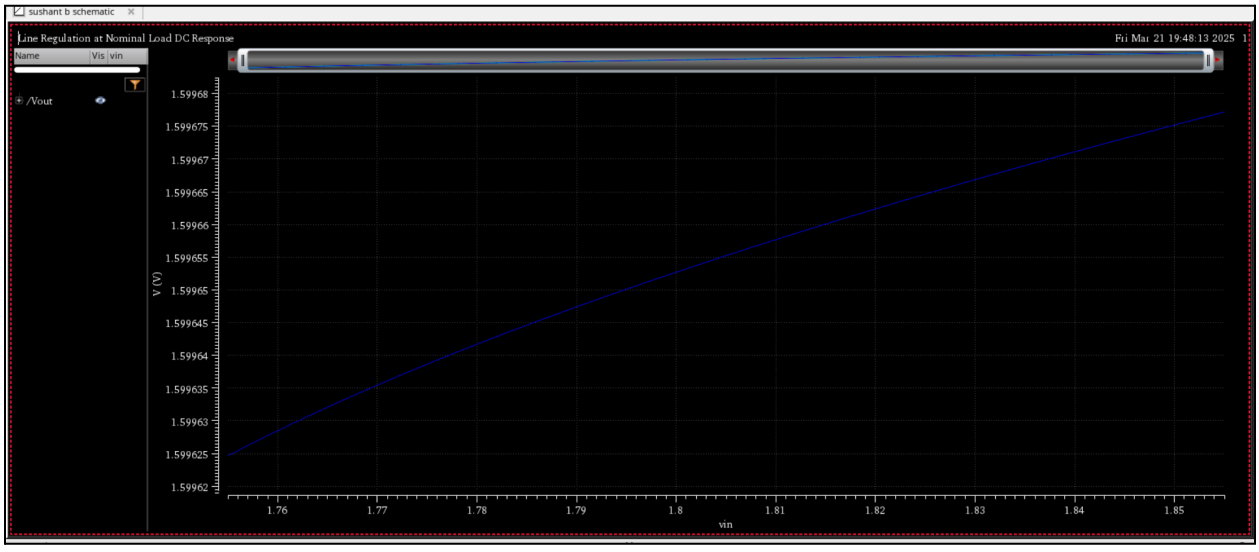

Figure 7: Line Regulation at Nominal Load

– $Line\ Regulation \leq 0.025\%\ of\ Vout$

Power Supply Rejection Ratio

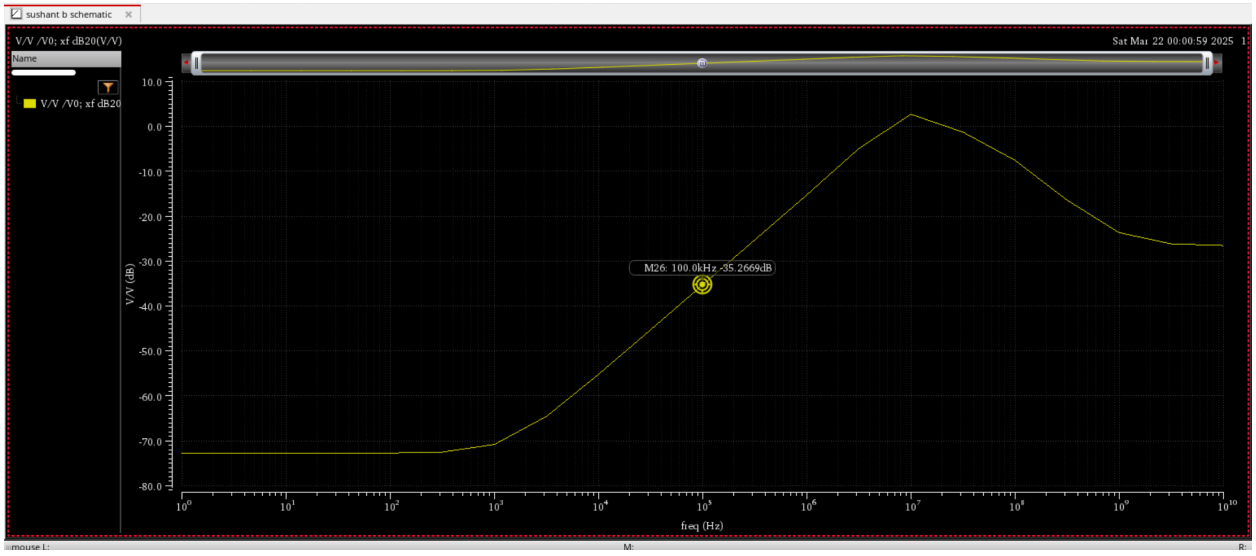

Figure 8: Power Supply Rejection Ratio

$PSRR = \ -35.2669\ dB\ at\ 100kHz$

Sr. No	Parameter	Performance
1	Efficiency	$\geq$ 88.46% across load range
2	Phase Margin	$\geq$ 60° across load range
3	Load Regulation	$\leq$ 0.045% across load range
4	Line Regulation	$\leq$ 0.025% for $\pm$2.5% input voltage variation
5	PSRR	-35dB at 100 KHz
6	Transient Response	Overshoot/Undershoot $\leq$130mV
		Settling Time $\leq$ 250ns

Table 6. LDO Voltage Regulator Performance Summary