3T RRAM for Multibit Storage in In - Memory Computing

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AGENDA

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- RRAM Fundamentals
- 3T RRAM
- Multi-bit RRAM Concepts
- Project Goal & Scope
- Implementation Details (Model, Cell, Array)
- Simulation Results
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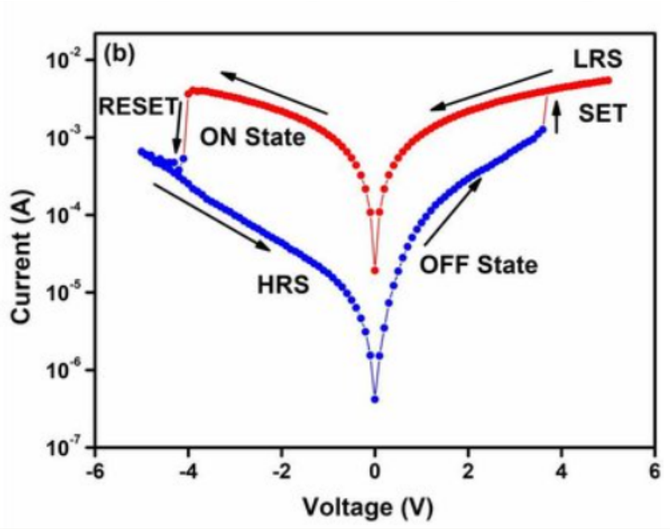
Introduction & Motivation

- **Computing Challenge**: Traditional architectures like Von Neumann face bottlenecks due to data movement, especially critical for modern AI & Big Data workloads.
- **RRAM as Solution**: Offers low-power, non-volatile memory with unique potential for In-Memory Computing (IMC).
- **IMC Advantage**: RRAM crossbars enable efficient Matrix Multiplication directly within memory, drastically reducing data transfer overhead.
- **Why Multi-bit?**: Storing multiple levels per cell boosts density and allows for more precise analog value representation needed for advanced IMC.

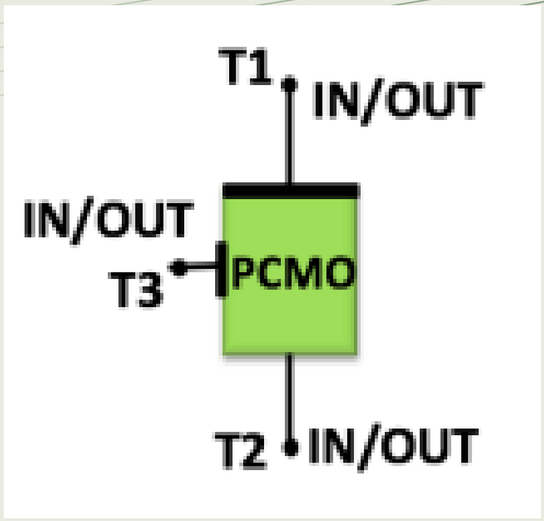
RRAM Fundamentals

- **Device Basics:** RRAM is a 2-terminal memory (Metal-Insulator-Metal) where data is stored as resistance states (High/Low).
- **Switching Mechanism:** Resistance is changed by applying voltage to form (SET) or rupture (RESET) tiny conductive filaments within the insulator.
- **Key States:** SET operation switches the device to a Low Resistance State (LRS); RESET switches it to a High Resistance State (HRS).
- **Electrical Signature:** Device behavior is shown by a characteristic I-V hysteresis loop, clearly indicating LRS, HRS, and switching voltages.



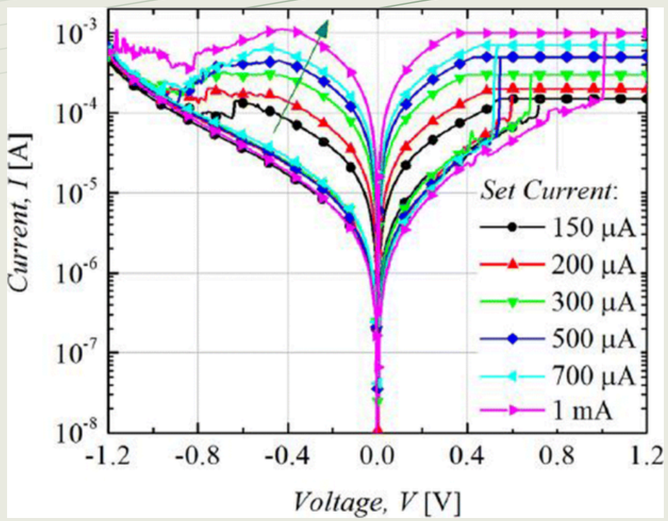
3T RRAM

- **Device Basics:** 3T RRAM has V_{input} at two terminals and R_{out} at the third terminal.
- **Advantage:** Single cycle, single device IMC
- Unlike 2T RRAM, which takes 3 cycles (initialisation, compute, read) to perform IMC; 3T RRAM takes a single cycle.
- No extra cycle for read.
- Less energy consumption and can provide significant results in large scale IMC



Multi-bit RRAM Concepts

- **Goal:** Store multiple distinct resistance levels (Intermediate Resistance States - IRS) between the standard LRS and HRS in a single cell.
- **How:** Achieved by precisely controlling filament properties during programming (e.g., using current limits, specific voltage pulses - briefly mention your method).
- **Advantages:** Significantly increases storage density and provides efficient representation for analog values (like AI model weights).
- **Challenges:** Ensuring stability of intermediate states, managing variability between devices/cycles, and requiring precise control circuitry.



Project Goal & Scope

- **Overall Aim:** To design and simulate a 3T multi-bit RRAM crossbar array performing Vector-Matrix Multiplication (VMM) using Cadence tools.
- **Key Demonstrations:** Characterize single-cell switching, show multi-level programming/readout via simulation, and verify VMM operation on the array.
- **Simulation Focus:** Design 3T multi-bit RRAM memristor to simulate I-V characteristics and transient array behavior.
- **Application:** Project involves simulation of a 3x3 matrix multiplication

Implementation Details

Resistance States

- State 1: R1 = 250 Ω (Low resistance state)
- State 2: R2 = 500 Ω (Intermediate resistance state 1)
- State 3: R3 = 1000 Ω (Intermediate resistance state 2)
- State 4: R4 = 10000 Ω (High resistance state)

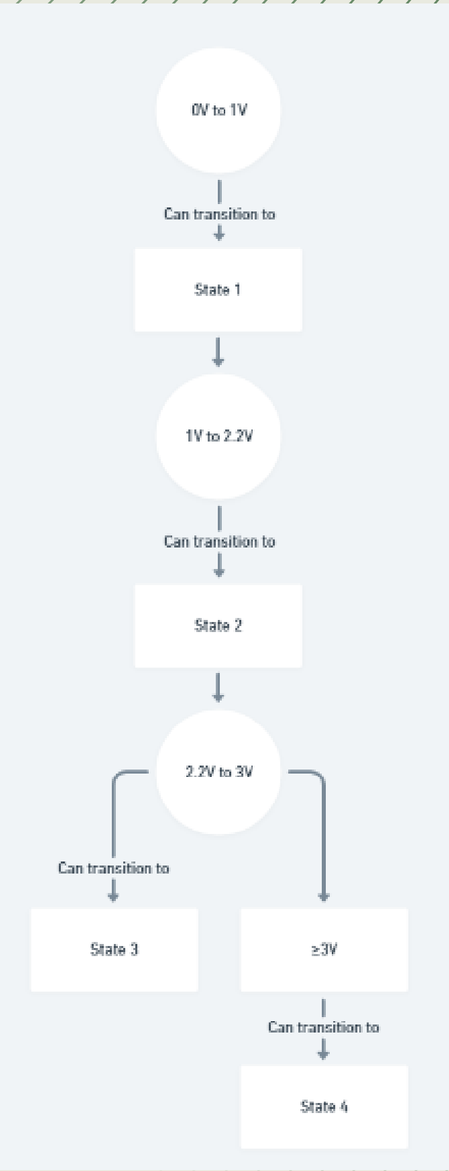
State Transition Rules

- Positive voltage transitions: State can only increase (or stay the same)
- Negative voltage transitions: State can only decrease (or stay the same)
- Initial state parameter: init_state = 1

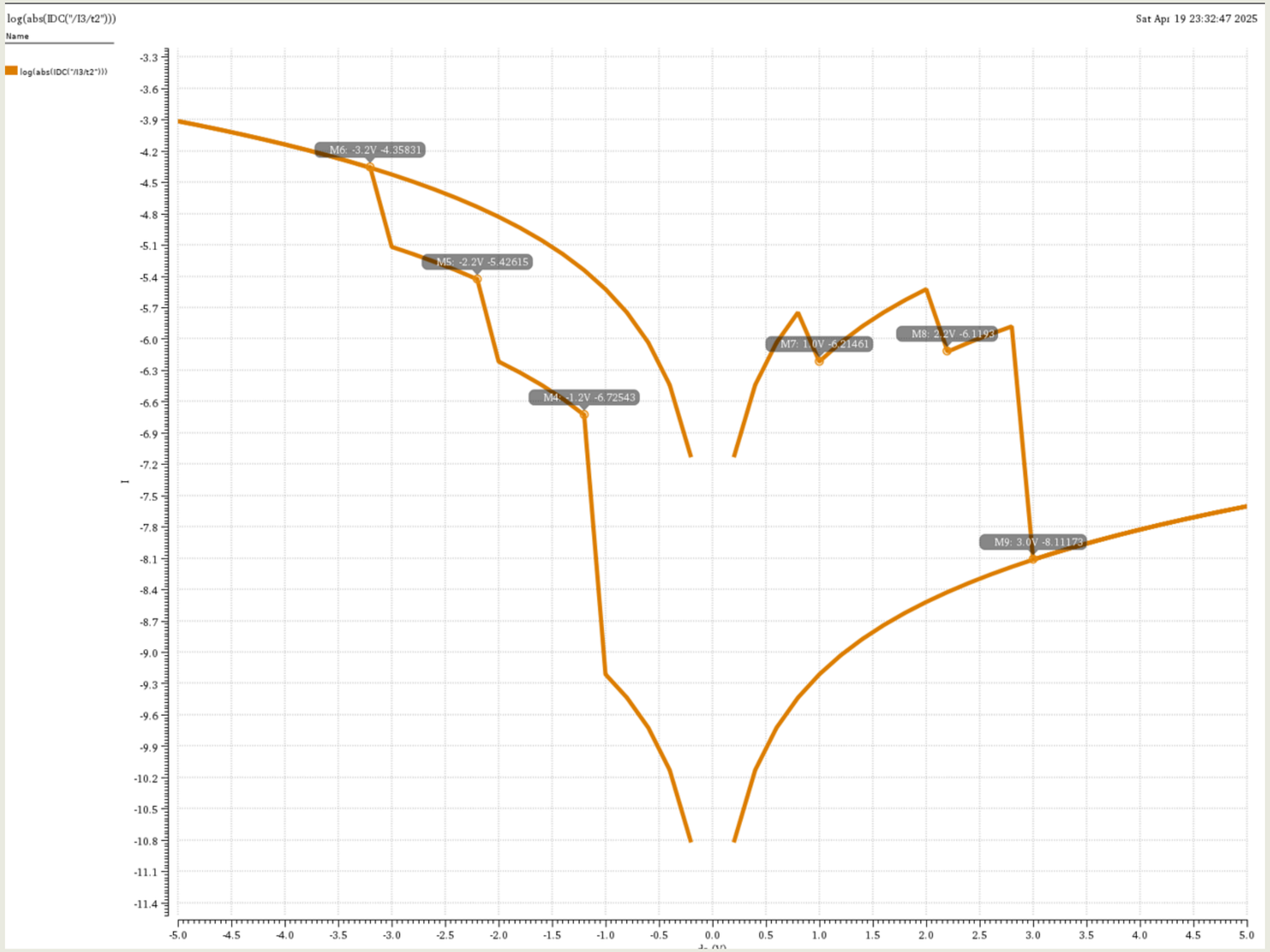
Implementation Details

Set/Reset Voltage Thresholds

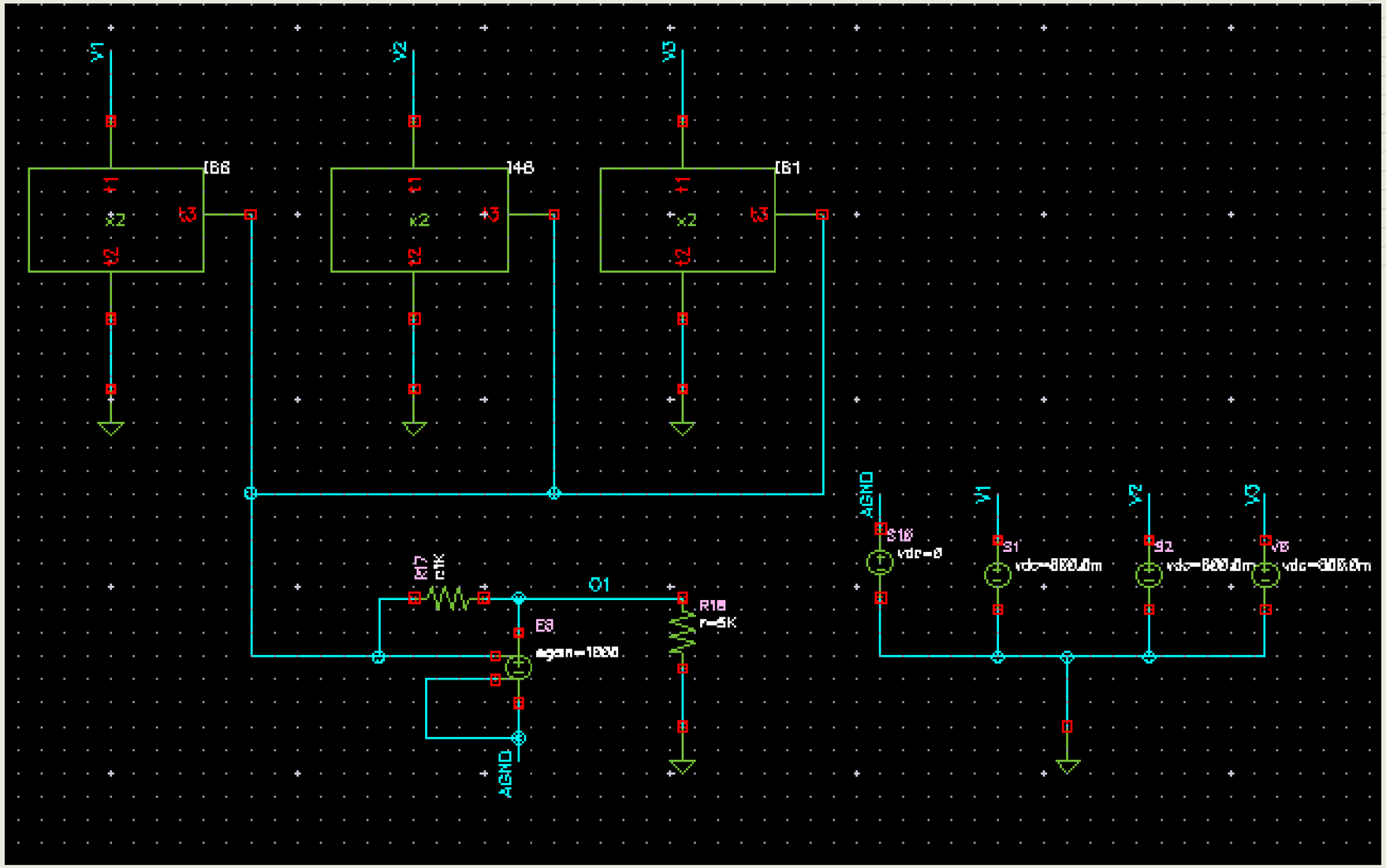
- **Positive Programming (SET operation - incremental resistance increase):**
  - 0V to 1V: Can transition to State 1
  - 1V to 2.2V: Can transition to State 2
  - 2.2V to 3V: Can transition to State 3
  - ⩾3V: Can transition to State 4
- **Negative Programming (RESET operation - decremental resistance decrease):**
  - 0V to -1V: Can transition to State 4
  - -1V to -2.2V: Can transition to State 3
  - -2.2V to -3V: Can transition to State 2
  - ⩽-3V: Can transition to State 1



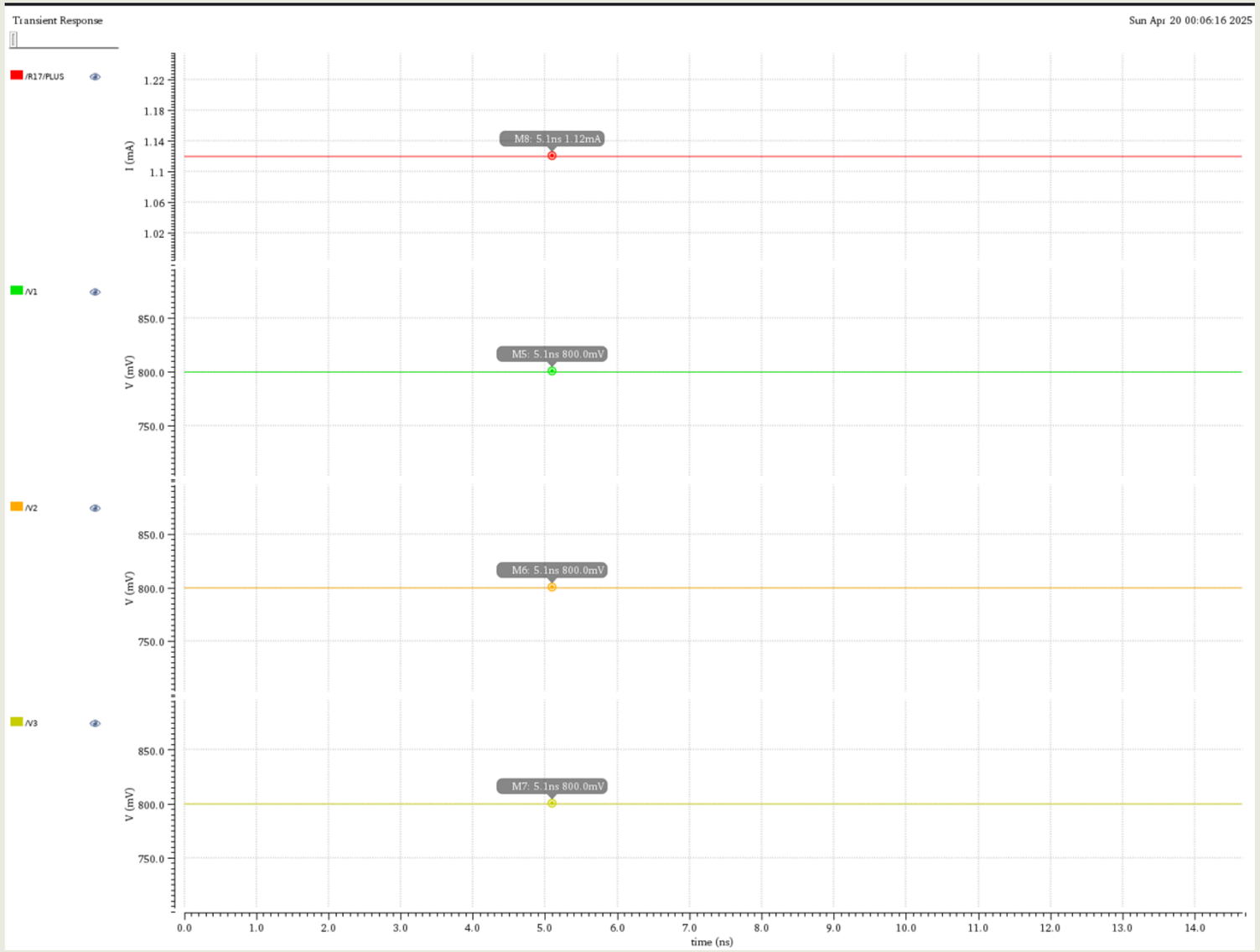
2 bit RRAM IV curve



Single MAC unit



Output of single MAC unit

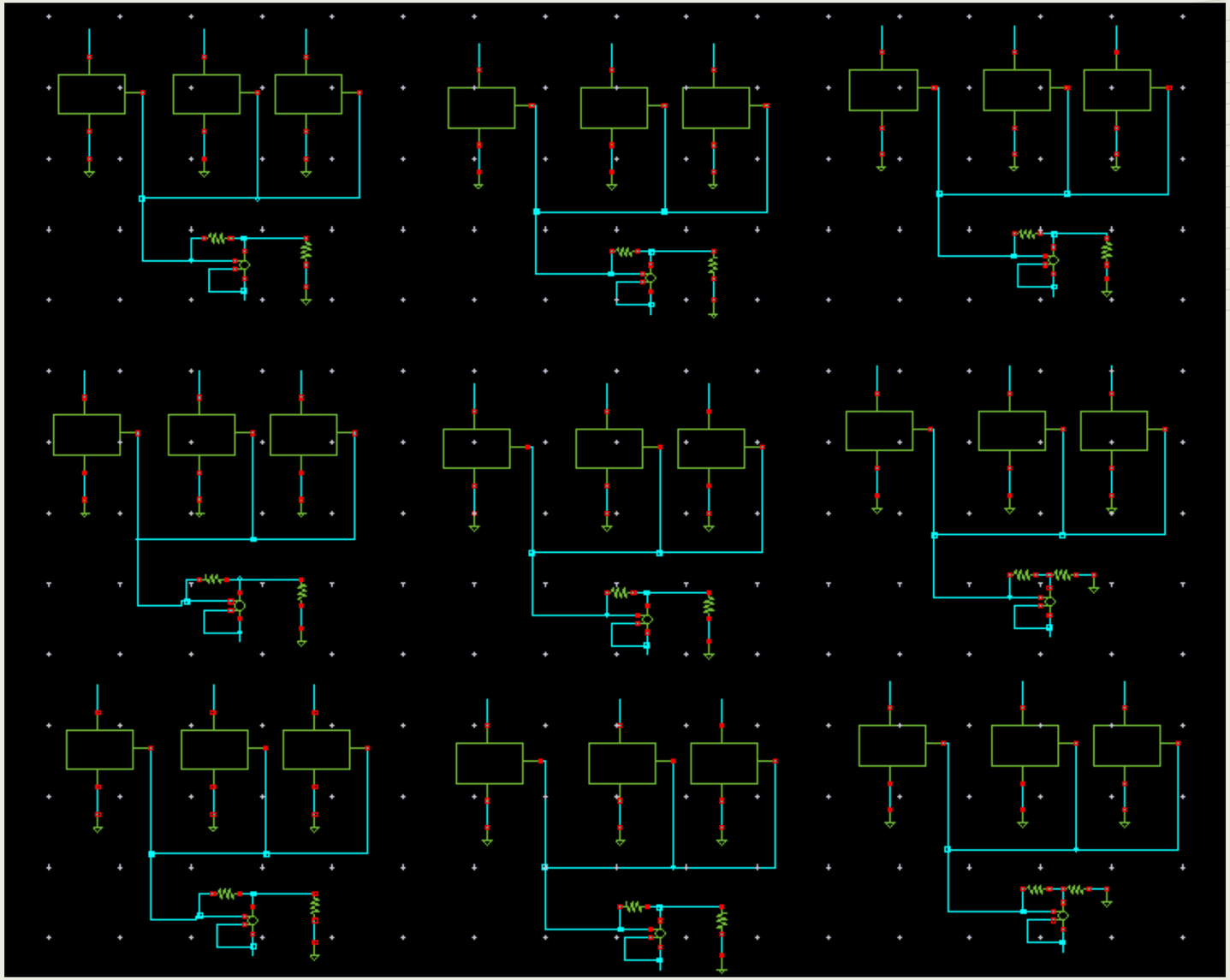


1. V1=0.8V, R1=250
2. V2=0.8V, R2=500
3. V3=0.8V, R3=1000

I = 0.2(0.8/250 + 0.8/500 + 0.8/1000)
= 1.12mA

V = 5.6 V

Array of MAC for 3x3 VMM



References

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[3] A. P. Patil et al., “Forming-free bipolar resistive switching characteristics in AL/MN3O4/FTO RRAM device,” Journal of Physics and Chemistry of Solids, https://www.sciencedirect.com/science/article/abs/pii/S0022369722001172 (accessed Apr. 20, 2025).

Thank you.