**Experiment / Assignment / Tutorial No. \_\_\_*2*\_\_\_**

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of the Staff In-charge with date**

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| B**atch: B3 Roll No.: 121 Experiment / assignment / tutorial No.: 2** |

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| **Title:** Binary Adders and Subtractors |

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**Objective:** To implement half and full adder–subtractor using gates and IC 7483

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**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

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**Books/ Journals/ Websites referred:**

* **VLab Link:** <http://vlabs.iitb.ac.in/vlabs-dev/labs/dldesignlab/experimentlist.html>
* R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
* M .Morris Mano, “Digital Logic & computer Design”, PHI
* http://physics.niser.ac.in/labmanuals/sem5/elect/7\_ADDER%20SUBTRACTO  [R%20CIRCUITS.pd](http://physics.niser.ac.in/labmanuals/sem5/elect/7_ADDER%20SUBTRACTOR%20CIRCUITS.pdf)f

**Pre Lab/ Prior Concepts:**

**Adder:** Addition of two binary digits is most basic operation performed by the digital computer. There are two types of adder:

* Half adder
* Full adder

**Half Adder:** Half adder is combinational logic circuit with two inputs and two outputs. It is the basic building block for addition of two single bit numbers.

**Full adder:** A half adder has a provision not to add a carry coming from the lower order bits when multi bit addition is performed. for this purpose a third input terminal is added and this circuits is to add A,B,C where A and B are the nth order bits of the number A and B respectively and C is the carry generated from the addition of (n-1) order bits. This circuit is referred to as full adder.

**Subtractor:** Subtraction of two binary digits is one of the most basic operations performed by digital computer .there are two types of subtractor:

* Half subtractor
* Full subtractor

**Half subtractor:** Logic circuit for the subtraction of B from A where A,B are 1 bit numbers is referred to as half subtract or .the subtract or process has two input and difference and borrow are the two outputs.

**Full subtractor:** As in the case of the addition using logic gates, a full subtractor is made by combining two half-sub tractors and an additional OR-gate. A full subtractor has the borrow in capability (denoted as BORIN) and so allows cascading which results in the possibility of multi-bit subtraction.

**IC 7483**

For subtraction of one binary number from another, we do so by adding 2’s complement of the former to the latter number using a full adder circuit.

IC 7483 is a 16 pin, 4-bit full adder. This IC has a provision to add the carry output to transfer and end around carry output using Co and C4 respectively.

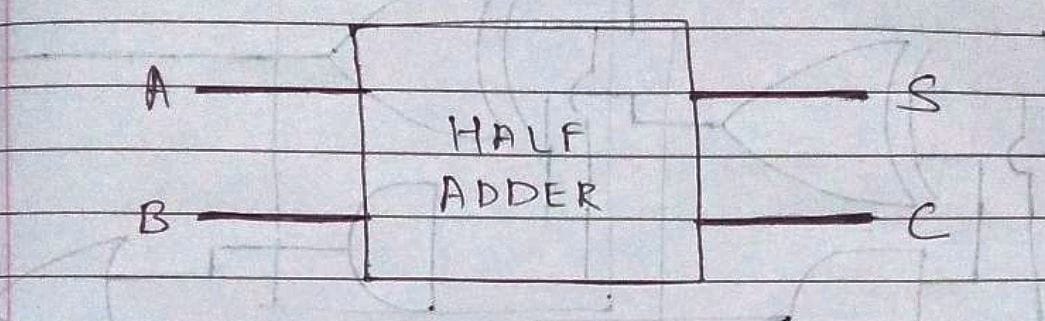
**2’s complement:** 2’s complement of any binary no. can be obtained by adding 1 in 1’scomplement of that no.

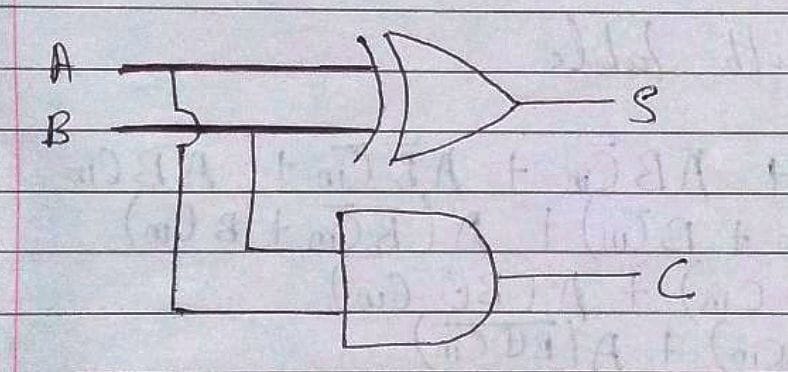
e.g. 2’s complement of +(10)10 =1010is

|  |  |  |  |
| --- | --- | --- | --- |
| 1C of 1010 |  | | 0101 |
|  |  | + | 1 |
| -(10)10 |  | | 0110 |

In 2’s complement subtraction using IC 7483, we are representing negative number in 2’s complement form and then adding it with 1st number.

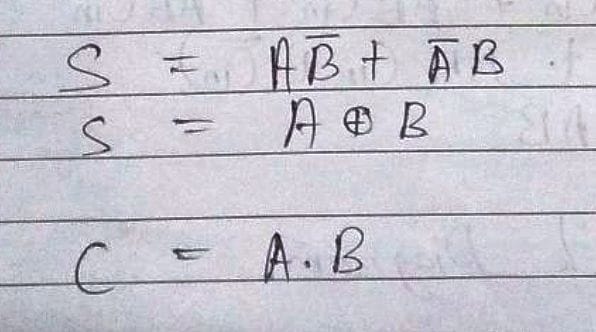
**Implementation Details:**

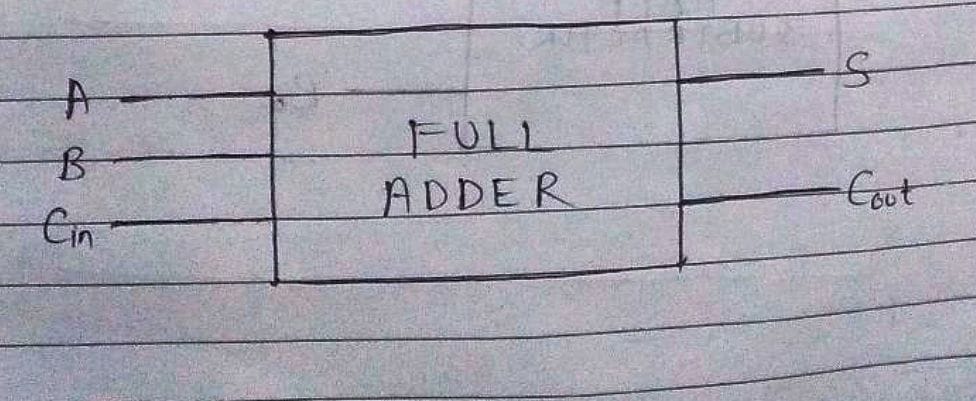
**Half Adder Block Diagram**

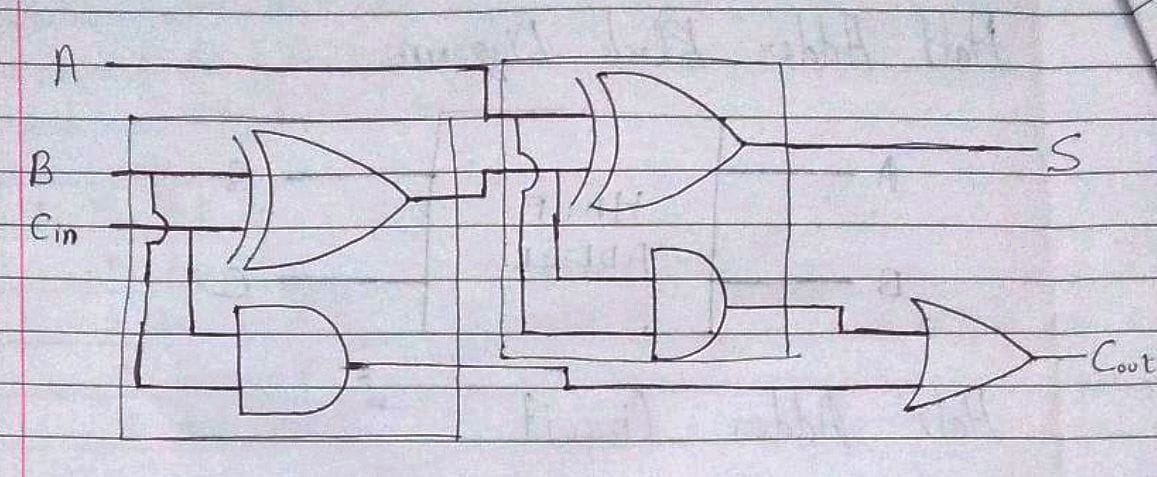
**Half Adder Circuit**

**Truth Table for Half Adder**

|  |  |  |  |
| --- | --- | --- | --- |
| **Inputs** | | **Outputs** | |
| **A** | **B** | **S** | **C** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**From the truth table (with steps):**

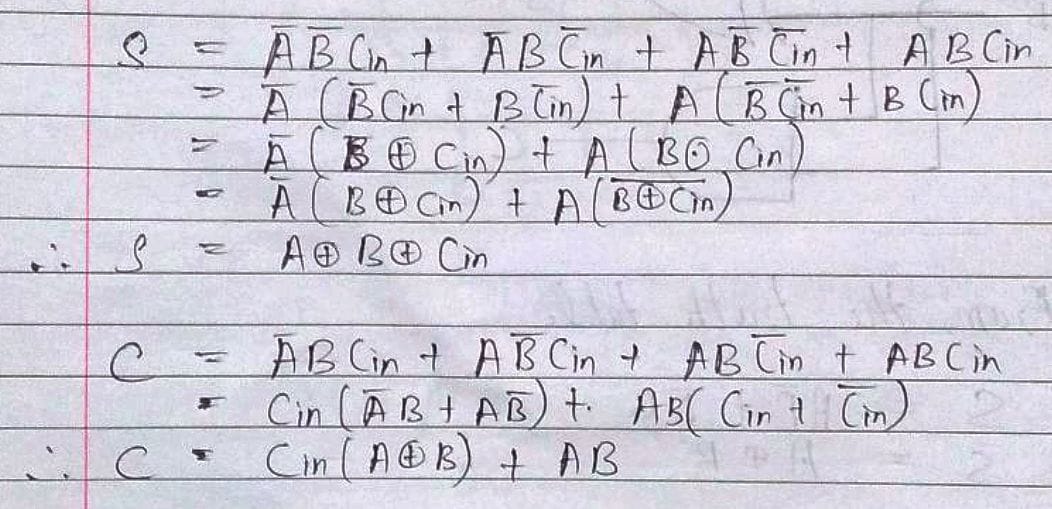
**Full Adder Block Diagram**

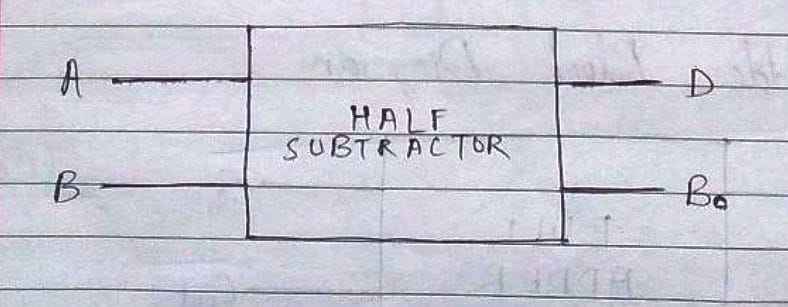
**Full Adder Circuit**

**Truth Table for Full Adder**

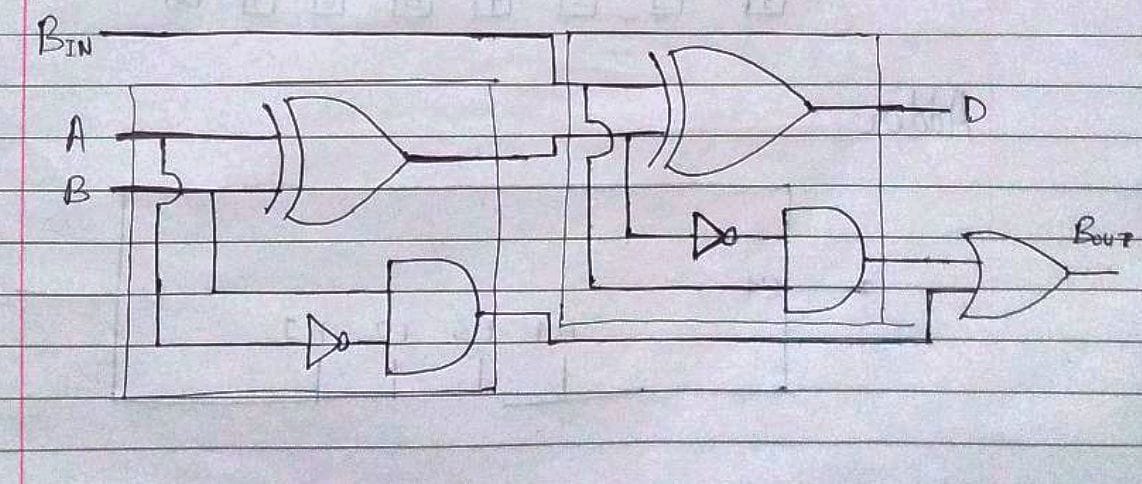
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **CIN** | **S** | **COUT** |
|  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 |
|  |  |  |  |  |
| 0 | 0 | 1 | 1 | 0 |
|  |  |  |  |  |
| 0 | 1 | 0 | 1 | 0 |
|  |  |  |  |  |
| 0 | 1 | 1 | 0 | 1 |
|  |  |  |  |  |
| 1 | 0 | 0 | 1 | 0 |
|  |  |  |  |  |
| 1 | 0 | 1 | 0 | 1 |
|  |  |  |  |  |
| 1 | 1 | 0 | 0 | 1 |
|  |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 |
|  |  |  |  |  |

**From the truth table (with steps):**

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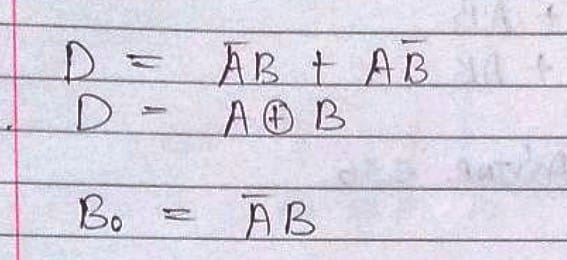
**Half Subtractor Block Diagram**

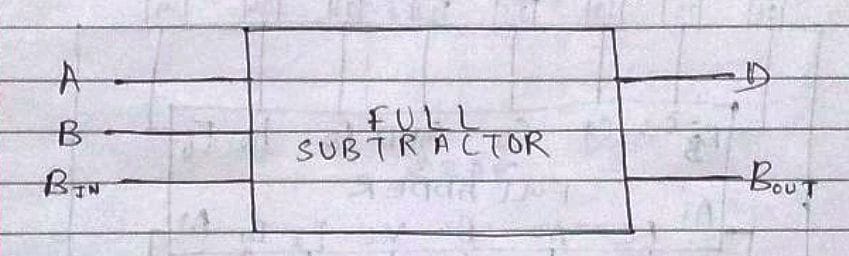
**Half Subtractor Circuit**

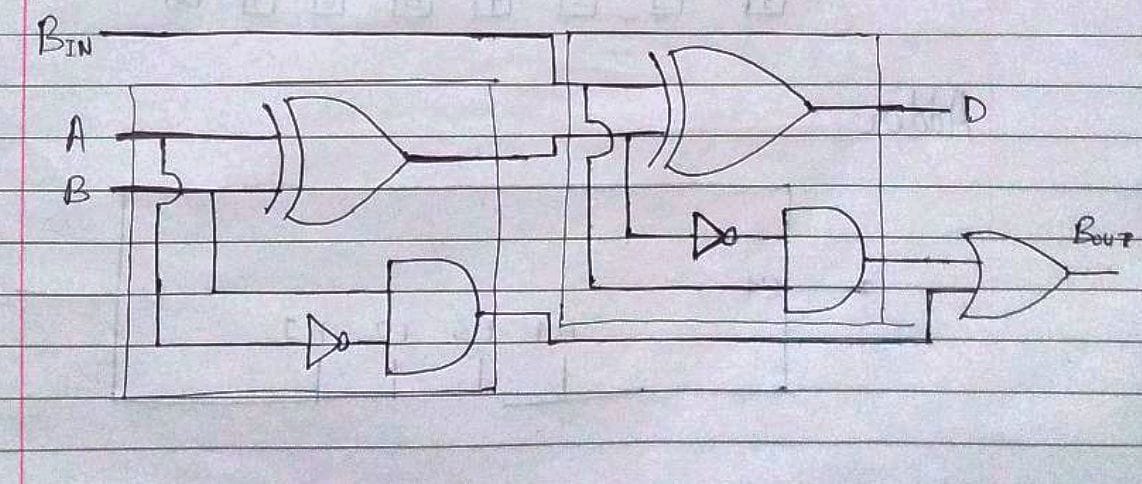


**Truth Table for Half Subtractor**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
| **A** | **B** | **DIFFERENCE(D)** | **BORROW(Bo)** |  |
|  |  |  |  |  |
| 0 | 0 | 0 | 0 |  |
|  |  |  |  |  |
| 0 | 1 | 1 | 1 |  |
|  |  |  |  |  |
| 1 | 0 | 1 | 0 |  |
|  |  |  |  |  |
| 1 | 1 | 0 | 0 |  |
|  |  |  |  |  |

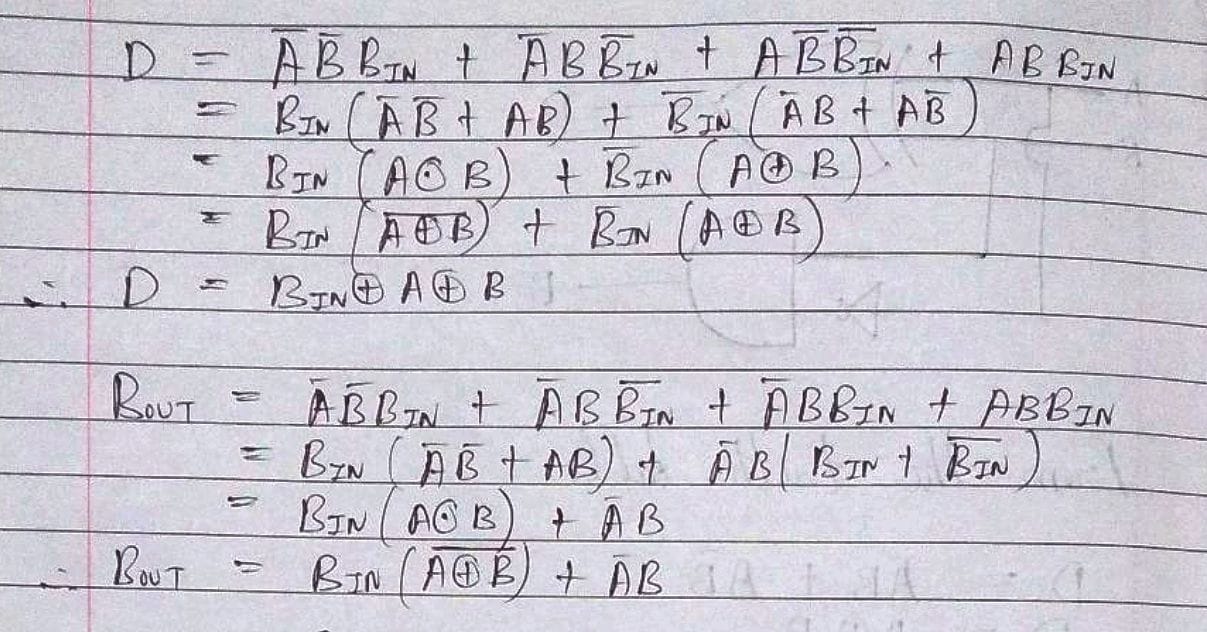
**From the truth table (with steps) :**

**Full Subtractor Block Diagram**

**Full Subtractor Circuit**

**Truth Table for Full subtractor**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **BIN** | **D** | **BOROUT** |
|  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 |
|  |  |  |  |  |
| 0 | 0 | 1 | 1 | 1 |
|  |  |  |  |  |
| 0 | 1 | 0 | 1 | 1 |
|  |  |  |  |  |
| 0 | 1 | 1 | 0 | 1 |
|  |  |  |  |  |
| 1 | 0 | 0 | 1 | 0 |
|  |  |  |  |  |
| 1 | 0 | 1 | 0 | 0 |
|  |  |  |  |  |
| 1 | 1 | 0 | 0 | 0 |
|  |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 |

**From the truth table (with steps):**

**IC 7483**

**Procedure:**

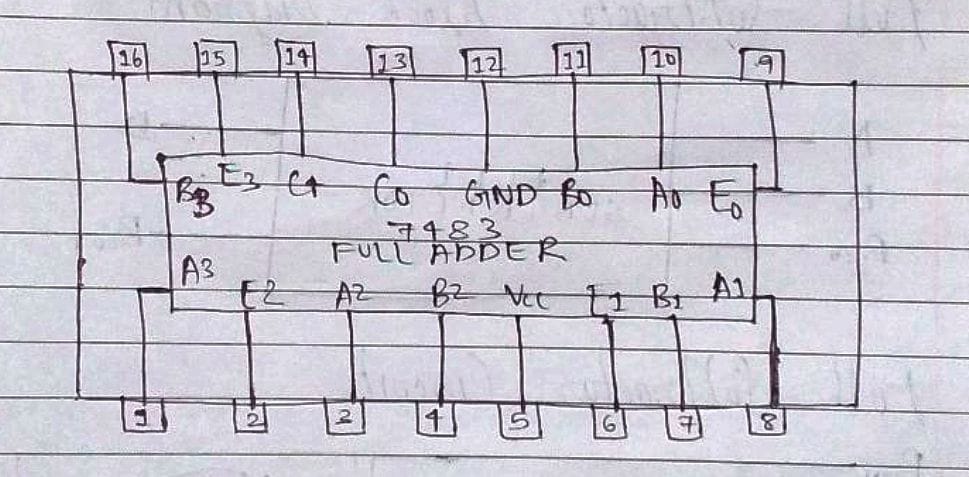
1. Locate the IC 7483 and 4-not gates block on trainer kit.
2. Connect 1st input no. to A4-A1 input slot and 2nd (negative) no. to B4-B1 through 4-not gates (1C of 2nd no.)
3. Connect high input to Co so that it will get added with 1C of 2nd no. to get 2C.
4. Connect 4-bit output to the output indicators.
5. Switch ON the power supply and monitor the output for various input combinations.

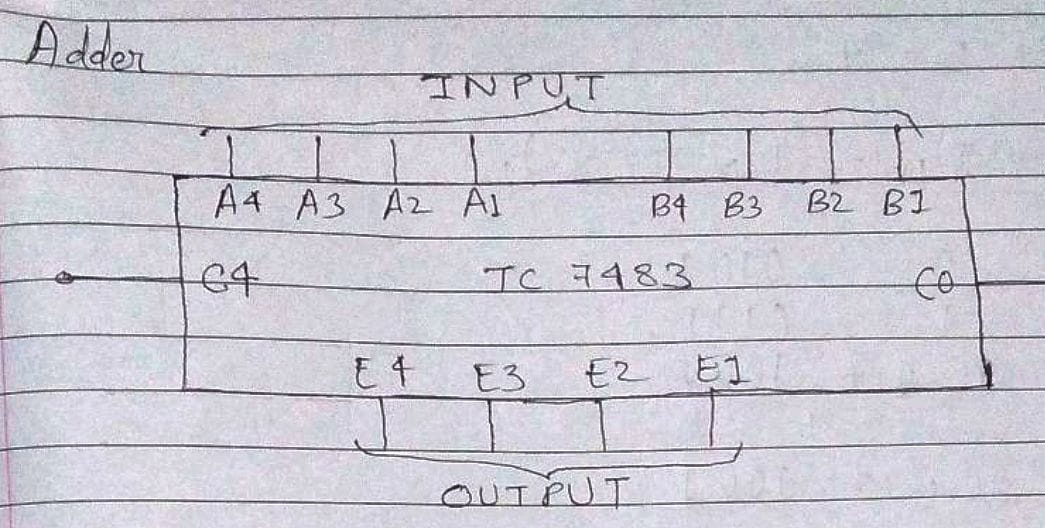
**Example:**

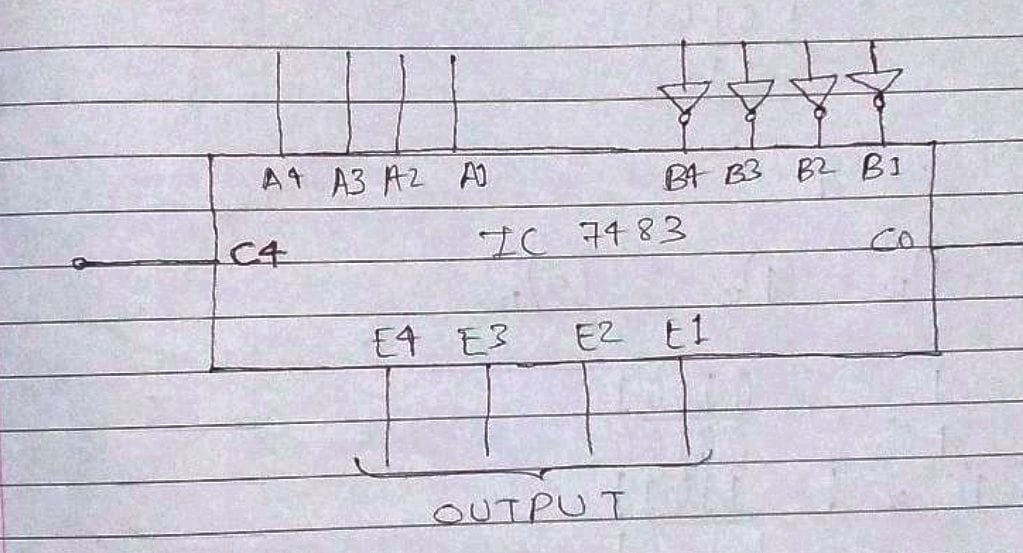
|  |  |  |
| --- | --- | --- |
| 1) 710 -210 = 510 | |  |
| 7 |  | 0111 |
| 2 |  | 0010 |
| 1’C of 2 | | 1101 |
|  |  | + 1 |
| 2’C of 2 | | 1110 |

0111 + 1110 1 0101

**Pin Diagram IC7483**

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**Adder**

**Subtractor**

**Conclusion:**

Thus, in this experiment, the symbols and circuits for half-adders, full-adders, half-subtractors and full-subtractors was learnt. Further, it was learnt that the IC 7483 processor can perform full addition as well as full subtraction. Thus, it is a useful component in any logic circuit.

**Post Lab Descriptive Questions**

1. What is difference between half and full adder, half and full subtractor?

Ans.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Sr. No. | Half Adder | Full Adder | Half Subtractor | Full Subtractor |
| 1. | There are two inputs, A and B. | There are three inputs, A, B and Cin (input carry) | There are two inputs, A and B. | There are three inputs, A, B and Bin (input borrow). |
| 2. | Its logical expression is S = A B and C = A.B | Its logical expression is S = A B Cin and Cout = Cin.(AB) + A.B | Its logical expression is D = AB and Bo = | Its logical expression is D = BinAB and Bout = Bin.(AB)+ |
| 3. | It consists of one EX-OR Gate and one AND Gate. | It consists of two EX-OR Gates, two AND Gates and one OR Gate. | It consists of one EX-OR Gate, one NOT Gate and one AND Gate. | It consist of two EX-OR Gates, two NOT Gates, two AND Gates and one OR Gate. |
| 4. | The generated output is Sum and Carry from the input of two bits. | The generated output is Sum and Carry from the input of three bits including input Carry. | The generated output is Difference and Borrow from the input of two bits. | The generated output is Difference and Borrow from the input of three bits including input Borrow. |

1. Perform the following Binary subtraction with the help of appropriate ICs:
2. 7-5
3. 5-7
4. 9-4

Ans.

