**Experiment / Assignment / Tutorial No. \_\_\_4\_\_\_**

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of the Staff In-charge with date**

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| **Batch: B3 Roll No.: 121 Experiment / assignment / tutorial No.: 4** |

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| **Title:** 4 bit Magnitude Comparator |

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**Objective:** Design a 2-bit comparator using logic gates and verify 4-bit magnitudecomparator using IC 7485

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**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

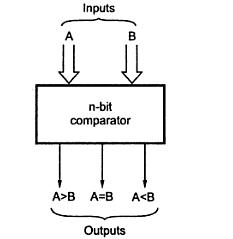
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**Books/ Journals/ Websites referred:**

* VLab Link: <http://vlabs.iitb.ac.in/vlabs-dev/labs/dldesignlab/experimentlist.html>
* R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
* M .Morris Mano, “Digital Logic & computer Design”, PHI
* http://elnsite.teilam.gr/ebooks/digital\_design/lab/dataSheets\_page/7485.pdf

**Pre Lab/ Prior Concepts:**

The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.



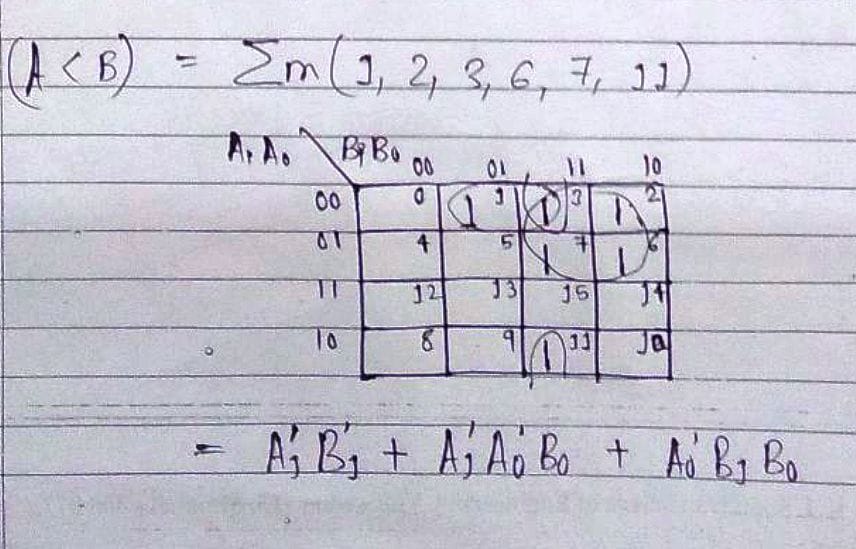
**Two Bit Magnitude Comparator Implementation Details:**

**Truth Table**

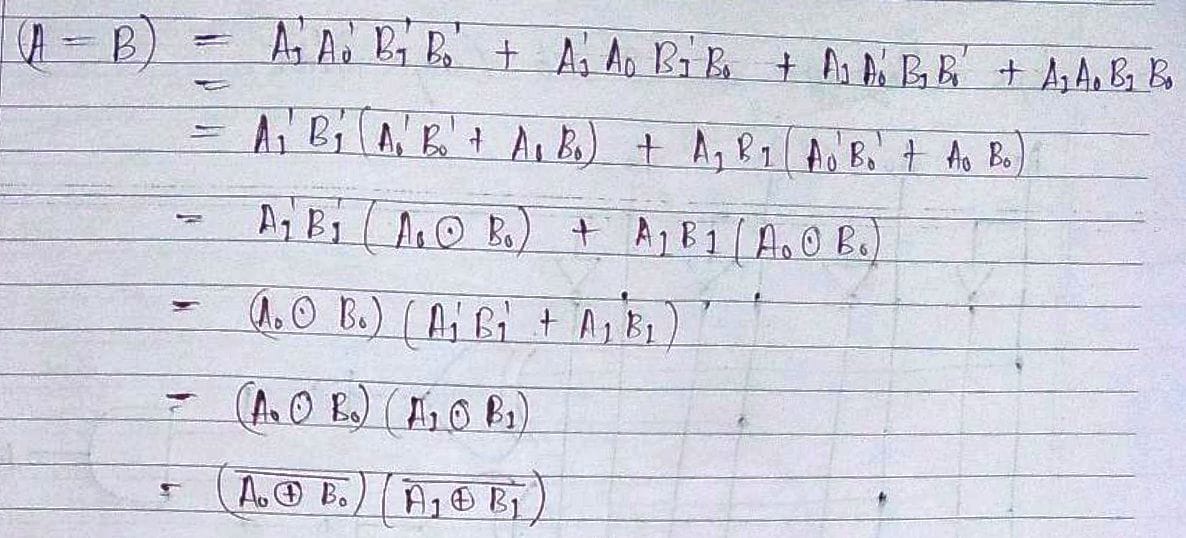
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A1** | **A0** | **B1** | **B0** | **A > B** | **A = B** | **A < B** |
|  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
|  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
|  |  |  |  |  |  |  |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
|  |  |  |  |  |  |  |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
|  |  |  |  |  |  |  |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
|  |  |  |  |  |  |  |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |
|  |  |  |  |  |  |  |

**From the Truth Table:**

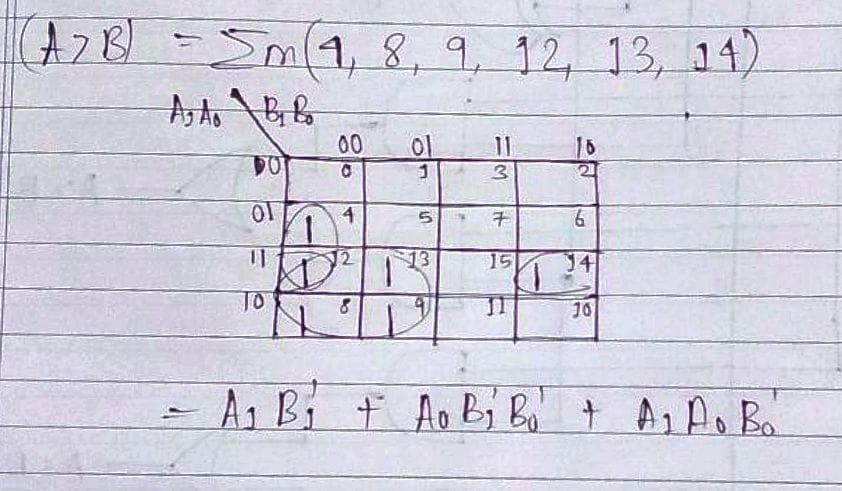
**(A<B)=** A1’B1’ + A1’A0’B0 + A0’B1B0

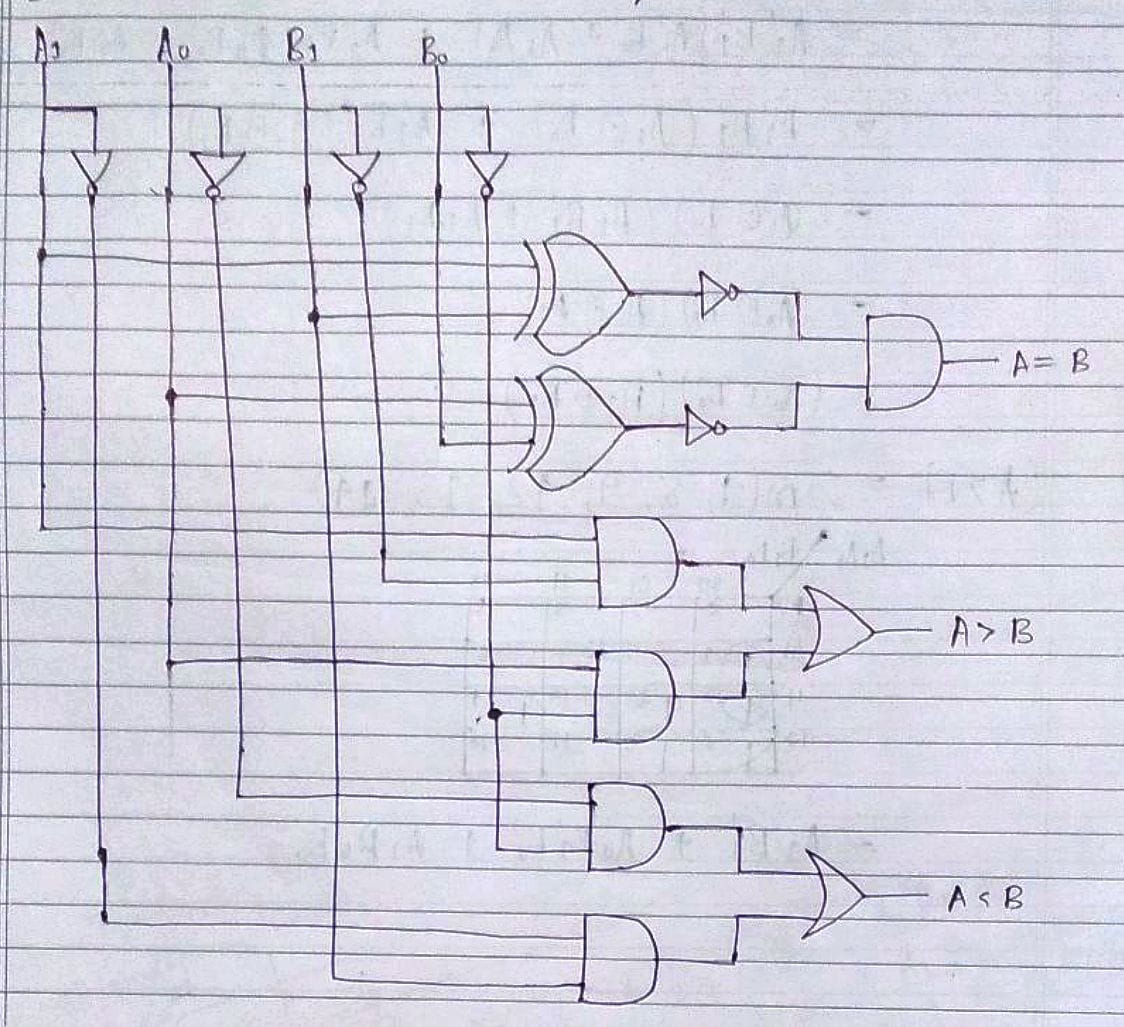
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**(A=B)= (**A0 B0).(A1B1)

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**(A>B)=** A1B1’ + A0B1’B0’ + A1A0B0’

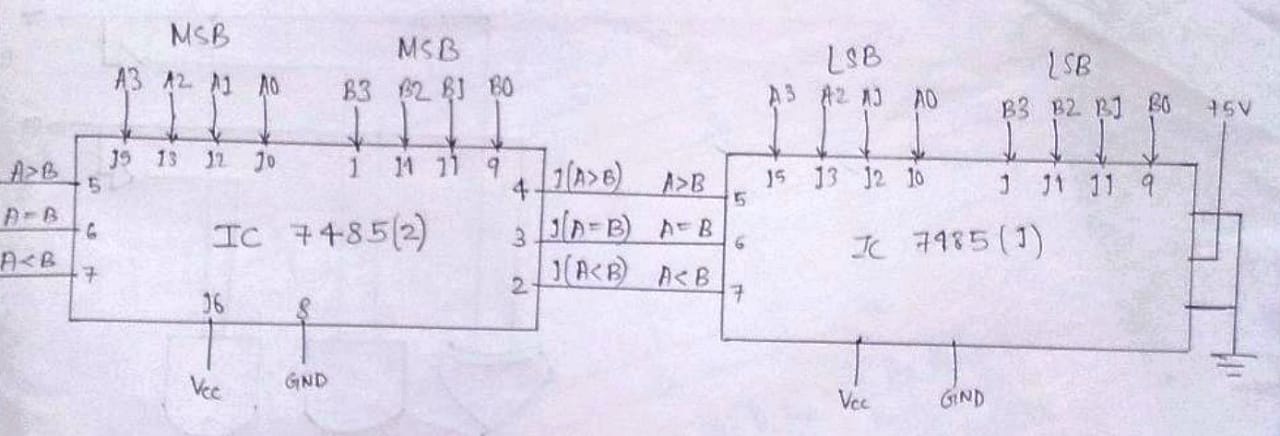
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**Logic Diagram of 2 bit Comparator**

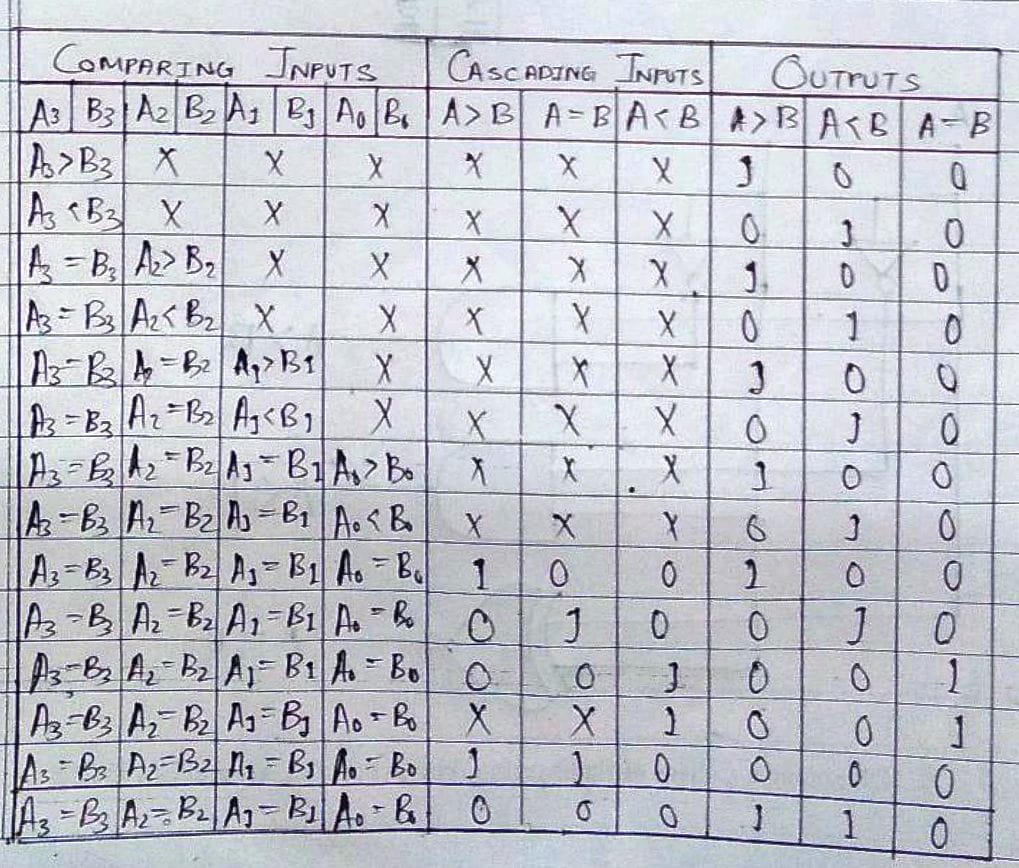
**Four Bit Magnitude Comparator Implementation Details**

**Pin Diagram of IC 7485**



**Logic Diagram of IC 7485**

**Comparing Table**

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**Conclusion:** Thus, in this experiment, details about the two bit and the four bit comparator have been studied and implemented using the IC Board. The IC 7485 can compare 4 bits. If however, more bits are to be compared, then Cascading Inputs can be used.

**Post Lab Descriptive Questions**

1. Design a 1- bit magnitude comparator using logic gates.