**Experiment / Assignment / Tutorial No. \_\_\_5\_\_\_**

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of the Staff In-charge with date**

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| **Batch: B3 Roll No.: 121 Experiment / assignment / tutorial No.: 5** |

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| **Title:** Flip Flops |

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**Objective:**Design of JK Flip flop, D flip flop, T flip flop using NAND Gates & verification of the same flip flop using IC7476

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**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

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**Books/ Journals/ Websites referred:**

* VLab Link: [http://vlabs.iitkgp.ernet.in/dec/#](http://vlabs.iitkgp.ernet.in/dec/)
* R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
* M .Morris Mano, “Digital Logic & computer Design”, PHI
* A.P.Godse, D.A.Godse, “Digital Logic Design”

**Pre Lab/ Prior Concepts:**

Flip-flop is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

**JK-flip flop:** has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge, then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.

**D Flip Flop:** tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate.

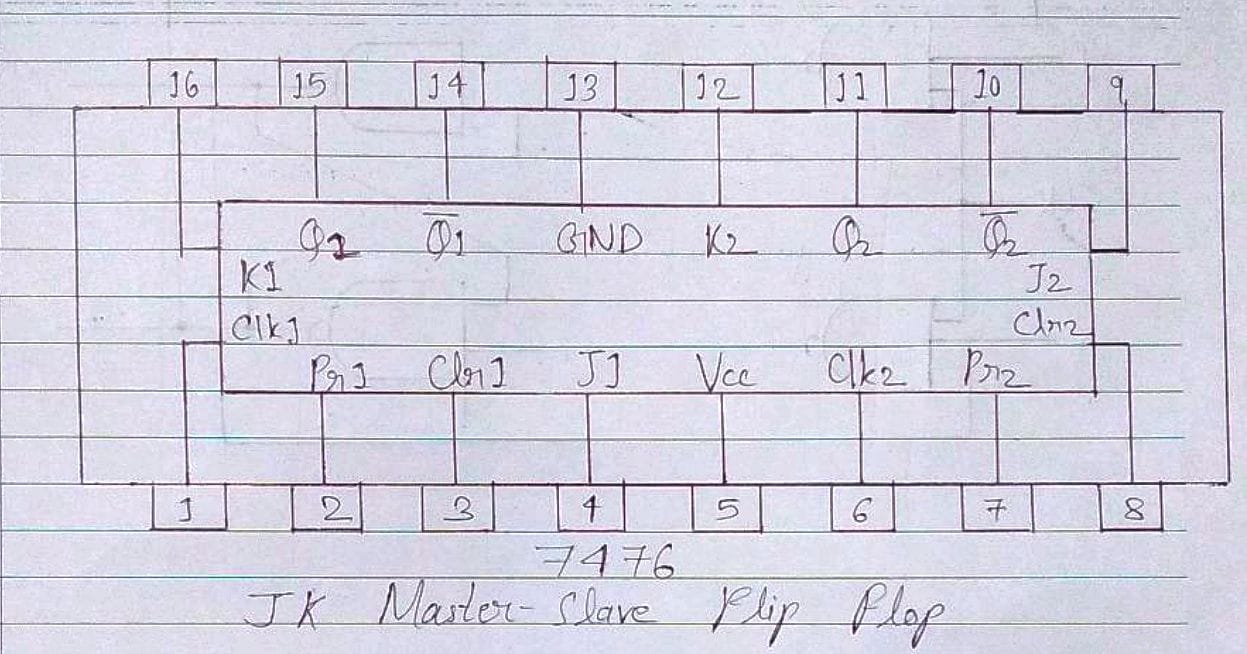
**T Flip Flop:** T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

**Implementation Details:**

**Procedure**

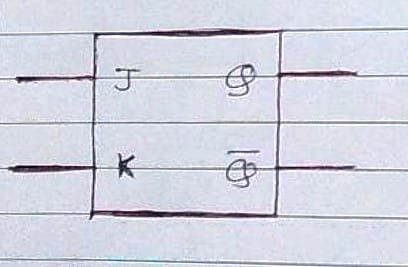
1. Locate IC 7476 on Digital trainer kit
2. Apply various inputs to J & K pins by means of the output on logic output indicator.
3. Connect a pulsar switch to the clock input.
4. Connect the J&K as D and T flip flop as shown in diagrams and verify the respective truth tables.

**Pin Diagram of IC 7476 JK Master- Slave FF**



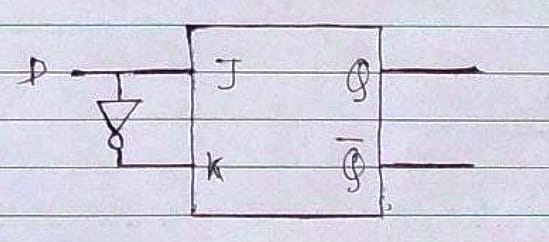
**Logic Symbol Truth Table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **J** | **K** | **Q** | **Q’** | **Qn+1** | **Qn+1’**  **n+1** |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | **1** |

 **JKFF**

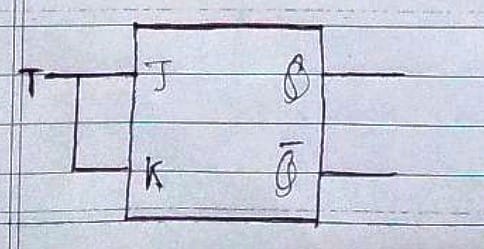
**D FF Truth Table**

|  |  |
| --- | --- |
| **D** | **O/P** |
| 0 | 0 |
| 1 | 1 |

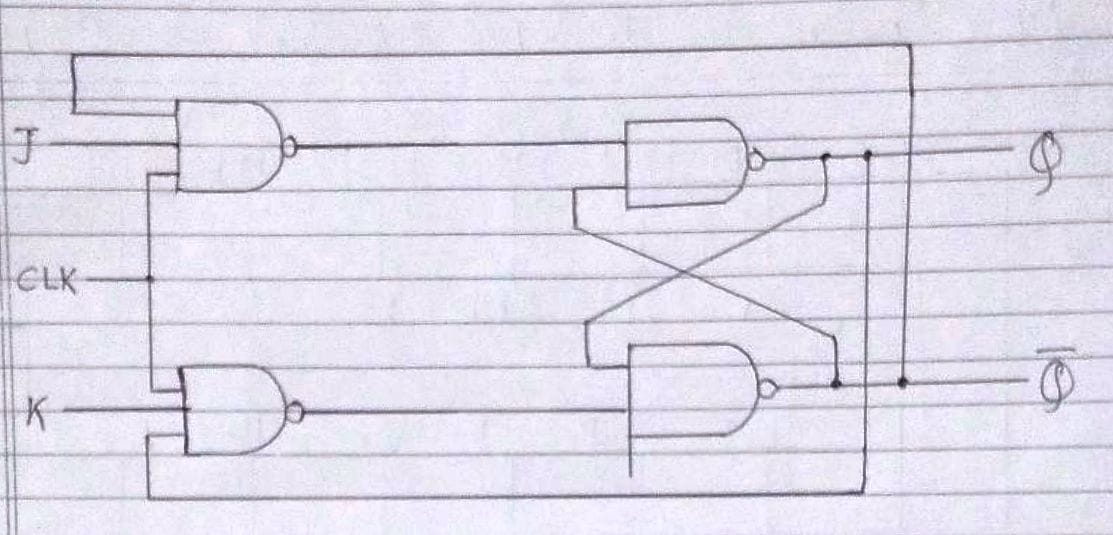


**TFF Truth Table**

|  |  |
| --- | --- |
| **T** | **O/P** |
| 0 | Qn |
| 1 | Qn’ |



**Diagram of JK Flip Flop using NAND gates**



**Conclusion:**

Thus, in this experiment, IC 7476 has been used to understand about JK flip-flop, D flip-flop and T flip-flop.

**Post Lab Descriptive Questions**

1. How does a JK flip-flop differ from an SR flip-flop in its basic operation?

Ans. The difference between a JK flip-flop and an SR flip-flop is that when both inputs of an SR flip-flop is set to 1, the circuit produces the invalid states as outputs (Q = Q’, which is invalid). Hence, it is not used. However, in a JK flip-flop, when both the inputs are 1, then toggle operation is achieved i.e., if Q is the input then Q’ is the output. Thus, the JK flip-flop can be used even when both the inputs are 1, as opposed to the SR flip-flop. Thus, this is an advantage of JK flip-flop over SR flip-flop.

1. What is use of characteristic and excitation table?

Ans. A characteristic table is a short form of the truth table. It provides the information about what the next state of the flip-flop will be on a specific input. On the other hand, an excitation table shows the minimum inputs that are necessary to generate a particular next state (in other words, to “excite” it to the next state) when the current state is known.

1. How many flip flops due you require storing the data 1101?

Ans. The data 1101 consists of four bits. Since one flip-flop is required to store one bit, therefore four flip-flops are required to store the four bits of the data 1101.

1. Describe the basic difference between pulse-triggered and edge-triggered flip-flops.

Ans.

|  |  |  |
| --- | --- | --- |
| Sr. No. | Pulse-triggered flip-flop | Edge-triggered flip-flop |
| 1. | It has pulse generators that control the pulse width and generate narrow pulse during the active edge that can be positive edge. | Edge-triggering is when the flip-flop state is changed as the rising or falling edge of a clock signal passes through a threshold voltage. |
| 2. | Only one latch is used. | Two latches are used. |

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