深圳市展恒安科技有限公司
SHENZHENSHI ZHAN HENG AN TECHNOLOGY CO.,LTD

公司地址：深圳市龙华新区油松第十工业区富康商业广场 A 栋 6 楼　　QQ：2551-333-856　　Tel：18575548193

APPROVAL SHEET

承 认 书

记录编号：　　版本：v0.1

Customer 客户名称	
Part NO. 产品型号	Z240IT008
Product type 产品内容	Mode: Transmissive type .Normally white. TFT LCD Module LCD Module: Graphic 240RGB*320Dot-matrix
Remarks 备注栏	□APPROVAL FOR SEPCIFICATIONS ONLY ■APPROVAL FOR SEPCIFICATIONS AND SAMPLE
Signature by Customer: 客户确认签章	

展恒安确认

核准	审核	定制

客户确认

核准	审核	审核

公司地址：深圳市龙华新区油松第十工业区富康商业广场 A 栋 6 楼　　QQ：2551-333-856　　Tel：18575548193

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1.General Description

Z240IT008 is a 240RGB*320 dots matrix TFT LCD module. It has a TFT panel composed of 720 sources and 320gates. The LCM can be easily accessed by micro-controller.

2. Features

Display Mode	Transmissive
	a-TFT
Display Format	Graphic 240RGB*320 Dot-matrix
Input Data	3 线串口/4 线串口/8bits /16bits parallel interface
Viewing Direction	12 o'clock
Drive	ILI9341

3. Mechanical Specification

Item	Specifications	Unit
Dimensional outline	42.72(W)*60.26(H)*3.45+/-0.1 (T) (FPC not include)	mm
Resolution	240RGB*320	dots
LCD Active area	36.72(W)*48.96(H)	mm
Pixel size	0.153(W)*0.153(H)	mm

4. Mechanical Dimension

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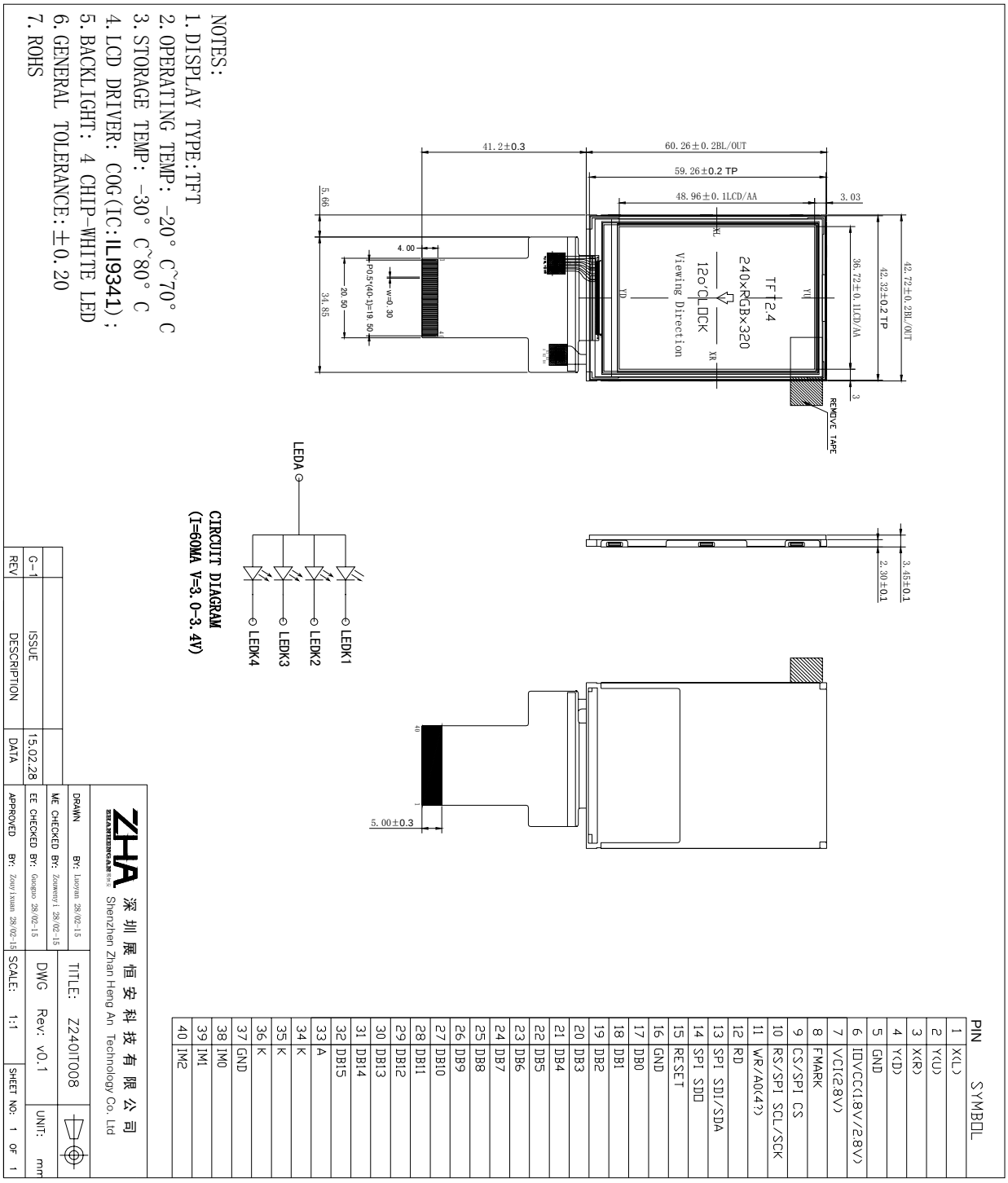


5. Maximum Ratings

Item	Symbol	Min	Max	Unit	Note
Supply voltage	V	-0.3	4.6	V	
Operating temperature	V_T	-0.3	Vcc+0.3	V	
Storage temperature	T_{OPR}	-20	70	℃	
Storage temperature	T_{STR}	-30	80	℃	

6. Electrical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Logic	V_{CC}		2.7	2.8	3.3	V
Input Voltage	H level	T_{IH}		0.8*IOVCC		IOVCC	V
	L level	T_{IL}		-0.3		0.2* IOVCC	
Storage temperature		I_{DD}	With internal voltage generation V_{CC}=2.8V; T_{emp}=25℃			TBD	mA

7. Backlight Characteristic

Item	Symbol	Min	Typical	Max	Unit
LED module Forward voltage	V_{LED}	3.0	3.2	3.4	V
LED module current	V_{LED}		60		mA
L/G Surface Luminance ★1	L_S	3000			Cd/m^3
LCM Surface brightness uniform ★2	L_D	80			%

★ 1Test condition is:

(a) Center point on active area.

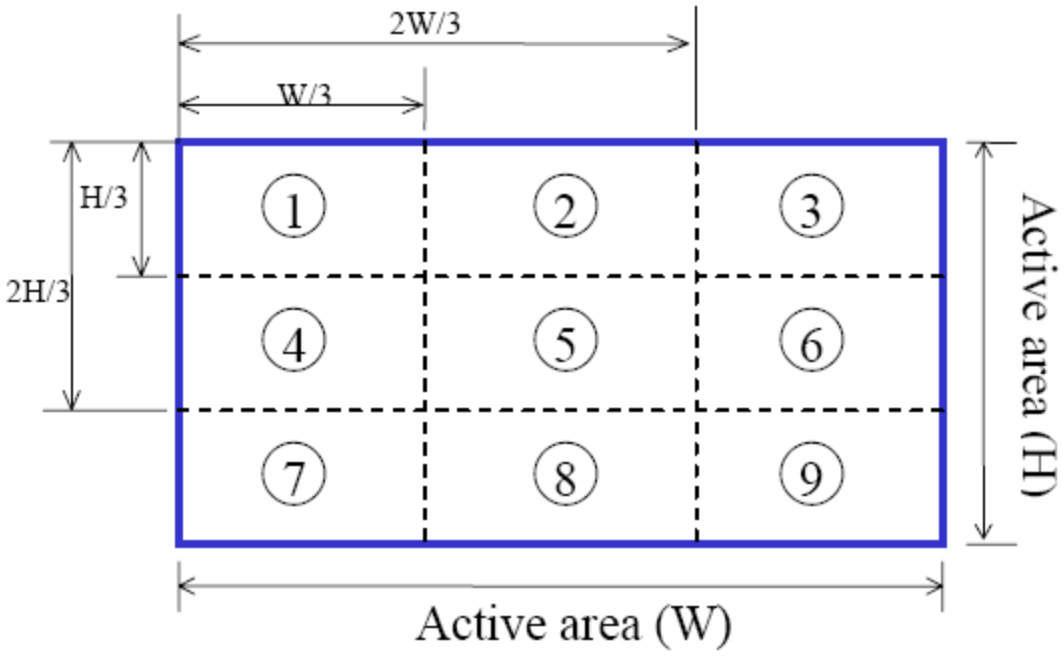
(b)Best Contrast.

★2Uniform measure condition:

(1)Measure 9 point. Measure location show below;

(2)Uniform=(Min. brightness /Max. brightness)*100%

(3)Best Contrast.



8. Module Function Description

8.1Pin Descriptions

PIN No.	Symbol	Description
1	X(L)	Touch panel control pin (触摸屏控制脚)
2	Y(U)	Touch panel control pin (触摸屏控制脚)
3	X(R)	Touch panel control pin (触摸屏控制脚)
4	Y(D)	Touch panel control pin (触摸屏控制脚)
5	GND	Ground （接地脚）
6	IOVCC	Power supply for LCM（2.8V-3.3V） （屏供电脚）
7	VCI	Power supply for LCM（2.8V-3.3V） （屏供电脚）
8	FMARK	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin. (帧同信号,不用时悬空)
9	CS/SPI CS	Chip select pin (“Low” enable) （屏驱动芯片片选脚，低电平有效）
10	RS/SPI SCL/SCK	This pin is used to select “Data or Command” in the parallel interface or serial data interface. (用于并口或者串口) Parallel(并口): When RS= ’1’, data is selected.(选择数据) When RS= ’0’, command is selected.(选择寄存器) Serial(串口): This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. (3线串口或者4线串口的时钟信号) If not used, this pin should be connected to IOVCC or GND.

		(不用时接 IOVCC 或者接地)
11	WR/A0(4 线)	Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. *Fix to*IOVCC *level when not in use.* （并口的写控制脚或者 4 线串口的寄存器/数据选择，不用时接 IOVCC）
12	RD	Serves as a read signal and MCU read data at the rising edge. *Fix to* IOVCC *level when not in use.* （并口的读控制脚,不用时接 IOVCC）
13	SPI SDI/SDA	Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND (串口数据输入信号,不用时接 IOVCC 或者接地)
14	SPI SDO	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin (串口数据输出信号，不用时悬空)
15	RESET	LCM Reset pin Signal is active low. （屏复位脚,低电平复位）
16	GND	Ground （接地脚）
17-24	DB0-DB7	Data bus *Fix to* GND *level when not in use* (低 8 位数据线,不用时接地)
25-32	DB8-DB15	Data bus *Fix to* GND *level when not in use* (高 8 位数据线,不用时接地)
33	A	Anode of Backlight (3.0V-3.4V Typical:3.2V) （背光正极供电脚,电压范围:3.0-3.4V,典型值:3.2V）
34-36	K	Cathode of Backlight （背光负极供电脚）
37	GND	Ground （接地脚）

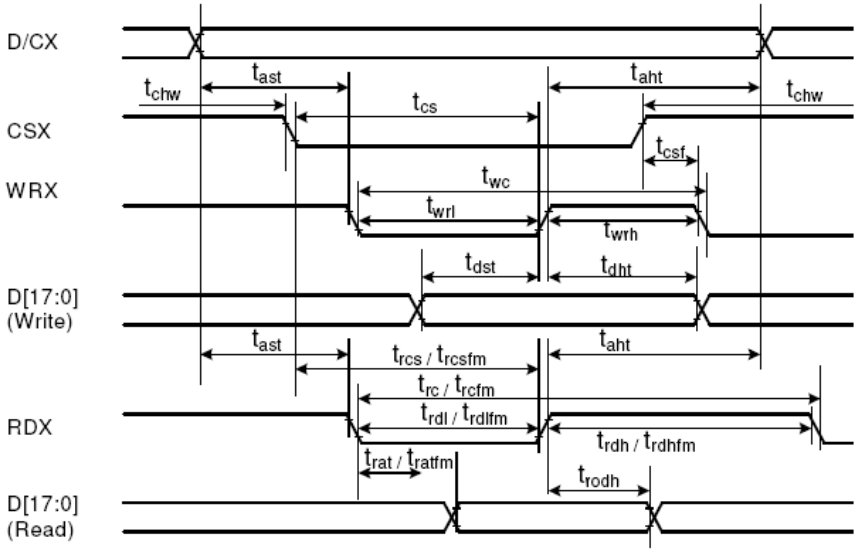
<table>
<tr><td>38</td><td>IM0</td><td rowspan="3">Select the MCU interface mode
(接口选择)
IM2　IM1　IM0
<table><tr><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr><tr><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:10]</td></tr><tr><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:0]</td></tr><tr><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:9]</td></tr><tr><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface Ⅱ</td><td colspan="2">SDI: In
SDO: Out</td></tr><tr><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface Ⅱ</td><td colspan="2">SDI: In
SDO: Out</td></tr></table>NOTE:
D[8:1]即低 8 位数据线 DB7-DB0D
D[17:10]即高 8 位数据线 DB15-DB8</td></tr>
<tr><td>39</td><td>IM1</td></tr>
<tr><td>40</td><td>IM2</td></tr>
</table>

关于供电说明：

IOVCC 和 VCC 连一起，用 2.8V-3.3V 供电；背光 LED 可以单独供电（3.0-3.4 V），也可以和 VCC 共用一组电压（A 为正接 VCC，K 连一起作为负接地）.

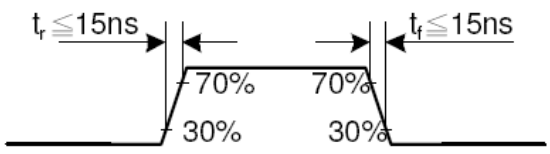
8.2 Timing characteristics.

18.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ system)

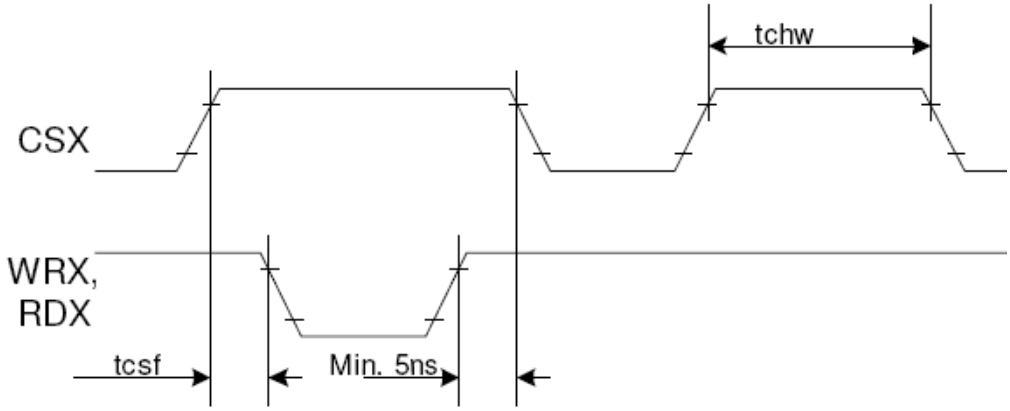


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

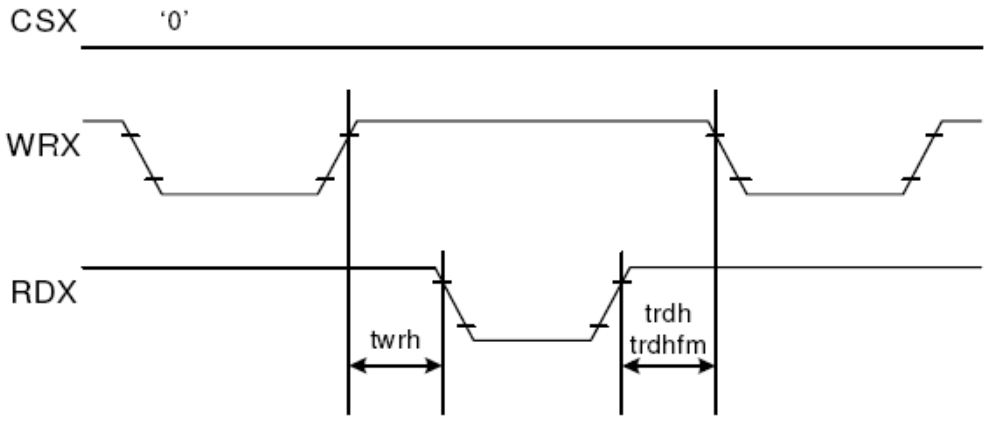


CSX timings :



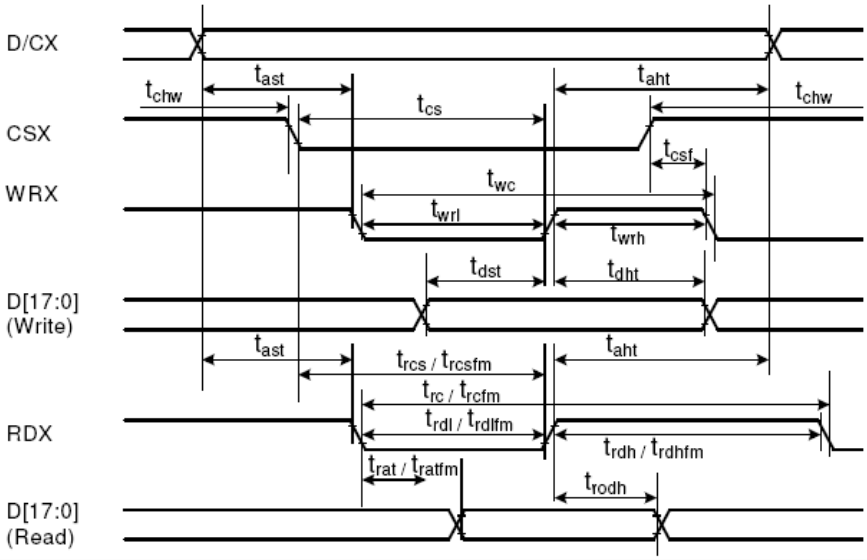
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



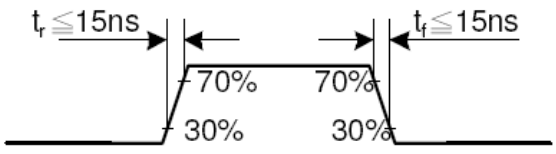
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

18.3.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-Ⅱ system)

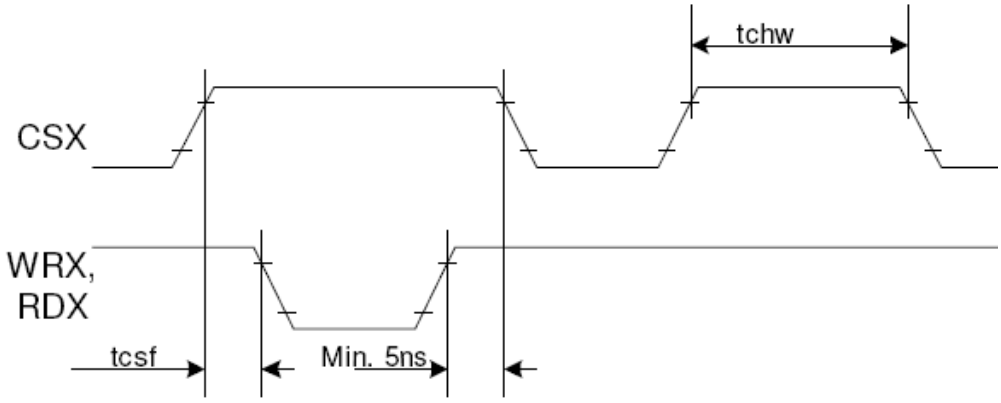


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

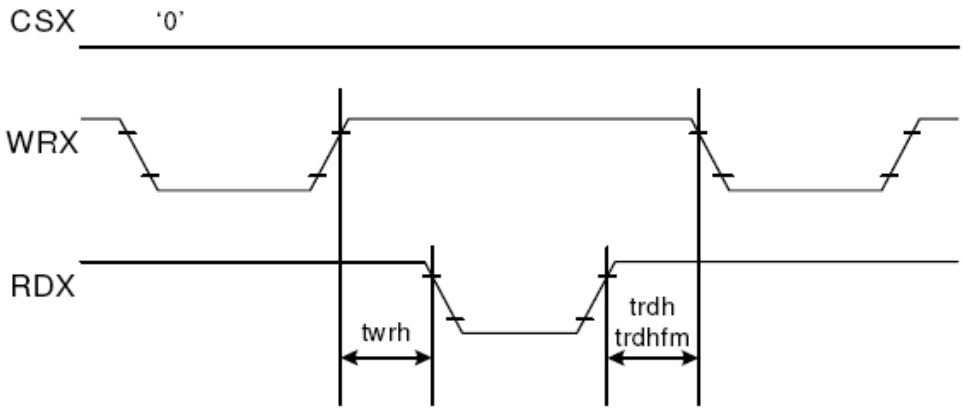


CSX timings :



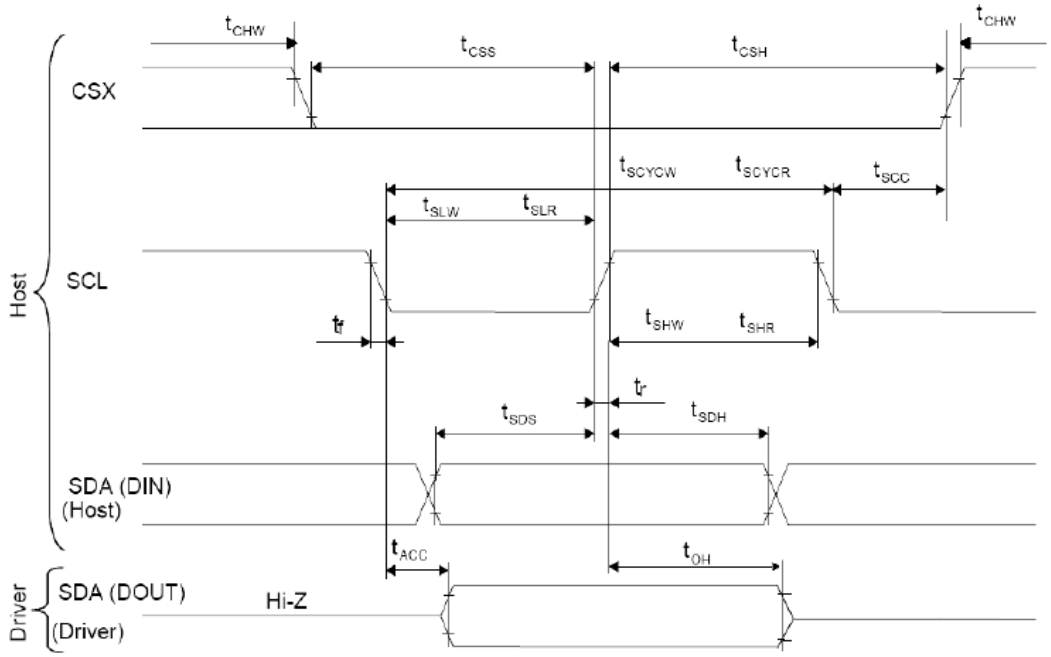
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



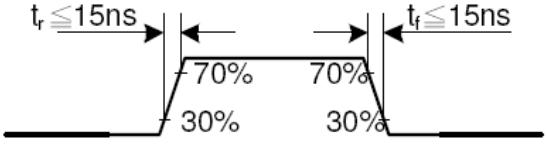
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

18.3.3 Display Serial Interface Timing Characteristics (3-line SPI system)

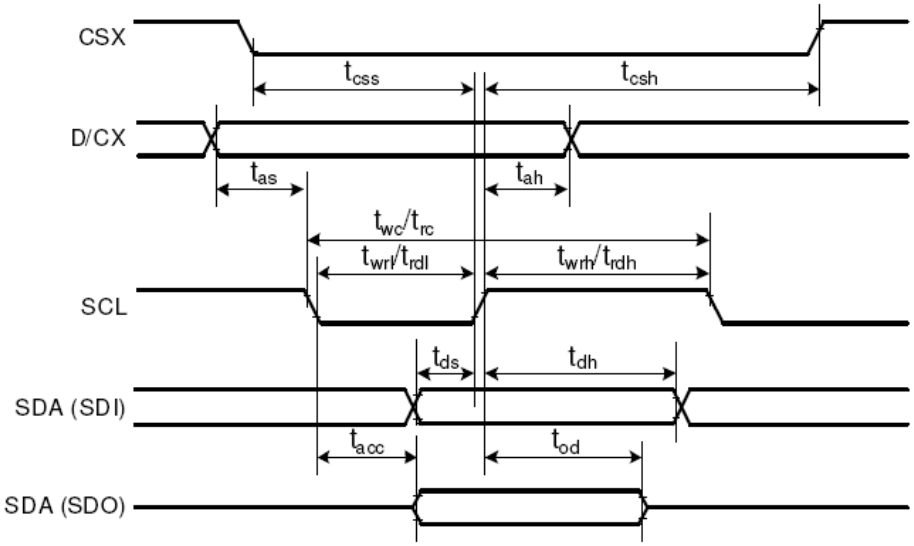


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

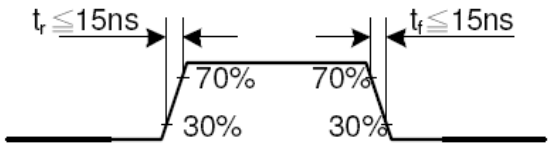


18.3.4 Display Serial Interface Timing Characteristics (4-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL “H” pulse width (Write)	40	-	ns	
	twrl	SCL “L” pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



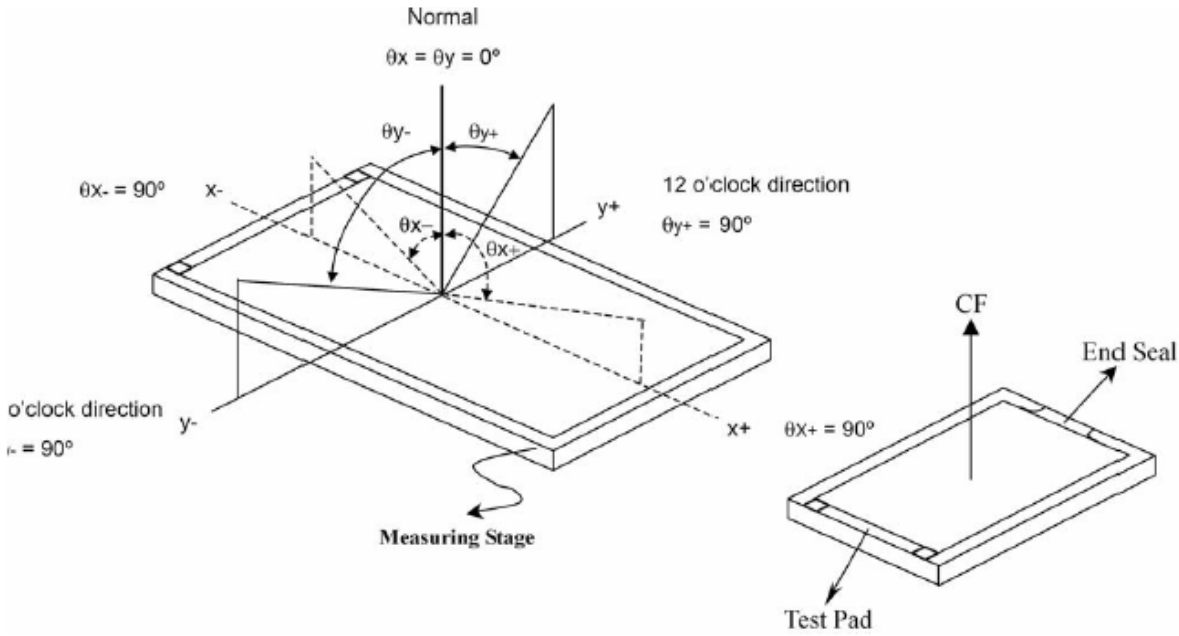
9.Electro-optical Characteristics

Item	Symbol	Conditions	Temp	Min.	Typ.	Max.	Unit	Note
Response Time	T_R	θ = ϕ =0	25℃		TBD	TBD	msec	NOTE2
	T_F				TBD	TBD		
Viewing Angle Range	ϕ =0^0(6”)	ϕ =90^0(3”)	ϕ =180^0(12”)			ϕ =270^0(9”)		NOTE3
θ（25℃）CR≥10	TBD	TBD	TBD			TBD		NOTE3

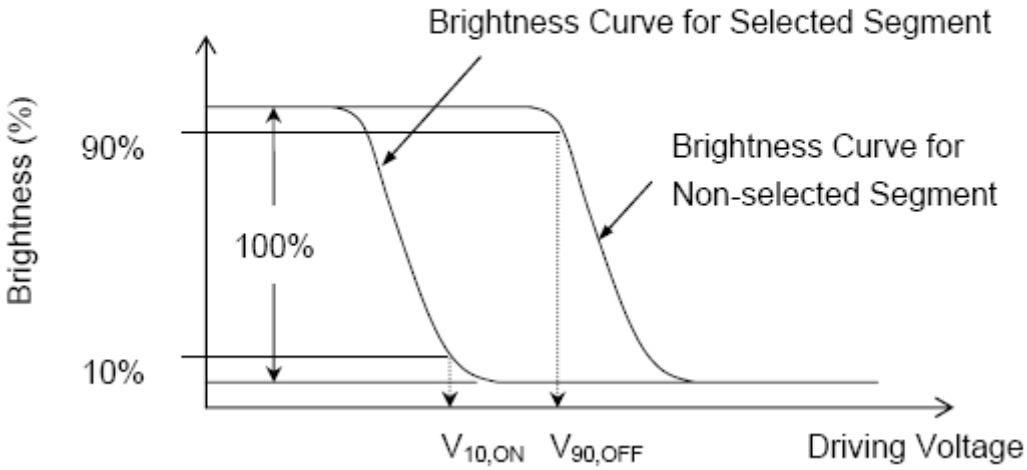
The above “viewing angle” is the measuring position with the largest contrast ratio. Not for good image quality. Viewing direction for good image quality is 12 O’clock.

●For panel only

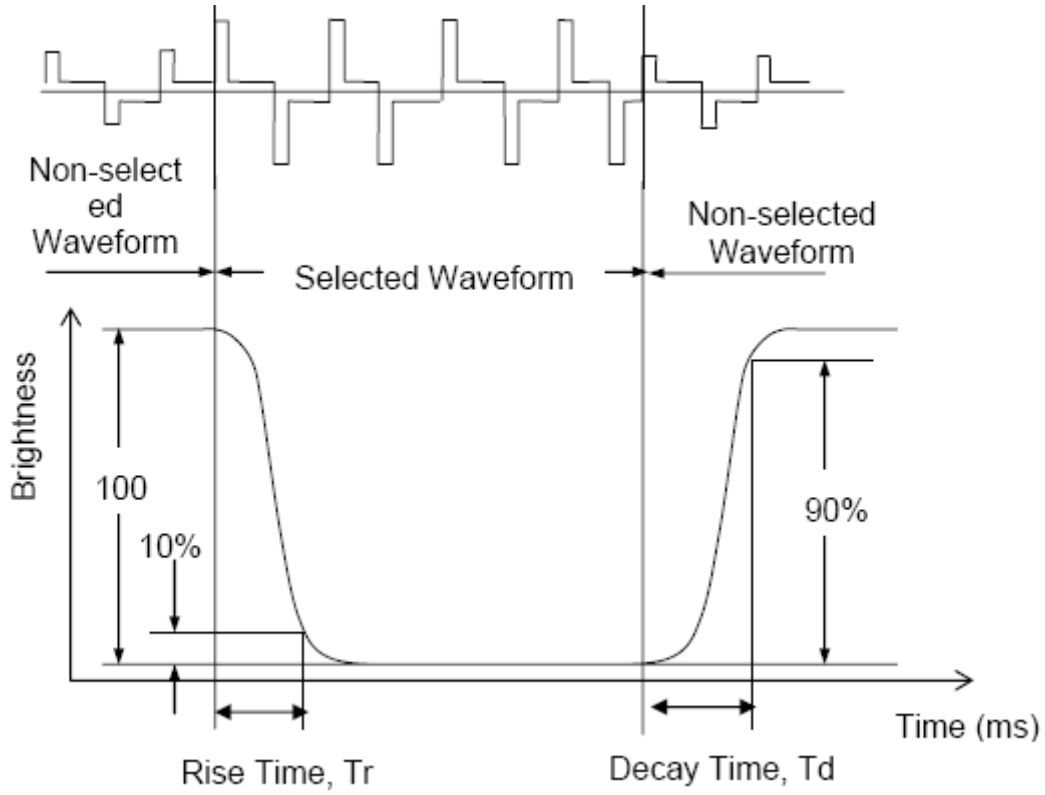
●Electro-Optical Characteristics Test Method



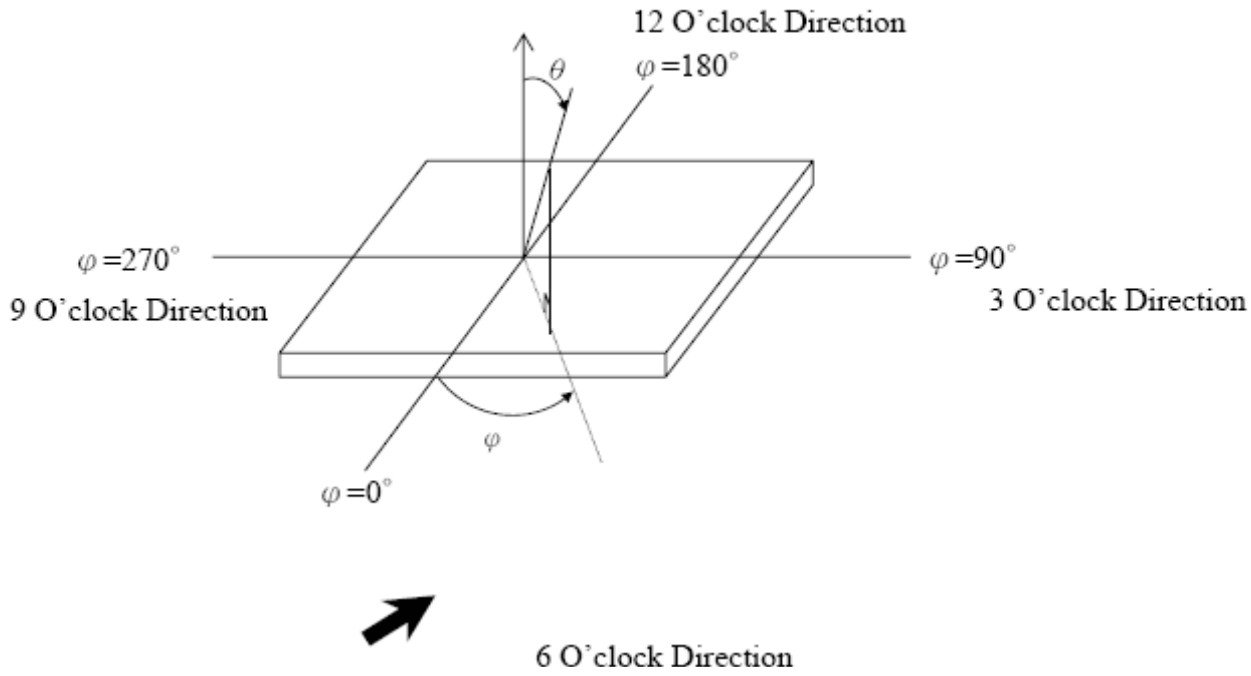
$Vop = (V_{10, ON} + V_{90, OFF})/2$



.Note2.Definition of Optical Response Time:

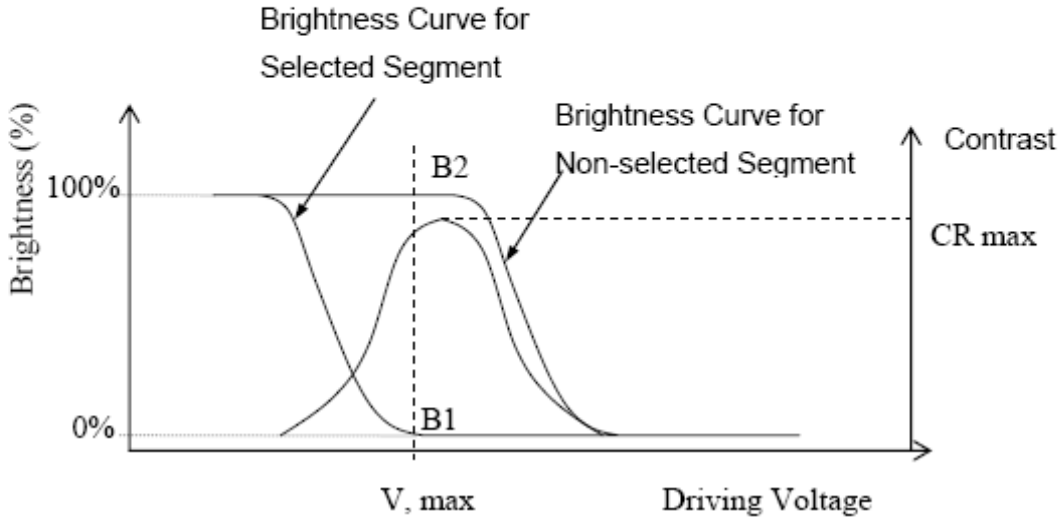


.Note3.Definition of Viewing Angle θ and ϕ :



Note4.Definition of Contrast ratio (CR):

$$CR = \frac{\text{Brightness of Non-selected Segment (B2)}}{\text{Brightness of Selected Segment (B1)}}$$



10. Reliability

10.1Mtbf

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal

10.2Test condition

NO.	ITEM	CONDITION	CRITERION
1	High Temperature Non-Operating Test	80℃*240Hrs	。No Defect Of Operational Function In Room Temperature Are Allowable 。IDD of LCM in Pre-and Post-Test Should Follow Specification
2	Low Temperature Non-Operating Test	-30℃*240Hrs	
3	High Temperature/Humidity Non Operating Test	60℃*90%RH*240Hrs	
4	High Temperature Operating Test	70℃*240Hrs	
5	Low Temperature Operating Test	-20℃*240Hrs	
6	Thermal Shock Test	-20℃(30Min) ↔70℃(30Min) *10CYCLES	

Notes:

1. Judgments should be made after exposure in room temperature for two hours.
2. The distill water is used for the high temperature/humidity test.
3. The sample above is individually for every reliability tests condition.

11.Inspection standards

1.AQL(Acceptable Quality Level

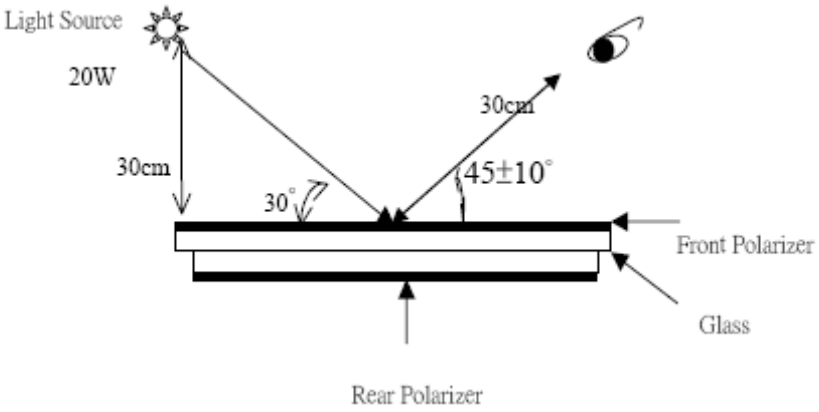
AQL of major and minor defect.

	MAJOR DEFECT	MINOR DEFECT
AQL	0.65	1.5

2. Basic conditions for inspection

The LCM face to us, in normal environment, the lux is 1000±200.(Darkroom's lux: 100±50),About an angle of incidence 30,a distance of 30 cm with an angle of 45 degree to check the products without uncovering the film!

(As shown below)

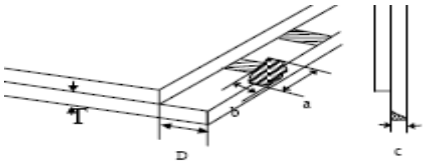
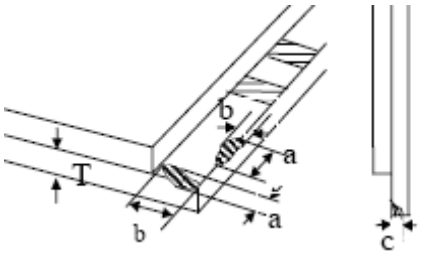
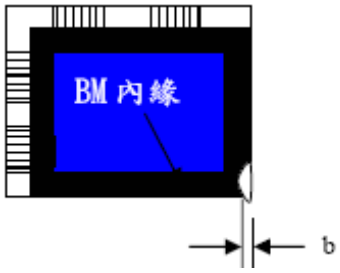


3.Inspection item and criteria

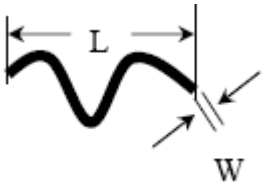
3.1 Visual inspection criterion in immobility

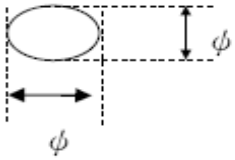
3.1.1Glass defect

NO	Defect item	Criteria	Remark
1	Dimension Unconformity (Major defect)	By Engineering Drawing	
2	Cracks (Major defect)	1. Linear cracks panel 【Reject】 2. Nonlinear crack contrast by limited sample	
3	Glass extrude the conductive area (minor defect)	a: disregards and no influence assemblage. 1) b≤1/3Pin width(non bonding area)	A: Length, b: Width

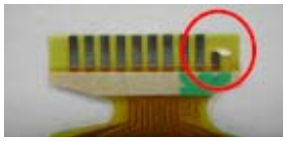
		【Accept】 2)bonding area≤0.5㎜ 【Accept】	
4	Pin-side ,conductive area damaged (minor defect)	(a c: disregards) b≤1/3of effective length for bonding electrode 【Accept】	a: length, b: Width, c: Thickness 
5	Pin-side,non-conductive area damaged (minor defect)	1)Damage area don't touch the ITO (Inclueling contraposition mark, except scribing mark) 【Accept】 2)C<T b≦BM1/3of width 【Accept】 3)c=T b not touch the seal glue 【Accept】 4)a disregards	a: Length, b: Width c: Thickness 
6	Non-pin-side damage (minor defect)	c<T 1)b exceeds 1/3Bm 【Reject】 c=T b not touch the seal glue 【Reject】	c: Thickness b: width of  damage

3.1.2LCD appearance defect(View area)

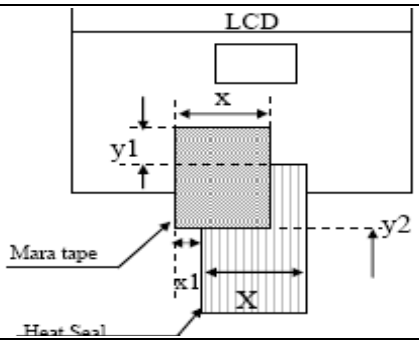
NO	Defect item	Criteria		Remark
1	Fiber、glass cratch、polarizer scratch/folded (minor defect)	Specification	Allowable	note1:L: Length, W: Width note2: disregard if out of AA 
		W≦0.03mm	disregard	
		0.03mm<W≦0.05㎜; L≦3.0㎜	2	
		0.05mm<W≦0.1㎜; L≦3.0㎜	1	
		W>0.1mm;L>3.0mm	0	
2	Polarizer bubble、concave and convex	φ≦0.2mm	disregard	note1: φ=(L+W)/2,L:Length, W :Width
		0.2mm<φ≦0.3㎜	2	

	(minor defect)	0.3mm< ϕ ≦0.5㎜	1	note2:disregard if out of AA
		0.5mm< ϕ	0	
3	Black dots、dirty dots、impurities、eye winker (minor defect)	ϕ ≦0.15mm	disregard	note2:disregard if out of AA 
		0.15mm< ϕ ≦0.25㎜	2	
		0.25mm< ϕ ≦0.3㎜	1	
		0.3mm< ϕ	0	
4	Polarizer prick (minor defect)	ϕ ≦0.1mm	disregard	note1: ϕ=(L+W)/2, L=Length, W=Width note2:the distance between two dots>5mm
		0.1mm< ϕ ≦0.25㎜	3	
		ϕ >0.25㎜	0	

3.1.3FPC

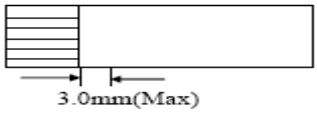
NO	Defect item	Criteria		Remark
1	Copper screen peel (minor defect)	Copper screen peel 【Reject】		
2	No release tape or peel	No release tape or peel 【Reject】		
3	Dirty dot and impurity of FPC for customer using side (minor defect)	Specification	Allowable	Note1: Cannot have stride ITO impurities
		ϕ ≦0.25mm	2	
		ϕ >0.25	0	

3.1.4Black tape &Mara tape

NO	Defect item	Criteria	Remark
1	FPC or H/S black tape (minor defect)	1. shift spec: 1) glue to the polarize 【Reject】 2) IC bare 【Reject】 2. left-and-right spec: 1)exceed of FPC edge or H-S edge【Reject】 2) IC bare 【Reject】	
2	No black tape (major defect)	No black tape 【Reject】	
3	Tape position mistake	Not by engineering drawing	

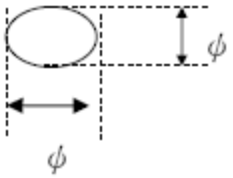
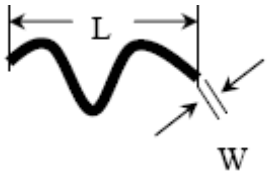
	(minor defect)		
4	Mara tape defect (minor defect)	Peel before pulling the protecting film 【Reject】	

3.1.5Silicon and Taffy glue

NO	Defect item	Criteria	Remark
1	Quantity of silicon (major defect)	Uncover the ITO and circuit area 【Reject】	note: compared by engineering
2	Taffy glue (major defect)	1.Uncover the reveal copper area【Reject】 2.Cover layer 0.3mm(Min)~3.0mm(Max) 【Reject】	note: if customer has special requirement, refer to the technical document 
3	Depth of glue covering (major defect)	Depth of glue covering overtop front Polarizer 【Reject】	Except of the special requirement

3.2Electrical criteria

NO	Defect item	Criteria	Remark
1	No display (major defect)	No display 【Reject】	
2	Missing line (major defect)	Missing line 【Reject】	
3	Seg-com light and dark (major defect)	Seg-com light and dark 【Reject】	ND filter 2% test
4	No display in immobility (major defect)	No display in immobility 【Reject】	
5	Flicker of Pattern (major defect)	Flicker of Pattern 【Reject】	
6	Mura (major defect)	ND filter 2%test	
7	Over current (major defect)	Over current 【Reject】	
8	Voltage out of specification (major defect)	Voltage out of specification 【Reject】	

9	Pattern blur, error code (major defect)	Pattern blur, error code 【Reject】		
10	Dark light, Flicker (major defect)	Dark light, Flicker 【Reject】		
11	Black/white dots 、 Dirty dots、eye winker (major defect)	Specification	Allowable	Note1:disregard if out of AA 
		Φ ≦0.15mm	disregard	
		0.15mm< Φ ≦0. 25mm	2	
		0.25mm< Φ ≦0. 3mm	1	
		0.3mm< Φ	0	
12	Fiber、glass crutch、Polarizer scratch/folded (major defect)	W≦0.03mm	disregard	Note1:L: Length, W: Width Note2: disregard if out of AA 
		0.03mm<W≦0. 0. 05mm L≤3. 0mm	2	
		0.05mm<W≦0. 1mm L≤3. 0mm	1	
		W>0.1mm;L>3.0mm	0	

12.Precautions for using LCD modules.

12.1 Safety

(1)Do mot swallow any liquid crystal ,even if there is no proof that liquid crystal is poisonous.
(2)If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
(3)If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

12.2Srorang Conditions

(4)Store the panel or module in a dark place where the temperature is 23±5℃and the humidity is below 45 ±20%RH.
(5)Store in anti-static electricity container.
(6)Store in clean environment, free from dust, active gas, and solvent.
(7)Do not place the module near organics solvents or corrosive gases.
(8))Do not crush, shake, or jolt the module.

12.3Handling Precautions

(9)Avoid static electricity, which can damage the CMOS LSI.
(10)The polarizing plate of the display is very fragile, please handle if very carefully.
(11)Do not give external shock.
(12)DO mot apply excessive force on the surface.
(13)Bo not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
(14)Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.
(15)Do not operate it above the absolute maximum rating.
(16)Do not remove the panel or frame from the module.

12.4Warranty

The period is within twelve months since the date of shipping out under normal using and storage conditions.

13.Factory

FACTORY NAME:
FACTORY ADDRESS:
FACTORY PHONE:

14.Revision history

Version	Revise record	Date
v0.0	**Original version**	**2014-12-16**
V0.1	**Changed TP Pad**	**2015-02-28**