International Scientific Journal of Contemporary Research in Engineering, Science and Management (ISJCRESM) ISSN : 2456–1134
Vol. 1, Issue 2, Pages : 36-44, June-August 2016.

ADAPTABLE LOW POWER DIGITAL DOWN CONVERTER FOR WIMAX STANDARD

Dr. R. Latha

Associate Professor, Department of Electronics and Communication Engineering
Faculty of Engineering, Christ University, Bangalore, Karnataka, 560 074, India.
Email: lathagopal26@gmail.com

Abstract:-

A fundamental process of many digital communications receivers are accomplished by Digital Down Converters (DDC). Digital radio receivers often utilize fast Analog to Digital Converters (ADC's) to digitise the band limited RF or IF signal generating high data rates; but in many cases, the signal of interest represents a small proportion of that bandwidth. To extract the band of interest from high sample rate would require a prohibitively larger digital filter designs. A DDC allows the frequency band of interest to be moved down the spectrum so that the sampling rate can be reduced, filter requirements and further processing on the signal of interest become more easily realisable. The DDC performs this task by performing the complex task of mixing, filtering and decimation, it is because of this reason it occupies a significant on-chip area and consumes large amount of power as well. In this paper, a novel method to implement the DDC has been presented. The paper focuses on 4G WIMAX Standard. The DDC has been designed and implemented on Xilinx Virtex 4 FPGA using a CORDIC based NCO and CIC based Filter networks. The Noise adaptable DDC has been proposed and area occupied has been analysed.

Keywords: *Digital Down Converter (DDC)*, WIMAX, CIC Filter, Decimation, FPGA, FIR Filters.

1. Introduction

Communication is mainly classified into wired and wireless. The invention of wireless communication has been a boon to mankind. Information can now be transmitted from one place to another, without the use of a physical electrical medium. With the advances in wireless technology, information can be transmitted through a distance of few meters (Ex: Television remote control) to thousands of kilometres (Ex: Radio communication).

This would indeed come at the cost of on-chip area, speed and power where a lot of research is being carried out to optimize the same [1],[2],[3]. The wireless communication technology has evolved from the first generation (1G), which marks the beginning of the mobile cellular era; through the second and third generations (2G, 3G), where technologies such as GPRS, EDGE, GPS, GSM, video conferencing emerged; and now, to the fourth generation (4G), which

provides advanced services such as IP telephony, cloud computing, high-definition mobile TV, etc. When a signal is being transmitted over a wireless medium, it may be affected by Inter-Symbol Interference (ISI) which causes the signal to distort. In order to avoid this, signal scaling is performed. At the transmitter side, the signal is up scaled from baseband to intermediate frequency (IF) signal and transmitted. On the receiver side, the signal is transformed back from IF to baseband frequency. This down scaling operation is performed by a DDC.

In this paper, an efficient 4G Digital Down Converter has been designed and implemented to cater the need of WiMAX standard specification Simulation is performed in MATLAB to verify the functionality of the design [4]. The design is then developed in VERILOG Hardware Description Language, simulated using the ModelSim simulator and then synthesized using the Xilinx Project Navigator. The design of the filter chain forms an intricate part of the DDC in reducing the sampling rate and in performing low pass filtering to obtain the actual baseband spectrum [5].

The two widely known filters that can be used to design the filter chain are: the Finite Impulse Response (FIR) filter and the Infinite Impulse Response (IIR) filter. The IIR filters do not provide linear phase response and are not stable, since they are recursive in nature and it consumes more power. On the other hand, the FIR filters, developed by Parks McClellan, are stable in nature, non-recursive in nature and consume low power[6].

Main advantage of FIR filter is that, it provides optimal filter coefficients using an indirect method. They provide linear phase response which implies that they have symmetrical coefficients. They are more suited for baseband, anti-aliasing and low pass filtering operations. Due to these advantages, FIR filters are used to design the filter chain of the DDC[7].

2. FIR FILTER ARCHITECTURE

Considering an FIR filter with S filter taps. The existing architecture would require S number of multipliers to implement such a filter. This general purpose architecture is known as the “unfolded filter architecture”. The proposed architecture, on the other hand, makes use of the symmetric property of the filter coefficients and provides a way to reduce the number of multipliers used. Thus, in a general case of an FIR filter with symmetrical coefficients, the number of multipliers required reduces to S/2, if S is even or ((S-1)/2) +1, if S is odd. This type of filter design is called the “folded filter architecture” [4]. An example of a 5 tap unfolded and folded FIR filter structure is as shown in Fig. 1.

In this example, S = 5 multipliers are needed in the unfolded architecture, whereas only (S-1/2) +1 = 3 are needed for the folded. Multipliers are the ones that consume majority of the power and space. Each multiplier consists of around 200 full-adders. Thus, the unfolded architecture would require 5*200 = 1000 full-adders, while the folded architecture would just require 3*200 = 600 full-adders. This implies that the unfolded architecture has huge area requirement. The larger the on-chip area, the higher the power consumed. The folded architecture provides a way to reduce this area requirement by a significant amount. Lesser the area required, better the speed and lesser the power consumed.

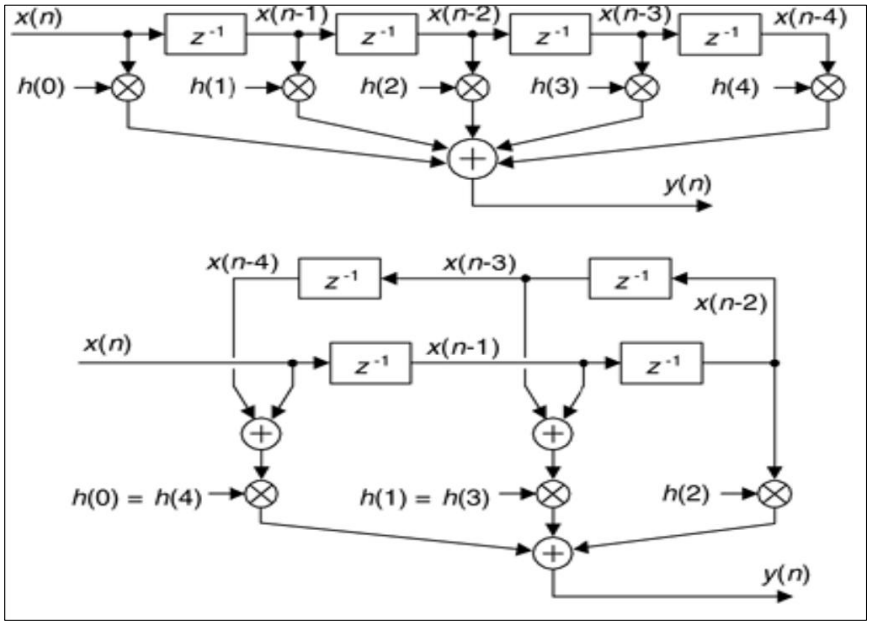

Figure 1 Unfolded and Folded Architecture

3. Design of NCO and Filter Chain

The WiMax based DDC filter structure is shown in Figure 2.The Numerically Controlled Oscillator has been implemented using the widely used, Look-up Table (LUT) approach. The NCO produces a cosine signal having IF frequency. The mixer, upon mixing this signal with the received input signal, produces the baseband frequency signal, which is then fed to the filter chain. The NCO in this paper is done with two algorithm and a comparison on the speed and area is done. The filter chain consists of three levels of filtering [3]. The first stage consists of a 35 tap FIR filter, followed by decimation by a factor of 4 (denoted as D4 in Fig. 1). The transition band for this filter is wide, i.e., it is not sharp. The second stage consists of a 63 tap filter, followed by decimation by a factor of 2 (denoted as D2 in Fig. 1). The transition band for this filter is moderate. The last stage contains a single rate 111 tap filter which provides a sharp transition band. The decimators are used to reduce the sampling rate.

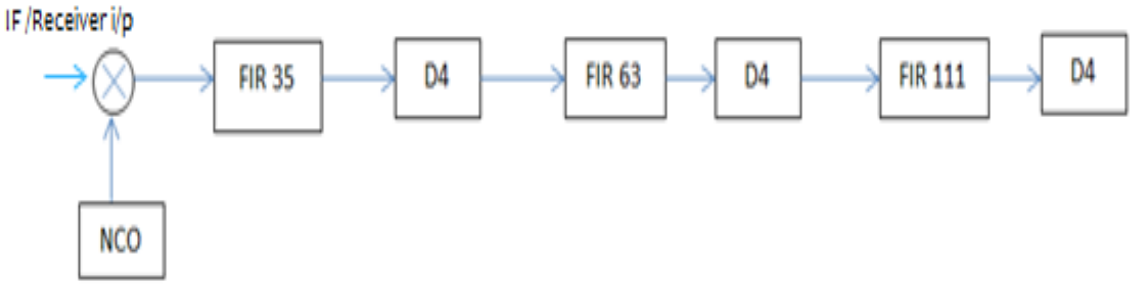

Figure 2 WIMAX Standard Filter Architecture at Receiver

4. PROPOSED METHODOLOGY

The proposed Structure of DDC is shown in Figure 3. As shown in the proposed diagram the signal is obtained at the output of DDC after the filtering stages. The signals are made to enter into the Filter taps inorder to remove the noise. Thus, inorder to extract the noise from the signal, the IF mixed with the NCO is made to pass through High Pass Filter (HPF). HPF is used here because noise is available only at higher frequencies .On extracting the higher frequency components the message signals are not disturbed or mixed with the removed high frequency components, because the Message Signal on its maximum only ranges from 0 to 20kHz. On passing the signal through the filter it is the signal frequency that is being taken care and not the sampling frequency. Hence the transmitted message signal is not affected.
The signal after HPF is decimated by 8 since the total decimation at the signal path is 8. In order to make SNR comparision this process of decimation is taken. Adaptable DDC concept is imported into the DDC model by the Signal to Noise Ratio concept. Though the folded form of architecture is being followed for FIR design to reduce power and area, huge amount of power is still getting wasted. The Filter coefficients are the one which absorb power and occupies memory space. The filter coefficients need to be active only in the presence of noise in the environment. FIR is made up of multipliers and each multiplier increases the power efficiency of filters. Filters are designed to remove the noise, and if noise is less it leads to increase in SNR. If environment noise is very less all the filter networks can be disabled to reduce the power consumption and if the noise environment is high then the filter networks can be enabled such that introducing a new form of adaptable Digital Down Converter.

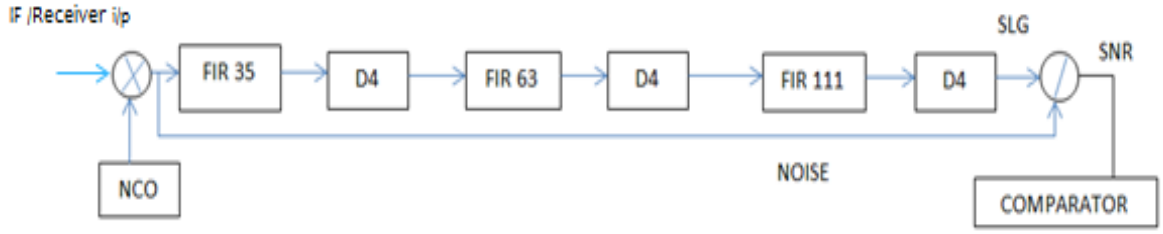

Figure 1 Proposed Block Diagram of WiMAX DDC at the Receiver

5. SIMULATION AND RESULTS

The existing Wimax DDC bock diagram consists of filter tap of 35, 63 and 111 respectively. Initially the filter is to be designed in MATLAB with the pass band frequency to 35 tap as 5 MHz and sampling frequency as 89.6MHz.and other needed specifications[8]. Similarly for 63 tap filter the sampling frequency is about 22.4MHz with pass band frequency of 3.5 MHz, for 111 tap filter the design specification is that the sampling frequency is 11.2MHz and passes band frequency as 3MHz. The attenuation is set as 100dB in common and the designed filter output is as shown in figure 4,5 and 6 respectively.

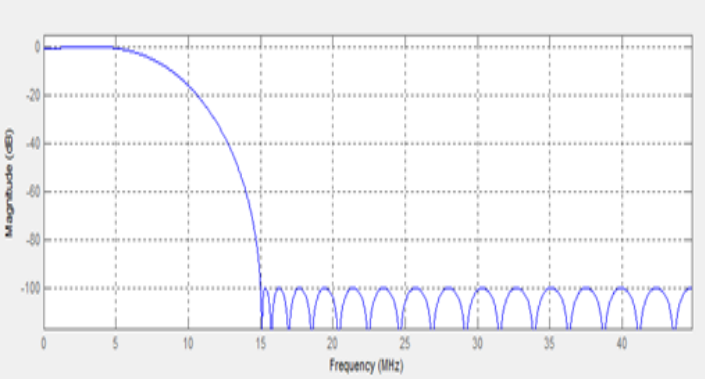

Figure 2 Frequency Response of FIR Filter with 35 tap

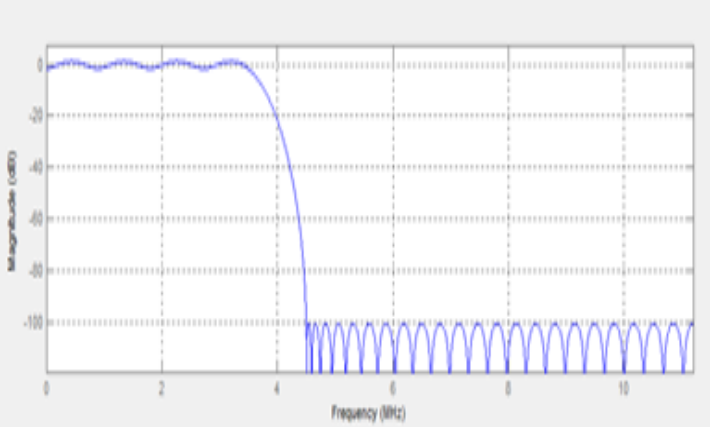

Figure5 Frequency Response of FIR Filter with 63 tap

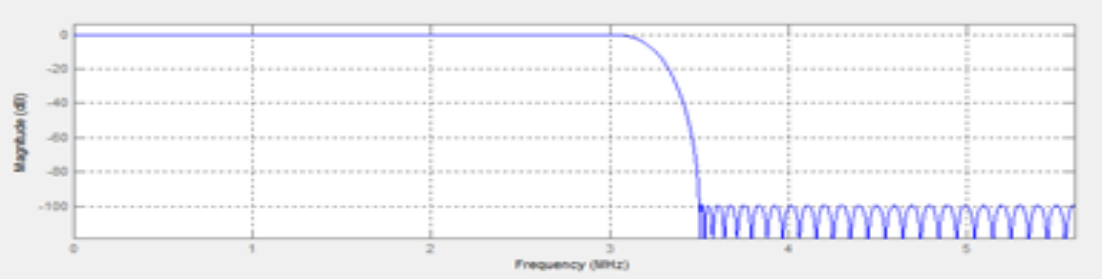

Figure 3 Frequency Response of FIR Filter with 111 tap

The algorithms considered for the design of NCO are Look Up Table and CORDIC Algorithm.

A **lookup table** is none other than the sample and hold circuit, it is an array that replaces runtime computation with a simpler array indexing operation. The savings in terms of processing time can be significant, since retrieving a value from memory is often faster than undergoing an 'expensive' computation or input/output operation. The tables may be pre-calculated and stored in static program storage, calculated (or "pre-fetched") as part of a program's initialization phase, or even stored in hardware in application-specific platforms. The internal LUT operation is shown in Figure 7.

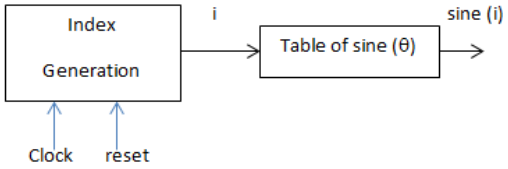

Figure 4 Internal Structure of Look Up Table format

Figure 8 shows the Look Up Table concept output in which the intermediate frequency of WIMAX according to IEEE standard is 89.6 MHz thus the sample values of this frequency is obtained in obtained from MATLAB and the samples are stored and pre-fetched as and when required here in this paper 45 samples are obtained stored as shown below.

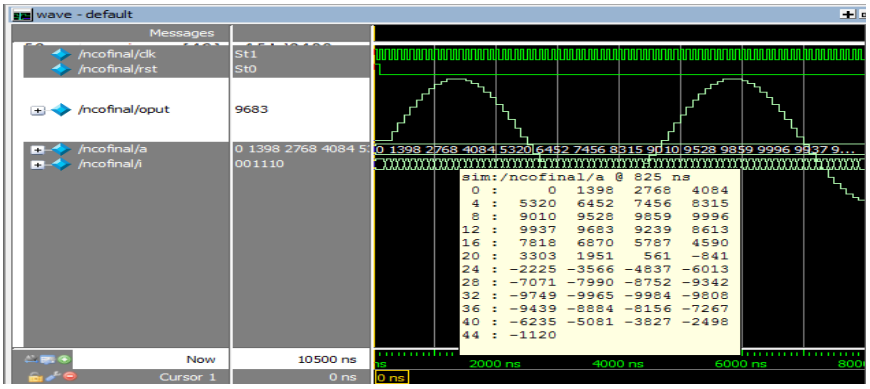

Figure 5 NCO Generated Sine wave with Look Up Table Format

NCO can also be generated using an another form of algorithm namely the CORDIC(**CO**ordinate **R**otation **DI**gital **C**omputer) algorithm also known as **Volder's algorithm**, this algorithm is a iterative method that uses vector rotation to compute the trigonometric functions where it uses shift and add technique. The vector rotation is suitable for hardware implementation. This is also called as Digit –By-Digit method. The internal Structure of CORDIC Algorithm is shown in Fig 9. Figure 10 shows the theta values generated using the CORDIC algorithm.

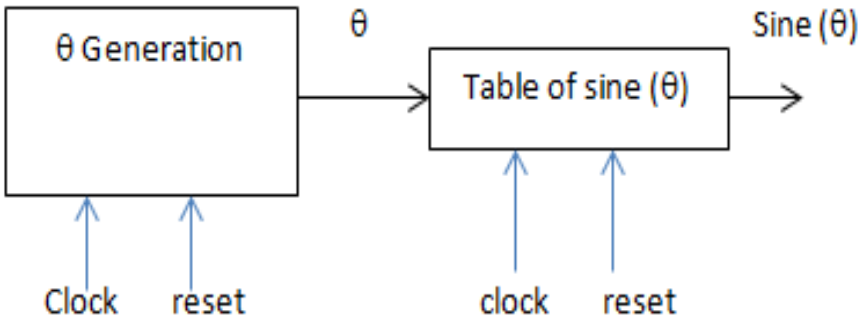

Figure 6 Internal Structure of CORDIC Algorithm

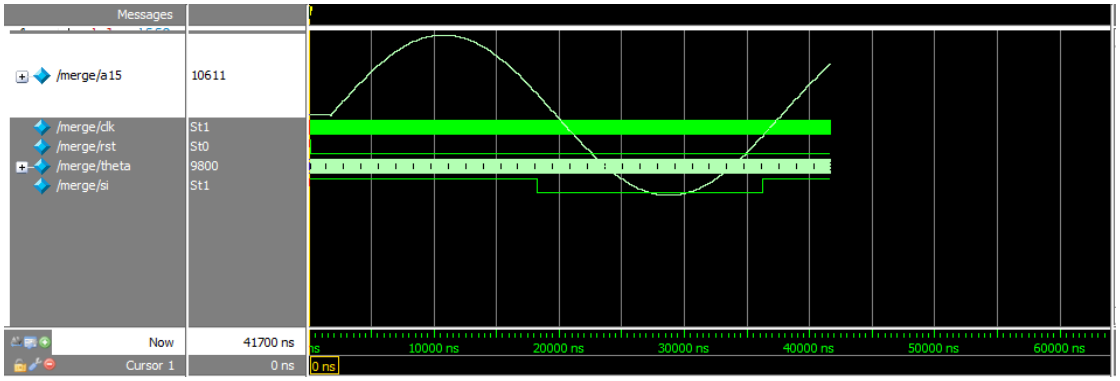

Figure 7 Theta value generated using CORDIC Algorithm in the NCO

Once the NCO generation is completed the next step is the filtering part. For Hardware implementation the coding is to be done in VERILOG. Thus with the Coefficient value obtained from the Filter design in MATLAB the VERILOG code is initially made and as an input the impulse response is considered. Architecture of folded and unfolded consists of delays hence D flip flop is taken into design for delay. Figure 11, 12, 13 shows the VERILOG design output of WIMAX filter.

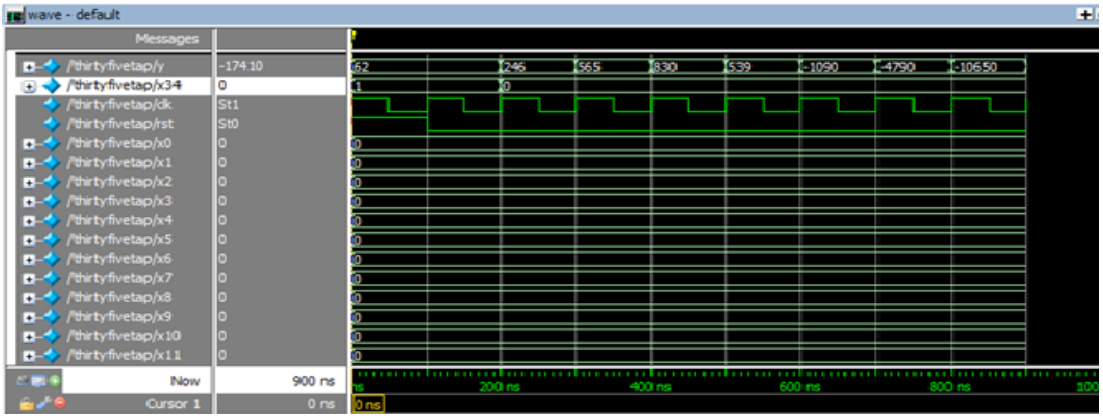

Figure 8 35 Tap Filter Response in VERILOG with Impulse as Input

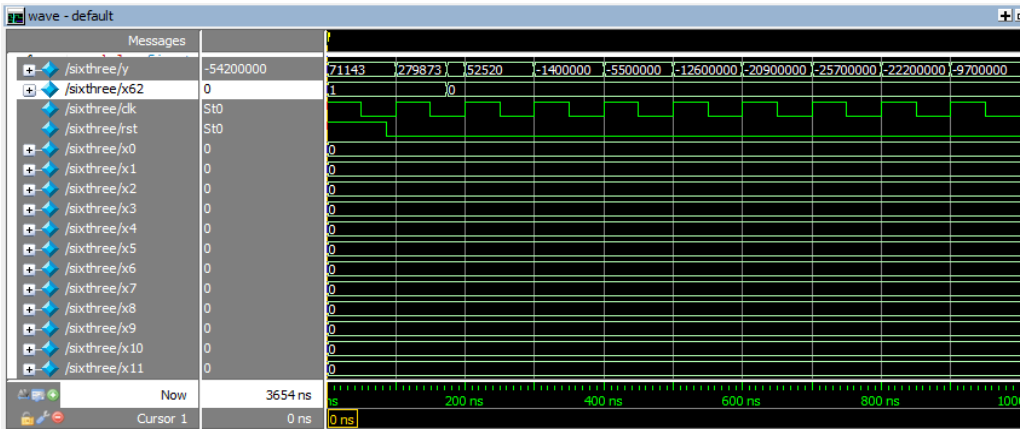

Figure 9 63 Tap Filter Response in VERILOG with Impulse as Input

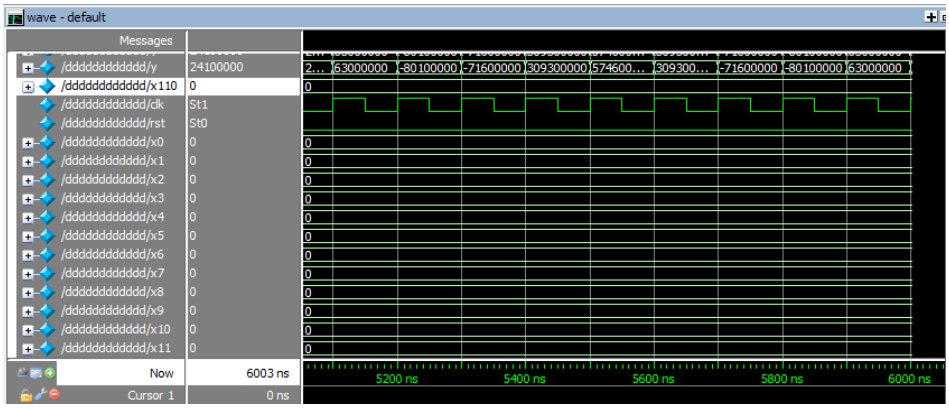

Figure 10 111 Tap Filter Response in VERILOG with Impulse as Input

On analysing the output in VERILOG design it is seen that the coefficients are symmetric in nature. The output obtained for Folded and Unfolded remains the same the only difference is the number of multipliers involved in the designing is reduced in the folded structure.

6. CONCLUSION

An efficient 4G Digital Down Converter has been implemented using VERILOG Hardware Description Language. The filter chain of the DDC has been implemented using both, the existing architecture, i.e. unfolded and the proposed folded architecture. On comparison of the results, it is clearly seen that the folded architecture provides a significant improvement in terms of area efficiency and speed. Future work focuses on implementation of DDC using hardware/ FPGA.

7. REFERENCES

[1] Huddar, S.R.; Rupanagudi, S.R.; Kalpana, M.; Mohan, S., "Novel high speed vedic mathematics multiplier using compressors," Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), 2013 International Multi-Conference on , vol., no., pp.465,469, 22-23 March 2013

[2] Sushma R. Huddar, Sudhir Rao Rupanagudi, Venkatesh Janardhan, Surabhi Mohan, and S. Sandya, "Area and Speed Efficient Arithmetic Logic Unit Design Using Ancient Vedic Mathematics on FPGA," in Advances in Computing, Communication, and Control, pp. 475-483, Springer, Berlin Heidelberg, 2013.

[3] Huddar, S.R.; Rupanagudi, Ramya R.; Yadav S.; Jan S., “Novel Architecture for Inverse Mix Columns for AES using Ancient Vedic mathematics on FPGA,” International Conference on advances in Computing, Communication and informatics (ICACCI). IEEE 2013.

[4] Qingxiang Zhang and Xiaoxiao Su, “The Design of Digital Down Converter Based on FPGA”, Sch. Of Electron. & Inf. Eng., Harbin Inst. Of Technol., Harbin, China, September 2009.

[5] Mingxian Li, Lingyu Chen and Jiang Hong Shi, "Intermediate Frequency Design of Broadband Wireless Adhoc Network System", Dept. of Commun. Eng, Xiamen Univ., Xiamen, China, August 2009.

[6]R.Latha, P.T.Vanathi "Digital Filter Architectures for Multi- Standard Wireless Transceivers", International Journal of Engineering and Technology (IJET) ISSN:0975-4024, Volume 6 No (2), April-May 2014;

[7] R. Latha and P. T. Vanathi, "Hybrid Architecture of Digital Filter for Multi-standard Transceivers", International Journal of Applied Engineering Research ISSN 0973-4562 Volume 9, Number 21 (2014) pp. 11583-11600.

[8] R. Latha and P.T.Vanathi, "Design of Digital Filters for Multi-standard Transceivers", International Journal on Electrical Engineering and Informatics - Volume 7, Number 3, September 2015

Author's Biography

R. Latha obtained her Bachelor's degree in Electronics and Communication Engineering and Master's degree in Applied Electronics from Bharathiar University, Tamil Nadu, India and her PhD degree under Anna University, Chennai, Tamil Nadu, India. At present, she is working as an Academician at Christ University- Faculty of Engineering, Bangalore, in the Department of Electronics and Communication Engineering. Dr. R. Latha's specializations include Microelectronics, Microcontroller Architectures, Digital Signal Processing and VLSI design. Her current research interests are in the area of Multi-rate Digital filter design, wireless Communication and architecture optimization using HDL's.