# Simulation of a Single Phase Cascaded H-Bridge Multilevel Inverter using SHEPWM

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#### **Abstract**

Nowadays Multilevel inverters have been widely used for high-power and high-voltage applications. When compared to conventional two-level inverters, their performance is most superior due to their lower electromagnetic interference, higher dc link voltages, lower total harmonic distortion (THD) and lower switching losses. In this paper, a novel approach for solving non linear transcendental selective harmonic elimination equations by Newton Raphson method is proposed with any random initial guess in a single phase cascaded h-bridge eleven level inverter. Selective harmonic elimination pulse width modulation (SHE PWM) technique is used to minimize lower order harmonics by solving non-linear equations, while the fundamental is satisfied. A simulation in the MATLAB/SIMULINK platform has validated the proposed idea that eliminated the lower order harmonics such as 5<sup>th</sup>, 7th, 11th and 13<sup>th</sup> while maintaining the amplitude of the required fundamental voltage.

**Keywords:** Multilevel inverter, Cascaded H-Bridge multilevel inverter, Total Harmonic Distortion, SHEPWM, MATLAB/SIMULINK

### 1. INTRODUCTION

Numerous industrial applications require electrical power in large quantities and of high quality and the demands are fast growing in recent years [1]. For various industrial drives applications, power-electronic inverters are becoming more popular [2]. A multilevel inverter is a power electronic device having several levels of dc voltages as inputs and produces a desired output voltage. Recently, multilevel power conversion technology has been developing very fast in the area of power electronics with good potential for future developments. As a result, the medium to high voltage range is the most attractive application of this technology [3]. A multilevel inverter not only enables the use of renewable energy sources, but also achieves high power ratings. A multilevel inverter system can be easily interfaced to renewable energy sources such as photovoltaic, wind, and fuel cells for high power applications.

The advantages of multilevel inverters is their smaller stepped output voltage, which results in lower switching losses, lower harmonic components, better electromagnetic compatibility, high voltage capability and high power quality [4]. For both low switching frequency and high switching frequency PWM, multilevel inverters are available with configurations. It must be noted that high switching frequency PWM means lower efficiency and higher switching loss and low switching frequency PWM means higher efficiency and lower switching loss [5].

The patent result search shown that multilevel inverter circuits have been around for more than 25 years. Today, in medium voltage levels with high-power applications, multilevel inverters are widely used [6]. The main field applications are in laminators, pumps, conveyors, compressors, fans, blowers, and mills. Later, there are several topologies have been developed for multilevel converters [7]. There are

three different topologies proposed for multilevel inverters are as follows cascaded multi cell with separate dc sources, diode clamped (neutral-clamped) and capacitor-clamped (flying capacitors). These topologies have a different mechanism for providing the voltage level. The series H-bridge was the first topology introduced and more configurations have been developed for this topology [7]. Since this topology consists of series power conversion cells, the power and voltage levels may be scaled easily. The Series H-bridge topology was followed by the diode-clamped converter that utilized a bank of series capacitors [8]. After few years, flying capacitor topology followed diode-clamped topology. This topology uses floating capacitors to clamp the voltage levels, instead of series connected capacitors [9]. H-bridge inverters do not require either flying capacitor or clamping diode inverters because they have isolation transformers to isolate the voltage source.

Moreover, more than enough modulation techniques and control models have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others [10], [11]. In this paper, in order to generate the switching signals of the power converter a special sinusoidal pulse-width modulation (SPWM) technique was implemented. Some requirements must be satisfied when shoot through states are generated, for instance, shoot-through states have to be uniformly distributed during the whole output voltage period with constant width and the average output voltage should remain unaffected. These features result in several merits, such as low ripple input current, low value of the passive elements, reduction in output voltage THD, and gaining of the desired boost factor[12]. In addition, many multilevel converter focused on applications such as industrial medium-voltage motor drives [13], utility interface for renewable energy systems [14], flexible AC transmission system (FACTS) and traction drive systems [15], [16]. To improve the power quality in the distribution network, Shunt Active Power Filters using PI, PID and Fuzzy Logic Controller (FLC) for power line conditioners (PLC) have been proposed [17]. In order to maintain the output load voltage at the desired value to supply the power for a variety of loads with a minimum THD, a deadbeat-based proportional-integral (PI) controller using a battery cell as the primary energy source for a stand-alone single-phase voltage source inverter has been proposed [18].

In paper [19], in order to eliminate the Total Harmonic Distortion (THD) and improve the power factor, DSTATCOM drawn from a Non-Linear Diode Rectifier Load has been proposed. In this paper [20], a nine stepped multilevel power inverter has been designed, which chooses a multi-PWM optimized using genetic algorithms (GA), and minimizing Total Harmonic Distortion (THD) of the first 50 harmonics to about 0% has been presented. In addition,[21] a 43-level asymmetric uniform step cascaded multilevel inverter (CMLI) has been introduced which consists of four H-bridges per phase, with different dc sources of values E, 2E, 7E and 11E and a mixed integer linear programming (MILP) optimization model was employed to determine the switching angles of the CMLI power switches which can minimize the values of any undesired harmonics.In [22], the elimination of harmonics for multilevel converters by a genetic algorithm is proposed. However, this method is only applicable to equal dc sources and needs considerable computational time. Moreover, for some modulation indexes this method has failed to find switching angles which have solutions [23],[24].

In this paper, Selective harmonic elimination pulse width modulation technique is used to eliminate low order harmonics by solving non-linear equations, while the fundamental is satisfied. Experimental results are presented to confirm the simulation results.

This paper has been arranged as follows. After the introduction in section I, Section II gives an outline of cascaded h-bridge multilevel inverter topology. Selective Harmonic Elimination Pulse Width

Modulation is presented in Section III. The sections IV show the simulation results that validate the proper operation of the inverter. Conclusion and final remarks are made in Section V.

### 2. CASCADED H-BRIDGE MULTILEVEL INVERTER TOPOLOGY

Fig. 1 and 2 show the Schematic diagram and Output voltage waveform of a single-phase cascaded h-bridge eleven level inverter. A single-phase 11-level inverter is formed by connecting five identical inverter modules in series. All five identical inverter modules having the same magnitude are fed by DC voltage sources. During the positive half cycle, the power electronic switches (Q11, Q13) are in the on-state, and the power electronic switches (Q12, Q14) are in the off-state. Likewise, during the negative half cycle the power electronic switches (Q11, Q13) are in the off-state, and the power electronic switches (Q12, Q14) are in the on-state and vice versa. The output voltage of the inverter has eleven voltage levels from -5 Vdc. to +5 Vdc. Each of the different full-bridge inverter ac output levels are connected in series such that the total voltage waveform is the sum of the inverter outputs.

The number of phase output voltage levels m in a cascaded h-bridge inverter is given by

$$m = 2n+1$$
....(1)

where n is the number of separate dc sources.

Each H-bridge unit produces a quasi-square waveform by phase-shifting the switching timings of its positive and negative phase legs.

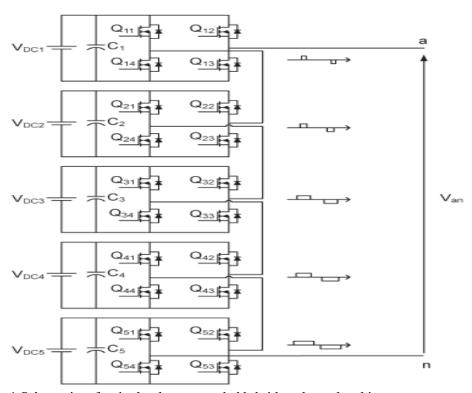


Figure : 1 Schematic of a single-phase cascaded h-bridge eleven level inverter

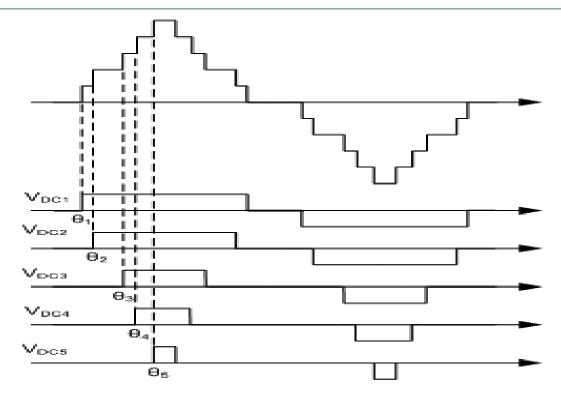


Figure: 2 Output voltage waveform of a single-phase cascaded h-bridge eleven level inverter

### 3. SELECTIVE HARMONIC ELIMINATION PULSE WIDTH MODULATION (SHEPWM)

SHE PWM technique uses many mathematical approaches to eliminate specific harmonics such as 5th, 7th, 11th and 13<sup>th</sup> harmonics. Selective Harmonic Elimination PWM (SHE PWM) technique is used to find appropriate switching angles namely $\theta$ 1,2, $\theta$ 3,...,  $\theta$ N so that the (N-1) odd harmonics can be eliminated and control of the fundamental voltage is also achieved. The harmonic components in the symmetric staircase waveform can be describes as follows:

- \* dc component amplitude equals zero
- \* fundamental component amplitude, n = 1, and odd harmonic component are given by:

h1= 4Vdc/π cos θk sk=1 , and hn= 4Vdc/nπ cos nθk sk=1

\* All even harmonics amplitude equals zero

Thus, only the odd harmonics need to be eliminated in the quarter-wave symmetric multilevel waveform. The switching angles of the waveform will be adjusted to eliminate the selected harmonics. In order to control the fundamental amplitude and to eliminate the 5th, 7th, 11<sup>th</sup> and 13th lower order harmonics, the nonlinear transcendental equations set (4) must be

solved and the five switching angles  $\theta$ 1,  $\theta$ 2,  $\theta$ 3,  $\theta$ 3 and  $\theta$ 5 are calculated to have a total output voltage with a harmonic minimal distortion rate and to minimize the harmonics for each modulation index.

$$\cos \theta 1 + \cos \theta 2 + \cos \theta 3 + \cos \theta 4 + \cos \theta 5 = 3\pi M/4$$
 .....(1)  
 $\cos 5\theta 1 + \cos 5\theta 2 + \cos 5\theta 3 + \cos 5\theta 4 + \cos 5\theta 5 = 0$  .....(2)  
 $\cos 7\theta 1 + \cos 7\theta 2 + \cos 7\theta 3 + \cos 7\theta 4 + \cos 7\theta 5 = 0$  .....(3)  
 $\cos 11\theta 1 + \cos 11\theta 2 + \cos 11\theta 3 + \cos 11\theta 4 + \cos 11\theta 5 = 0$  .....(4)  
 $\cos 13\theta 1 + \cos 13\theta 2 + \cos 13\theta 3 + \cos 13\theta 4 + \cos 13\theta 5 = 0$  .....(5)

the modulation index for the multilevel inverter waveform is given as:

$$M = h1sV$$

Where, h1 is the fundamental component amplitude. From equation (1), control the amplitude of the fundamental component by varying the modulation index value. The other s-1 nonlinear equations subject to the undesirable harmonic components 5<sup>th</sup>, 7th, 11th and 13<sup>th</sup> to be eliminated. These equations are solved by Newton-Raphson method.

The algorithm for The Newton -Raphson method is as follows and is implemented in MATLAB / SIMULINK Programming environment.

- 1. Assume any random initial guess for switching angles
- 2.  $0 <= \alpha_1 < \alpha_2 < \dots < \alpha_5 <= \pi/2$
- 3. Set Mi = 0.
- 4. Calculate Jacobian matrix
- 5. Compute  $\delta \alpha$  during the iteration
- 6. Update the switching angles
- 7. To bring switching angles between zero and  $\pi/2$
- 8. Repeat the steps (3) to (6) for sufficient number of iterations to attain error goal.
- 9. Repeat steps (2) to (8) for whole range of Mi.
- 10. Increment Mi by a fixed step.
- 11. Repeat steps (2) to (8) for complete range of Mi.

#### 4. SIMULATION RESULTS

A simulation is carried out in MATLAB/SIMULINK software for an eleven level cascaded H-bridge inverter with equal dc sources to validate the computational results for switching angles. The elements

and the parameters considered for simulation are presented in Table I for the cascaded h-bridge eleven level inverter topology.

Parameters	Values
No. of H-Bridge levels	5
No. of Switches	20
DC source voltage for individual H- bridge	17.5V
Fundamental frequency	50Hz
Load resistor	100 Ohm
Load Inductor	40mH

Table I Parameters Of The Cascaded H-Bridge Inverter

The simulation model of cascaded h-bridge eleven level inverter topology using SHE PWM is shown in fig.3. The main power circuit consists of five H-bridges whose dc voltage is considered to be 34.8 V and the eleven level stepped output voltages are obtained and the harmonics are reduced. It also consists of PWM block and has parameters as amplitude, pulse width period and phase delay which is used to determine the shape of the output .Therefore the inverter efficiency is increased. The inverter must perform reliably and efficiently to supply a wide range of ac loads with the voltage and required power quality necessary for reliable and efficient load and system performance. The advantages of the proposed topology are high power high voltage handling capability, lower harmonics and lower switching loss. The output voltage and output current of cascaded h-bridge eleven level inverter has eleven levels. The inverter fundamental frequency is 50 Hz. The loads are connected across the cascaded H-bridge eleven level inverter is shown in fig.4.

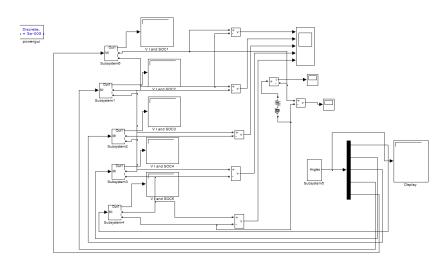


Figure: 3 Simulation model of cascaded h-bridge eleven level inverter topology

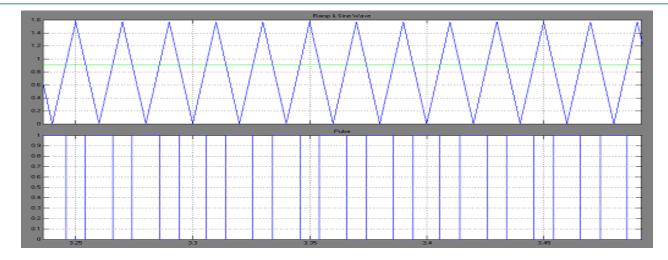


Figure : 4 PWM signals for Cascaded h-bridge eleven level inverter

The Output voltage and current waveform of Cascaded h-bridge eleven level inverter are shown in fig. 5 & 6.

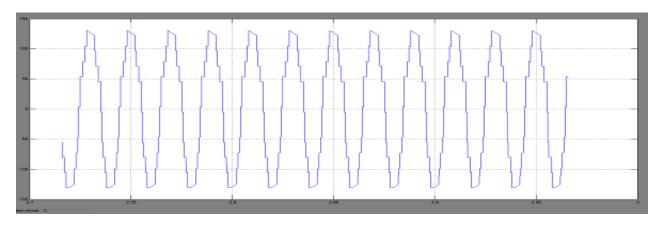


Figure: 5 Output voltage waveform of Cascaded h-bridge eleven level inverter

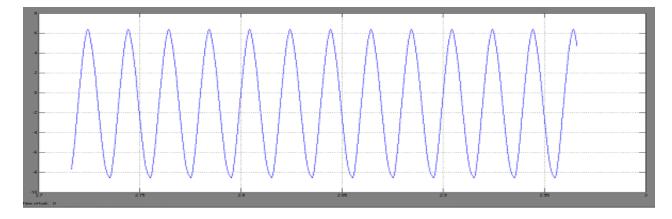


Figure: 6 Output current waveform of Cascaded h-bridge eleven level inverter obtained.

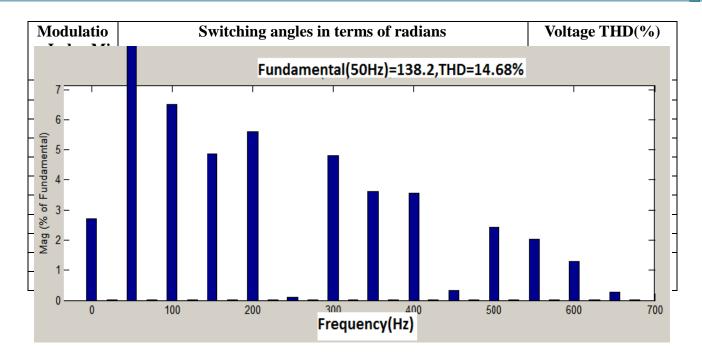


Figure: 7 Harmonic spectrum of the inverter output voltage

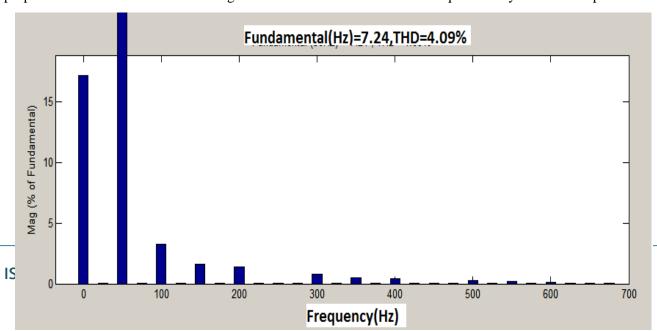
Figure: 8 Harmonic spectrum of the inverter output current

From the harmonic spectrum of the inverter output voltage and output current shown in fig.7 & 8, it can be seen that the magnitudes of lower order 5th, 7th, 11th, and 13th harmonics are negligible. The NR algorithm is simulated at different modulation indices and at each modulation index % Voltage THD and switching angles are tabulated in Table II. From Table II, it is observed that least %THDv i.e 14.68% is produced at modulation index of Mi = 0.84.

Table II - % Voltage THD and switching angles

#### 5. CONCLUSION

In this paper, elimination of lower order harmonics such as 5<sup>th</sup>, 7th, 11th and 13<sup>th</sup> using SHEPWM strategy is investigated and the amplitude of the required fundamental voltage is maintained. The proposed method is used for solving non linear transcendental SHE equations by Newton Raphson



method with any random initial guess in a single phase cascaded h-bridge eleven level inverter. Simulation results also illustrate the performance and effectiveness of the proposed circuit for generates a high-quality output voltage waveform and harmonic components of output voltage are low.

### REFERENCES

- [1] J. Rodriguez, J. S. Lai and F. Z. Peng, "Multilevel inverters: Survey of topologies, controls, and applications," IEEE Trans. Ind. Elect., vol. 49, no. 4, pp. 724-738, Aug. 2002.
- [2] Beser, E.; Camur, S.; Arifoglu, B.; Beser, E.K., "Design and application of a novel structure and topology for multilevel inverter," in Proc. IEEE SPEEDAM, Tenerife, Spain, 2008, pp. 969 974.
- [3] R.H. Baker, "High-Voltage Converter Circuit," U.S. Patent Number 4,203,151, May 1980.
- [4] S. Mekhilef and M. N. Abdul Kadir "Voltage control of three-stage hybrid multilevel inverter using vector transformation" IEEE Trans. Power Electron.,vol.25,no.10,pp 2599-2606, Oct. 2010.
- [5] L.M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel PWM Methods at Low Modulation Indices," IEEE Trans. Power Electron.,vol. 15, no. 4, pp. 719-725, July 2000.
- [6] M. N. A. Kadir S. Mekhilef, and H. W. Ping "Voltage vector control of a hybrid three-stage eighteen-level inverter by vector decomposition" IET Trans. Power Electron.,vol.3,no. 4, pp.601-611, 2010.
- [7] E. Babaei, M. T. Haque, and S. H. Hosseini, "A novel structure for multilevel converters," in Proc. ICEMS, 2005, vol. 2, pp. 1278–1283.
- [8] A.Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Applicat., vol. IA-17, no. 5, pp. 518–523, Sep./Oct 1981.
- [9] T. A. Meynard and H. Foch, "Multilevel conversion: High voltage choppers and voltage-source inverters," in Proc. IEEE PESC, Toledo, Spain 1992, pp. 397–403.
- [10] S. Mekhilef and M. N. Abdul Kadir "Novel vector control method for three-stage hybrid cascaded multilevel inverter" IEEE Trans. Ind. Elect., vol. 58, no. 4, pp. 1339-1449, May 2010.
- [11] S. Mekhilef, A. M. Omar and N. A. Rahim, "Modeling of three-phase uniform symmetrical sampling digital PWM for power converter" IEEE Trans. Ind. Electron.,vol. 54, no. 1, pp.427-432, Feb. 2007.
- [12] Carlos Roncero-Clemente, Oleksandr Husev, V. Miñambres-Marcos, Enrique Romero-Cadaval, Serhii Stepenko, Dmitri Vinnikov, "Tracking of MPP for three-level neutral-point-clamped qZ-source off-grid inverter in solar applications". Informacije MIDEM. Journal of Microelectronics, Electronics Components and Materials. ISSN 0352-9045, Vol.43, No. 4, 2013, pp. 212-221. December 2013.
- [13] M. F. Aiello, P. W. Hammond, and M. Rastogi, "Modular Multilevel Adjustable Supply with Parallel Connected Active Inputs," U.S. Patent 6301 130,Oct. 2001.

- [14] L. M. Tolbert, F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems," in Proc. IEEE Power Eng. Soc. Summer Meeting 2000, vol. 2, pp. 1271-1274.
- [15] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel Inverters for Electric Vehicle Applications," IEEE Workshop on Power Electronics in Transportation, Dearborn, Michigan, 1998, , pp. 1424-1431.
- [16] M.N.Abdul Kadir S.Mekhilef and H.W.Ping, "Dual vector control strategy for a three –stage hybrid cascaded multilevel inverter," Journal of power Electronic, vol.10, no.2,pp.155-164,2010.
- [17] P. Karuppanan and Kamalakanta mahapatra, "PI ,PID and Fuzzy logic controlled cascaded voltage source inverter based active filter for phone line conditioners", Wseas transactions on power systems,vol.6 ,no.4 ,pp 100-109, Oct 2011.
- [18] Towleong Tiang and Dahamen Ishak, "Modelling and simulation of dead beat based PI controller in a single phase H-bridge inverter for standalone applications", Turkish journal of electrical engineering and computer sciences, 22, pp 43-56,2014.
- [19] B. Suryajitt, G. Sudhakar," Power Quality Improvement Using Cascaded H-Bridge Multilevel Inverter Based Dstatcom" Int. Journal of Engineering Research and Applications, ISSN: 2248-9622, Vol. 4, Issue 11(Version 3), pp. 31-37, November 2014.
- [20] Jorge Luis Diaz Rodriguez, Luis David Pabon, Aldo Pardo Garcia," THD improvement of a PWM cascade multilevel power inverters using genetic algorithms as optimization method" WSEAS TRANSACTIONS on POWER SYSTEMS, Volume 10, pp 46-54, 2015.
- [21] Mahmoud El-Bakry," A 43-level filterless CMLI with very low harmonics values" Journal of Electrical Systems and Information Technology, Volume 1, Issue 3, 2015.
- [22] B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, "Harmonic optimization of multilevel converters using genetic algorithms," IEEE Power Electron. Lett., vol. 3, no. 3, pp. 92–95, Sep. 2005.
- [23] H. Taghizadeh and M. Tarafdar Hagh," *Harmonic Elimination of Cascade Multilevel Inverters with Nonequal DC Sources Using Particle Swarm Optimization*," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3678-3684, Nov. 2010.
- [24] T.Jeevabharathi and V.Padmathilagam," Harmonic Elimination of Cascaded Multilevel Inverters Using Particle Swarm Optimization,"International Conference on Computing, Electronics and Electrical Technologies [ICCEET],pp301-306,2012.