Sushil Agarwal

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Profile

Senior Software Engineer with 25+ years of international experience in architecting, designing, implementing, testing and maintaining embedded software. An enthusiastic team player with an extensive background in Telecommunications and Operating Systems.

Technical Skills

- Extensive 'C' programming experience in areas such as embedded software, UNIX kernel, and router software.
- Solid understanding of the full software product life cycle (Waterfall and Agile models) conforming to ISO: 9001 and CMM Standards.
- Proficiency in writing Device Driver Development in UNIX.
- Championed the performance enhancements in UNIX SVR2.0 kernel to meet soft real-time requirements.
- Solved complex defects in UNIX SVR4.0 (ESMP) running on SIMD architecture.
- Designed and developed hardware diagnostics tests in embedded systems.
- Developed soft real-time OS (RTOS) for M68010 processor.
- Experienced in industrial firewall software including; Deep Packet Inspection (DPI), LUA signature, code optimization, IPS/IDS, and fixing vulnerabilities.
- Proficient with communication protocols such as TCP/IP, x.25, LAPB, HDLC VoIP, SS7, and ATM.
- Hands on experience using tools and technologies such as SCM (git, clearcase), Extraview, Gerrit, Jenkin, Coverity (static code analyzer), CodeCollaborato, CodeStriker, cscope, make, gcc, gdb, kernel-debugger, and Agile base development.
- Software configuration and release management experience.

Professional Experience

Staff Software Engineer, *GE Digital (formerly Wurldtech Security Technologies),* Vancouver 2014 – Present

- Enhanced industrial firewall by implementing protocol sniffer and hardening DPI Engine code for industrial space.
- Detected potential security evasions by writing rule based signature.
- Mitigated potential threats and vulnerabilities by strengthening standard protocols.

Senior Software Engineer, *Ericsson Canada (formerly Redback Networks),* Burnaby 2003 – 2014

Maintained and enhanced embedded software for BRAS and Edge router family of product line. Specifically:

- Developed Open Management Interface models for device configuration in Smart Service Router using IBM RSA tool chain to facilitate configuration through NETCONF.
- Ported the admin layer and related modules in packet source tree on Smart Ethernet chassis (SM480), enhanced the card level configuration to support E-CHT PPA2 cards, blocked the BRAS functionality at CLI level and reformatted the output of numerous operator commands to reflect the new E-CHT and cross connect controller cards.
- Addressed problems relating to 64-bit porting in BSD modules.
- Designed, developed and unit tested the feature to force core dump on active system module from standby module to better diagnose the active SM hang issues.
- Actively participated in day-to-day customer support activity by triaging the field issues, doing detailed investigation of system crashes (including reproduction in LAB) and providing possible software remedies.
- Enhanced the IP Access Control List (ACL) to detect and mark real time traffic (RTP/RTCP packets) for VoIP project.
- Architected and implemented a configuration mechanism based on "QoS policy" abstraction to allow individual subscriber to change packet internal priority based on classification ACLs.
- Designed and implemented PVC level policing in ATM. Also fixed various defects in existing rate limiting/policing algorithm.
- Added additional diagnostic capabilities on ATM OC12 I/O to improve the diagnosis of environmental failures.

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Professional Experience (Cont.)

Senior Software Engineer, *Intel Corporation (formerly Trillium Digital Systems),* Vancouver 1999 – 2003

- Architected the testing strategies and developed the Conformance Verification Plan for Xscale core components of ATM toolkit project targeted on Intel Network Processor (IXP2400 platform).
- Designed, developed, and unit tested "Statistics Manager" module in simulated environment using Microsoft Visual Studio on Windows NT. Conducted peer level review of High Level Design.
- Reinforced coding guidelines in IP QoS software building blocks. Built the QoS blocks on Windows NT platform using cigwin and GNU cross platform tools. Demonstrated the inter-working of QoS blocks using HP/Agilent Broadband Series Test equipment.
- Conducted SS7 level-2 protocol testing using I-NET protocol tester against Q.781 specifications.
- Led the porting of virtual OS API on customer hardware platform. As a part of porting changed memory management (Stream Buffer), Process scheduling and common timer subsystems of virtual OS. Championed the technology transfers of the final product to customer and remotely guided them in defect fixing.

Software Engineer, *Lucent Technologies (formerly Stratus Computer),* San Jose (USA) 1997 – 1999

- Successfully ported 32-bit IO drivers to 64-bit in HP-UX 11.0 kernel.
- Investigated and solved blocking defects in multi-processor (SMP), found during QA and engineering test cycles.
- Implemented Software watchdog in SMP SVR4.2 kernel base. Enhanced Memory driver to report single bit ECC errors.

Staff Programmer, *IBM Corporation,* Poughkeepsie (USA) 1996 – 1997

- Augmented automated performance regression test cases for process management and Inter Process Communication subsystems, on z/OS (OS/ 390 OpenEdition environment).
- Completed performance measurement of 'C' compiler using SpecInt 92 benchmarks, in z/OS on system/390 platform.

Software Analyst, *IBM Corporation,* Bangalore (India) 1995 – 1996

- Designed and developed concurrent connection-less client/server modules using Berkeley Sockets, for for Mercedes Benz in "Exhaust Test System Migration" project. Resolved communication issues during system study phase carried out at customer site in Germany.

Software Engineer, *Center for Development of Telematics (C-Dot),* New Delhi (India) 1990 – 1995

- Led the porting of C.85 protocol, a proprietary protocol derived from x.25 LAPB, device driver from UNIX to mission-critical embedded environment by designing RTOS (priority based task scheduler), developing data transfer protocol between main board and the new board, implementing and testing interrupt service routines and designing 'lock/unlock' APIs for data consistency in multi processor environment.
- Identified bottlenecks in C.85, which is used for inter-processor communication in Digital Switching System (DSS). Suggested improvements for increasing throughput at Link level.
- Enhanced the boot monitor (firmware) to support the multiple h/w boards during power on time. Additionally, reengineered the monitor code so that it fits in current EPROM space.
- Led internal validation and depletion in key field sites and customer support for IOP-XL, a front-end M68010 based UNIX box in C-DOT DSS.
- Championed the performance enhancement in UNIX kernel for soft real-time requirements including; designing SPAWN system call, advising and implementing 'MMU bypass' strategy, and enhancing memory management subsystem.
- Automated the kernel build process for multiple hardware platforms using make and shell scripts.

Worked as a Product Coordinator of IOP-XL, a front-end M68010 based UNIX box in C-DOT Digital Switching System. Scheduled and led performance studies, participated in internal validation processes, visited lead field sites and managed the customer support teams.

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Professional Experience (Cont.)

Member of Technical Staff, *Cadence Design Systems,* New Delhi 1989- 1990

- Developed ASIC library in Verilog, designed and implemented ASIC library development tool (VERILIB)

Education

UBC Continuing Studies, *University of British Columbia,* Vancouver 2003-2003

- C++ Programing Courses.

Bachelor of Technology, *Harcourt Butler Technological Institute,* Kanpur (India) 1985-1989

- Bachelor of Technology in Computer Sciences and Engineering with a GPA of 3.99/4.0.
- Awards & Scholarships

Gold Medalist: Awarded to the top student in the graduating class.
University Merit Scholarship (1985-1989): Full-tuition scholarship renewable over four years for demonstrating academic excellence.

Interests

Enjoys city walking, chess player, reading finance books, and avid yoga practitioner.