EEE 102
INTRODUCTION TO DIGITAL CIRCUIT DESIGN
RECITATION PROBLEM SET 6

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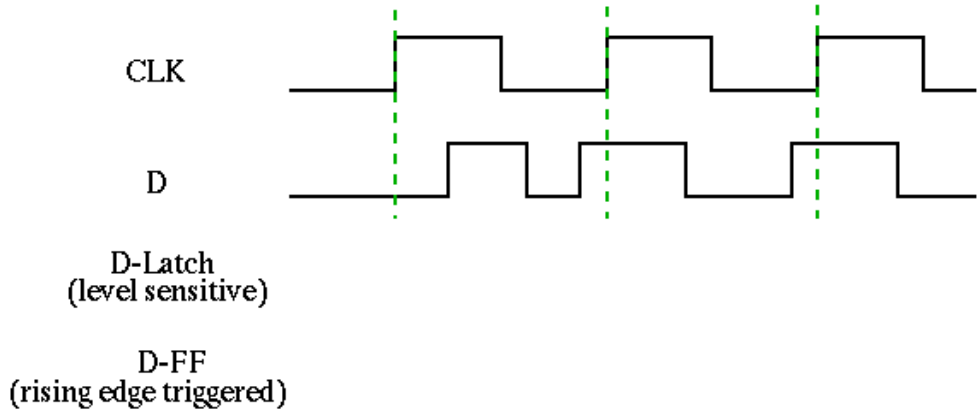
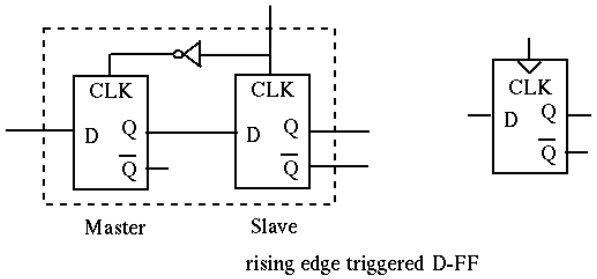
1. Flip Flop Implementation and Timing

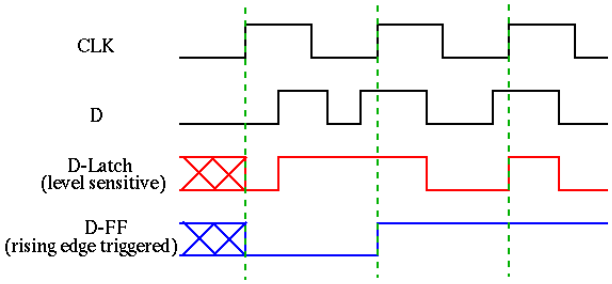
Problem: How to construct a D-FF from two D-Latch?
Complete the timing diagram of the the D-Latch and D-FF for the output Q:



Solution: The operation of a Master-Slave FF has two phases:

(1) During the high period of the clock, the master FF is active, taking both inputs and feedback from the slave FF. The slave FF is de-activated during this period by the negation of the clock so that the new output of the master FF won't affect it.
(2) During the low period of the clock, the master FF is deactivated while the slave FF is active. The output of the master FF can now trigger the slave FF to properly set its output. However, this output will not affect the master FF through the feedback as it is not active.





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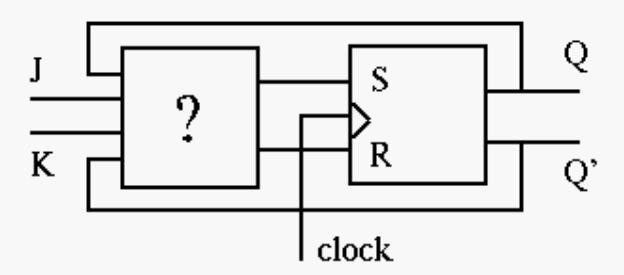
2. Flip Flop Conversion

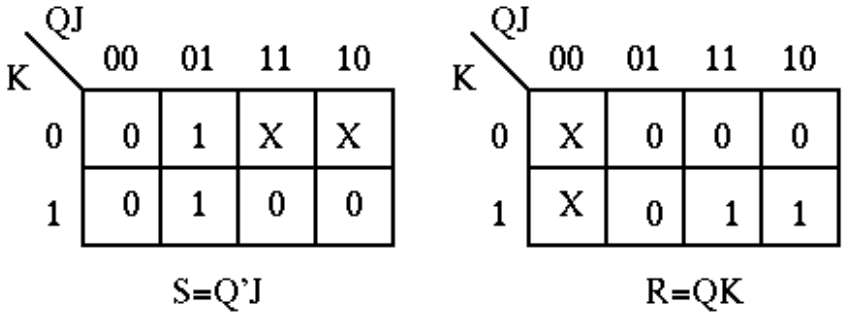
Problem: Convert a RS-FF to a JK-FF. The key here is to use the excitation table, which shows the necessary triggering signal (S,R, J,K, D and T) for a desired flipflop state transition $Q_t \to Q_{t+1}$:

Q_t	Q_{t+1}	S	R	J	K	D	T
0	0	0	x	0	x	0	0
0	1	1	0	1	x	1	1
1	0	0	1	x	1	0	1
1	1	x	0	x	0	1	0

Solution:



The desired signal S and R as functions of J, K and current FF state Q can be obtained from the Karnaugh maps:



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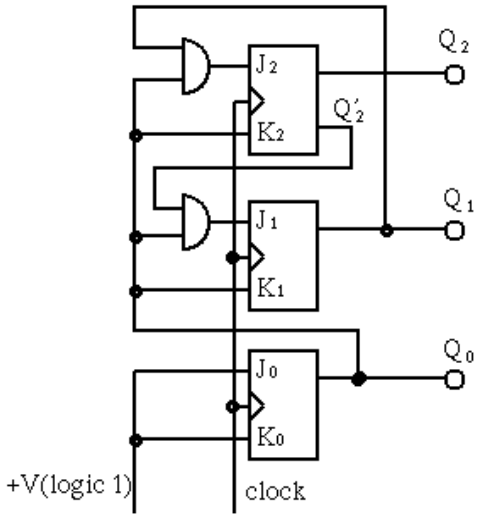
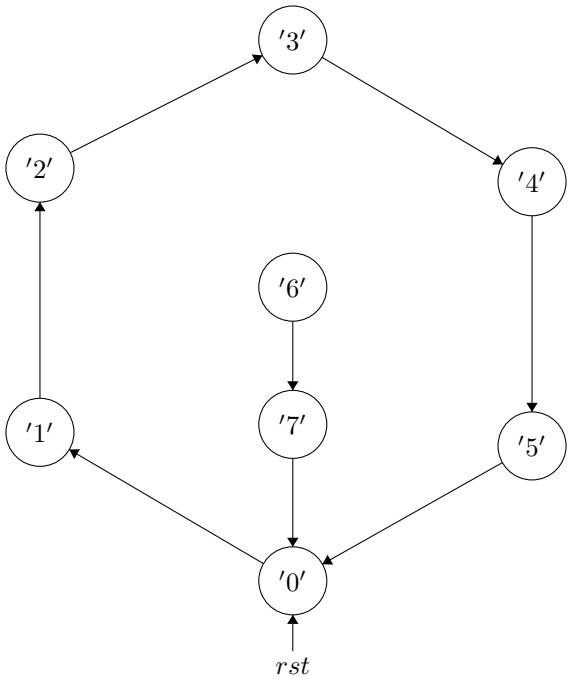
3. FSM Analysis

Problem: The schematic of a J-K flip-flop based FSM is shown below. Derive its state table (in general, the state table of a FSM shows the state and output as functions of previous state and input). Assume the initial state is $Q_0 = Q_1 = Q_2 = 0$, find out what the FSM does by drawing the state diagram.



Solution: $J_0 = K_0 = 1, \quad J_1 = Q_0 Q_2', \; K_1 = Q_0, \quad J_2 = Q_0 Q_1, \; K_2 = Q_0$

$Q_2(t)$	$Q_1(t)$	$Q_0(t)$	$Q_2(t+1)$	$Q_1(t+1)$	$Q_0(t+1)$	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1	1	1	1	1
0	1	0	0	1	1	0	0	0	0	1	1
0	1	1	1	0	0	1	1	1	1	1	1
1	0	0	1	0	1	0	0	0	0	1	1
1	0	1	0	0	0	0	1	0	1	1	1
1	1	0	1	1	1	0	0	0	0	1	1
1	1	1	0	0	0	1	1	0	1	1	1



It is a modulo 6 up counter.

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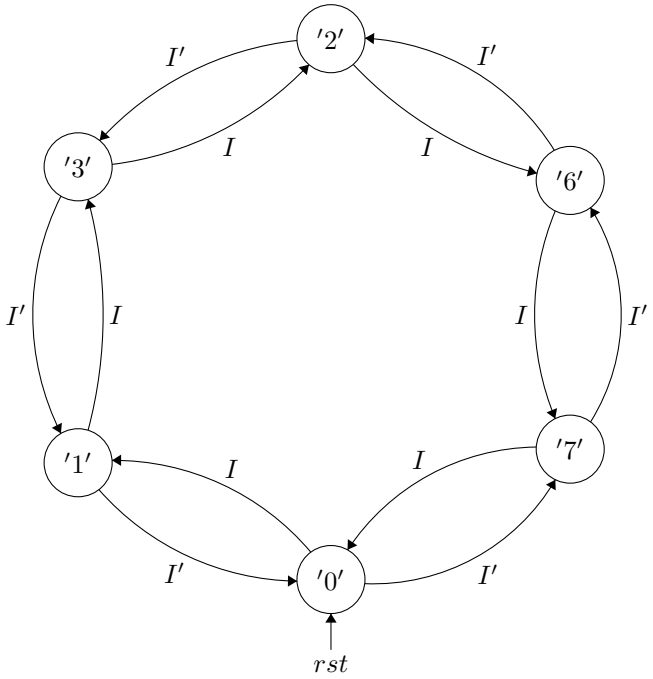
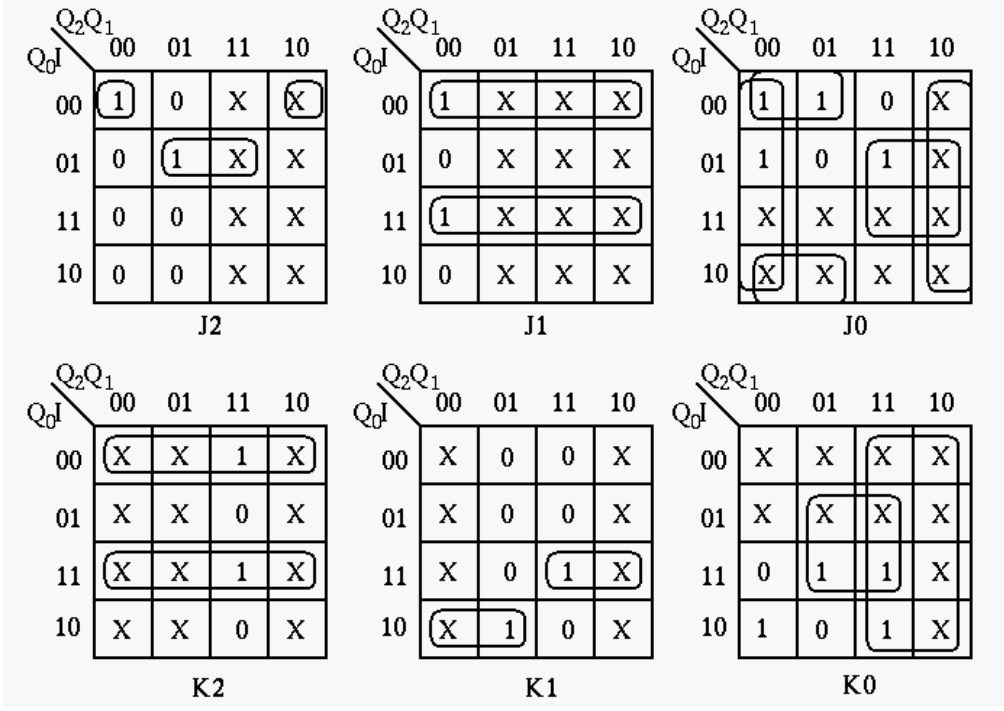
4. FSM Design

Problem: Design a non-ripple 3-bit up-down modulo 6 Gray code counter using 3 JK-FFs. (Modulo 6 counter counts from 0 to 5. In addition to the clock input, another input I is used to control whether the counter will count up (when I=1) or count down (when I=0). What you need to design is the combinational logic for the next-state logic that generates the proper J and K to trigger each JK flop-flop when the next clock pulse comes. The values for the J and K of each JK-FF can be determined from the excitation table, which provides the proper J and K values based on the desired transition from Q(t) to Q(t+1). (Hint: always treat impossible cases as don't cares to simplify the logic.).
Also think about what happens if initial state where 4 or 5. Is it able to continue counting after?

Solution:



	Present State $Q_2\ Q_1\ Q_0$	Input	Next State $Q_2\ Q_1\ Q_0$	$J_2\ K_2$	$J_1\ K_1$	$J_0\ K_0$
0	0 0 0	0	1 1 1	1 x	1 x	1 x
	0 0 0	1	0 0 1	0 x	0 x	1 x
1	0 0 1	0	0 0 0	0 x	0 x	x 1
	0 0 1	1	0 1 1	0 x	1 x	x 0
2	0 1 1	0	0 0 1	0 x	x 1	x 0
	0 1 1	1	0 1 0	0 x	x 0	x 1
3	0 1 0	0	0 1 1	0 x	x 0	1 x
	0 1 0	1	1 1 0	1 x	x 0	0 x
4	1 1 0	0	0 1 0	x 1	x 0	0 x
	1 1 0	1	1 1 1	x 0	x 0	1 x
5	1 1 1	0	1 1 0	x 0	x 0	x 1
	1 1 1	1	0 0 0	x 1	x 1	x 1



$$J_2 = Q_1 Q_0' I + Q_1' Q_0' I', \quad K_2 = Q_0' I' + Q_0 I$$
$$J_1 = Q_0' I' + Q_0 I, \quad K_1 = Q_2' Q_0 I' + Q_2 Q_0 I$$
$$J_0 = Q_1' + Q_2 I + Q_2' I', \quad K_0 = Q_2 + Q_1 I + Q_1' I'$$

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