EEE 102
Introduction to Digital Circuit Design

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Instructor

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- **Unlimited office hours**
  - **Contact me whenever you need help**
  - Best way to contact me: e-mail
  - For appointment: send me an e-mail
  - Response within 24 hours guaranteed

Primary Textbook

- Fundamentals of Digital Logic with VHDL Design, Stephen Brown and Zvonko Vranesic, Fourth Edition, McGraw-Hill, 2023
- Course Website: https://moodle.bilkent.edu.tr/

Supplementary Textbooks

- Logic and Computer Design Fundamentals, M. M. Mano and C. R. Kime, Prentice Hall
- Digital Design Principles and Practices, John F. Wakerly, Pearson Prentice Hall

Lecture Attendance

- You are required to attend at least 15 lectures to be able to take the final exam
- Please make sure to sign your name every lecture and please remind me if I forget to pass the attendance sheet

Recitations (Not Graded)

- Recitations are useful for your learning
- Recitations will be given by the TAs
- You are strongly recommended to attend the recitations and ask many questions (attendance is not required but strongly recommended)
- The first recitation will be during the 4th week
  - Do not miss

Laboratory Work (14%)

- 7 labs (each lab is done individually, not group work)
- Labs are graded equally (2% each)
- The first lab will be **during week 3**
- Please buy the necessary equipment and get ready as soon as possible (preferably this week)

Laboratory Attendance

- **Attendance is mandatory** for the lab sessions
- You need **non-zero grades from all labs in order to be able to take the final exam**
- **Late submission** of lab work will be **penalized**

Project (16%)

- Students choose their own project topic
- Project is done individually (not group work)
- You are required to obtain non-zero grade from the project presentations to be able to take the final exam

Quizzes (0%)

- Quizzes will be submitted online on Moodle
- Deadlines and submission procedures will be announced with the quizzes

Exams (65%)

- Midterm exam (30%)
- Final exam (35%)

Final Exam (35%) Note

- To be able to take the final exam:

1) obtain non-zero grade from the project presentations and labs **AND**

2) attend at least 15 lectures **AND**

3) obtain no disciplinary penalty related with this course

Course Grading

- Attendance (5%)
- Labs (14%)
- Project (16%)
- Midterm exam (30%)
- Final exam (35%)

Warning About Cheating

- You have to do the project by yourself
- **Cheating** (from online resources or other students) will be penalized: **direct FAIL**
- If you have accounts at websites such as chegg, I strongly recommend you to close those accounts now. We will **detect cheaters and they will FAIL** this course.
- FYI: some students were caught cheating in the project and/or exams and failed this course in the past

Suggestions for Success

- Although there is not much MATH required, understanding hardware could be demanding
- You will get lost if you do not attend the lectures
  - Once you get lost, it will be extremely difficult to catch up again

If you have any questions, ask now
** Do not wait until the exam **

- **Understanding** is much more important than memorizing
  - Do the project by yourself and prepare in advance for the exams!!

Tentative Course Outline

- Digital representation of information
- Simple logic gates (not, and, or, nor, nand, xor, nxor). Truth tables. Canonical design. Bubble-to-bubble logic.
- Boolean algebra. Axioms and theorems
- Karnaugh maps and combinational circuit minimization
- Introduction to Very High Speed Integrated Circuits Hardware Description Language (VHDL)
- Number representation and arithmetic circuits
- Decoders, encoders, tristate devices, muxes, and demuxes
- Implementation of combinational circuits with decoders and muxes, comparators, parity circuits, adders-subtractors
- Bistable elements, latches, flip-flops
- Registers and counters
- Synchronous sequential circuits

Course Learning Objectives

With the successful completion of this course:

Students will be able to analyze and design combinational digital circuits

Students will be able to analyze and design basic sequential digital circuits

Students will demonstrate knowledge of the experimental skills on digital circuits

Students will have the ability to design basic digital circuits using a hardware description language (VHDL) and FPGAs

Students will demonstrate engineering skills by working on a design project

Tentative Course Schedule

Week	Start date	Tuesday 8:30PM to 10:20PM for S1 Tuesday 10:30PM to 12:20PM for S2	Thursday 13:30PM to 15:20PM for S1 Thursday 15:30PM to 17:20PM for S2	Activity	Notes
1	Jan 29	Lecture-1	Lecture-2		Jan 29: classes begin
2	Feb 5	Lecture-3	Lecture-4		Feb 2: add/drop Feb 6, 8:00: exam reservation
3	Feb 12	Lecture-5	Lecture-6	Lab 1	
4	Feb 19	Recitation-1	Lecture-7	Lab 2	
5	Feb 26	Lecture-8	Lecture-9	Lab 3	
6	Mar 4	Lecture-10	No class (March 7)	Project Proposal	Mar 7- Mar 10: Spring Break
7	Mar 11	Recitation-2	Lecture-11	Lab 4	
8	Mar 18	Lecture-12	Lecture-13	Revised Project Proposal/Lab 5	Mar 20: Withdraw deadline
9	Mar 25	Recitation-3	Lecture-14	Midterm (after 14 lectures, weekend)	
10	Apr 1	Lecture-15	Lecture-16	Lab 6	
11	Apr 8	No class	No class		Holiday
12	Apr 15	Recitation-4	Lecture-17	Lab 7	
13	Apr 22	No class	Lecture-18	Project Demo	Holiday
14	Apr 29	Recitation-5	Lecture-19		
15	May 6	Lecture-20	Lecture-21		
16	May 13			Project Final Demo	May 17: Last day of classes

Communication

- Communicate with the instructor on a regular basis
- Unlimited office hours with appointment
- Provide feedback from day 1
- Continue to provide feedback throughout the semester
  - What do you

Let us work together for an enjoyable learning experience and a successful semester