Lastname, Name:_____
ID:_____

EEE 102: Digital Systems Design

Final Exam

May 28, 2015

Duration: 90 min

Q	1	2	3	4	Total
Pts	25	25	25	25	100
Score					

This is a closed-book and closed-notes exam.

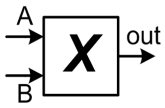
NO CREDIT will be given to answers without clear, formal and clean

JUSTIFICATION.

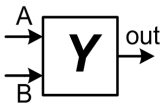
1. **[25 pts]**

   - (a) (5 Points) Design a half adder with a minimum number of 2-1 multiplexers. The complements of the variables are NOT available. However, you can use logic 1 and 0. No other gates are available.
   - (b) (10 Points) Implement F(X,Y,X) = X(YZ+YZ) with a single 2-to-4 decoder and a single 2-to-1 multiplexer.
   - (c) (10 Points) Design a 3-to-8 line decoder using two 2-to-4 line decoders and eight 2-input AND gates.

2. **[25 pts]** Implement a $J-K$ flip-flop using an CD-type flip-flop and a combination of logic gates X and Y given below. Draw the schematic diagram of the $J-K$ flip-flop implemented this way. Complements of the variables are not available. Logic levels 0 and 1 are available. Z denotes that the output is Hi-Z for the given input combination. Complement of the CD-type flip-flop output Q is available. (Hint: Combinational logic gates can be implemented using X and Y).



AB	out
00	1
01	Z
10	Z
11	Z



AB	out
00	Z
01	Z
10	Z
11	0

C	D	$Q(t+1)$
0	0	$\overline{Q}(t)$
0	1	$Q(t)$
1	0	$Q(t)$
1	1	$\overline{Q}(t)$

3. **[25 pts]** Design a counter with three T flip-flops that goes through the following binary repeated sequence: $000 \rightarrow 001 \rightarrow 011 \rightarrow 111 \rightarrow 110 \rightarrow 100$ treating transition out of other states as don't cares. [15 pts]

   Based on this design, what happens when the counter enters the binary states 010 and 101 accidentally? [5 pts]

   Propose a method so that the counter will return to its normal operation even if it enters 010 or 101 accidentally. [5 pts]

4. **[25 pts]**

Design a special integer divider using ASM chart. Given two binary numbers A and B, your circuit should compute $\lfloor A/B \rfloor$, which is the integer number of B's in A. For example, if $A = 7$ and $B = 2$, then the result will be 3. The computation starts when go input $S = 1$.

- (a) Design an algorithm for the divider circuit. You may give it in pseudo-code. [5 pts]
- (b) Built the ASM chart for your divider algorithm. [10 pts]
- (c) Design the control unit of your ASM chart with a minimum number of JK-type flip-flips and combinational circuit elements. [10 pts]