Lastname, Name:_____
ID:_____

EEE 102: Digital Systems Design

Midterm Exam 1

March 13, 2015

Duration: 90 min

Q	1	2	3	4	Total
Pts	25	25	25	25	100
Score					

This is a closed-book and closed-notes exam.

NO CREDIT will be given to answers without clear, formal and clean

JUSTIFICATION.

1. **[25 pts]** Implement the following four functions (at the same time) using only three half adders. Complements of the variables and logic levels 0 and 1 are NOT available.
   $A = X \oplus Y \oplus Z$
   $B = X'YZ + XY'Z$
   $C = X'Z + XYZ' + Y'Z$
   $D = XYZ$

2. [**25 pts**] Design a circuit that takes 2's complement of any four-bit number by using only 3 XOR and minimum number of OR gates.

3. [**25 pts**] Design an even parity check circuit with 3 binary inputs, which counts the number of 1's in its input. If the number of 1's are even, then the output of the circuit is 1. If the number of 1s are odd, then the output is 0.

   - [**12 pts**] Implement in minimal Sum-of-Product form.
   - [**13 pts**] Implement in minimal Product-of-Sum form.

4. **[25 pts]** Implement the following Boolean function using a single 4-to-1 multiplexer and a **minimum** number of combinational gates:

$$F(X, Y, Z, W) = \bar{X}Z + \bar{Z}W + XW + \bar{X}YZ + XYZW.$$

Clearly present your truth table, multiplexer decomposition and schematic circuit.