Lastname, Name:_____
ID:_____

EEE 102: Digital Systems Design

Midterm Exam 2

April 27, 2013

Duration: 90 min

Q	1	2	3	Total
Pts	30	35	35	100
Score				

This is a closed-book and closed-notes exam.

NO CREDIT will be given to answers without clear, formal and clean

JUSTIFICATION.

1. **[30 pts]** Design a special 4-bit register with two 1-bit inputs $S1$ and $S2$. This clocked register performs the following operations depending on its inputs:

S1	S2	Operation
0	0	Circular shift left 1-bit
0	1	Circular shift right 1-bit
1	0	Parallel load
1	1	Idle

2. **[35 pts]**

Design a sequential circuit that outputs 1 when the total number of 1's on the input (including the current input) is a multiple of 3. Otherwise the circuit outputs 0. As an example,

x	0	1	1	0	1	0	1	...
y	0	0	0	0	1	1	0	...

where x is the input and y is the output.

You can only use MB-type flip-flop, where an MB type flip-flop is defined as follows:

M	B	Q(t+1)
0	0	1
0	1	1
1	0	0
1	1	Q(t)

and a minimum number of NAND gates.

3. **[35 pts]** Design an integer divider using an ASM chart. Your machine starts with loading two binary numbers: A in the register $R1$ and B in the register $R2$. Then, it calculates $\lfloor A/B \rfloor$ and stores the result in the register $R3$. Here, $\lfloor A/B \rfloor$ represents the integer number of B's in A. As an example if $A = 5$ and $B = 2$, then the result is $\lfloor A/B \rfloor = 2$ stored in $R3$.

   a. [5 pts] Give the algorithm in a pseudo-code form.

   b. [15 pts] Built the ASM chart for your divider.

   c. [15 pts] Design the control unit of your ASM using a minimum number of D-type flip-flops and combinational circuit elements. **Note:** You do not need to provide the inputs to the registers in your control unit, just the states and the inputs for the control unit are enough. You only need to design the hardware for the control unit, NOT for the other parts of your machine.