Recitation 4

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Example 5.15

Problem: Determine the functional behavior of the circuit in Figure 5.66. Assume that input *w* is driven by a square wave signal.

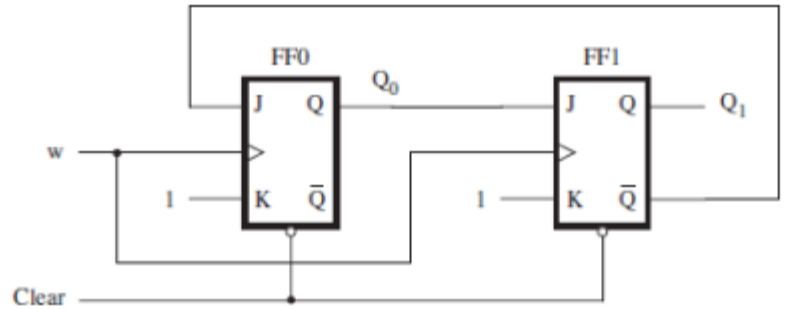


Figure 5.66 Circuit for Example 5.15.

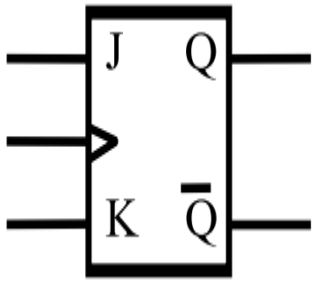
Solution: When both flip-flops are cleared, their outputs are $Q_0 = Q_1 = 0$. After the *Clear* input goes high, each pulse on the *w* input will cause a change in the flip-flops as indicated in Figure 5.67. Note that the figure shows the state of the signals after the changes caused by the rising edge of a pulse have taken place.

Time interval	FF0			FF1		
	J_0	K_0	Q_0	J_1	K_1	Q_1
Clear	1	1	0	0	1	0
t_1	1	1	1	1	1	0
t_2	0	1	0	0	1	1
t_3	1	1	0	0	1	0
t_4	1	1	1	1	1	0

Figure 5.67 Summary of the behavior of the circuit in Figure 5.66.

In consecutive time intervals the values of Q_1Q_0 are 00, 01, 10, 00, 01, and so on. Therefore, the circuit generates the counting sequence: 0, 1, 2, 0, 1, and so on. Hence, the circuit is a modulo-3 counter.

J	K	Q (t+1)
0	0	Q (t)
0	1	0
1	0	1
1	1	$\bar{Q}$ (t)



Problem: Design a circuit that can be used to control a vending machine. The circuit has five inputs: Q (quarter), D (dime), N (nickel), *Coin*, and *Resetn*. When a coin is deposited in the machine, a coin-sensing mechanism generates a pulse on the appropriate input (Q, D, or N). To signify the occurrence of the event, the mechanism also generates a pulse on the line *Coin*. The circuit is reset by using the *Resetn* signal (active low). When at least 30 cents has been deposited, the circuit activates its output, Z. No change is given if the amount exceeds 30 cents.

Design the required circuit by using the following components: a six-bit adder, a six-bit register, and any number of AND, OR, and NOT gates.

Name _____ Date _____

Money: Coins

Coin	Name	Value
	penny	1 cent 1¢ $0.01
	nickel	5 cents 5¢ $0.05
	dime	10 cents 10¢ $0.10
	quarter	25 cents 25¢ $0.25

Solution: Figure 5.68 gives a possible circuit. The value of each coin is represented by a corresponding five-bit number. It is added to the current total, which is held in register *S*. The required output is

$$Z = s_5 + s_4 s_3 s_2 s_1$$

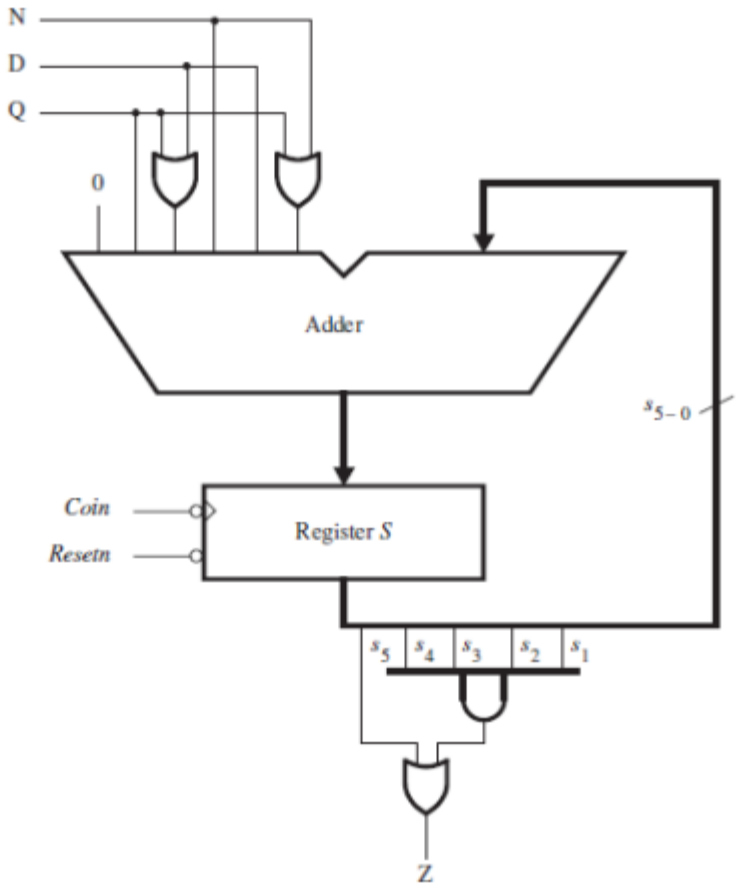


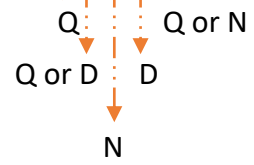
Figure 5.68 Circuit for Example 5.16.

$$(30)_{10} = (011110)_2$$

$$Q\text{: } (25)_{10} = (011001)_2$$

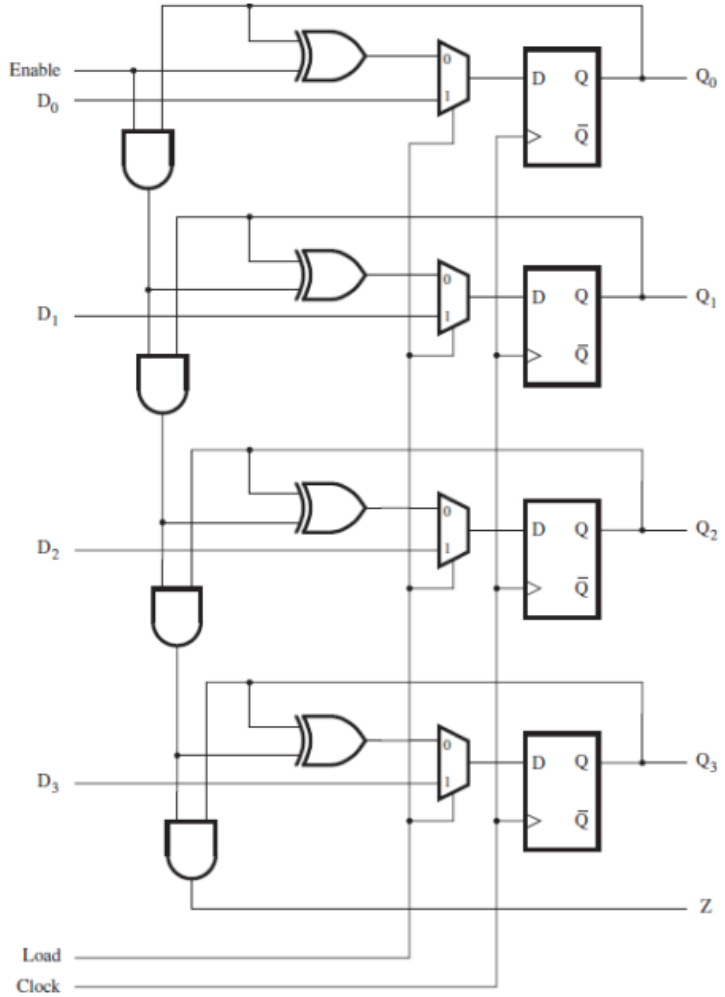
$$D\text{: } (10)_{10} = (001010)_2$$

$$N\text{: } (5)_{10} = (000101)_2$$



The register is clocked by the negative edge of the *Coin* signal. This allows for a propagation delay through the adder, and ensures that a correct sum will be placed into the register.

5.23 For the flip-flops in the counter in Figure 5.24, assume that $t_{su} = 3$ ns, $t_h =$ 1 ns, and the propagation delay through a flip-flop is 1 ns. Assume that each AND gate, XOR gate, and 2-to-1 multiplexer has the propagation delay equal to 1 ns. What is the maximum clock frequency for which the circuit will operate correctly?



The longest delay in the circuit is the from the output of FF_0 to the input of FF_3. This delay totals 5 ns. Thus the minimum period for which the circuit will operate reliably is

$$T_{min} = 3(t_{AND}) + t_{XOR} + t_{2to1} + t_{su} + t_{cQ}$$

$$T_{min} = 5 + 3 + 1 = 9 \text{ ns}$$

The maximum frequency is

$$F_{max} = 1/T_{min} = 111 \text{ MHz}$$

Problem: In Section 5.15 we presented a timing analysis for the counter circuit in Figure 5.62. Redesign this circuit to reduce the logic delay between flip-flops, so that the circuit can operate at a higher maximum clock frequency.

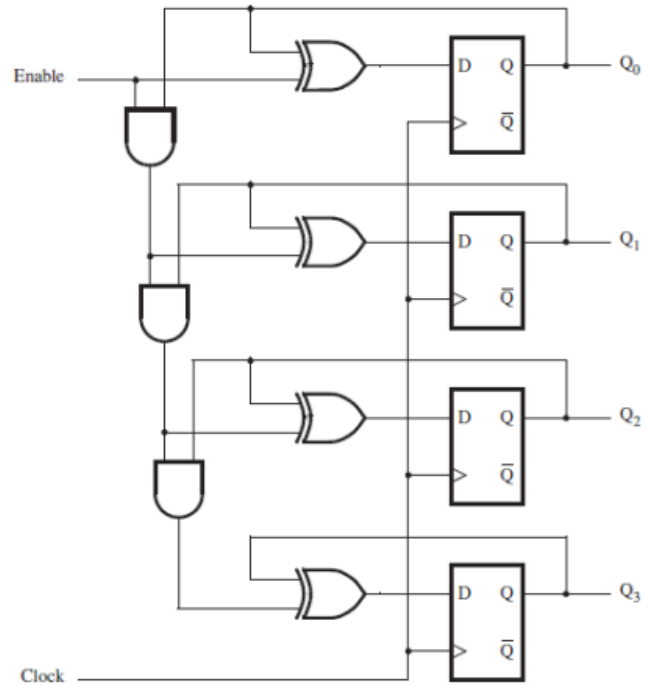


Figure 5.62 A four-bit counter.

$$T_{min} = t_{cQ} + 3(t_{AND}) + t_{XOR} + t_{su}$$

Using the maximum value of t_{cQ} gives

$$T_{min} = 1.0 + 3(1.2) + 1.2 + 0.6 \text{ ns} = 6.4 \text{ ns}$$
$$F_{max} = 1/6.4 \text{ ns} = 156.25 \text{ MHz}$$

Solution: As we showed in Section 5.15, the performance of the counter circuit is limited by the delay through its cascaded AND gates. To increase the circuit's performance we can refactor the AND gates as illustrated in Figure 5.70. We assume that the delay through a logic gate is $1 + 0.1k$, where k is the number gate inputs. The longest delay path in this redesigned circuit, which starts at flip-flop Q_0 and ends at Q_3, provides the minimum clock period

$$T_{min} = t_{cQ} + t_{AND} + t_{XOR} + t_{su}$$
$$= 1.0 + 1.4 + 1.2 + 0.6 \text{ ns} = 4.2 \text{ ns}$$

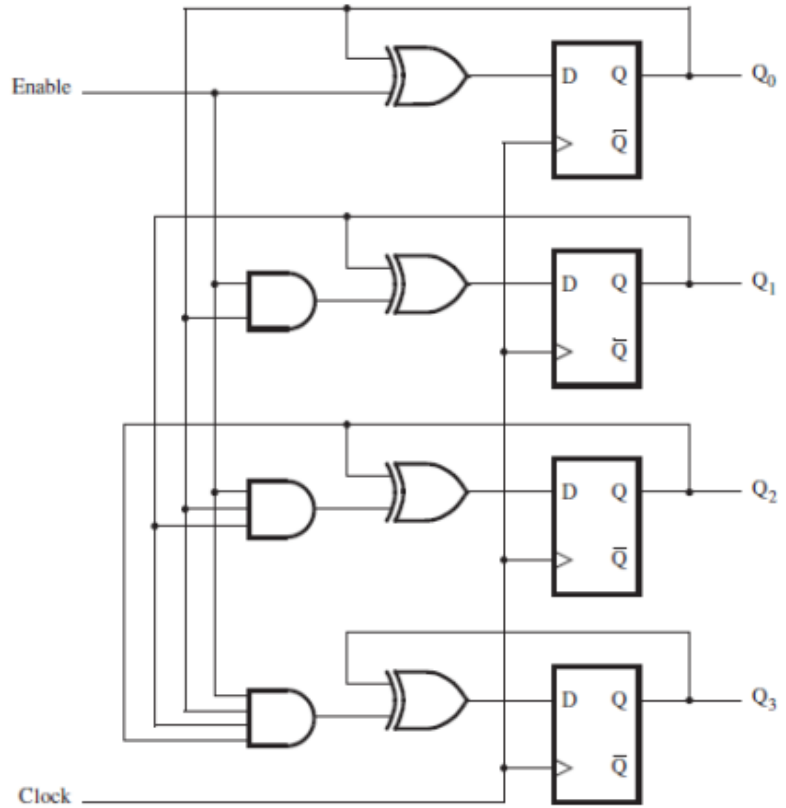


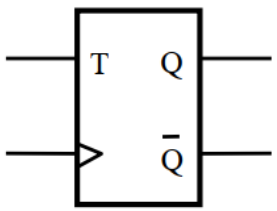
Figure 5.70 A faster 4-bit counter.

The redesigned counter has a maximum clock frequency of F_{max}=1/4.2 ns = 238.1 MHz, compared to the result for the original counter, which was 156.25 MHz.

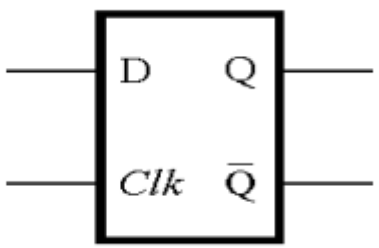
page 300

Q5.
Show how to build a D ff using a T ff with enable and combinational logic.
Solution:

T	$Q(t+1)$
0	$Q(t)$
1	$\bar{Q}(t)$



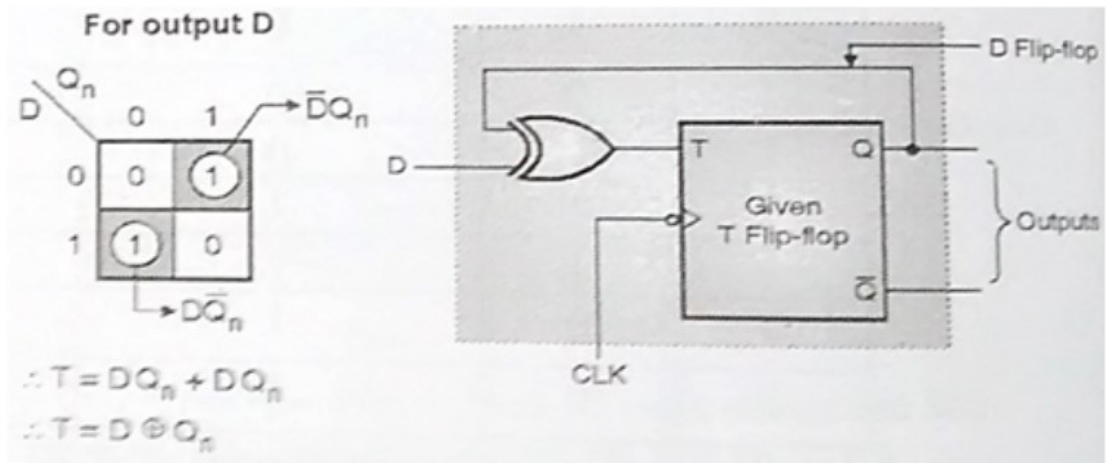
Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1



- A T flip flop can be converted to a D flip flop by the following table and K-map:

Inputs			Output
D	Previous state Q_n	Next state Q_{n+1}	T
0	0	0	0
1	0	1	1
0	1	0	1
1	1	1	0

Fig. Excitation table



5.7 Show how a JK flip-flop can be constructed using a T flip-flop and other logic gates.

Analysis

Step 1:

The characteristic table of the required flipflop i.e JK flipflop is:

J	K	Q_{n+1}
0	0	Q(n)
0	1	0
1	0	1
1	1	$\bar{Q}$(n)

Step-2:

The excitation table of the given flip-flop i.e. T flipflop is:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Step-3:

Finding the boolean expression

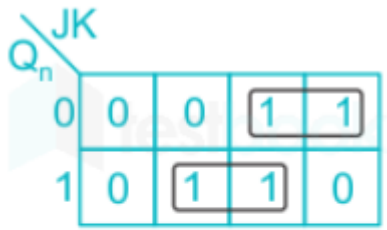
Q_n	J	K	Q_{n+1}	T
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1

5.7 Show how a JK flip-flop can be constructed using a T flip-flop and other logic gates.

Step-3:

Finding the boolean expression

Q_n	J	K	Q_{n+1}	T
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1



$$T = \bar{Q}_n J + Q K$$

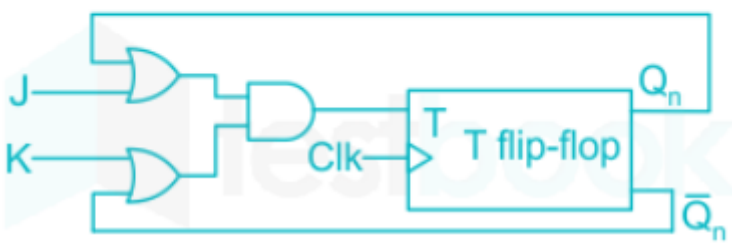
$= J\bar{Q}_n (1 + K) + KQ_n (1 + J)$

$= J\bar{Q}_n + J\bar{Q}_n K + JKQ_n + KQ_n$

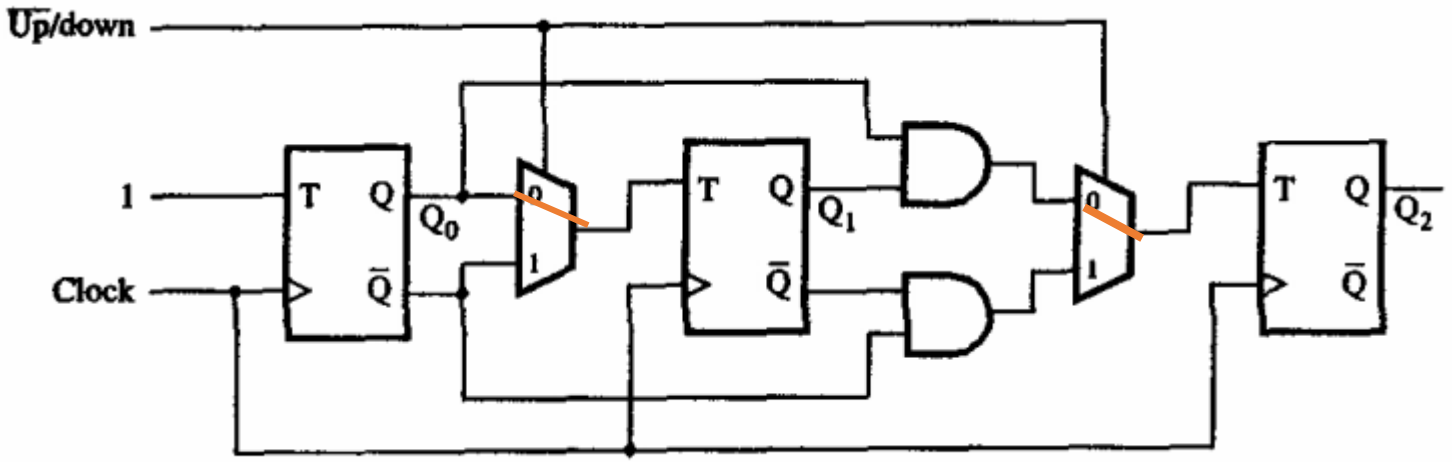
$= J\bar{Q}_n + KQ_n + JK(Q_n + \bar{Q}_n)$

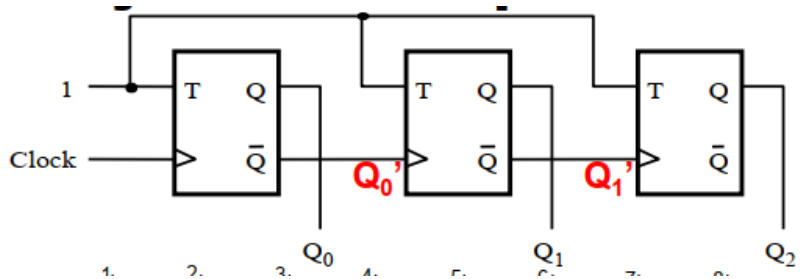
$= (J + Q_n)(\bar{Q}_n + K)$

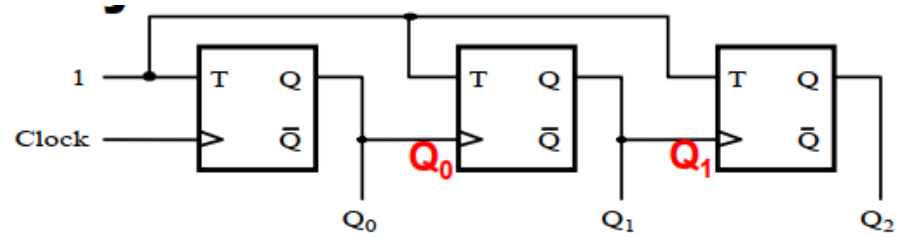
Logic diagram of the above expression will be

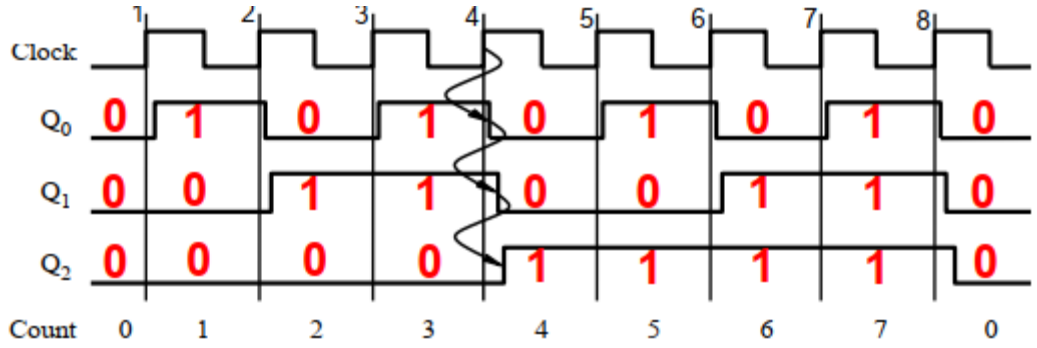


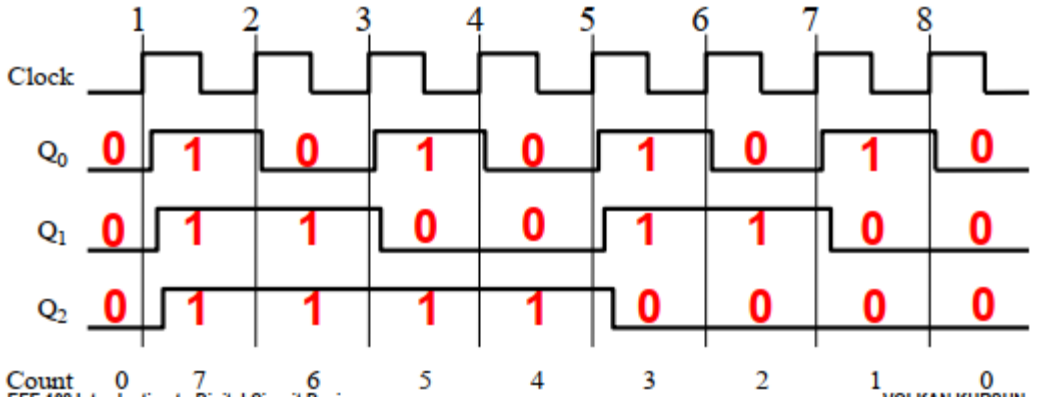
*5.15 Design a three-bit up/down counter using T flip-flops. It should include a control input called $\overline{\text{Up}}/\text{Down}$. If $\overline{\text{Up}}/\text{Down} = 0$, then the circuit should behave as an up-counter. If $\overline{\text{Up}}/\text{Down} = 1$, then the circuit should behave as a down-counter.





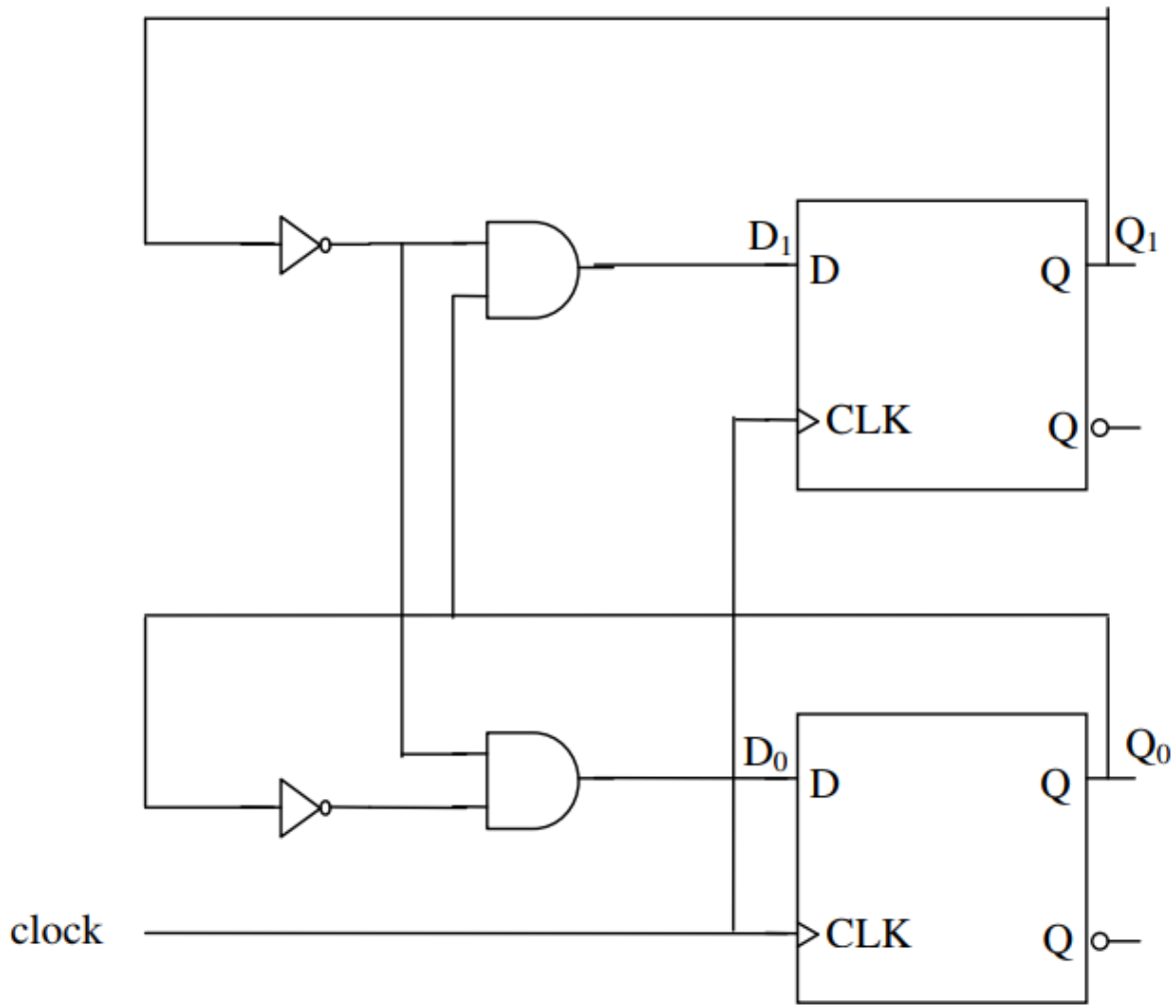






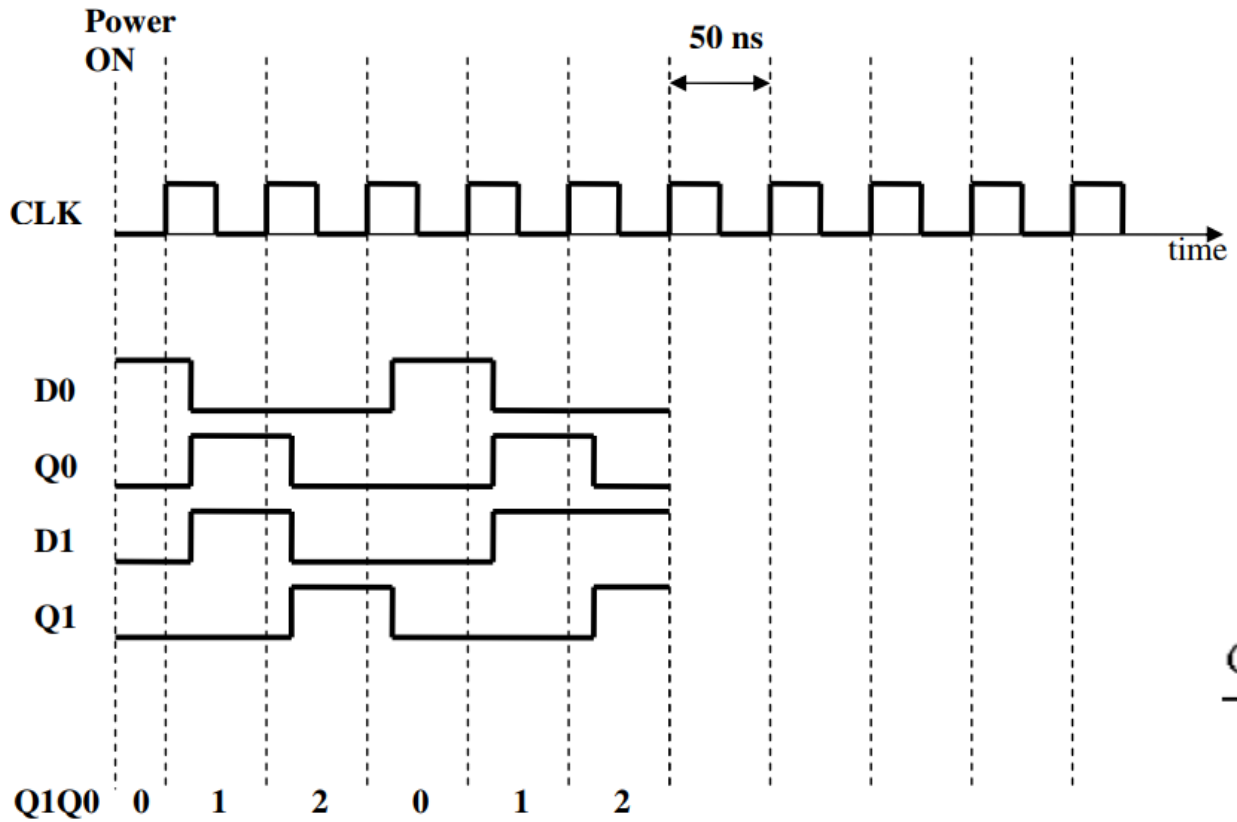
Q6.

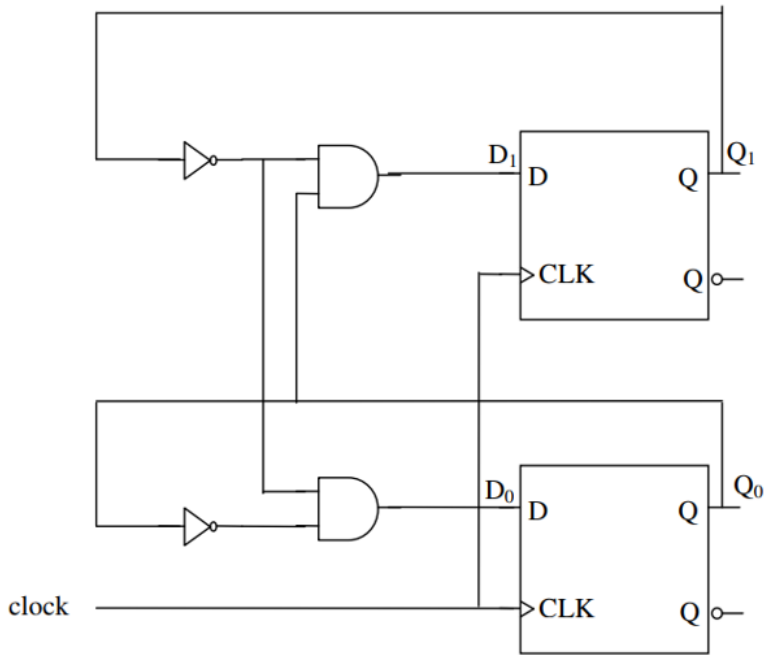
The Q_1 and Q_0 outputs of the FSM below are displayed on a 7-segment display to display the number which has the binary representation Q_1Q_0. Assume that the Q outputs of the flip flops are 0 at Power ON. Draw the waveforms of Q_1 and Q_0 for $t \geq 0$ where t is time and t = 0 is the time of Power ON. What is the counting sequence of this FSM? Assume that the ffs have a delay of 10 ns, that the other gates do not have any delays, and that the clock period is 50 ns.



Solution:

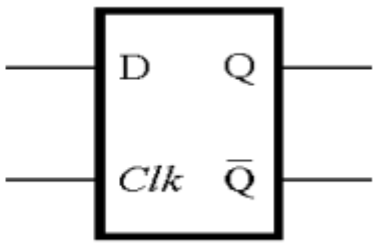
$D_1 = Q_1'Q_0$ $D_0 = Q_1'Q_0'$



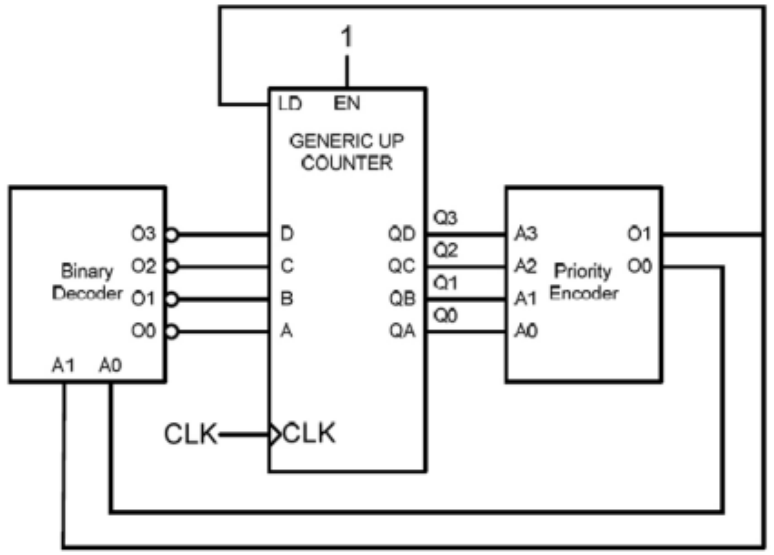


The counting sequence is 0,1,2,0,...

Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1



Q2.
Determine the counting sequence of the following configuration and fill in the following table. Assume that the counter is initially 0. Priority order is A3, A2, A1, and A0 from high to low in the priority encoder.



Next State Table to determine the counting sequence:

Q3	Q2	Q1	Q0	LD	Q3*	Q2*	Q1*	Q0*
0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1	0
0	0	1	0	0	0	0	1	1
0	0	1	1	0	0	1	0	0
0	1	0	0	1	1	0	1	1
1	0	1	1	1	0	1	1	1
0	1	1	1	1	1	0	1	1
1	0	1	1	1	0	1	1	1

4 to 2 Priority Encoder

I_3	I_2	I_1	I_0	O_1	O_0	v
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

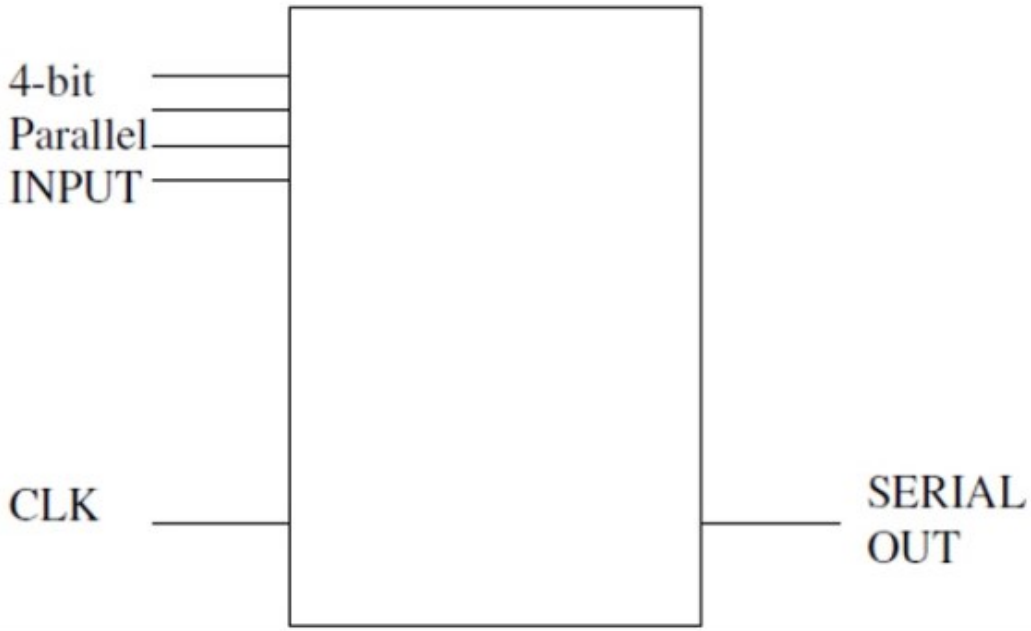
w_1	w_0	y_0	y_1	y_2	y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Q5.

a) You are to design a parallel-to-serial converter which loads 4-bit parallel data at every 4^{th} clock tick and shifts them in between. Thus for example at the nth clock tick it loads the data "ABCD" and its serial output becomes D, C, B, and A at the nth, n+1^{st}, n + 2^{nd}, and n + 3^{rd} clock ticks respectively. At the n + 4^{th} tick it loads a new 4-bit parallel data, and so on.

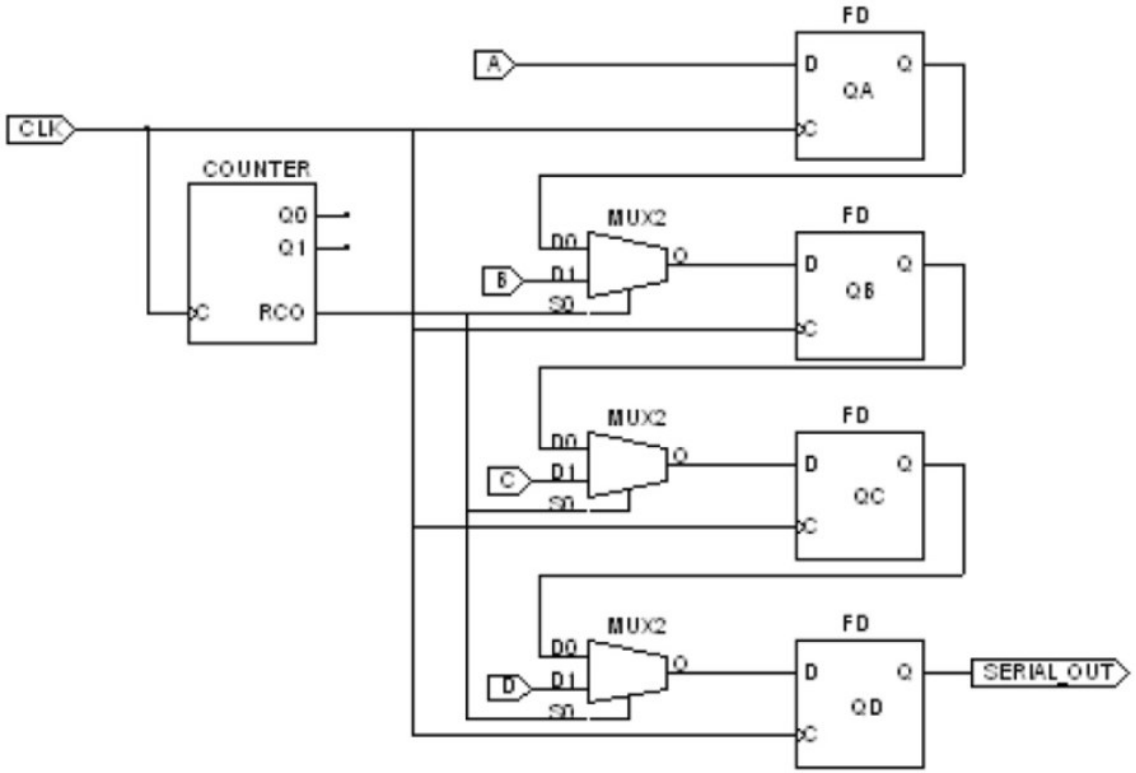
To achieve this, first modify the serial-in serial-out shift register structure in page 727 using three 2-to-1 multiplexers. And then use a 2-bit counter with RCO output to obtain the parallel-to-serial converter. Draw the timing diagram of your final circuit to illustrate the parallel to serial conversion.

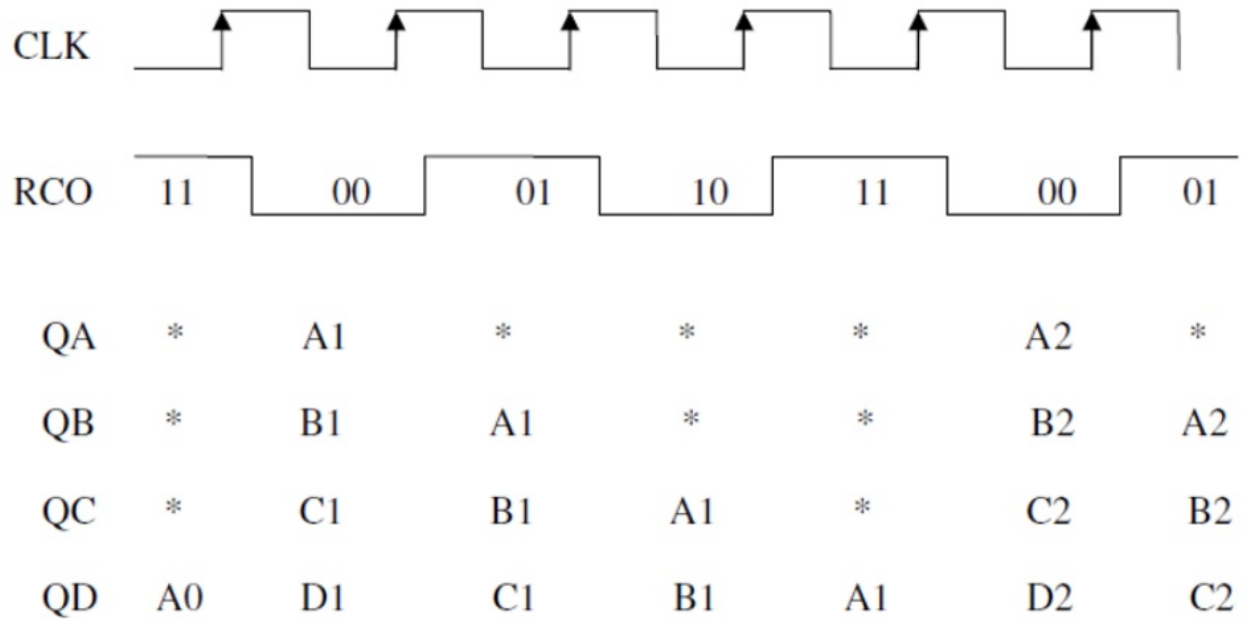
Your final design should have the following pin diagram:



Solution

a)


CLK
COUNTER
Q0
Q1
C
RCO
A
B
C
D
MUX2
D0
D1
S0
O
FD
D
Q
C
QA
QB
QC
QD
SERIAL_OUT


CLK
RCO 11 00 01 10 11 00 01
QA * A1 * * * A2 *
QB * B1 A1 * * B2 A2
QC * C1 B1 A1 * C2 B2
QD A0 D1 C1 B1 A1 D2 C2

A multibit register problem

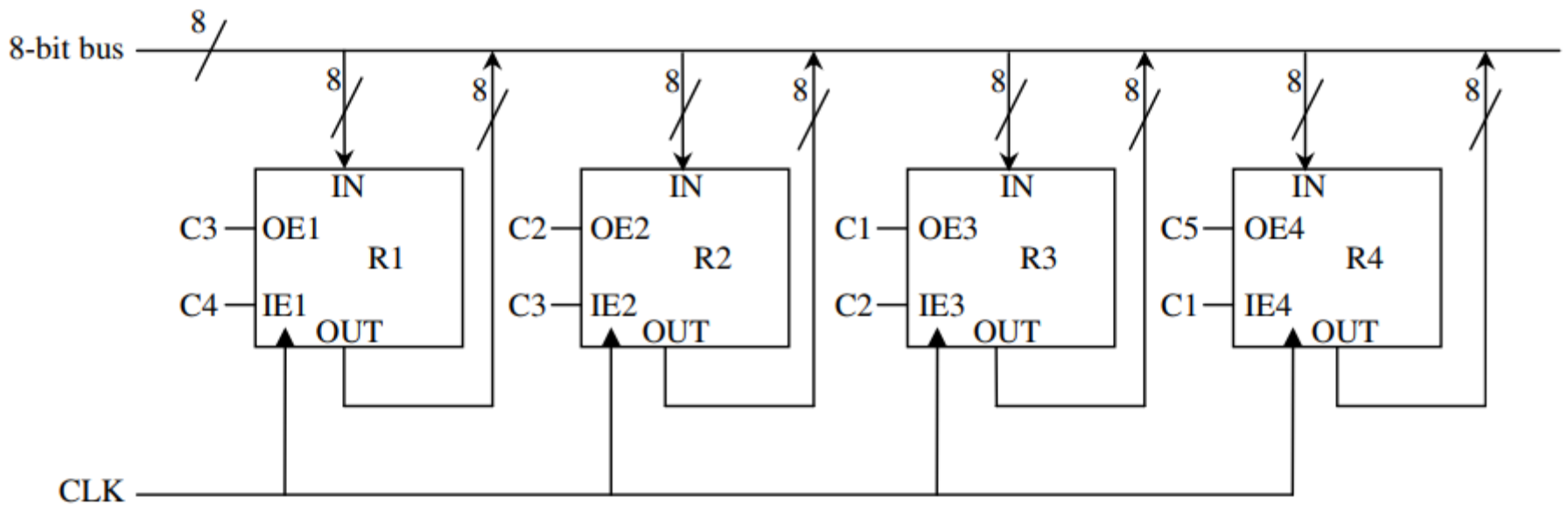
Question:

We have an 8-bit bus and four 8-bit positive edge triggered registers, R1, R2, R3, R4 connected to it. The register outputs are three-state and they have active high output enable (OE) controls. The registers also have active high input enable (IE) controls. There is also a START signal generated by another logic circuit. START is usually LOW and the registers are disabled. When it becomes HIGH, and as long as it is HIGH, synchronous with the clock ticks the following happen in order, only once:

- the contents of R3 are copied to R4,
- the contents of R2 are copied to R3,
- the contents of R1 are copied to R2,
- R1 receives new contents from the bus,
- the contents of R4 are applied to the bus for a clock cycle,
- once all these happen the registers are disabled.

There is also a positive edge triggered synchronous control circuit which generates an appropriate number of control signals in reference to the clock and the START signal, which are used to realize the above actions. Specify how the control signals must be and draw their waveforms together with the clock and the START signals.Be careful to show the relative delays of all signals with respect to each other. Draw your circuit including the bus, the registers, the control signals and the connections. Do not attempt to design a circuit which generates the control signals. All circuits operate from the same clock. Design the control signals such that all actions happen in a minimum number of clock cycles.

Solution:



The timing diagram for the control signals is

The timing diagram for the control signals is