Bilkent University, EEE 102 Final Exam, Spring 2020

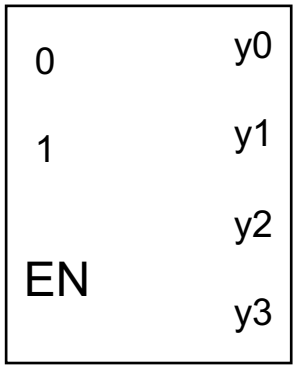
Question 1 [20 pts] – Time: 30 minutes

Implement the Boolean function

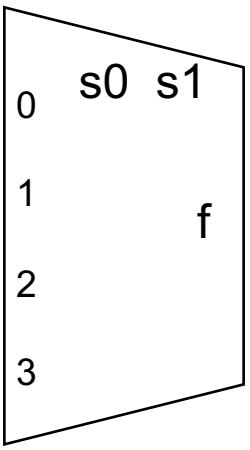
$$F(A,B,C,D,E) = \bar{A}\,D(\bar{B}\,\bar{C}\,\bar{E} + B\,\bar{C}\,E) + CE$$

using ONLY one 2-to-4 decoder with ENABLE and one 4-to-1 multiplexer. Logic levels 0 and 1 are available (i.e., you can use them as inputs). Complements of the variables are NOT available.

2-to-4
Decoder with Enable



4-to-1
Multiplexer



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Question 2 [30 pts] – Time: 40 minutes

Design a Moore machine that has a single input X and a single output Y that works as follows.

- Machine is always in one of the two modes: **free** and **blocked**.
- If machine is **free** and X=0, then in the next three CLKs, it will emit sequence 101 as output. It will be **blocked** until the entire sequence is emitted.
- If machine is **free** and X=1, then in the next three CLKs, it will emit sequence 010 as output. It will be **blocked** until the entire sequence is emitted.
- Inputs that arrive when the machine is **blocked** do not affect the output.

An example input-output sequence is given below:

Time →										
X	0	1	1	1	0	1	1	0	1	0
Y	d	1	0	1	0	1	0	0	1	0

(i) Draw the state diagram with minimum number of states. **[15 pts]**

(ii) What is the minimum number of flip-flops needed to implement this circuit? Will there be any unused flip-flop states? If so, how many? **[5 pts]**

(iii) **[This part is not related to (i) and (ii)]** Implement the state table given below using minimal number of JK flip-flops. X is the input, Y is the output. Find minimal sum-of-products forms for flip-flop input equations and output equation. Note: d represent don't care. **[10 pts]**

Present State	Next State		Output
	X=0	X=1	
Q1Q0	Q1+Q0+	Q1+Q0+	Y
00	10	0d	1
01	01	dd	0
11	dd	dd	1
10	d0	d1	0

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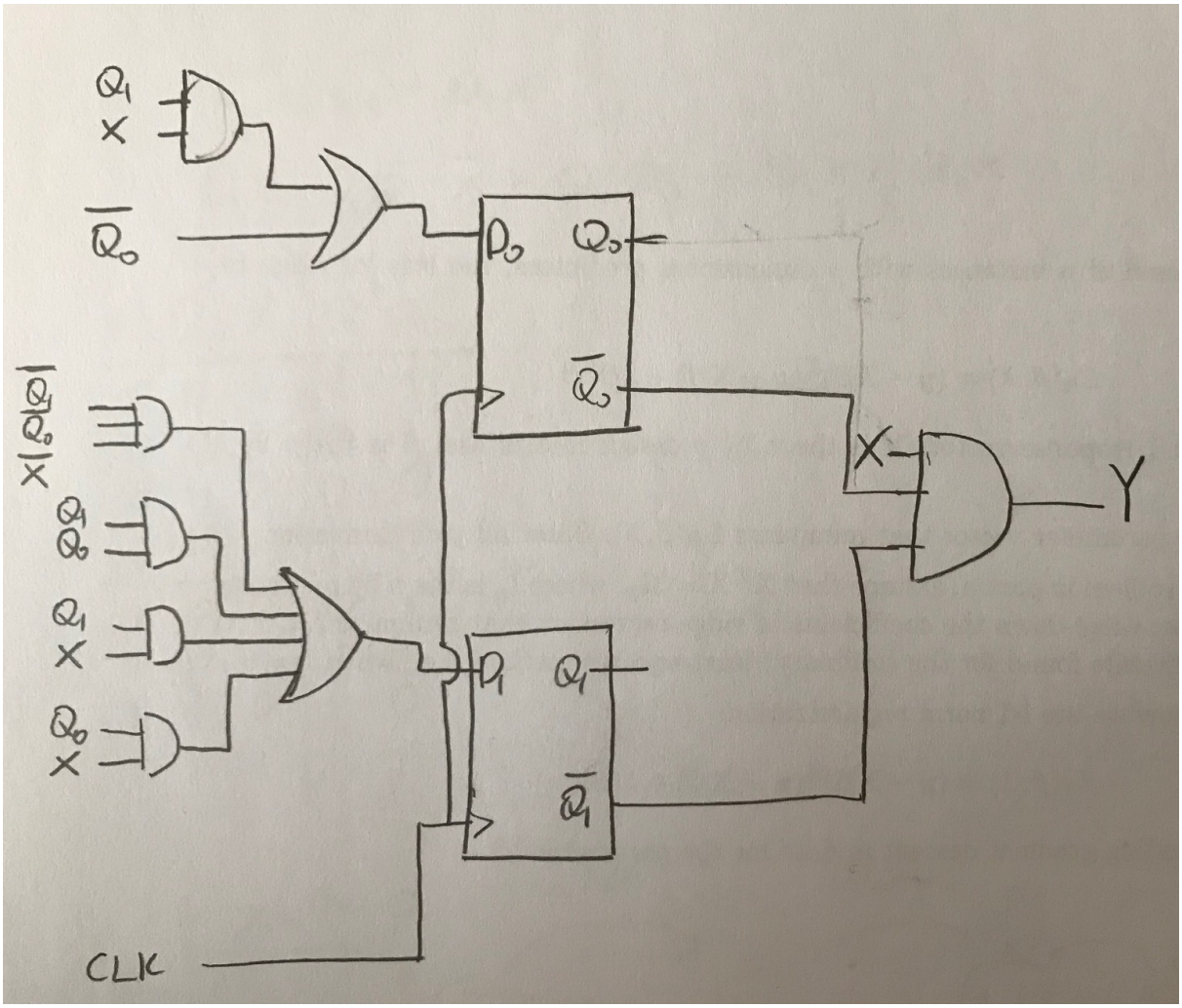
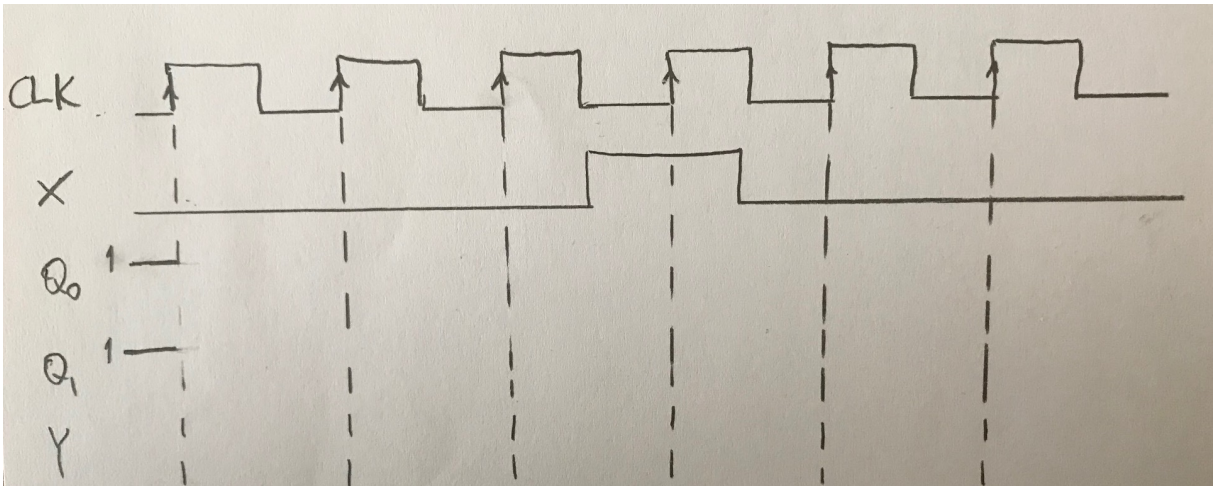
Question 3 [30 pts] – Time: 40 minutes



(i) Consider the sequential circuit above made up of 2 type D flip-flops with input X and output Y. Draw the state diagram for this circuit. [15 pts]

(ii) Complete the timing diagram for this Mealy FSM, given below starting from initial state 11. Is this FSM working as expected? Identify if there is a problem with the output and propose a way to solve this problem. [15 pts]



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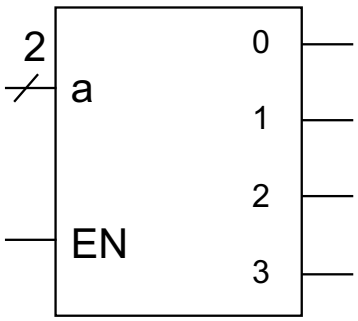
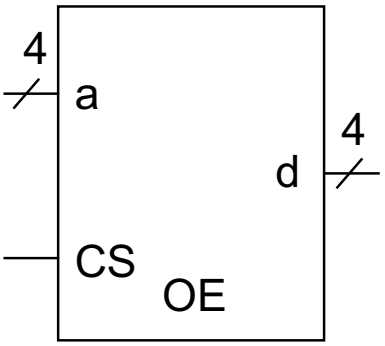
Question 4 [20 pts] – Time: 30 minutes

You have access to the following components:

(1) 2-to-4 decoders with enable input:



(2) 16 nibble ROMs with 4-bit address $a = a_3a_2a_1a_0$, chip select 'CS' and output enable 'OE' inputs:



Using ONLY these components, design a 64 nibble ROM that also has chip select 'CS' and output enable 'OE' inputs. Draw its diagram, showing all connections.