Lastname, Name:	
ID:	

## EEE 102: Digital Systems Design Midterm Exam 2 April 27, 2015 Duration: 90 min

Q	1	2	3	4	Total
Pts	25	25	25	25	100
Score					

This is a closed-book and closed-notes exam.

NO CREDIT will be given to answers without clear, formal and clean

JUSTIFICATION.

1.	1. [25 pts] Implement a JK flip-flop using a T flip-flop and minimal number of AND and OR gates. Complements of the $J$ and $K$ variables and logic levels 0 and 1 are not available. Complement of the $T$ flip-flop output $Q$ is available.							

2. [25 pts] Design a sequential circuit with serial input X and serial outputs  $Z_1$  and  $Z_2$  which performs the following operation. Whenever the circuit receives a sequence 1100 on input it should output  $Z_1 = 1$  and  $Z_2 = 0$ . Whenever the circuit receives a sequence 0101 on input it should output  $Z_1 = 0$  and  $Z_2 = 1$ . Otherwise it should output  $Z_1 = 0$  and  $Z_2 = 0$ . An example of input output sequence is shown below:

Write down the state diagram and the state table using minimum number of states.

## 3. [25 pts]

Design a sequential circuit that outputs 1 when it receives a three consecutive number of 0's on the input (including the current input) As an example,

where x is the input and y is the output.

You can only use PR-type flip-flop, where an PR-type flip-flop is defined as follows:

Р	$\mathbf{R}$	Q(t+1)
0	0	0
0	1	1
1	0	$egin{array}{c} ar{Q}(t) \ Q(t) \end{array}$
1	1	Q(t)

and a minimum number of NOR gates.

## 4. [25 pts]

Design a sequential circuit that counts up or counts down depending on the input x. If the x=0, then the circuit counts down from 2 to 0 in a circular manner. Else if x=1, then the circuit counts up from 0 to 2 in a circular manner. As an example,

where x is the input and y is the output.

You can only use T-type flip-flops and a minimum number of NAND gates.