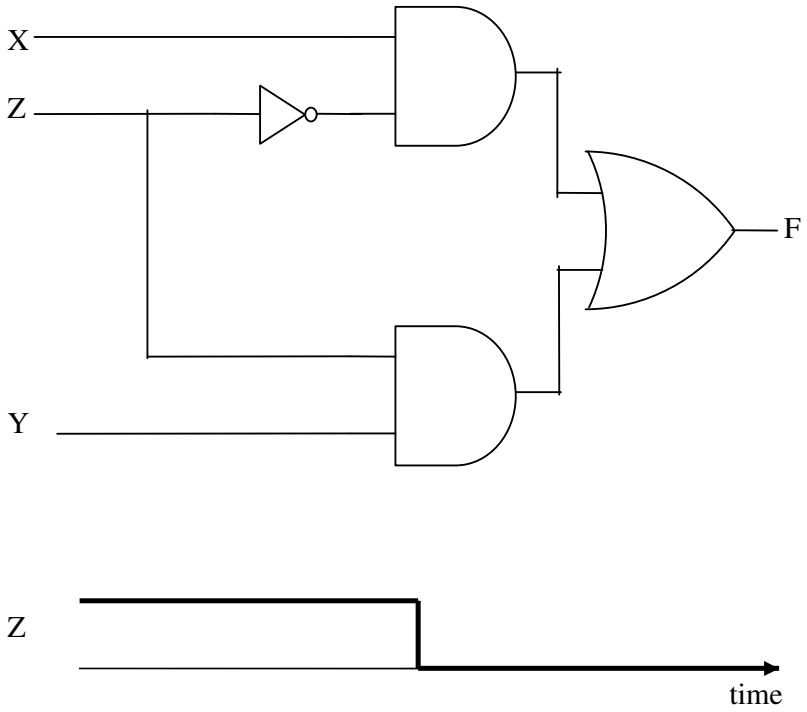
EEE102
Sample Problems for Fall 2009
16-9-2008
LOGIC GATES and CANONICAL DESIGN

Q1.
For the following circuit and the time waveform of Z

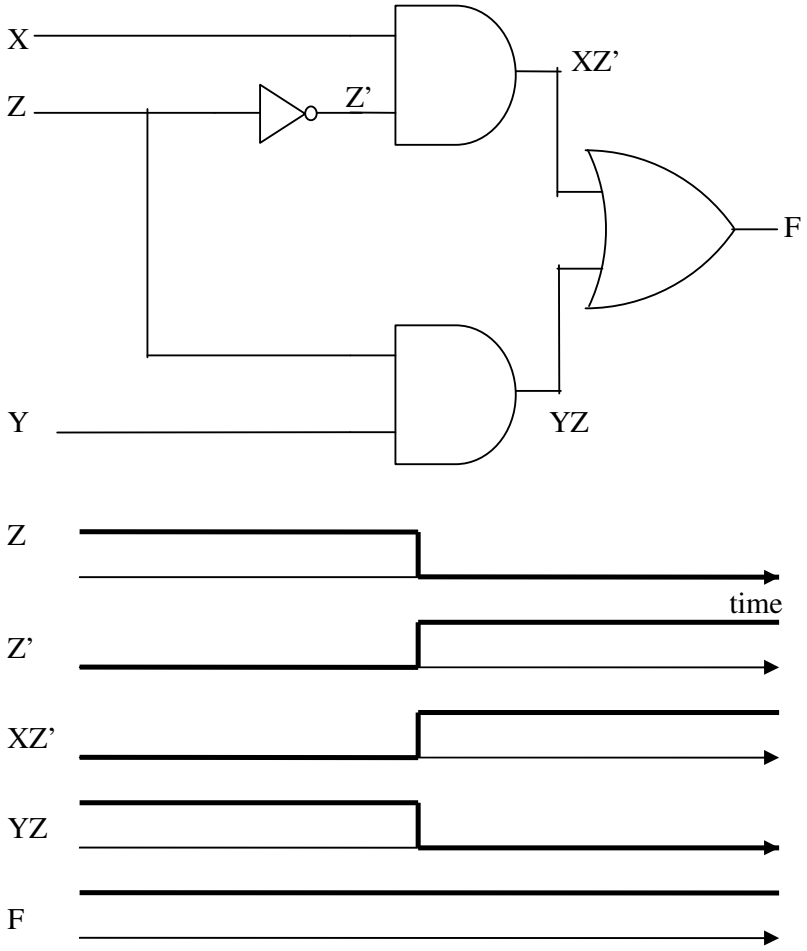


a) Draw the time waveform of F if the gates do not have any delays,
b) Draw the time waveform of F if each gate has 10 ns delay.

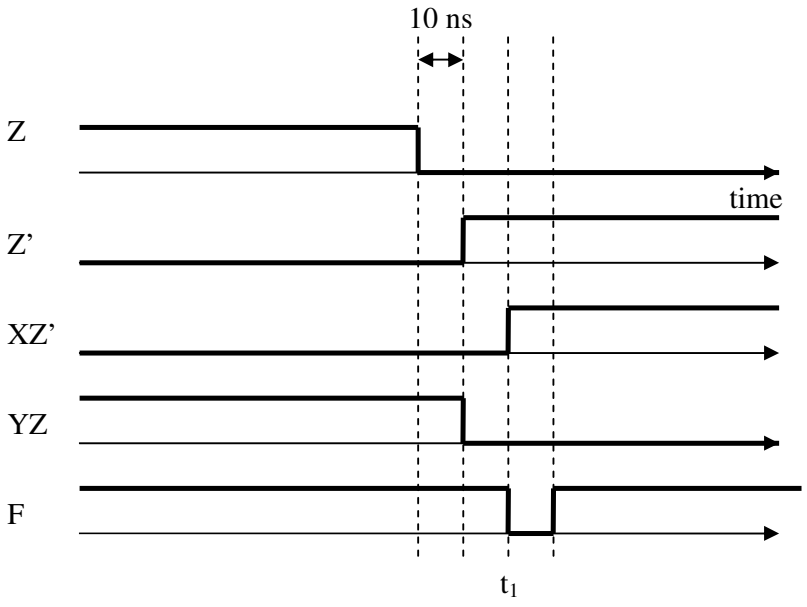
Asume X = Y = 1 throughout.

Solution:

a)



b)



Note that at time t_1 F goes to 0 because at time t_1-10ns such a decision was made. Also at t_1+ (right after t_1) another decision is made which is to raise F to 1 again, but this new decision is executed at t_1+10ns.

Another important observation is as follows. F = XZ'+YZ=1Z'+1Z=Z'+Z=1. Thus F must be 1 always looking at the expression for F. However such expressions are steady state (long term) expressions. In other words they tell us what happens if the inputs are fixed for a long time. As we see in part b) the transient response (short-term response) is quite different due to the delays. Another interpretation for the expression for F is that it is valid if gates do not have any delays.

Q2.
Write the TT for the function F = XZ + Y'Z + X'YZ'

Solution:

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Q3.
For the TT you have found above find
a) two-level canonical SOP expression for F
b) two-level canonical POS expression for F

Solution
a) F = X'Y'Z + X'YZ' + XY'Z + XYZ
b) F = (X+Y+Z)(X+Y'+Z')(X'+Y+Z)(X'+Y'+Z)

Q4.
For the TT given below find
a) two-level canonical SOP expression for F
b) two-level canonical POS expression for F

X	Y	Z	F
0	0	0	1
0	0	1	1

0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

F is the output and X,Y,Z are inputs.

Solution:

a) F = X'Y'Z' + X'Y'Z + X'YZ' + XY'Z + XYZ
b) F = (X+Y'+Z')(X'+Y+Z)(X'+Y'+Z)

Q5.
. For the TT given below find

a) two-level canonical SOP expression for F
b) two-level canonical POS expression for F

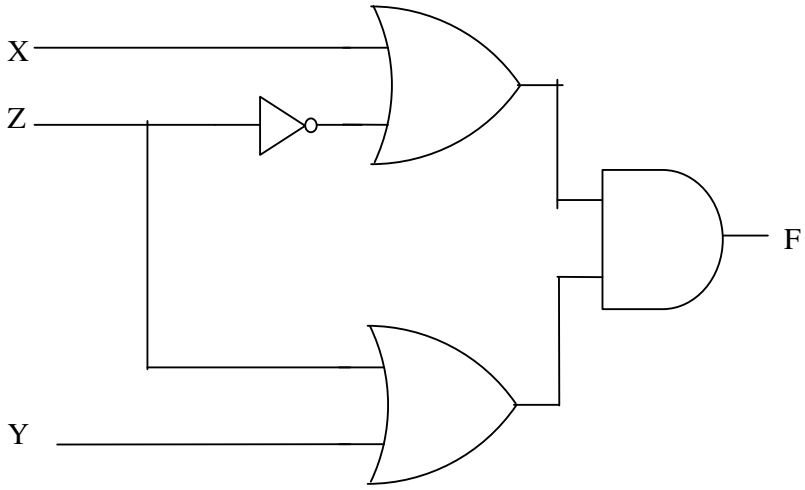
X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

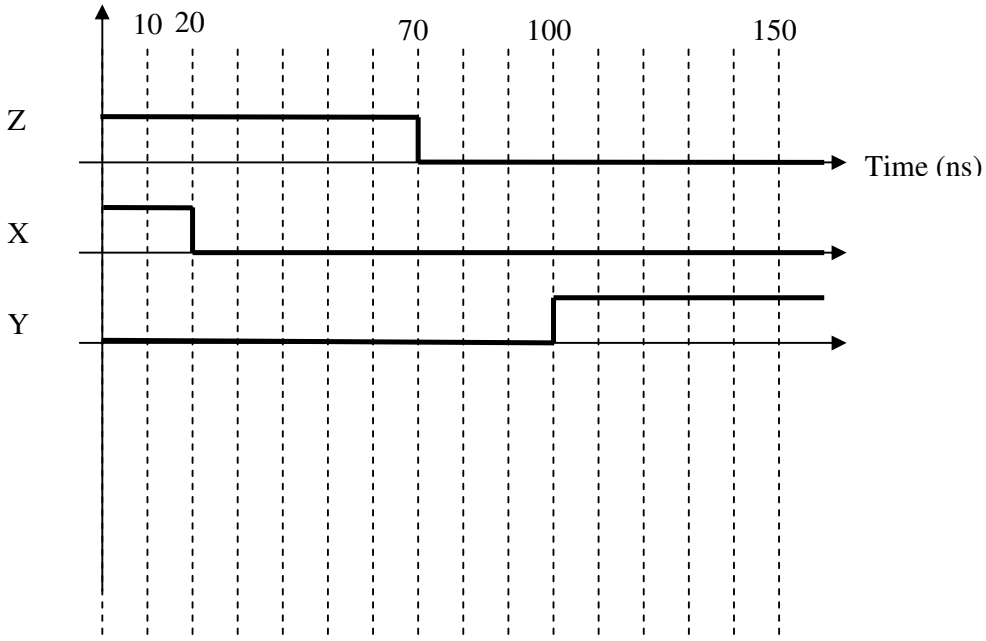
F is the output and X,Y,Z are inputs

Solution:

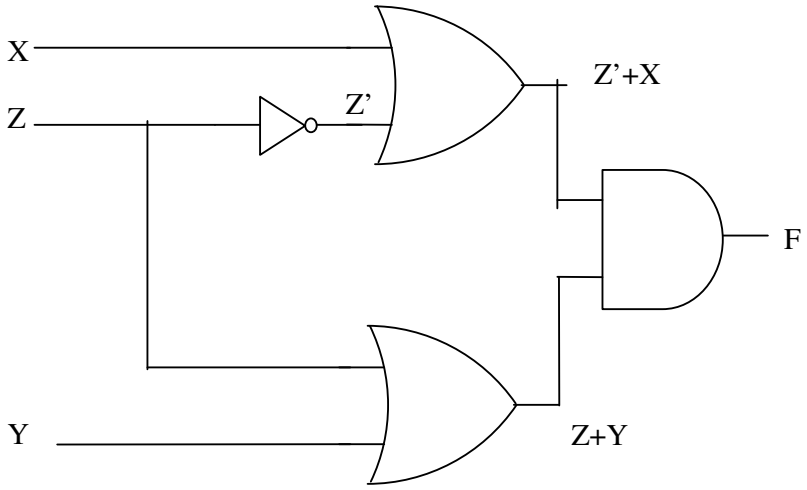
a) F = X'Y'Z' + X'Y'Z + X'YZ + XY'Z + XYZ
b) F = (X+Y'+Z)(X'+Y+Z)(X'+Y'+Z)

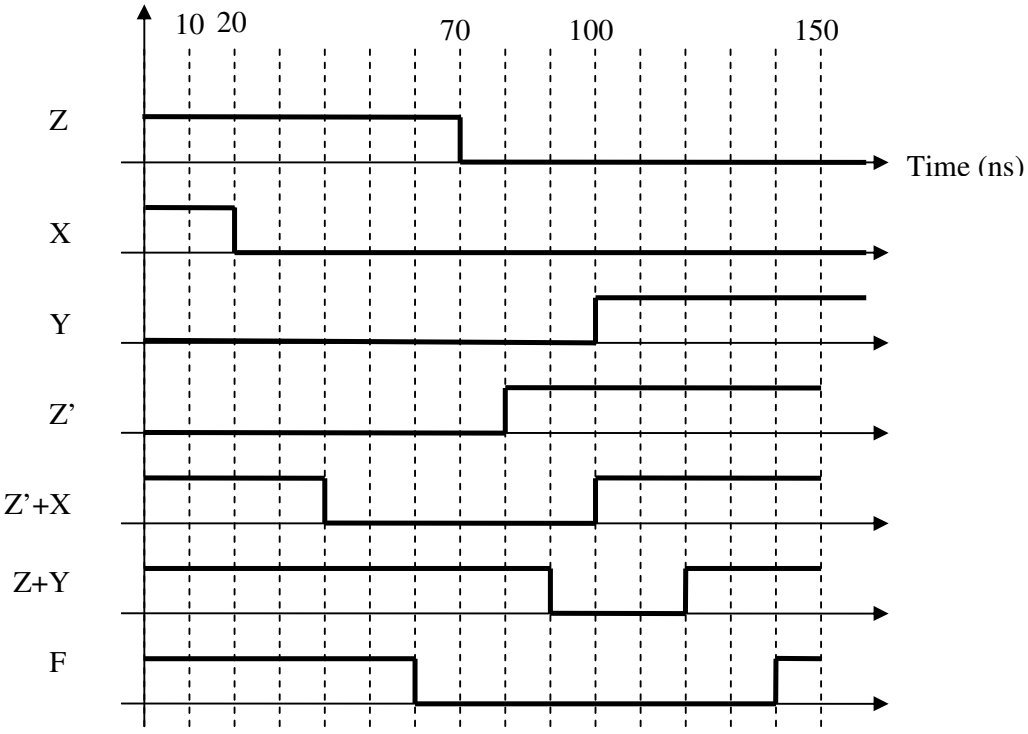
Q6.
For the following circuit and the given time waveforms of X, Y, and Z, draw the time waveform of F for $0 \leq$ time ≤ 150 ns, if the inverter has 10 ns delay, and the other gates have 20 ns delays.



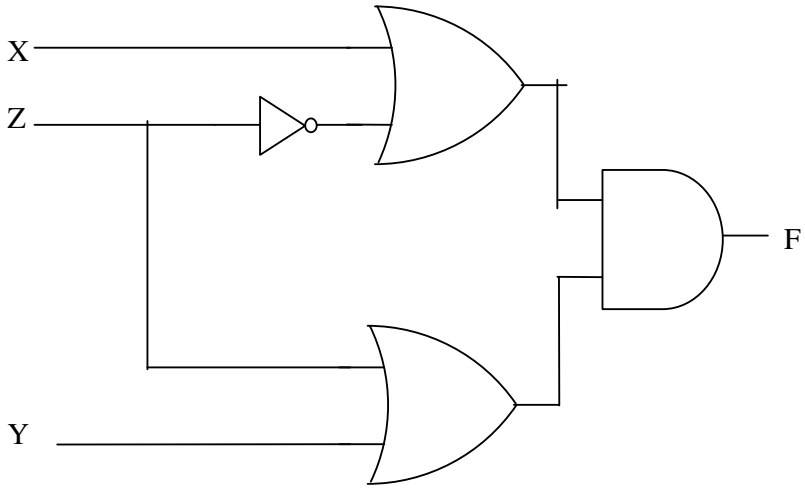


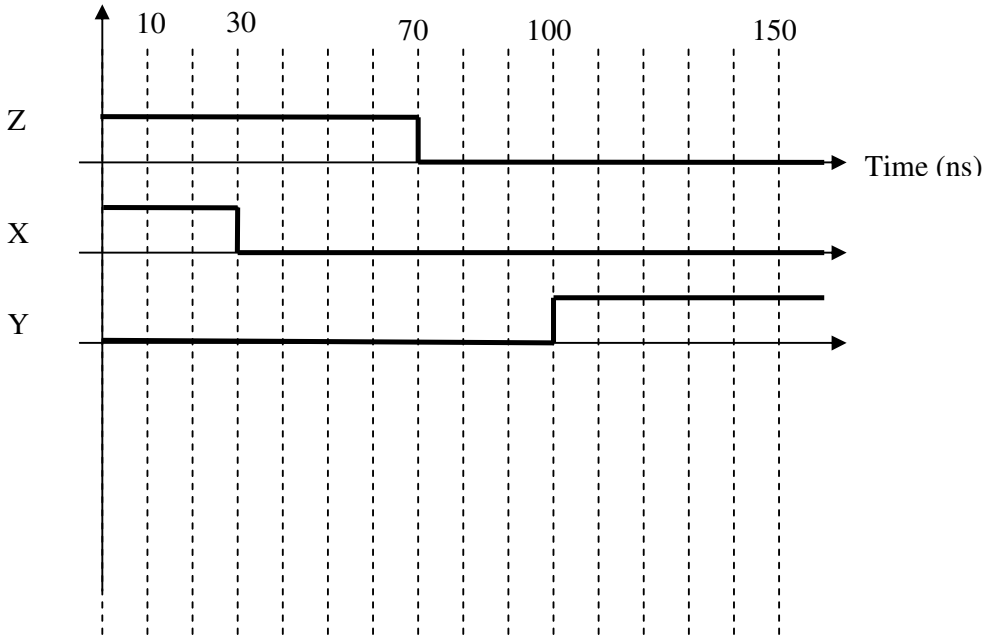
Solution:



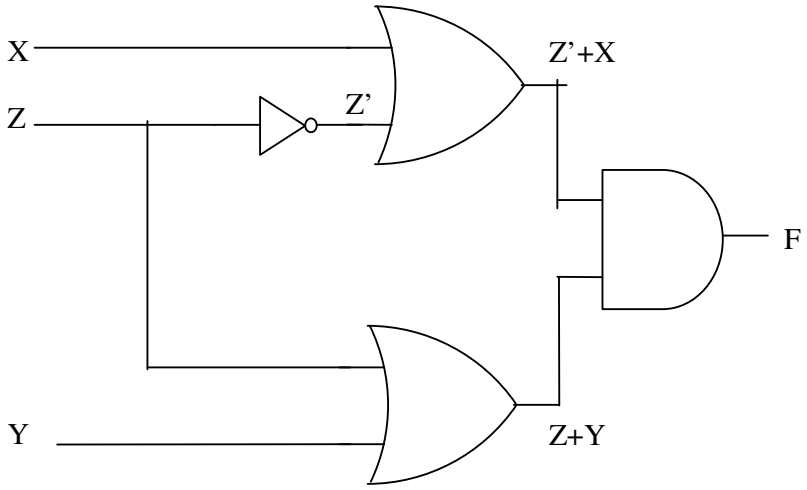


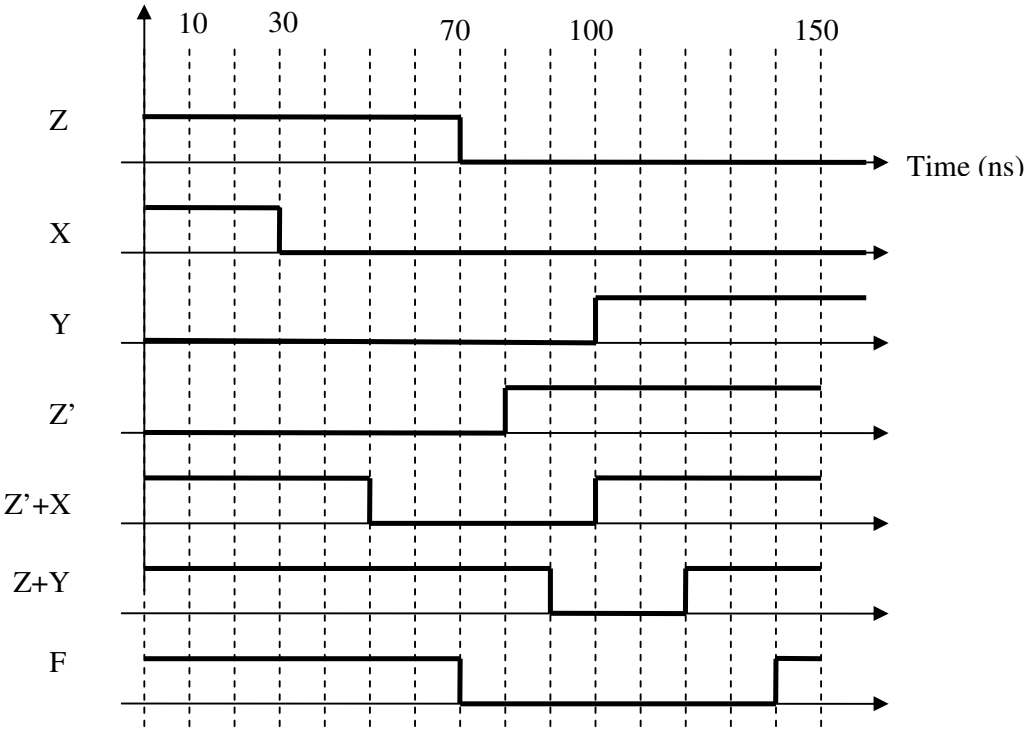
Q7.
For the following circuit and the given time waveforms of X, Y, and Z, draw the time waveform of F for $0 \leq$ time ≤ 150 ns, if the inverter has 10 ns delay, and the other gates have 20 ns delays.



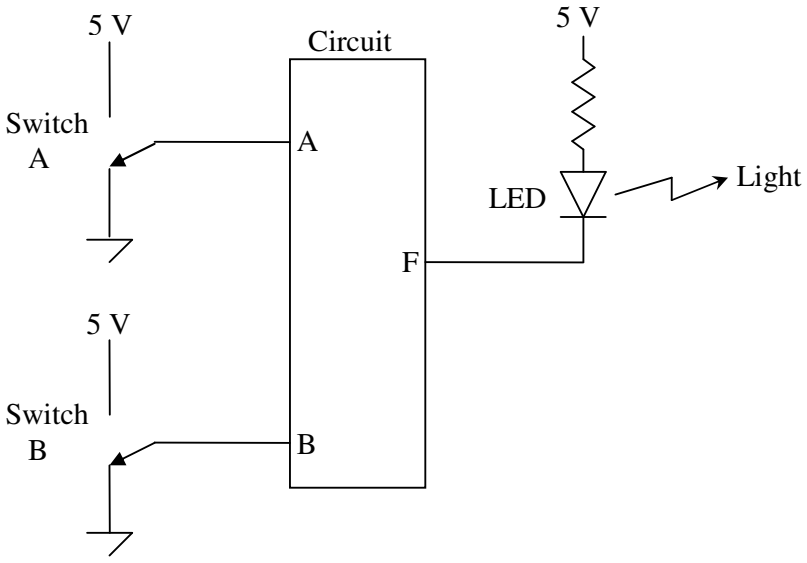


Solution:


X
Z
Z'
Z'+X
F
Y
Z+Y


10
30
70
100
150
Z
Time (ns)
X
Y
Z'
Z'+X
Z+Y
F

Q8.
A "two-way switch" system is used at homes to turn a light ON or OFF from two switches located in two different places.



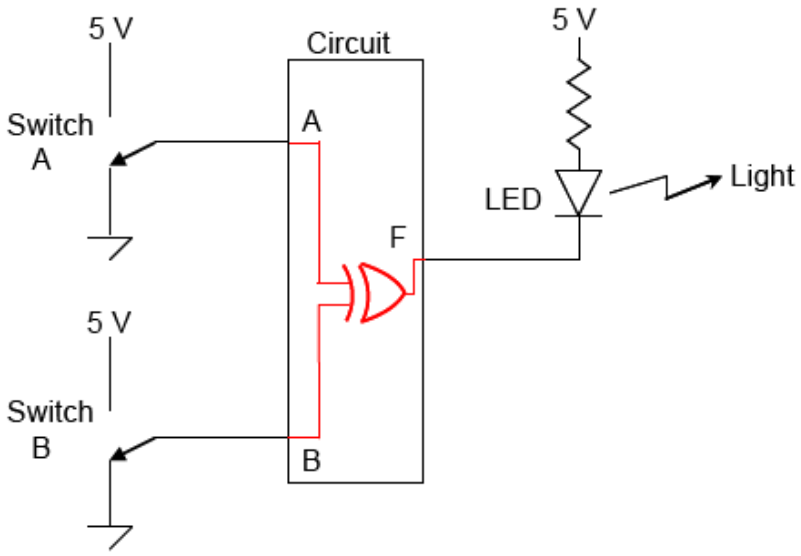
If switch A is pulled UP then the signal A becomes 1 and if it is pulled DOWN then the signal A bocomes 0. Similarly for switch B.

Now suppose switch A is located at the bottom of a stairway and switch B is located at the top. The LED (Light Emitting Diode) is used to illuminate the stairway. Assume, as a scenario, that the the LED is OFF at the beginning. A person who wants to climb up the stairs toggles switch A to turn the light ON. He then climbs up the stairs and at the top he toggles switch B to turn the light back OFF. This scenario is given as an example to explain how the system is used.

Design and draw the inside of the "Circuit" using as few gates as possible.

Notes: 1) For the LED to be ON, F must be 0. To turn it OFF, F must be 1.
2) "Toggle" means "change the position of the switch".
3) The initial positions of the switches are unknown although they are drawn in the above figure as at DOWN position.

Solution:



Explanation

Assume that both switches are DOWN, and LED is OFF at the beginning. This gives "*F = 1 when A=0 and B=0*". Next, we should switch on the light by toggling either one of A or B. This gives "*F=0 when A=1 and B=0*", and "*F=0 when A=0 and B=1*". Finally, we should switch off when the light is ON by toggling either one of A or B. This gives "*F=1 when A=1 and B=1*" and "*F=1 when A=0 and B=0*". The latter was already covered by the initial case. Combining the givens into a truth table, we have:

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

This is the truth table of an XNOR (equivalence) gate.

With the same reasoning and different initial conditions (e.g. "*both switches DOWN and LED is ON*", or "*one of the switches UP, one of the switches DOWN, and LED is ON*"), we will end up with the truth table of an XOR gate.

Note that in practice initial conditions do not matter: We build the circuit by using one XOR gate or one XNOR gate, and if the LED is ON, we switch it off by toggling one of the switches.