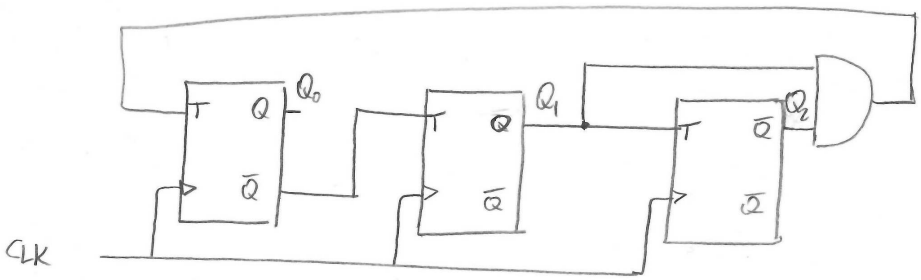
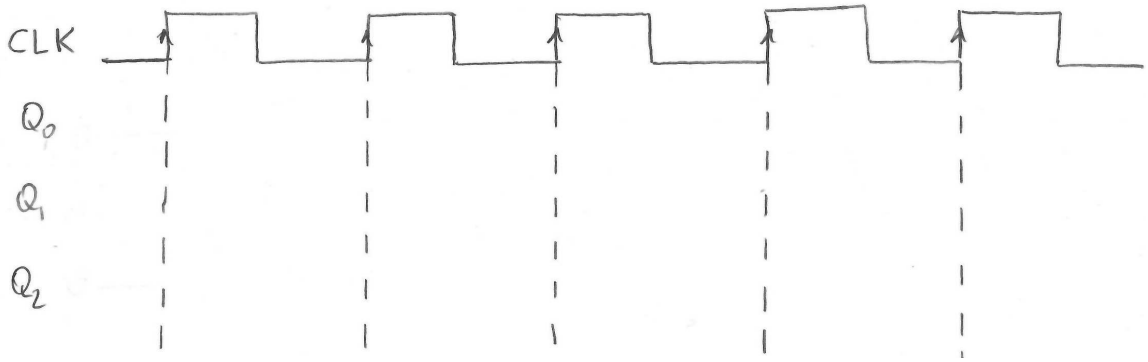
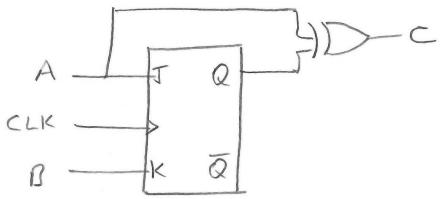
1. **[25pts]** Complete the timing diagrams of the circuits given below. Assume that the flip-flop states (outputs) are 0 initially.

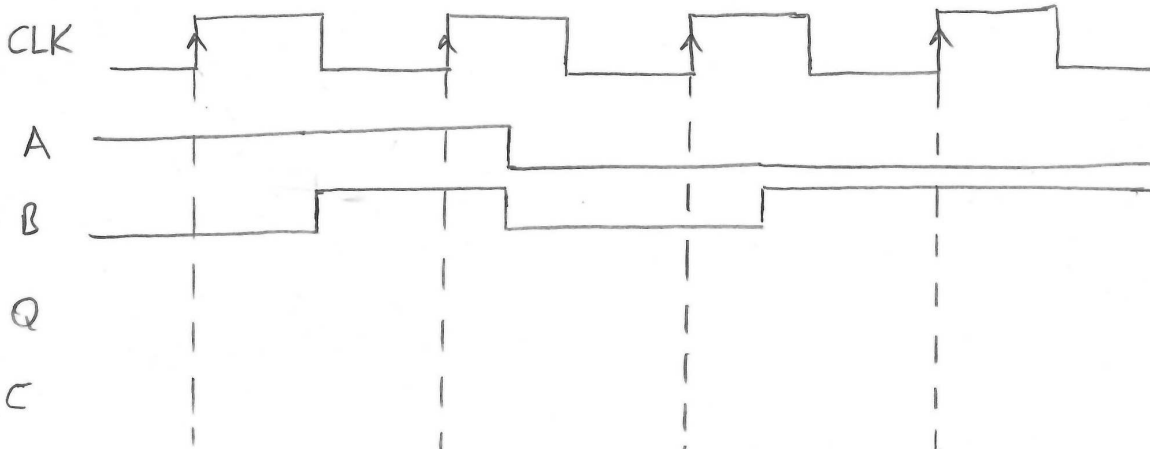
a [12 pts]





b [13 pts]





2. **[25 pts]**

Design a 3-bit shift register with inputs R (1 bit), S_1S_0 (2 bits) and $I_2I_1I_0$ (3 bits), and outputs $Q_2Q_1Q_0$ (3 bits) that performs the following operations:

- $S_1S_0 = 00$: No change, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = Q_2(t)Q_1(t)Q_0(t)$
- $S_1S_0 = 01$: Shift right, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = RQ_2(t)Q_1(t)$
- $S_1S_0 = 10$: Circular shift left, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = Q_1(t)Q_0(t)Q_2(t)$
- $S_1S_0 = 11$: Load, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = I_2(t)I_1(t)I_0(t)$

You are only allowed to use D-flip flops and multiplexers (make sure that you don't use more than necessary number of multiplexers and flip-flops).

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Each question must be solved on a separate blank sheet. On top of each sheet, you must write and sign the following honor code:

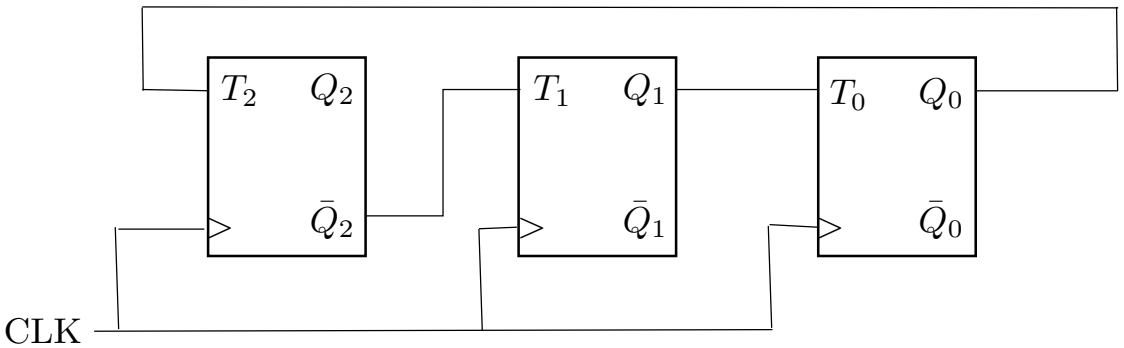
On my honor, I have neither given nor received unauthorized aid on this exam question

Your full name: **Your signature:**

Questions solved without a signed honor code **will not be graded. Solutions must be hand written. Typed solutions will not be graded.**

Question 2 [25 pts]

(i) Consider the circuit below that consists of T flip flops with output $Q_2Q_1Q_0$:



Draw the timing diagram for the output, starting from state $Q_2Q_1Q_0 = 000$, for the next 6 CLK cycles. [10 pts]

(ii) When we start from $Q_2Q_1Q_0 = 000$ in the circuit above, which states will never be visited? [5 pts]

(iii) Construct a PR flip flop, whose characteristic table is given below, using a T flip flop and AND, OR, NOT gates. [10 pts]

P	R	Q(t+1)
0	0	Q'(t)
0	1	Q(t)
1	0	1
1	1	0

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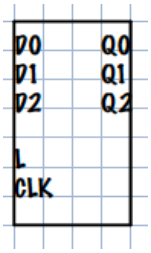
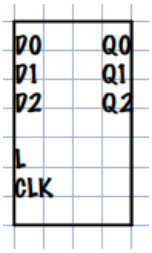
Question 3 [25 pts]

You are given two synchronous 3-bit up counters with synchronous parallel load capability as shown below. L represents the load input (load operation is performed when L=1), CLK represents the clock input, D2D1D0 represent the data inputs and Q2Q1Q0 represent the count outputs. Assume that one of the counters is initialized to Q2Q1Q0 = “000” and the other one is initialized to Q2Q1Q0 = “001”.





Using these counters and some combinational logic (e.g., basic gates like and/or etc.) design a 6-bit synchronous counter that counts in the following repeating pattern (in decimal):

$$1 \rightarrow 10 \rightarrow 19 \rightarrow 28 \rightarrow 32 \rightarrow 1 \rightarrow 10 \rightarrow \cdots$$

(i) Draw the circuit diagram. [15 pts]

(ii) Draw the timing diagram for each bit of the count output and load inputs for 6 CLK cycles. [10 pts]

Hint: Work on 6-bit unsigned (binary) representation of the decimal sequence given above.