Lastname, Name:_____
ID:_____

EEE 102: Digital Systems Design

Midterm Exam 1

March 15, 2016

Duration: 90 min

Q	1	2	3	4	Total
Pts	25	25	25	25	100
Score					

This is a closed-book and closed-notes exam.

NO CREDIT will be given to answers without clear, formal and clean

JUSTIFICATION.

1. **[25 pts]** Consider the following logic function:

$$F(A, B, C, D) = (A \oplus B)\overline{(C \oplus D)}$$

i) Implement $F(A, B, C, D)$ in simplest sum-of-products form. Draw the logic diagram only using NAND gates. Calculate the gate input cost. (12pts)

ii) Implement $F(A, B, C, D)$ in simplest product-of-sums form. Draw the logic diagram only using NOR gates. Calculate the gate input cost. (12pts)

iii) Which implementation has smaller gate input cost? (1pts)

For this question complements of the variables ARE available.

2. **[25 pts]** Consecutive integers are integers that follow each other in order. The magnitude of the difference between two consecutive integers is always 1. Design a circuit that identifies if two 2-bit unsigned integers X_1X_0 and Y_1Y_0 are consecutive or not. Let O denote the output of the circuit which is equal to 1 if X_1X_0 and Y_1Y_0 are consecutive and 0 otherwise.

   Examples of some input-output combinations are given below.

$$\text{Inputs: } X_1X_0 = 00 \ \ \& \ \ Y_1Y_0 = 01 \Rightarrow \text{Output: } O = 1$$
$$\text{Inputs: } X_1X_0 = 11 \ \ \& \ \ Y_1Y_0 = 10 \Rightarrow \text{Output: } O = 1$$
$$\text{Inputs: } X_1X_0 = 11 \ \ \& \ \ Y_1Y_0 = 00 \Rightarrow \text{Output: } O = 0$$

   (i) Draw the truth table of the circuit. (7pts)
   (ii) Implement the circuit using a single 3-to-8 decoder, a single 2-to-1 MUX and minimum number of two input OR gates. (18pts)

   For this question complements of the variables and logic levels 0/1 are NOT available

3. **[25 pts]**

a) Design a 16-to-1-line multiplexer using a 4-to-16-line decoder and a 16x2 AND-OR. [10 pts]

b) Design a 4-to-1-line multiplexer using a 2-to-4-line decoder and 4 tri-state buffers.[15 pts]

4. **[25 pts]** Design a circuit which has two 2-bit binary inputs, A and B, given in two's complement number system. The circuit has one binary output F. If $A > B$, then $F = 0$. Otherwise, if $A \leq B$, then $F = 1$.

   a) Construct the truth table. [7 pts]

   b) Implement the circuit with a single 4-1 multiplexer and a mimimum number of logical gates. Complements of the variables are available. [18 pts]