Bilkent University, EEE 102 Digital Design 2nd Midterm Exam

Each question must be solved on a separate blank sheet. . On top of each sheet, you must write and sign the following honor code:

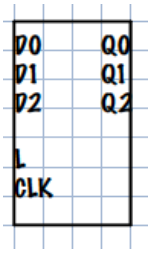
On my honor, I have neither given nor received unauthorized aid on this exam question

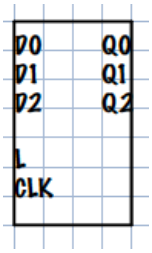
Your full name: **Your signature:**

Questions solved without a signed honor code **will not be graded. Solutions must be hand written. Typed solutions will not be graded.**

Question 3 [25 pts]

You are given two synchronous 3-bit up counters with synchronous parallel load capability as shown below. L represents the load input (load operation is performed when L=1), CLK represents the clock input, D2D1D0 represent the data inputs and Q2Q1Q0 represent the count outputs. Assume that one of the counters is initialized to Q2Q1Q0 = “000” and the other one is initialized to Q2Q1Q0 = “001”.





Using these counters and some combinational logic (e.g., basic gates like and/or etc.) design a 6-bit synchronous counter that counts in the following repeating pattern (in decimal):

$$1 \rightarrow 10 \rightarrow 19 \rightarrow 28 \rightarrow 32 \rightarrow 1 \rightarrow 10 \rightarrow \cdots$$

(i) Draw the circuit diagram. [15 pts]

(ii) Draw the timing diagram for each bit of the count output and load inputs for 6 CLK cycles. [10 pts]

Hint: Work on 6-bit unsigned (binary) representation of the decimal sequence given above.