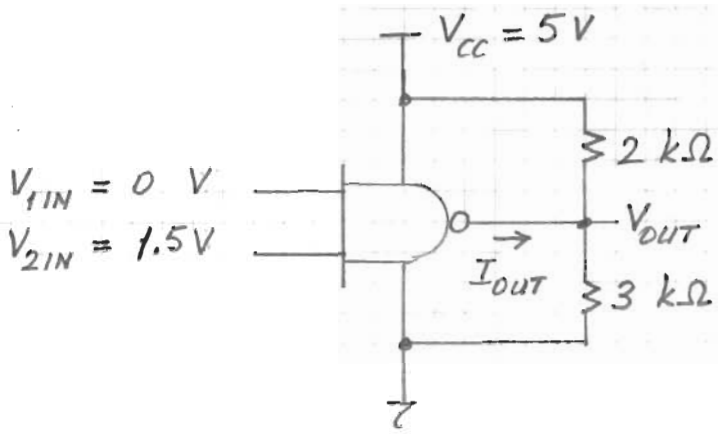
1. Find $V_{OUT}$ and $I_{OUT}$ in the following circuit. The internal resistances of the transistors associated with each input are as given.



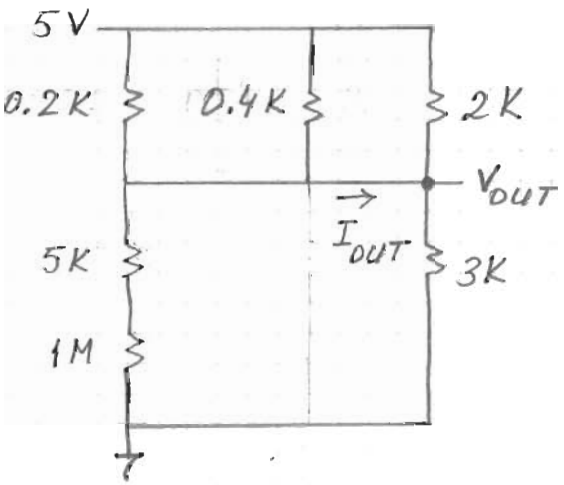

INTERNAL RESISTANCES

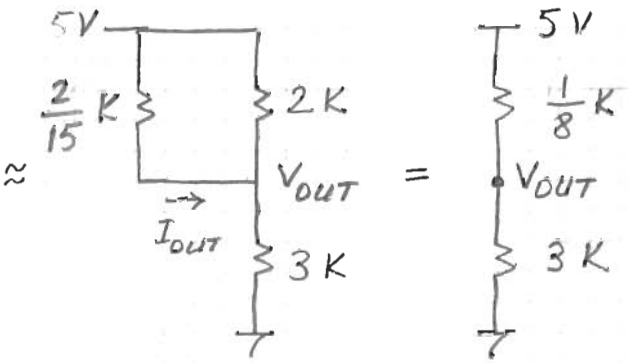
$R_{1ON} = 200\,\Omega \quad R_{1OFF} = 1\,M\Omega$

$R_{2ON} = 400\,\Omega \quad R_{2OFF} = 5\,k\Omega$

SOLUTION

Equivalent circuit :

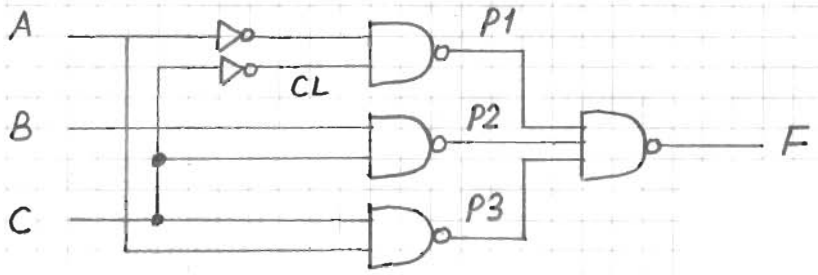


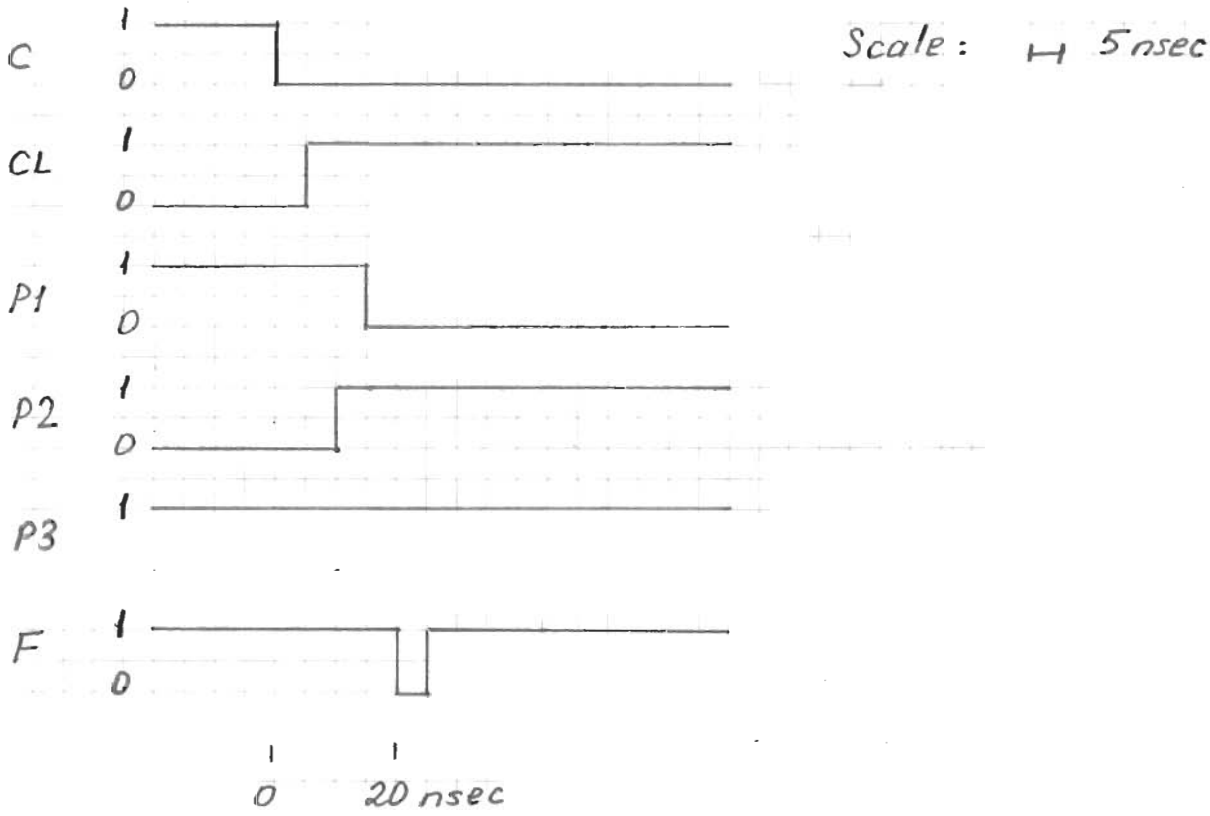




$$V_{OUT} = \frac{3}{3+\frac{1}{8}} \times 5 = 4.8\ V$$

$$I_{OUT} = \frac{5-4.8}{\frac{2}{15}} = 1.5\ mA$$

2. In the following circuit inverters have a 5 nsec propagation delay and the NAND gates 10 nsec. Plot the output waveform if A = 0, B = 1 and C changes from 1 to 0 at t = 0.



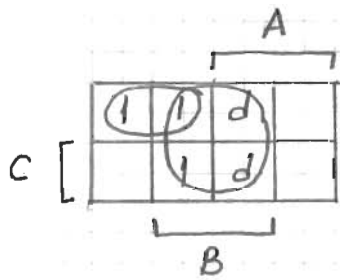



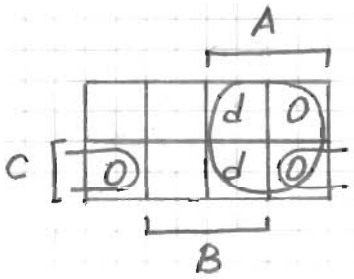
3. Obtain a minimal S.O.P representation ($F_1$) and a minimal P.O.S. representation ($F_2$) of

$$F(A,B,C) = \Sigma m(0,2,3) + \Sigma d(6,7)$$

Are $F_1$ and $F_2$ equal ? Explain.

SOLUTION




$F_1 = B + A'C'$

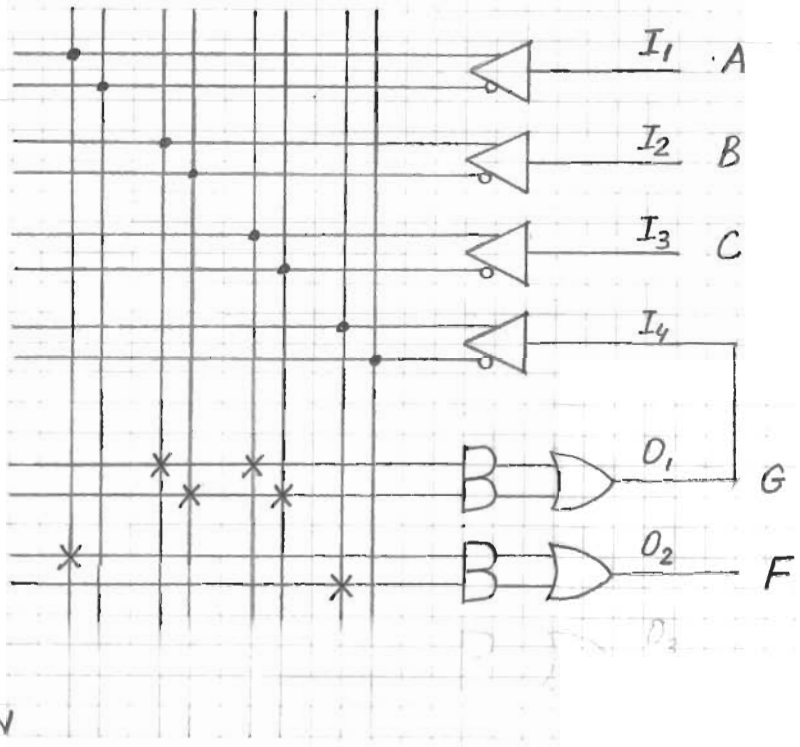
$F_2 = A'(B+C')$

$A = B = 1 \Rightarrow F_1 = 1, F_2 = 0 \Rightarrow F_1 \neq F_2$

4. Implement $F = A + BC + B'C'$

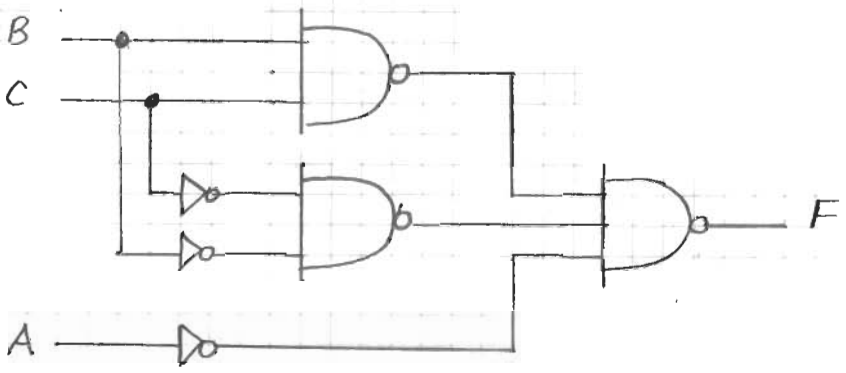
a) using a two-level NAND/NAND circuit plus inverters

b) using the following PAL




SOLUTION

a)




b) $F = A + G$, $G = BC + B'C'$

Implementation above.

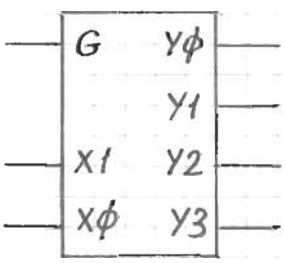
5. Draw the block diagram and write down the truth table of the circuit implemented by the following VHDL code.

```
library IEEE;
use IEEE.std_logic.1164.all;

entity BOX is
   port ( G: in STD_LOGIC;
          X: in STD_LOGIC_VECTOR (1 downto 0);
          Y: out STD_LOGIC_VECTOR (0 to 3));
end BOX;

architecture ABOX of entity BOX is
signal Z: STD_LOGIC_VECTOR (0 to 3);
begin
   with X select
      Z <= "1000" when "00",
           "0100" when "01",
           "0010" when "10",
           "0001" when "11",
           "0000" when others;
   Y <= Z when G='1' else "0000";
end ABOX;
```

SOLUTION




| G | X(1) | X(0) | Y(0) | Y(1) | Y(2) | Y(3) |
|---|---|---|---|---|---|---|
| 0 | x | x | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |