Bilkent University, EEE 102 Final Exam, Part I, Fall 2020 [75 minutes]

All of your work/derivation must be shown on the paper to get credit.

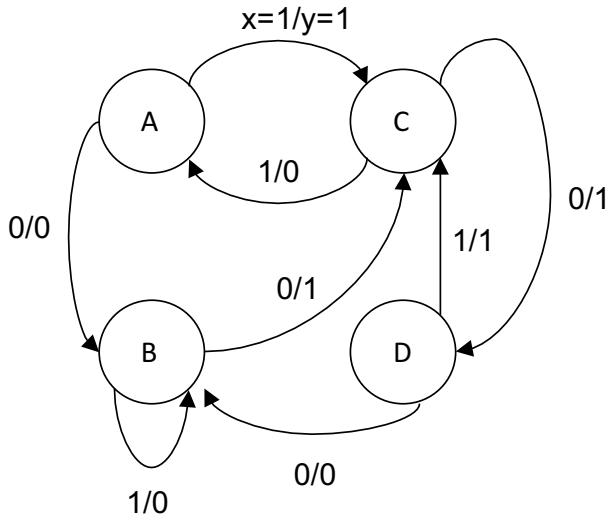
Question 1 [25 pts] Design 4-to-1 multiplexer by using **one** 2-to-4 decoder, and **minimum number** of 2-input AND and 2-input OR gates (if necessary). For this question, complements of the variables are **NOT** available.

Question 2 [25 pts] Design synchronous counter that counts through the sequence

$$1 \rightarrow 3 \rightarrow 5 \rightarrow 7 \rightarrow 1 \rightarrow \ldots$$

using **minimum number** of T flip flops and **minimum number** of AND and OR gates (if necessary).

Question 3 [15 pts] Consider the following state diagram where x is the input, y is the output. Identify equivalent states and draw the minimal state diagram.



Bilkent University, EEE 102 Final Exam, Part II, Fall 2020

All of your work/derivation must be shown on the paper to get credit.

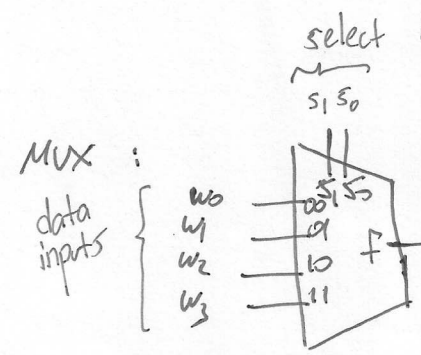
Question 4 [15 pts] Design a 3-bit shift register that shifts to left at each positive edge of the clock using J-K flip flops and minimum number of other gates (if needed), i.e.,

$$Q_2(t+1)Q_1(t+1)Q_0(t+1) = Q_1(t)Q_0(t)S_{in}$$

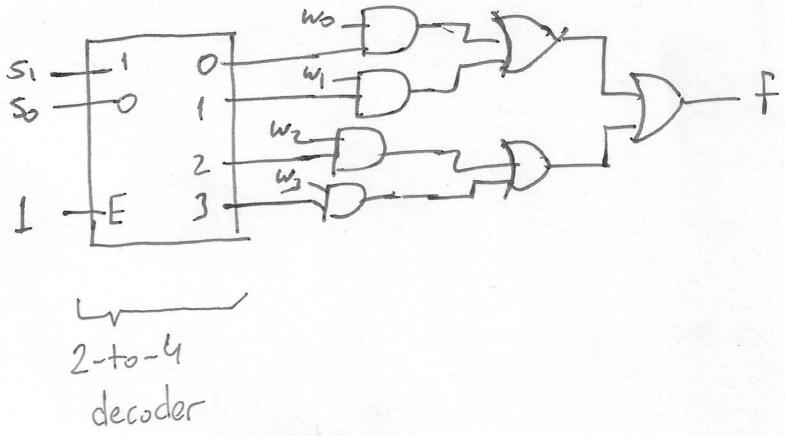
where $Q_i(t)$ represents the state of flip flip i and S_{in} represents 1-bit shift input.

Question 5 [20 pts] Design 8 Byte RAM by combining 4 nibble RAMs.

Q1) 4-to-1 MUX :



$w_0 \bar{s_1} \bar{s_0} + w_1 \bar{s_1} s_0 + w_2 s_1 \bar{s_0} + w_3 s_1 s_0$ (output)



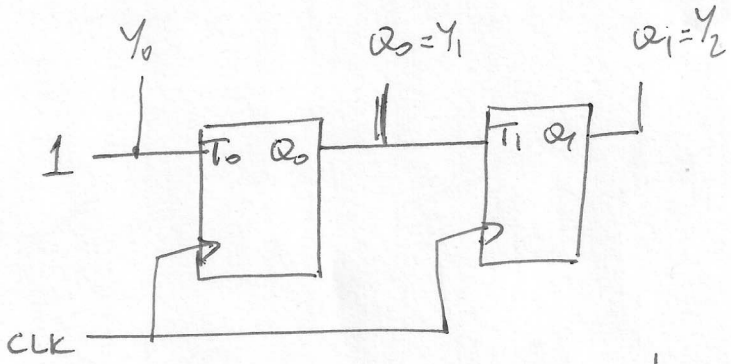
2-to-4 decoder

Q2) 4-states => 2 TFFs (minimum)

State mapping:

	$Q_1\ Q_0$
1	00
3	01
5	10
7	11

2-bit synchronous up counter



state → next state logic

State	Qt	
$Q_1 Q_0$	$Y_2 Y_1 Y_0$	
0 0	0 0 1	(1)
0 1	0 1 1	(3)
1 0	1 0 1	(5)
1 1	1 1 1	(7)

$Y_2 = Q_1$
$Y_1 = Q_0$
$Y_0 = 1$

} output logic

Q3)

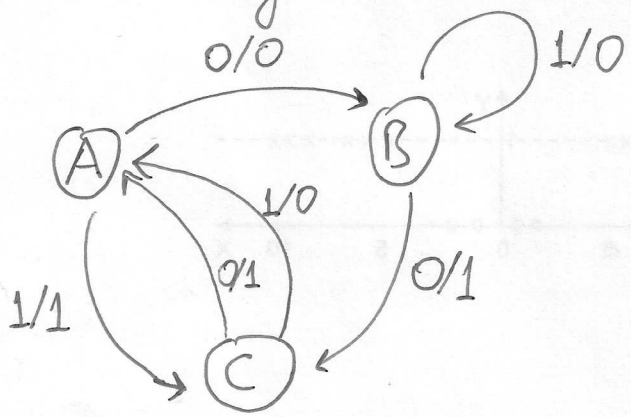
P.S	N.S. x=0	N.S. x=1	o/t x=0	o/t x=1
A	B	C	0	1
B	C	B	1	0
C	D	A	1	0
D	B	C	0	1

States A and D are equivalent.

reduced state table:

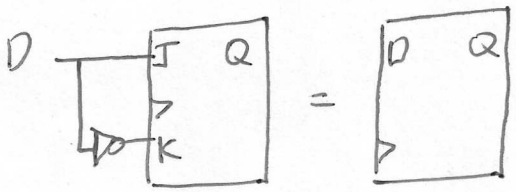
P.S.	N.S. x=0	N.S. x=1	o/t x=0	o/t x=1
A	B	C	0	1
B	C	B	1	0
C	A	A	1	0

minimal state diagram:

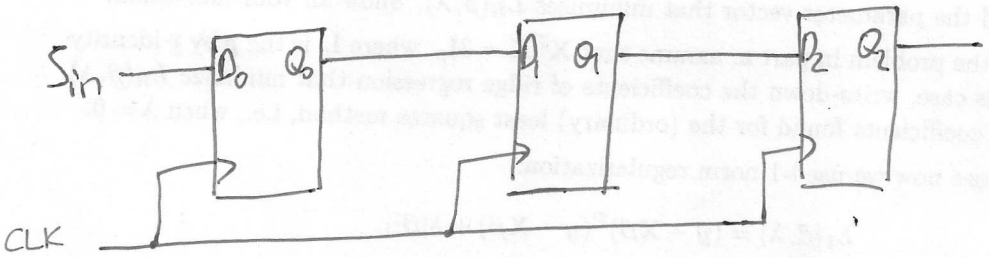


Q4)

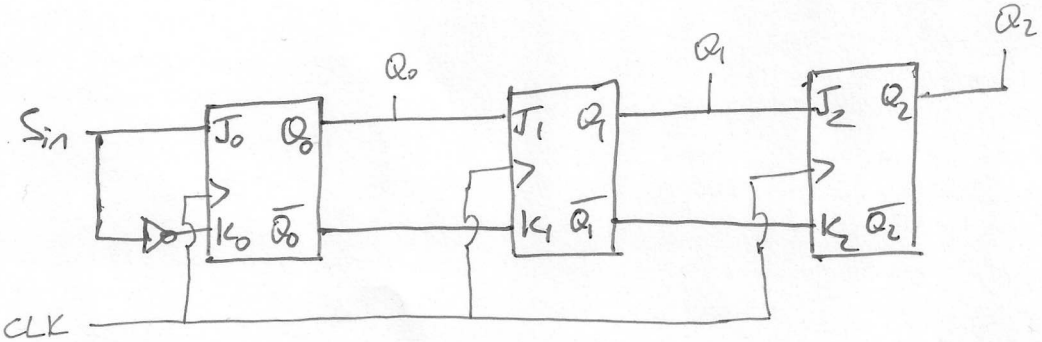
J K	Q(t+1)
0 0	Q(t)
0 1	0
1 0	1
1 1	$\bar{Q}(t)$



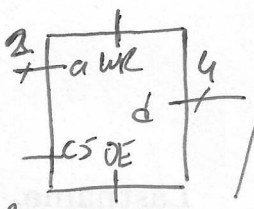
Shift register with D-FF;



Shift register with JK-FF:



Q5) 4-nibble RAM:



8 Byte RAM

address : $a_2 a_1 a_0$
write : WR
output enable : OE
chip select : CS
data : $d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$

} inputs

input/output