EEE 102: Introduction to Digital Circuit Design
Recitation 6

Fall 2023

Problem 1: A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

$$D_A = \bar{X}A + XY \qquad D_B = \bar{X}A + XB \qquad Z = XB$$

(a) Draw the logic diagram (truth table) of the circuit.

(b) Derive the state table.

(c) Derive the state diagram.

Problem 2: Design a sequential circuit with two D flip-flops A and B and one input X. When $X = 0$, the state of the circuit remains the same. When $X = 1$, the circuit goes through the state transitions from 00 to 10 to 11 to 01, back to 00, and then repeats.

Problem 3: The state table for a twisted ring counter is given below. The circuit has no inputs, and its outputs are uncomplemented outputs of the flip-flops.

(a) Design the circuit using D flip-flops. Assume that the unspecified next states are don't care conditions.

(b) Add the necessary logic to the circuit to initialize it to state 000 on power-up master reset.

(c) For the circuit you designed, how would you deal with a situation in which it accidentally enters an unused state if it is implemented in (i) a child's toy, or (ii) a commercial airliner?

Present State	Next State
ABC	ABC
000	100
100	110
110	111
111	011
011	001
001	000

Problem 4: Draw a state diagram for a clocked synchronous state machine with two inputs, $INIT$ and X, and one Moore-type output Z. As long as $INIT$ is asserted, Z is continuously 0. Once $INIT$ is negated, Z should remain 0 until X has been 0 for two successive ticks, regardless of the order of occurrence. Then Z should go to 1 and remain 1 until $INIT$ is asserted again.
Hint: No more than ten states are required.

Problem 5:

(i) A ring counter is a shift register with serial output connected to the serial input.

(a) Starting from an initial state of 1000, list the sequence of states of the four flip-flops after each shift.

(b) Beginning in state 10...0, how many states are there in the count sequence of an n-bit ring counter? How many unused states are there?

(ii) A switch-tail ring counter (Johnson counter) uses the complement of the serial output of a right shift register as its serial input.

(a) Starting from an initial state of 0000, list the sequence of states of the four flip-flops after each shift until register turns to 0000.

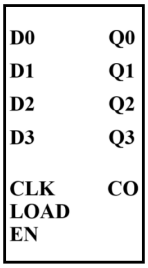
(b) Beginning in state 00...0, how many states are there in the count sequence of an n-bit switch-tail counter? How many unused states are there?

(iii) How many flip-flop values are complemented in an 8-bit binary ripple counter to reach the next count value after,

(a) 11101111

(b) 01111111

Problem 6: Using two binary counters of the type shown in figure and logic gates, construct a binary counter that counts from decimal 9 through decimal 129. Add an additional input to the counter that initializes it synchronously to 9 when the signal $INIT$ is 1.



Problem 7:

(a) Derive the state diagram for an FSM that has an input W and output Z. The machine has to generate $Z = 1$ when the previous four values of W were 1001 or 1111; otherwise, $Z = 0$. Overlapping input patterns are allowed. An example of the desired behavior is:

$$W : 010111100110011111$$
$$Z : 000000100100010011$$

(b) Write the VHDL code for the FSM you derived.