Bilkent University

EEE 102 Digital Design Midterm Exam

12 November 2020, 14:30-16:30

Student Name:

Signature:

I hereby declare that this exam is written by me and is a result of my own work. I am aware of the fact that violation of these clauses is regarded as cheating and can result in annulment of the examination in accordance with the regulations of Bilkent University.

Grade:

1.

2.

3.

4.

1. (15 pts) Short answer questions

What are the binary equivalents of the following decimal numbers?

19 = 10011

1023 = 1111111111

0.5 = 0.1

2.3 = $10.0\overline{1001}$

0.3
0.6
1.2
0.4
0.8
1.6

What are the decimal equivalents of the following signed (two's complement) numbers?

001101 = 13

010001 = 17

110001 = $-32+17=-15$

What are the hexadecimal equivalents of the following binary numbers?

10101 = 15

111100 = 3C

110.1100 6.C

What are the binary equivalents of the following hexadecimal numbers?

E2 = 1110 0010

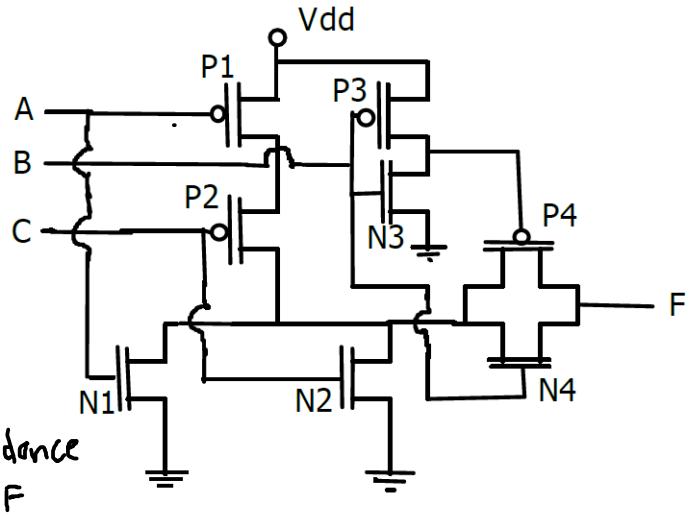
F92 = 1111 1001 0010

What is the result of the following 4-bit signed (two's complement) addition? (3 pts)

1100 + 1111 = 1011

$(-4)+(-1)=(-5)$ result is correct
no overflow

2. (25 pts) For the CMOS circuit below, fill in the table. Your table should display whether NMOS and PMOS transistors are ON or OFF for each of the states of inputs and write down the state of output F. One incorrect answer cancels one correct answer.



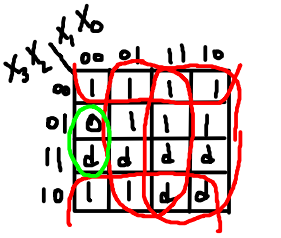
H: high Z: high impedance
L: low 1: ON 0: OFF

A	B	C	N1	P1	N2	P2	N3	P3	N4	P4	F
L	L	L	0	1	0	1	0	1	0	0	Z
L	L	H	0	1	1	0	0	1	0	0	Z
L	H	L	0	1	0	1	1	0	0	1	H
L	H	H	0	1	1	0	1	0	1	0	L
H	L	L	1	0	0	1	0	1	0	0	Z
H	L	H	1	0	1	0	0	1	0	0	Z
H	H	L	1	0	0	1	1	0	1	0	L
H	H	H	1	0	1	0	1	0	1	0	L

3. (35 pts) **Draw** the minimum the sum-of-product and minimum product-of-sum solutions for the digital circuit described by the VHDL code. In your drawing, you can use not-gates, and- and or-gates with any number of inputs.

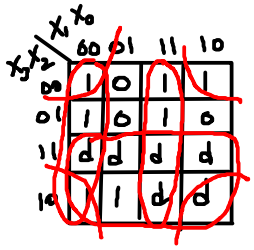
```
entity q3 is
   Port ( x : in STD_LOGIC_VECTOR (3 downto 0);
          s : out STD_LOGIC_VECTOR (1 downto 0));
end q3;

architecture q3_arch of q3 is
begin
 with x select
  s <= "11" when "0000",
       "10" when "0001",
       "11" when "0010",
       "11" when "0011",
       "01" when "0100",
       "10" when "0101",
       "10" when "0110",
       "11" when "0111",
       "11" when "1000",
       "11" when "1001",
       "--" when others;  -- this is DON'T CARE
end q3_arch;
```



$S_1 = (\bar{X}_2 + X_1 + X_0)$ SOP and

$= (\bar{X}_2 + X_1 + X_0)$ POS solutions are the same

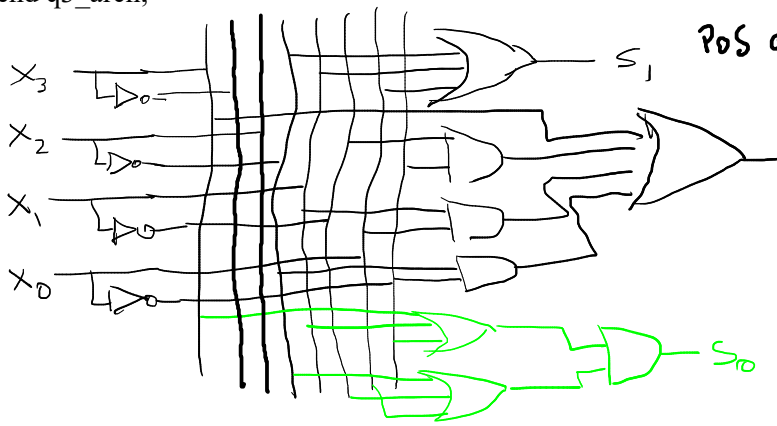


$S_0 = X_3 + \bar{X}_1 \cdot \bar{X}_0 + X_1 \cdot X_0 + \bar{X}_2 \cdot \bar{X}_0$

min SOP

$S_0 = (X_3 + X_1 + \bar{X}_0) \cdot (\bar{X}_2 + \bar{X}_1 + X_0)$

min POS



POS and SOP circuits are the same

SOP circuit

POS circuit

4. (25 pts) Design a circuit that performs the following operation using only full adders. No other gates or components are allowed.

Inputs: Three 4-bit numbers A = $a_3a_2a_1a_0$, B = $b_3b_2b_1b_0$, C = $c_3c_2c_1c_0$

Output: One 4-bit number D = $d_3d_2d_1d_0$

We want D = A + $(-1)^{V(C)}$ x B, where all numbers A, B, C, D are in two's complement representation, and V(C) represents the decimal equivalent of C.