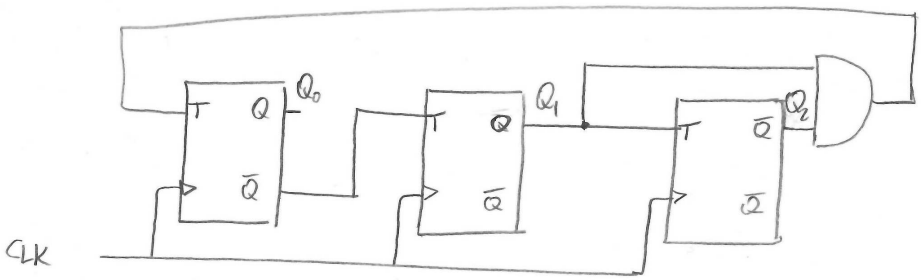
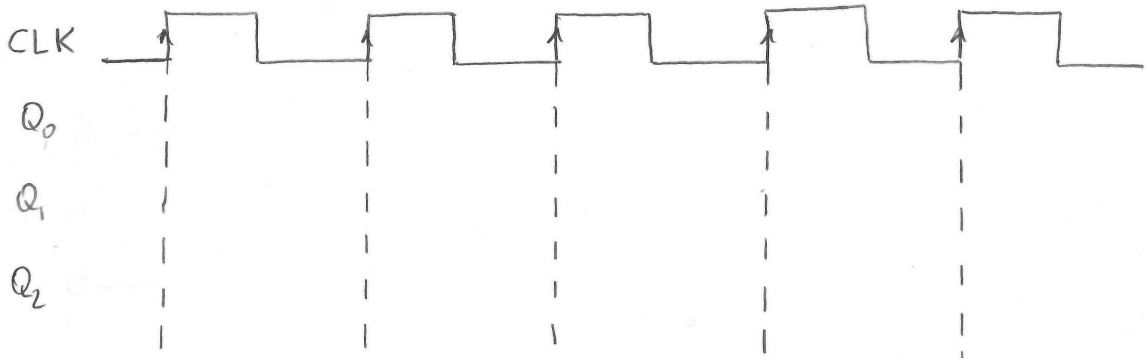
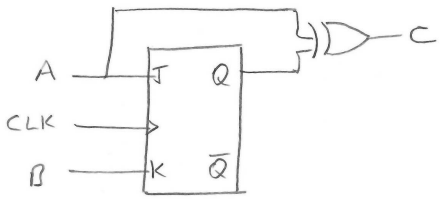
1. **[25pts]** Complete the timing diagrams of the circuits given below. Assume that the flip-flop states (outputs) are 0 initially.

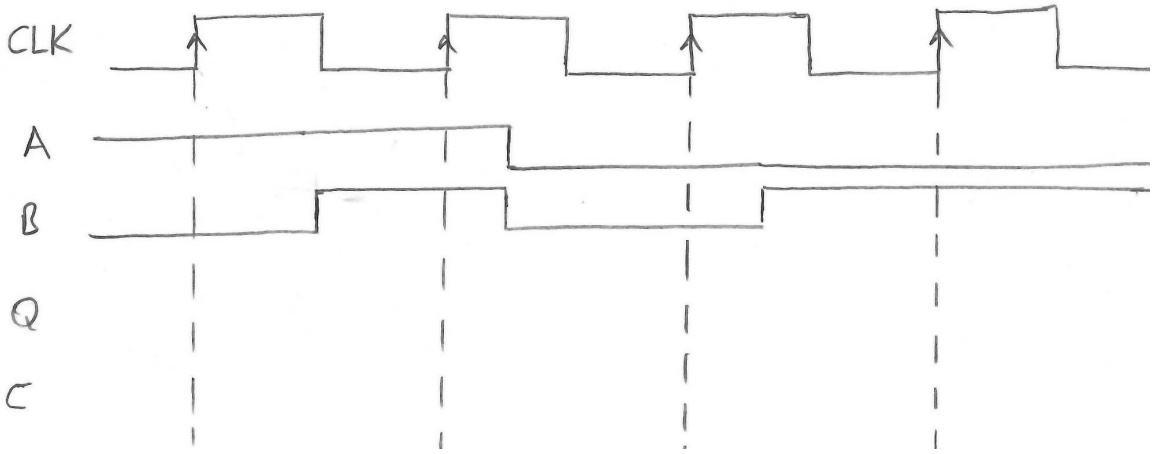
a [12 pts]





b [13 pts]





2. **[25 pts]**

Design a 3-bit shift register with inputs R (1 bit), S_1S_0 (2 bits) and $I_2I_1I_0$ (3 bits), and outputs $Q_2Q_1Q_0$ (3 bits) that performs the following operations:

- $S_1S_0 = 00$: No change, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = Q_2(t)Q_1(t)Q_0(t)$
- $S_1S_0 = 01$: Shift right, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = RQ_2(t)Q_1(t)$
- $S_1S_0 = 10$: Circular shift left, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = Q_1(t)Q_0(t)Q_2(t)$
- $S_1S_0 = 11$: Load, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = I_2(t)I_1(t)I_0(t)$

You are only allowed to use D-flip flops and multiplexers (make sure that you don't use more than necessary number of multiplexers and flip-flops).