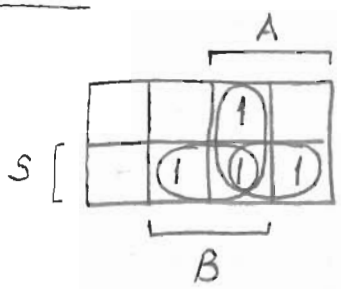
1. a) Design a minimal NAND/NAND circuit with three inputs S, A, B and one output F that has the following function table.

S	F
0	A AND B
1	A OR B

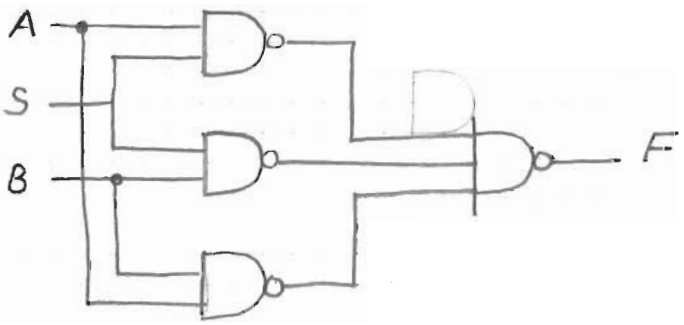
b) Implement F in part (a) with a minimal NOR/NOR circuit

SOLUTION:

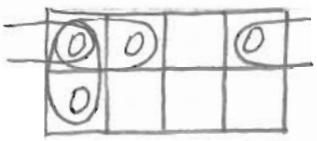
a)



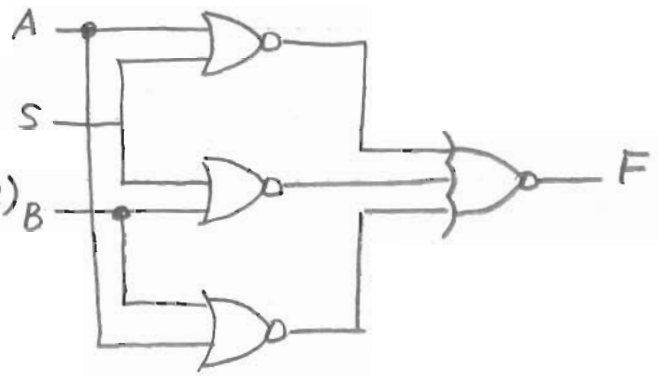
$F = AB + SA + SB$



b)

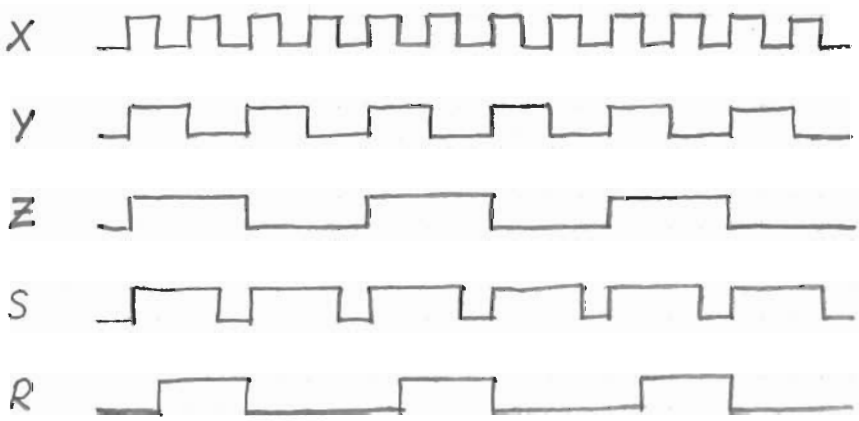


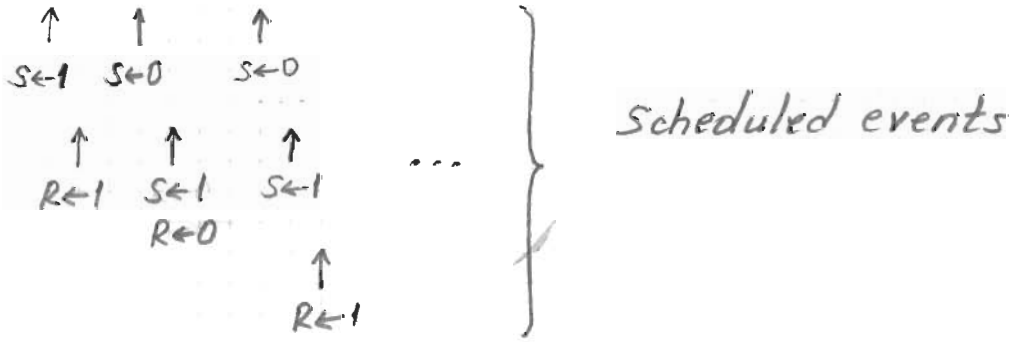
$F = (A+B)(S+A)(S+B)$



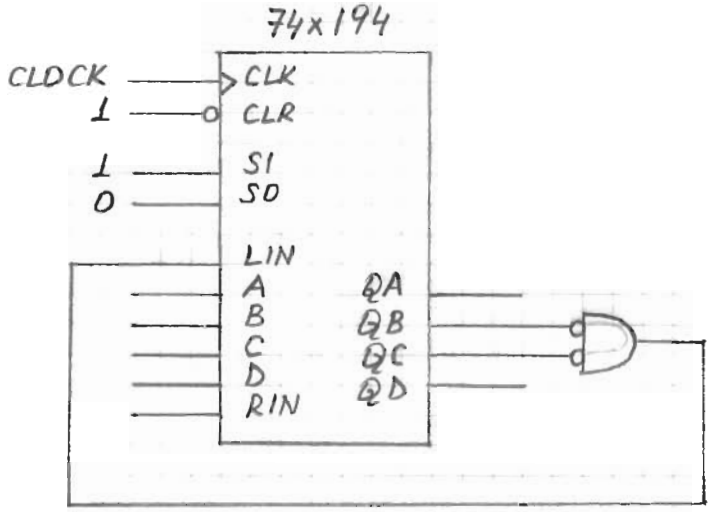
2. The following process is part of the architecture of an entity with inputs X, Y, Z and outputs S and R. Plot the waveforms of S and R corresponding to given X, Y and Z. Indicate the time instants at which an event is scheduled together with the scheduled event.

```
process (X,Y)
begin
   S ⇐ X or Y;
   R ⇐ S and Z;
end process;
```





3. Draw the state diagram of the following sequential circuit whose states are coded as $Q_A Q_B Q_C Q_D$. The function table of the shift register 74x194 is as given.



SI	SO	QA^*	QB^*	QC^*	QD^*
0	0	QA	QB	QC	QD
0	1	RIN	QA	QB	QC
1	0	QB	QC	QD	LIN
1	1	A	B	C	D

SOLUTION :

Wired as left-shift register with $LIN = (QB + QC)'$

(0) 0000 ↓ (1) 0001 ↓ (3) 0011 ↓ (6) 0110 ↓ (12) 1100 ↓ (8) 1000 ↓ (1) 0001

(2) 0010 ↓ (4) 0100 ↓ (8) 1000

(11) 1011 ↓ (6) 0110

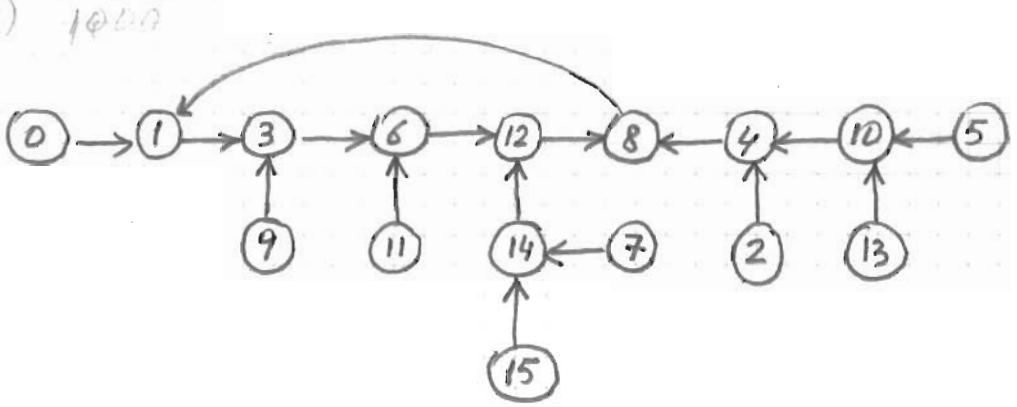
(5) 0101 ↓ (10) 1010 ↓ (4) 0100

(13) 1101 ↓ (10) 1010

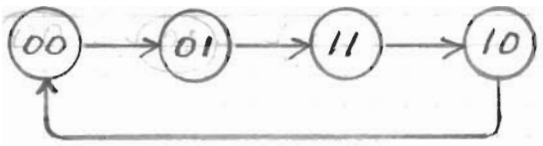
(7) 0111 ↓ (14) 1110 ↓ (12) 1100

(15) 1111 ↓ (14) 1110

(9) 1001 ↓ (3) 0011



4. a) Design a 2-bit counter that has the following state diagram. Use D flip flops.



b) Use the counter in part (a) and a generic 4-to-1 multiplexer (but nothing else) to construct a Mealey machine with four inputs A, B, C, D and one output Y such that Y is A at the first tick of the clock, B at the next tick, C at the third tick, D at the fourth tick, A again at the fifth and so on.

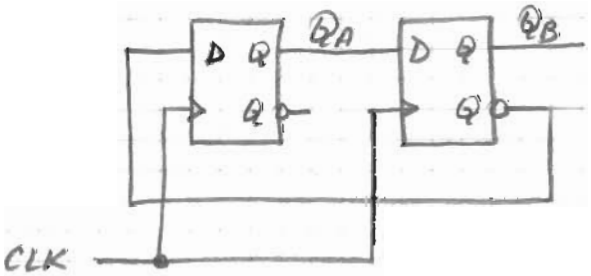
SOLUTION :

a)

Q_B	Q_A	Q_B^*	Q_A^*
0	0	0	1
0	1	1	1
1	0	0	0
1	1	1	0

$D_B = Q_A$

$D_A = Q_B'$



b)