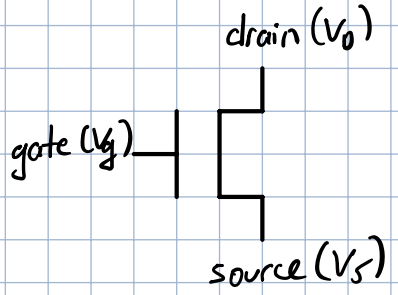
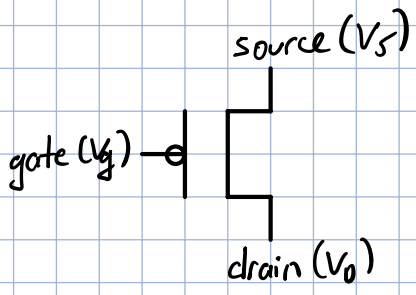
Chapter 3

Transistors

MOSFET: Metal-oxide semiconductor field effect transistor

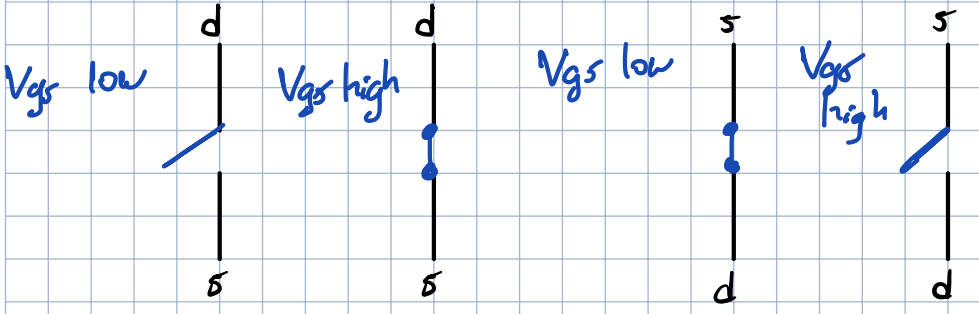




$V_{gs} = V_g - V_S$

NMOS

PMOS



Act like a switch controlled by V_{gs}.

For NMOS: if $V_{gs} > V_T$ ($V_T \sim 0.2 V_{DD} \sim 1$ volt) then

transistor is on, drain-source resistance is low $\sim 1\,k\Omega$

else if $V_{gs} < V_T$ then

transistor is off, drain-source resistance is very high $\sim 10^{12}\,\Omega$

For PMOS: if $V_{gs} < -V_T$ then

transistor is on

else if $V_{gs} > -V_T$ then

transistor is off

How many transistors modern processors have?

Core i7 Haswell: 2.6 billion (2014)

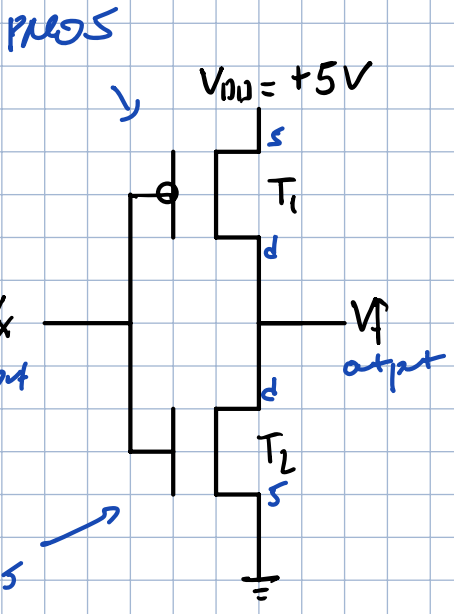
Apple A12 Bionic: 6.9 billion (2018)

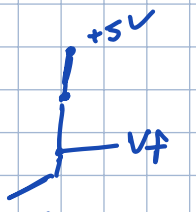
Apple A14 Bionic: 11.8 billion (2020)

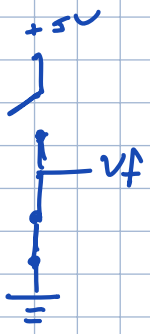
Apple M1 : 16 billion

Apple A17 Pro : 19 billion

Complementary MOS (CMOS) Logic Gates







	V_x	T_1	T_2	V_f
L	0	on	off	5
H	5	off	on	0

(*) default convention

positive logic: 5V = logic 1

0V = logic 0

x	f
0	1
1	0

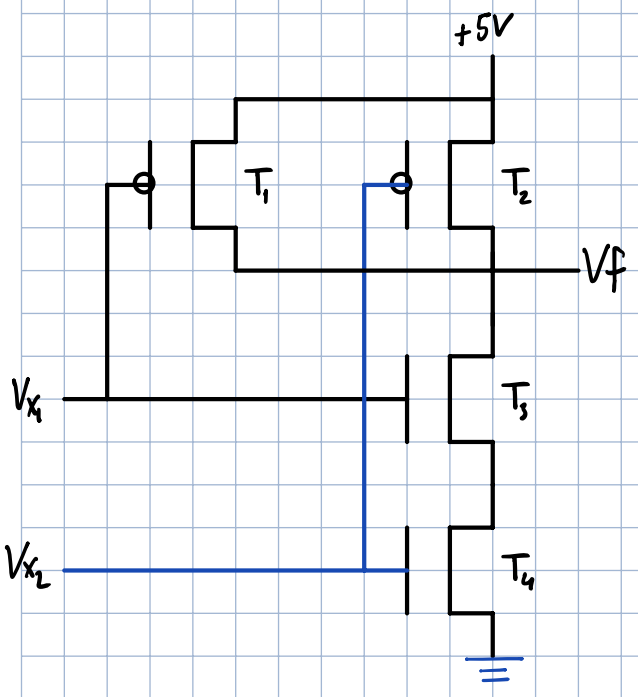
=> inverter

* No current flow when input signal is stable (high or low)

⇒ No power dissipation

$f = \overline{x_1 \cdot x_2} = \bar{x}_1 + \bar{x}_2$ ⇒ PMOS in parallel

⇒ NMOS in series since it is complementary to PMOS.



V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	H
H	L	H
H	H	L

⇒ positive logic / standard

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

x_1 NAND x_2

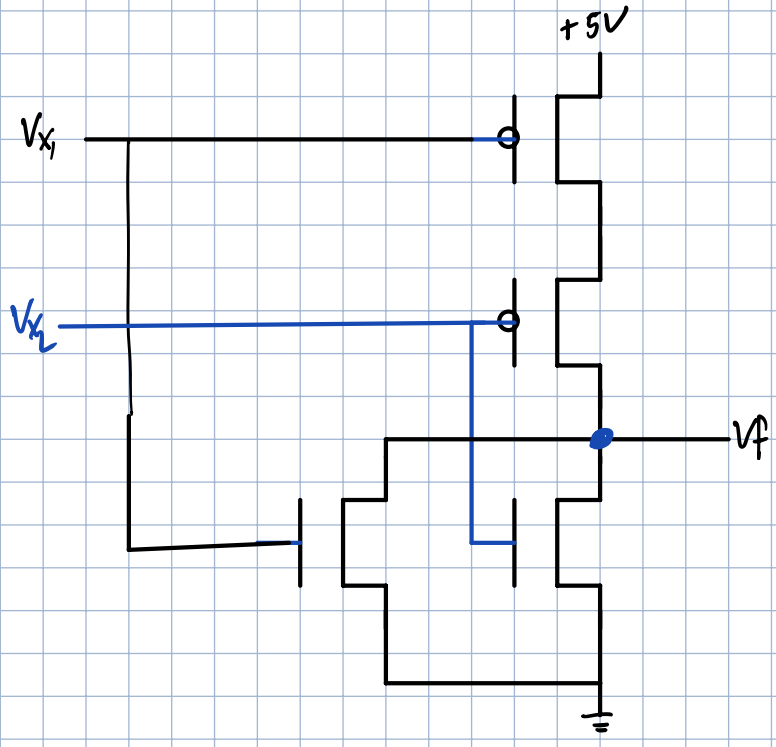
⇒ negative logic

(H = logic 0, L = logic 1)

x_1	x_2	f
1	1	0
1	0	0
0	1	0
0	0	1

x_1 NOR x_2

$f = \overline{x_1 + x_2} = \bar{x}_1 \cdot \bar{x}_2$ ⇒ PMOS in series ⇒ NMOS in parallel



V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	L
H	L	L
H	H	L

⇒ positive logic

x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

NOR

⇒ negative logic

(H = logic 0, L = logic 1)

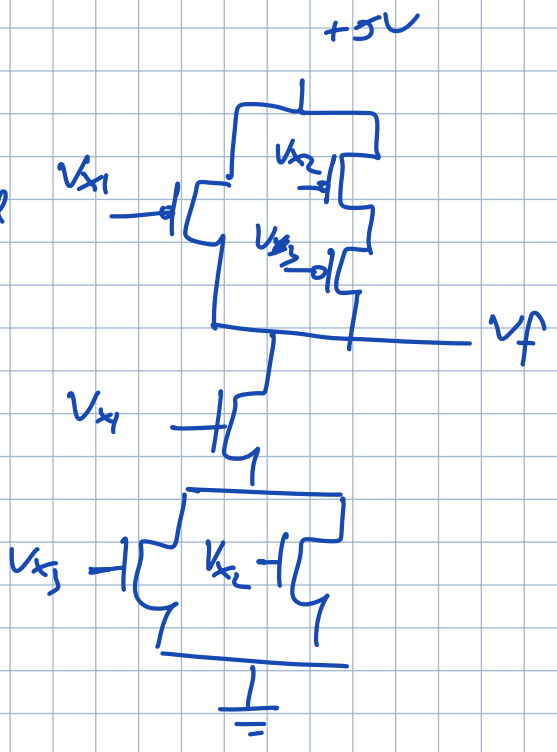
x_1	x_2	f
1	1	0
1	0	1
0	1	1
0	0	1

NAND

Logic Functions in CMOS

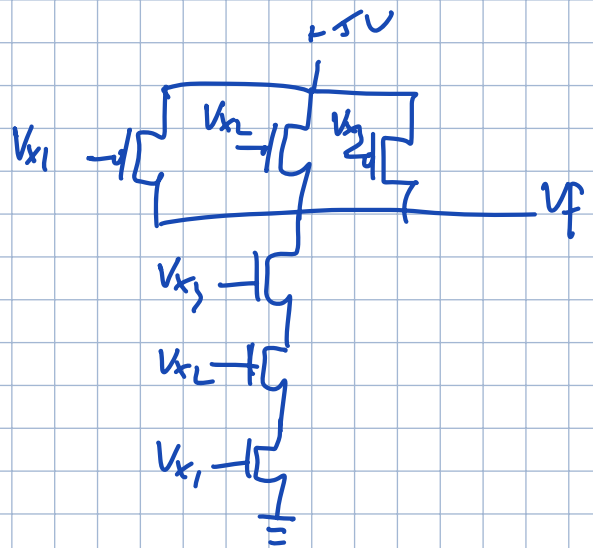
Example: $f = \bar{x}_1 + \bar{x}_2 \bar{x}_3$ — PMOS series; PMOS in parallel

x_1	x_2	x_3	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

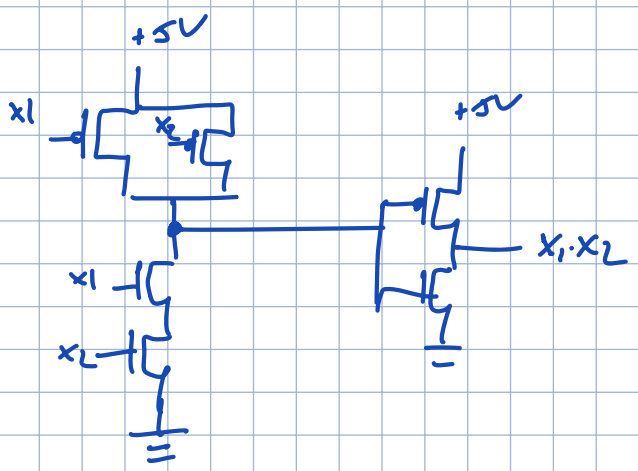


(3-input NAND)

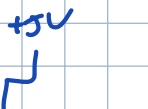
$f = \overline{x_1 \cdot x_2 \cdot x_3} = \bar{x}_1 + \bar{x}_2 + \bar{x}_3$

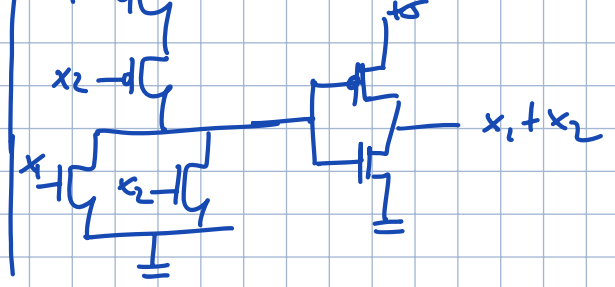


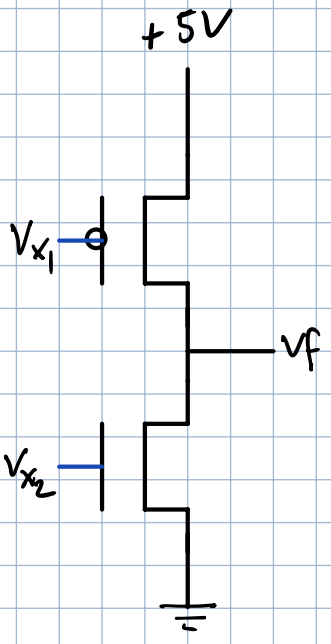
$f = x_1 \cdot x_2$ (AND)



$f = x_1 + x_2$ (OR)

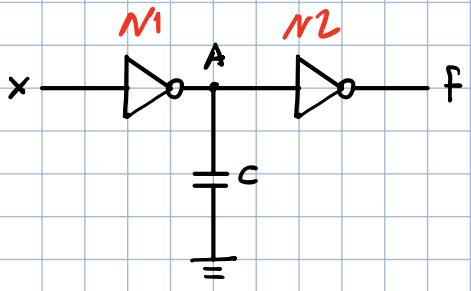


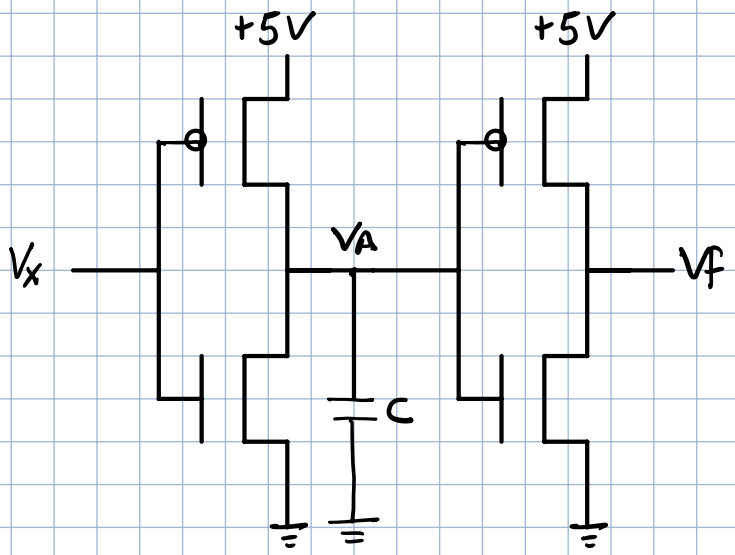




V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	short
H	L	Z (high-Z, high impedance)
H	H	L

Delay

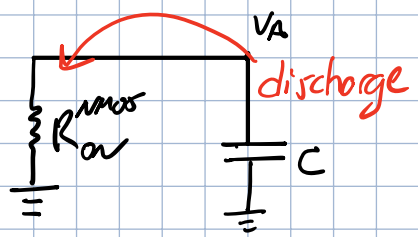




gate-source capacitance

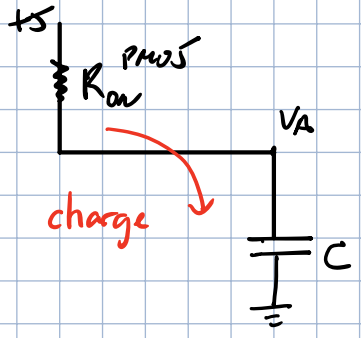
PMOS in N1 turns on ↑ V_{GS}
NMOS " " " " ↓ 0

Assume that initially $V_x = L$, $V_A = H$. Then $V_x = H$, $V_A : H \to L$

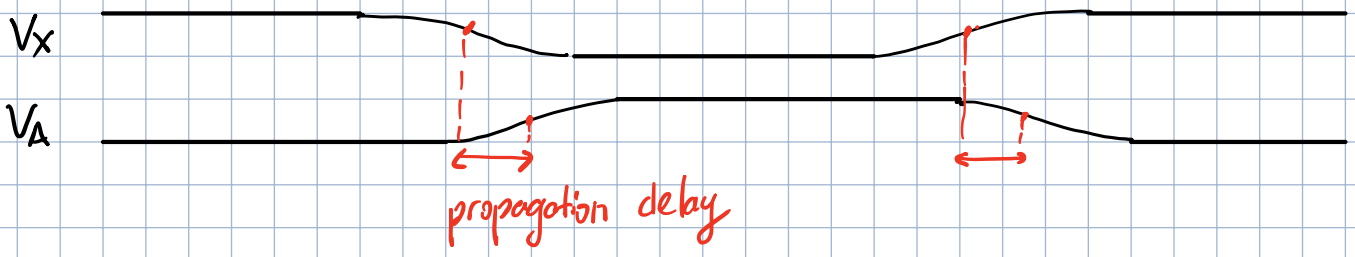


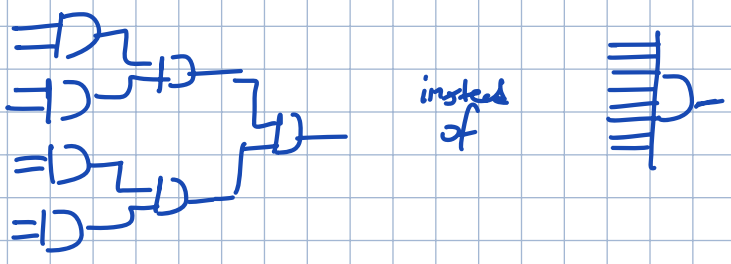
$R_{on}^{nmos} \times C = \tau_{off}$ (turn-off time)

Assume that initially $V_x = H$, $V_A = L$. Then $V_x = L$, $V_A : L \to H$



$R_{on}^{PMOS} \times C = \tau_{on}$ (turn-on time)





Fan-in

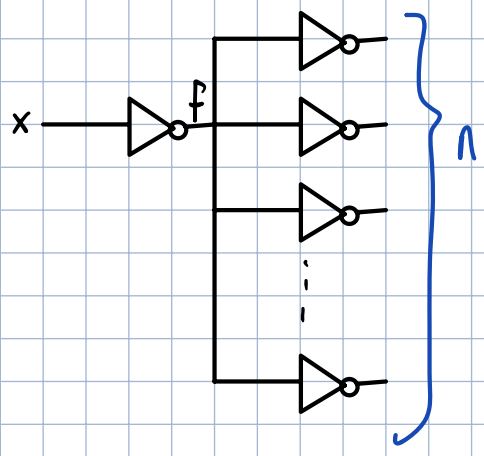
Number of inputs of the gate.

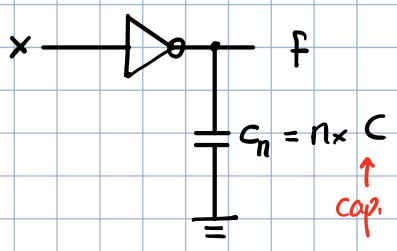
High fan-in CMOS is not practical

(ex: 100 input NAND requires 100 NMOS in series)

Fan-out

Number of gates driven by a gate

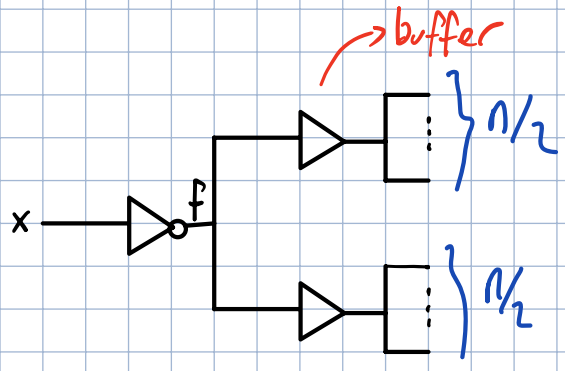


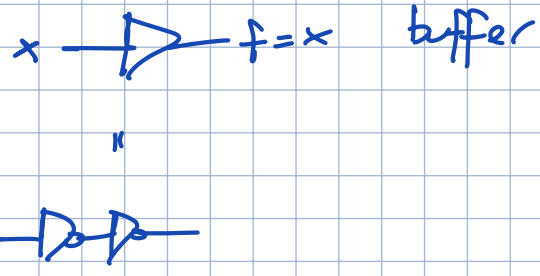


↑ cap. of each inverter connected to f

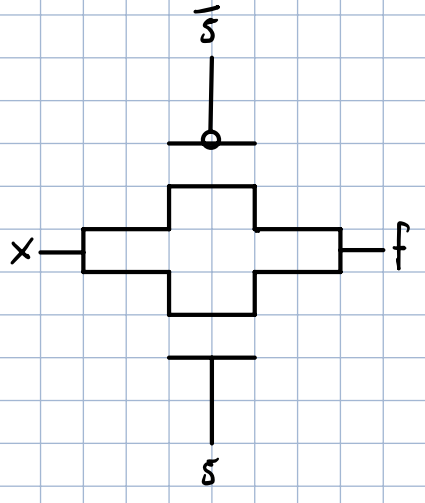
* high fan-out ⇒ high propagation delay

Solution: Use buffers to limit max number of gates driven by a gate.





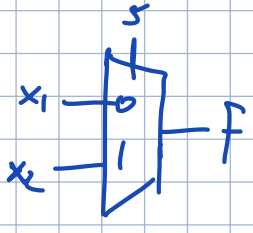
Transmission gate



$s=0 \Rightarrow x \not\leftrightarrow f$ disconnected

$s=1 \Rightarrow x \leftrightarrow f$ connected.

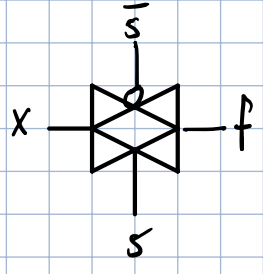
Multiplexer (2-to-1)



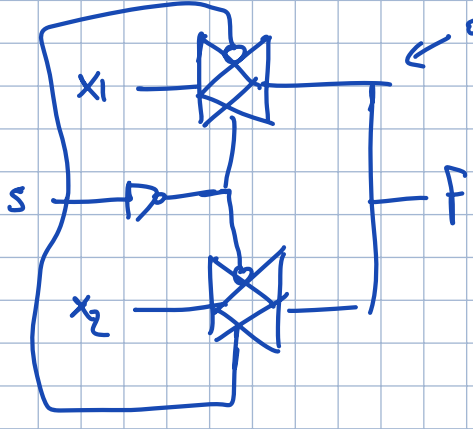
$f = x_1$ when $s=0$

$= x_2$ " $s=1$

symbol



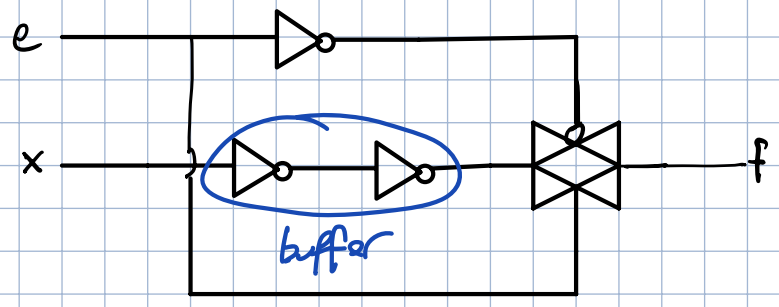
design using transmission gate



← one of them must be Z at all times

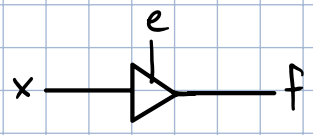
6 transistor implementation

Tri-state buffer

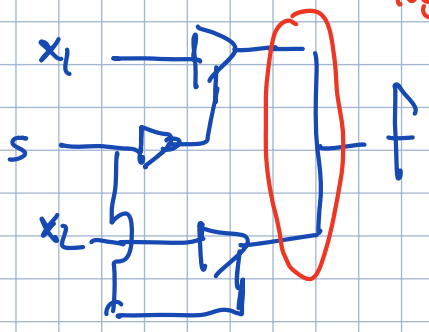


e	x	f
0	0	Z
0	1	Z
1	0	0
1	1	1

Symbol:

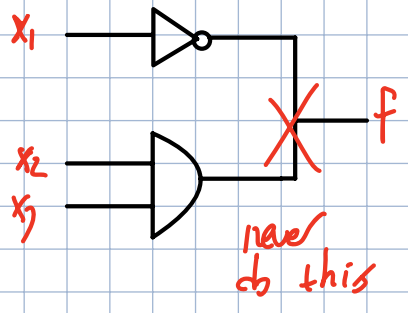


outputs connected together



2-to-1 MUX using tri-state buffers:

Can we connect outputs of ordinary gates together?



$x_1 = 0,\ x_2 = x_3 = 1,\ f = 1$

$x_1 = 0,\ x_2 = 0,\ x_3 = 1,\ f = ?$

$\Rightarrow$ short circuit — output conflict