Lastname, Name:_____
ID:_____

EEE 102: Introduction to Digital Circuit Design

Midterm Exam 2

April 4, 2019

Duration: 120 min

Q	1	2	3	4	Total
Pts	25	25	25	25	100
Score					

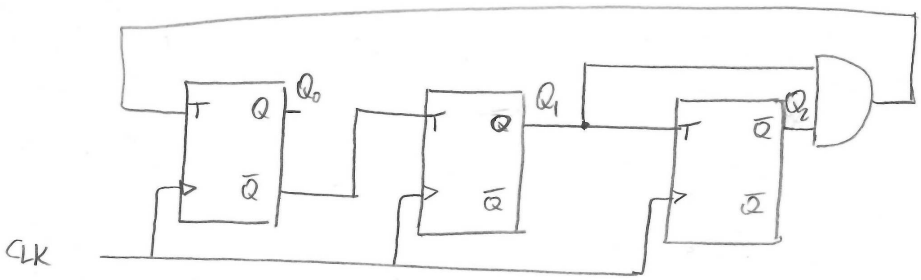
This is a closed-book and closed-notes exam.

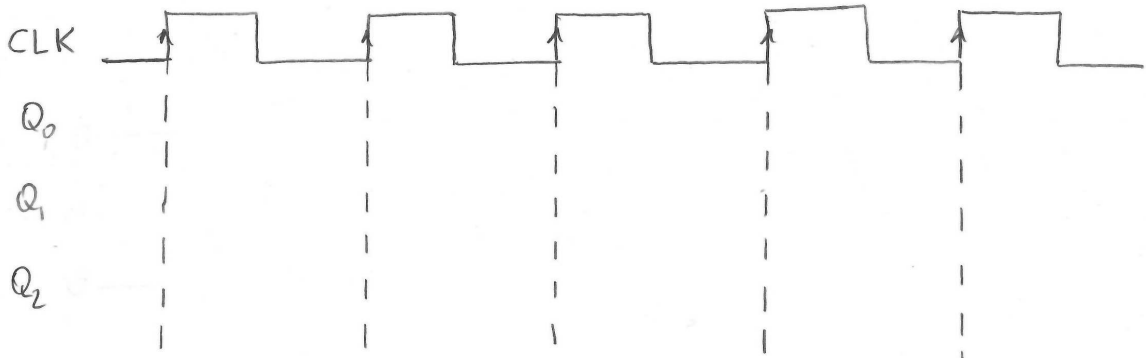
NO CREDIT will be given to answers without clear, formal and clean

JUSTIFICATION.

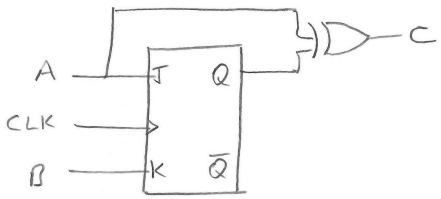
1. **[25pts]** Complete the timing diagrams of the circuits given below. Assume that the flip-flop states (outputs) are 0 initially.

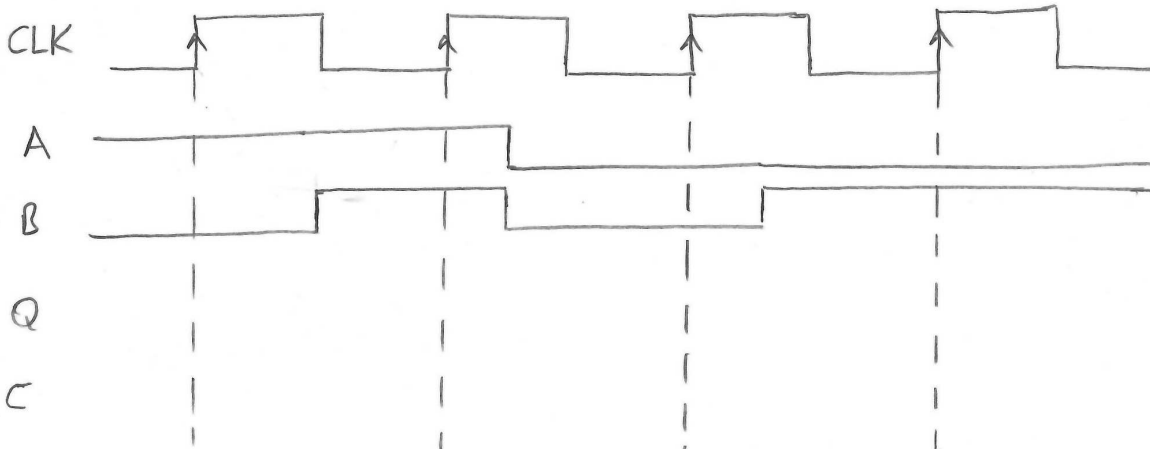
a [12 pts]





b [13 pts]





2. **[25 pts]**

Design a 3-bit shift register with inputs R (1 bit), S_1S_0 (2 bits) and $I_2I_1I_0$ (3 bits), and outputs $Q_2Q_1Q_0$ (3 bits) that performs the following operations:

- $S_1S_0 = 00$: No change, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = Q_2(t)Q_1(t)Q_0(t)$
- $S_1S_0 = 01$: Shift right, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = RQ_2(t)Q_1(t)$
- $S_1S_0 = 10$: Circular shift left, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = Q_1(t)Q_0(t)Q_2(t)$
- $S_1S_0 = 11$: Load, i.e., $Q_2(t+1)Q_1(t+1)Q_0(t+1) = I_2(t)I_1(t)I_0(t)$

You are only allowed to use D-flip flops and multiplexers (make sure that you don't use more than necessary number of multiplexers and flip-flops).

3. **[25 pts]**

a [12 pts] Design a 16-to-1-line multiplexer using a 4-to-16-line decoder and a 16x2 AND-OR, i.e., output of 16 2-input AND gates are OR'ed.

b [13 pts] Design a 4-to-1-line multiplexer using a 2-to-4-line decoder and 4 3-state buffers.[12 Points]

4. **[25 pts]**

   a [10 pts] Implement $F(A, B, C, D) = BC + DC + AC + \bar{D}$ in the optimal Sum of product (SOP) form.

   b [15 pts] Implement $F(A, B, C, D) = BC + DC + AC + \bar{D}$ using a minimum number of two input gates and a single 4 to 1 multiplexer.