

1. [25 pts]

- a. [10 pts] Implement the following function using a minimum number of 3-to-8 decoder and a single 2-to-1 multiplexer. Complemented variables and logic levels 0 and 1 are NOT available.

$$F(A, B, C, D) = AB(\bar{C}D + C\bar{D})$$

- b. [15 pts] Design a circuit using ONLY a minimum number of full adders that multiplies a given unsigned 3-bit number with 3. The complements of the variables are not available. You can use logic levels 0 and 1.

2. [25 pts]

- a. [10 pts] You are given a synchronous counter with a synchronous load and an asynchronous clear that counts $0, 1, 2, \dots, 15, 0, 1, 2, \dots$. With this counter implement a new counter that gives $5, 6, 7, 8, 9, 5, 6, 7, 8, 9, \dots$ using a minimum number of gates.
- b. [15 pts] A serial two's complementer is to be designed. A binary integer of arbitrary length is presented to the serial two's complementer, least significant bit first, on input X . When a given bit is presented on input X , the corresponding output bit is to appear during the same clock cycle on output Z . To indicate that a sequence is complete and that the circuit is to be initialized to receive another sequence, input Y becomes 1 for one clock cycle. Otherwise, Y is 0. Give the state diagram and the state table where you clearly explain the meaning of each state.

3. [25 pts] A single input (x), two output (y, z) synchronous sequential circuit checks the equality of two sequences at clock t . If $x_{t-2} = x_t$, then $y = 1$ and $z = x_t x_{t-1}$. Otherwise $y = 0$ and $z = 0$. Assume all inputs at $t < 0$ are 0. An example input and the corresponding output sequences are shown below:

t	0	1	2	3	4	5	6	7	...
x	0	0	0	1	0	1	1	1	...
y	1	1	1	0	1	1	0	1	...
z	0	0	0	0	0	0	1	1	...

- [7 pts] Find the state transition diagram.
- [8 pts] Give the state transition table and minimize it.
- [10 pts] Design the circuit with a minimum number of clocked T-type flip-flops and NAND gates.