Lastname, Name:_____
ID:_____

EEE 102: Digital Systems Design

Midterm Exam 2

April 12, 2016

Duration: 90 min

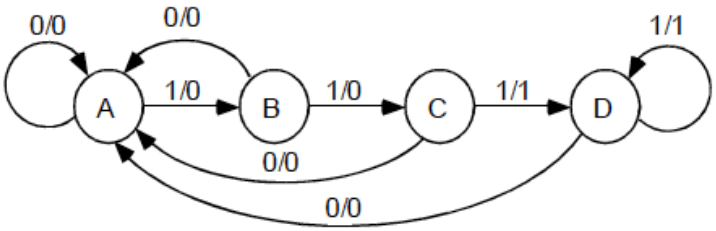
Q	1	2	3	4	Total
Pts	25	25	25	25	100
Score					

This is a closed-book and closed-notes exam.

NO CREDIT will be given to answers without clear, formal and clean

JUSTIFICATION.

1. **[25 pts]** Consider the state diagram given in the figure below. Consider the following **almost one hot state assignment** that requires three flip flops: $A = 000$, $B = 001$, $C = 010$, $D = 100$. **Treat transitions out of unused states as don't cares!**



(i) (10 pts) Draw the state and output table for the sequential circuit using this state assignment.
(ii) (10 pts) For each present state, input value and next state entry on the state table, write down on the state table the T flip flop inputs that will be used to achieve the corresponding state transition.
(iii) (5pts) Are there any equivalent states in the state diagram? If you answer is yes, identify them and write down the simplified state diagram.

2. [**25 pts**] Design a sequential circuit with one bit serial input X and serial output Z. The circuit outputs $Z = 1$ **immediately** when the number of times sequence 01 occurred in the input is odd and $Z = 0$ when the number of times sequence 01 occurred in the input is even (or 0). When the circuit is asynhronously reset, it will return into the state in which 01 has never occurred before. An example of input - output sequence is shown below:

X	1	0	0	1	1	0	1	1	0	0	1	0	...
Z	0	0	0	1	1	1	0	0	0	0	1	1	...

Design this circuit using minimal number of states. In your design use minimal number of D flip flops and minimal number of **two input** NAND gates. For this problem, complement of the input variable and complemented Flip Flop outputs are available.

3. **[25 pts]**

Design a sequential circuit, which synchronously outputs

Y : 1 0 0 0 1 0 0 0 1 0 0 0 1 ...

You can only use FG-type flip-flop, where an FG-type flip-flop is defined as follows:

F	G	Q(t+1)
0	0	inverse(Q(t))
0	1	1
1	0	0
1	1	Q(t)

and a minimum number of NOR gates.

4. **[25 pts]**

Design a clocked synchronous state machine with two inputs X and Y, and one output Z. The output should be $Z = 1$ if the number of 1 inputs on X and Y since reset is odd, and $Z = 0$ otherwise. You can only use T-type flip flops and a minimum number of NAND gates.