1)[25 Points]

i)(5 Points) Design a JK-type flip-flop using a T-type flip-flop and any type of minimum number of gates.

ii) (10 Points) Design a half adder with a minimum number of 2-1 multiplexers. The complements of the variables are NOT available. However, you can use logic 1 and 0. No other gates are available.

iii) (10 Points) Implement F(X,Y,X) = X(Y'Z+YZ') with a single 2-to-4 decoder and a single 2-to-1 multiplexer.

2) [25 Points] Design a clocked synchronous state machine with two inputs X and Y, and one output Z. The output should be 1 if the number of 0 inputs on X and Y since reset is a multiple of 4, and 0 otherwise. You are allowed to use only T-type flip flops

a) Find the state transition diagram. [5 Points]

b) Give the state transition table and minimize it. [5 Points]

c) Design the circuit with clocked T-type flip-flops and any gates. [15 Points]

3) [25 Points] Design a mod-4 up/down counter. There is a control input S. If S=0, then the counter counts up. If S=1, then the counter counts down.

a) [5 Points] Find the state diagram; clearly explain the meaning of each state.
b) [5 Points] Find the state table.
c) [15 Points] Implement the machine using a minimum number of any type of gates and the following AB-type flip-flop. An AB-type flip-flop is defined as follows:

A	B	Q(t+1)
0	0	0
0	1	0
1	0	1
1	1	Q(t)