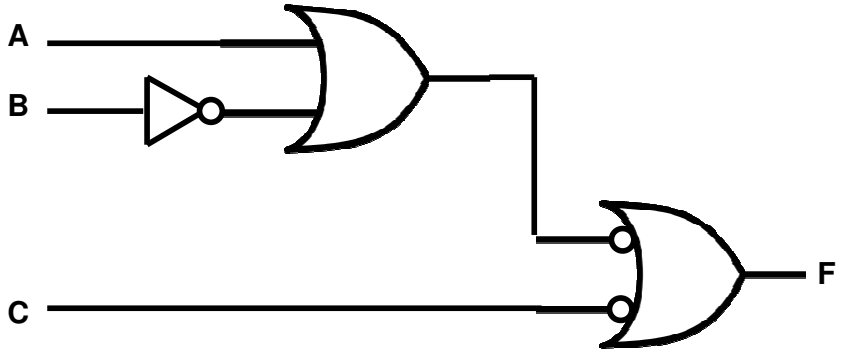
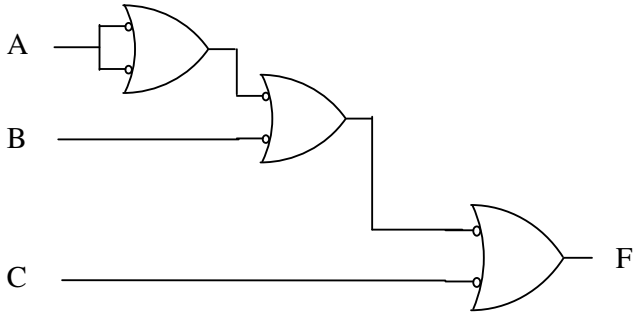
EEE102
Sample Problems for Fall 2009
19-9-2008
BUBBLE to BUBBLE LOGIC

Q1.
Draw the following logic circuit by using 2-input NAND gates only,

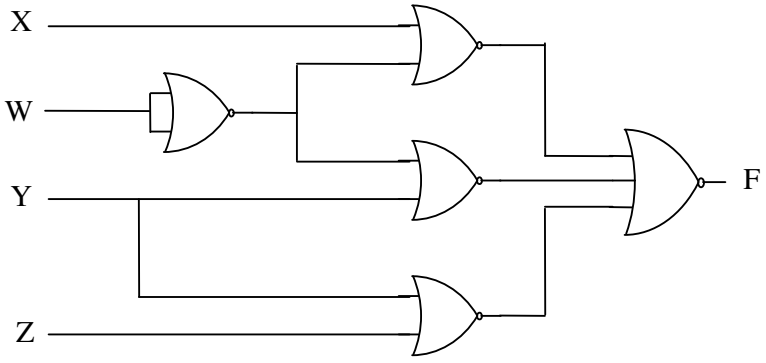


Solution:



Q2.
Draw the schematics of F = (W'+X)(W'+Y)(Y+Z) using NOR gates only.

Solution:



Q3.

For the function G = $(A \cdot B + (C \cdot D)') \cdot (E' + F')$,

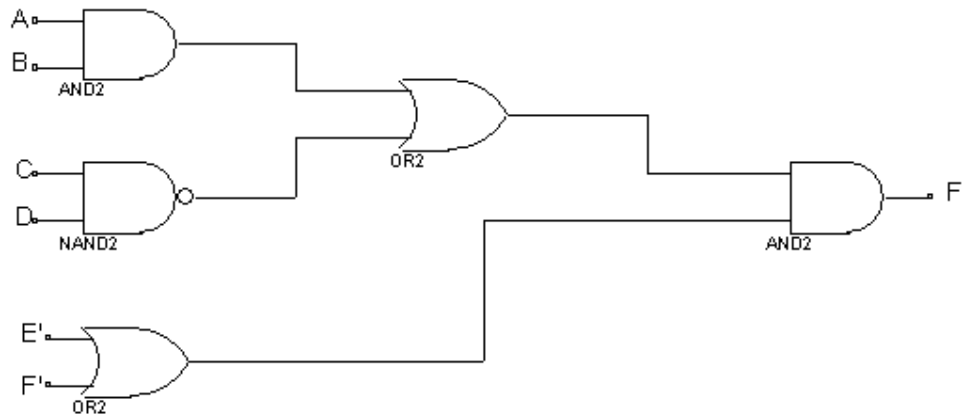
a) Draw the circuit diagram using AND, OR, NOT gates. Do not change the expression,

b) Change all gates to NAND gates including inverters if necessary,

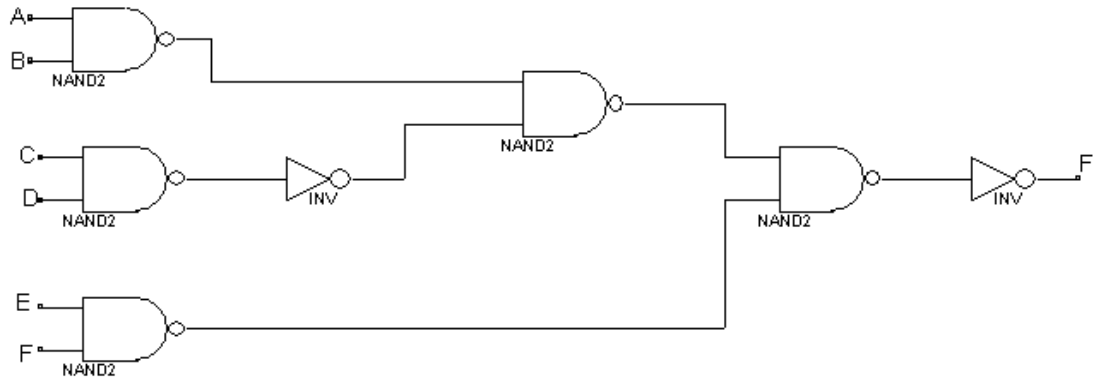
c) Change all gates to NOR gates including inverters if necessary.

Solution:

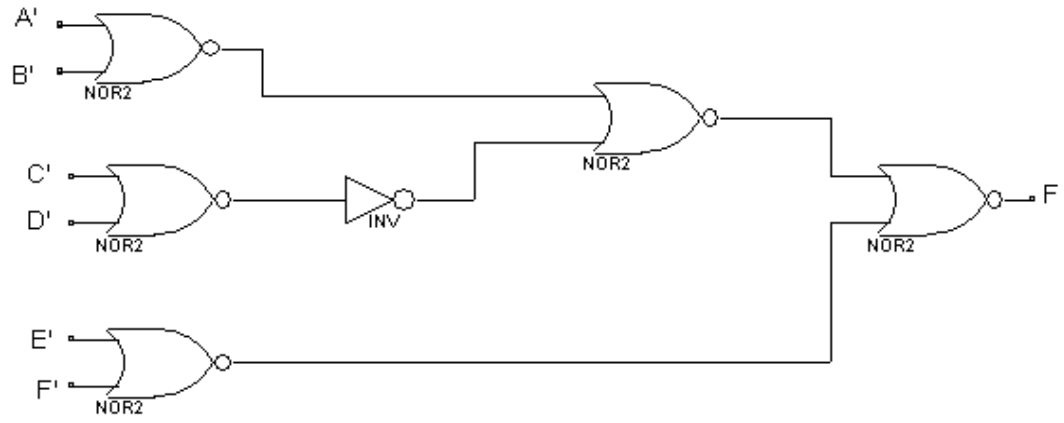
a)



b)



c)



Note that in the solutions above there are inverters which can be obtained from NAND gates or NOR gates. Similarly for the primed variables you need inverters.

Q4.

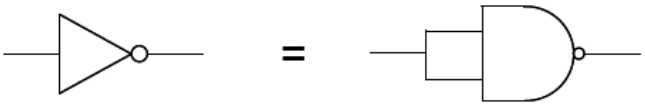
Prove using the canonical SOP representation of a combinational logic function that NAND gates are sufficient to implement any combinational logic circuit.

Solution:

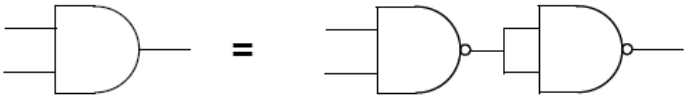
Method I:

Any combinational logic function can be represented in Canonical SOP form. It is trivially straightforward to implement the Canonical SOP form using inverters (to implement complemented literals), AND gates (to implement the products), and OR gates (to implement sums). It is sufficient to show that we can implement each of inverter, AND, and OR gate using NAND gates.

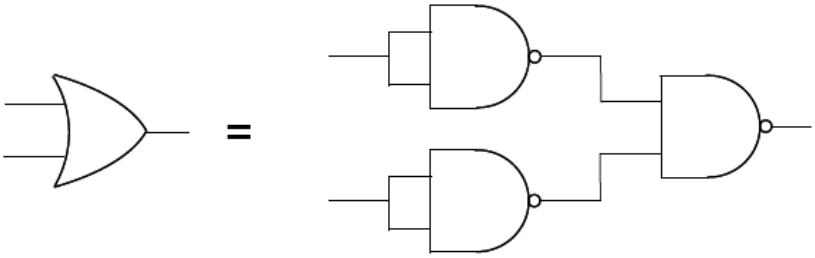
Inverter:



AND:



OR:



Method II: Show inverter implementation as in Method II. Instead of showing AND and OR implementation independently, just show the implementation of AND-OR combination used in Canonical SOP form.