1. (25 pts) Let $F(X_1, X_2, X_3, X_4) = (X_1 + X_2)\ \overline{X_3} + X_1\ X_2\ X_4 + \overline{X_1}\ \overline{X_3}$

(i) Fill the Karnaugh map for F given below. (7pts)

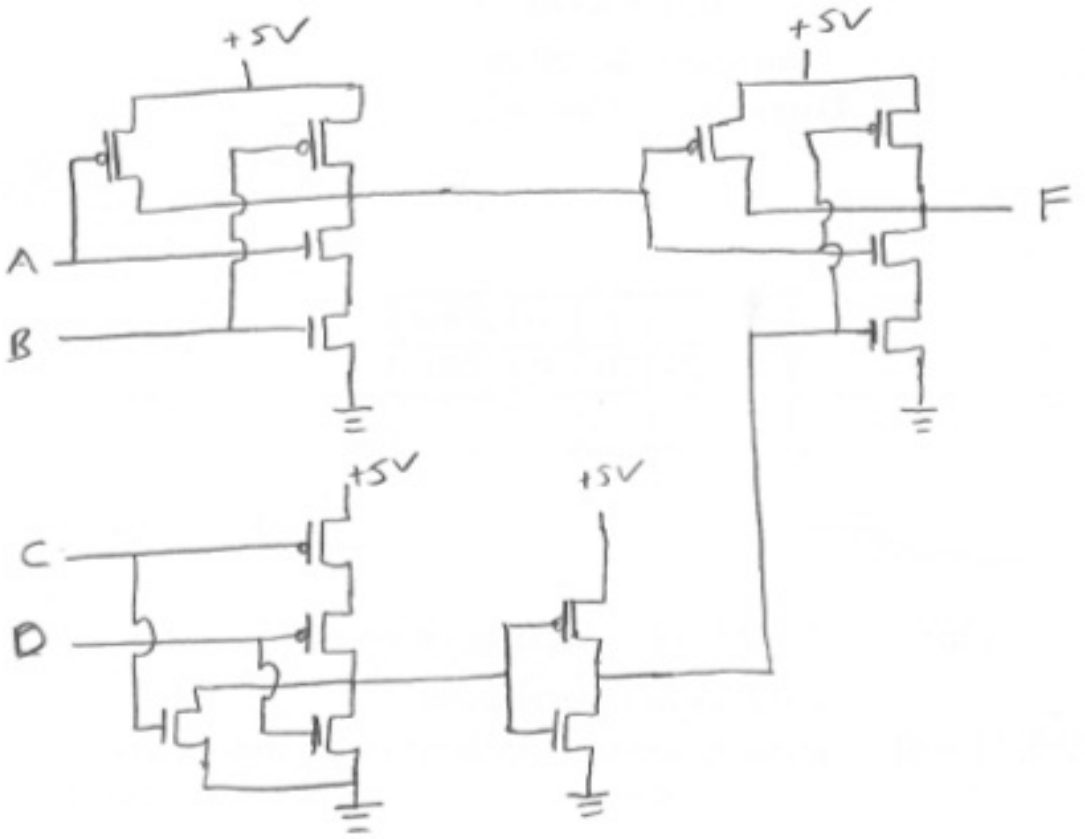
KMAP for F

X_3X_4 \ X_1X_2	00	01	11	10
00				
01				
11				
10				

(ii) Find the Boolean expression for the minimum sum of products form of F using the method of Karnaugh map (**your answer to part i must be correct to get credit from this part**). (10pts)

(iii) Implement F using minimum number of NAND gates (any input size is allowed). Complements of the variables and logic levels 0 and 1 are **not** available (you need to produce them). (8pts)

2. (25 pts)
(i) Write down the logic function Y=f(A,B,C,D) that the circuit below implements. (15 pts)



(ii) Implement Y= A B + C using minimum number of transistors in CMOS technology. Complements of the variables are available. (10 pts)

3. (25 pts) Design a circuit that converts any 3-bit number to its negative in two's complement system using only minimum number of full adders. Use of any other gates is not allowed. The complements of the variables are not available. You can use logic levels 0 and 1.

4. (25 pts)

(i) Convert 16.15_8 to binary. (5pts)

(ii) Convert 10111.001101_2 to hexadecimal. (5pts)

(iii) Convert 112.5_{10} to binary (5pts)

(iv) Design a 3-to-1 multiplexer (that selects one of the 3 inputs) using only transmission gates. Your design must only include transmission gates, no other gates are allowed. Complements of the variables are available. (10pts)