Lastname, Name:_____
ID:_____

EEE 102: Digital Systems Design

Midterm Exam 1

March 24, 2013

Duration: 90 min

Q	1	2	3	Total
Pts	30	35	35	100
Score				

This is a closed-book and closed-notes exam.

NO CREDIT will be given to answers without clear, formal and clean

JUSTIFICATION.

1. **[30 pts]**

   a. [15 pts] Design a half-adder using only a minimum number of 2-to-1 multiplexers. Logic levels 1 and 0 are available. However, complements of the variables are NOT available.

   b. [15 pts] In the two's complement number system, design a logic circuit that converts a 3-bit number to its negative, using a minimum number of NAND gates.

2. **[35 pts]**

a. [20 pts] Design a full subtractor (which is similar to a full adder) that performs subtraction between two 1-bit numbers. As the inputs, the circuit has a minuhend bit, a subtrahend bit and a previous borrow bit. As the outputs, the circuit has the result bit and the next borrow bit. You are allowed to use only two 3-to-8 decoders and a minimum number of OR gates. Complements of the variables, logic levels 1 and 0 are available. As an example,

Previous borrow	1
Minuhend bit	1
Subtrahend bit	0
Result bit	0
Next Borrow bit	0

b. [15 pts] Design a synchronous modulo-2 adder, e.g.,

Input	0	1	1	0	0	1	1	...
Output	0	1	0	0	0	1	0	...

3. **[35 pts]** Design a single input (x) synchronous sequential circuit required to operate as follows:

x	Output
0	0,1,2,3,0,1,2,3,0,...
1	3,2,1,0,3,2,1,0,3,...

using a minimum number of NOR gates. As an example, we have

x	0	0	0	0	1	1	0	...
Output	0	1	2	3	2	1	2	...