Design, Simulation, and Performance Analysis of Cascode Current Mirror Configurations for Enhanced Analog Circuit Efficiency

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Introduction

In the domain of analog and mixed-signal integrated circuit (IC) design, the ability to manage and control current flow is a critical determinant of circuit efficiency and reliability. Among the several techniques developed to achieve this objective, current mirrors (CMs) hold a place of fundamental importance. A current mirror is essentially a current-replicating device that senses current through an input branch and reproduces a proportional current in the output branch, maintaining consistency regardless of the load. Beyond simple replication, current mirrors are also capable of amplifying or attenuating the reference current, which makes them indispensable in biasing, signal processing, and power management within analog circuits.

Despite their wide applicability, traditional current mirror topologies face inherent limitations. Parameters such as output resistance, voltage headroom, common-mode rejection ratio (CMRR), noise suppression, and power efficiency become critical challenges, especially in nanoscale CMOS technologies where devices must operate under lower supply voltages while meeting stringent performance demands. These drawbacks necessitate circuit-level modifications to ensure higher precision, stability, and energy efficiency. It is within this context that cascode current mirrors (CCMs) emerge as a promising solution.

Cascode current mirrors represent a modified configuration of the conventional CM, designed specifically to address its limitations. By incorporating an additional transistor stack, CCMs achieve significantly enhanced output resistance and improved voltage gain, making them suitable for applications requiring high linearity and wide bandwidth. Moreover, their superior power supply rejection ratio (PSRR) ensures that signal integrity is preserved even under fluctuating supply conditions.

In summary, current mirrors form the backbone of modern analog and mixed-signal circuits, but their conventional versions face limitations that restrict their use in advanced applications. Cascode current mirrors offer a refined solution by enhancing output resistance, improving linearity, and reducing noise and distortion. This paper investigates three different cascode current mirror designs, presenting simulation results and comparative analysis of gain, noise PSD, and power consumption. By exploring these configurations in depth, the work underscores the potential of CCMs as a means to achieve enhanced analog circuit efficiency, paving the way for future innovations in integrated circuit design.

Problem Statement

The continuous advancement of analog and mixed-signal circuit technology has created a growing demand for efficient, reliable, and noise-resilient building blocks. Among these, current mirrors (CMs) play a fundamental role, as they are extensively used in operational amplifiers, voltage regulators, analog-to-digital converters, sensor interfaces, and communication circuits. Their ability to replicate or scale a reference current is critical for establishing stable biasing conditions and ensuring consistent circuit performance. However, while conventional current mirrors have proven useful, they suffer from inherent limitations that restrict their effectiveness in modern integrated circuits.

One of the primary issues with traditional current mirror topologies lies in their relatively low output resistance, which reduces gain and compromises accuracy. Additionally, they are highly sensitive to channel length modulation effects and device mismatches, resulting in degraded linearity and signal distortion. In high-frequency applications, these drawbacks become even more pronounced, leading to poor bandwidth performance and reduced stability. Moreover, as modern devices increasingly emphasize low-power operation, conventional current mirrors often fail to achieve optimal energy efficiency, as they exhibit higher power dissipation under certain operating conditions. These challenges underscore the necessity of exploring improved circuit architectures capable of meeting the stringent performance requirements of nanoscale CMOS technologies.

Cascode current mirrors (CCMs) have emerged as a promising solution to these challenges. By introducing additional transistors in a cascode arrangement, CCMs enhance output resistance, improve power supply rejection ratio (PSRR), and minimize the effects of device mismatches. This enables them to achieve higher gain, reduced noise, and superior linearity compared to simple mirror configurations. Furthermore, CCMs are particularly effective in applications such as differential amplifiers and unity gain buffers, where accurate signal replication and stable amplification are essential. Despite these advantages, the performance of different CCM configurations under varying input and supply conditions has not been comprehensively compared in terms of gain, noise power spectral density (PSD), and power consumption.

The problem, therefore, lies in identifying which cascode current mirror configuration provides the optimal balance of gain, noise suppression, and power efficiency for practical analog circuit applications. Without such an analysis, circuit designers face difficulties in selecting the most suitable topology for their specific needs, leading to potential inefficiencies and trade-offs in performance.

Objective

The central objective of this study is to design, simulate, and analyze cascode current mirror (CCM) configurations with the goal of improving the efficiency and reliability of analog circuits. Since current mirrors form the backbone of many analog and mixed-signal integrated circuits, enhancing their performance directly translates into higher circuit stability, reduced distortion, and better energy management in practical applications. The present research therefore seeks to evaluate multiple cascode current mirror topologies under different operating conditions and identify the configuration that offers the most favorable balance of gain, noise performance, and power consumption.

To achieve this overarching aim, the study is guided by the following specific objectives:

1. Design of Cascode Current Mirror Configurations

- Develop three distinct cascode current mirror circuits: (a) a differential pair with an active current mirror at 5V input, (b) a differential pair with an active current mirror at 1.5V input, and (c) a unity gain buffer circuit.

2.Simulation of Circuit Behavior

-Conduct AC analysis to determine the gain characteristics of each configuration, thereby assessing the ability of the circuits to provide effective signal amplification.

3.Comparative Performance Analysis

-Analyze and compare the results of the three configurations to understand trade-offs between gain, noise, and power consumption.

4.Validation of Cascode Topology Advantages

- Demonstrate how cascode modifications to traditional current mirrors improve performance parameters such as output resistance, linearity, bandwidth, and PSRR.

Through these objectives, the research aims not only to present a detailed performance evaluation of cascode current mirrors but also to provide design guidelines that can be adopted by engineers in creating future low-power, high-efficiency integrated circuits. Ultimately, the outcomes of this study will contribute to improved circuit design strategies for applications ranging from sensor interfacing to communication systems, where precision, low noise, and energy efficiency are of paramount importance.

Methodology

This study followed a structured approach consisting of circuit design, simulation, and performance analysis of cascode current mirror (CCM) configurations.

1. Design Setup

Tool: Cadence Virtuoso (ADE L).

Technology: 90 nm CMOS (GPDK90).

Supply Voltage: 5V DC.

2. Circuit Configurations

Case 1: Differential pair with active current mirror (5V input).

Case 2: Unity gain buffer using cascode mirror (1 µV input).

3. Simulations Performed

DC Analysis → Checked input-output behavior, biasing.

AC Analysis → Measured circuit gain across frequency range.

Noise Analysis → Calculated Noise Power Spectral Density (PSD).

4. Parameters Measured

Gain (dB) – Amplification capability.

Noise PSD ($\mu V^2/Hz$) – Signal quality and distortion level.

Power Consumption (pW) – Energy efficiency of each design.

5. Comparative Evaluation

All results tabulated and compared.

Trade-offs identified:

Case 1 → Lowest noise, efficient power.

Case 2 → Highest gain, slightly higher noise.

Case 3 → Very low gain, highest power usage.

6. Validation

Results confirmed advantages of CCMs in terms of output resistance, PSRR, and linearity over conventional current mirrors.

Literature Review/ Application Survey

Current mirrors have been an essential part of analog integrated circuits for decades due to their ability to replicate, scale, and stabilize currents within a design. Their simplicity and effectiveness have led to their adoption in applications such as operational amplifiers, low-dropout regulators, current-mode A/D converters, and voltage level shifters. However, as technology has advanced, limitations such as low output resistance, channel length modulation effects, and limited frequency response have prompted researchers to explore improved topologies.

Early studies focused on simple and Wilson current mirrors, emphasizing improved matching and output resistance. For instance, Deo et al. analyzed MOSFET-based differential amplifiers with different current mirror loads and reported that diode-connected topologies achieved higher CMRR (31.48 dB) compared to Wilson and Widlar mirrors. While these offered performance improvements, noise resilience and low-power operation remained major concerns in nanoscale CMOS processes.

Cascode current mirrors (CCMs) emerged as a refined topology to address these challenges. Xie et al. introduced an active-input cascode current mirror that consumed only 40 µW while maintaining less than 1.4% replication error, demonstrating the superiority of CCMs in power-sensitive designs. Similarly, Iqbal et al. performed simulations of folded cascode sources, showing that CCMs enhanced output resistance and bandwidth while providing improved linearity. These studies confirm that cascode architectures consistently outperform conventional mirrors in terms of gain, noise suppression, and power efficiency.

In terms of applications, CCMs have been widely deployed in differential amplifiers and unity-gain buffers. Differential pairs using CCMs exhibit higher output resistance, better linearity, and enhanced common-mode rejection ratio (CMRR), making them suitable for high-precision analog signal amplification. Unity gain buffer circuits with cascode configurations, on the other hand, are valued for their impedance transformation ability, extended bandwidth, and low distortion, which are critical in audio processing, sensor interfacing, and communication systems. Recent research has also highlighted their relevance in low-voltage and portable device designs, where high efficiency and minimal power loss are crucial for extended battery life.

Despite these advancements, there remains a lack of comparative studies evaluating multiple CCM configurations under the same design and technology conditions. While individual works have demonstrated specific benefits—such as low noise, high gain, or improved linearity—few studies present a holistic performance analysis that examines trade-offs among gain, noise PSD, and power consumption. This gap is particularly significant given the increasing demand for optimized building blocks in modern integrated circuits.

Therefore, this study contributes to the existing literature by performing a systematic comparison of three CCM-based configurations—two differential pairs with different input conditions and one unity gain buffer—using a consistent 90 nm CMOS framework. By analyzing gain, noise PSD, and power consumption in a unified environment, the work provides valuable insights into the suitability of different CCM topologies for diverse analog circuit applications.