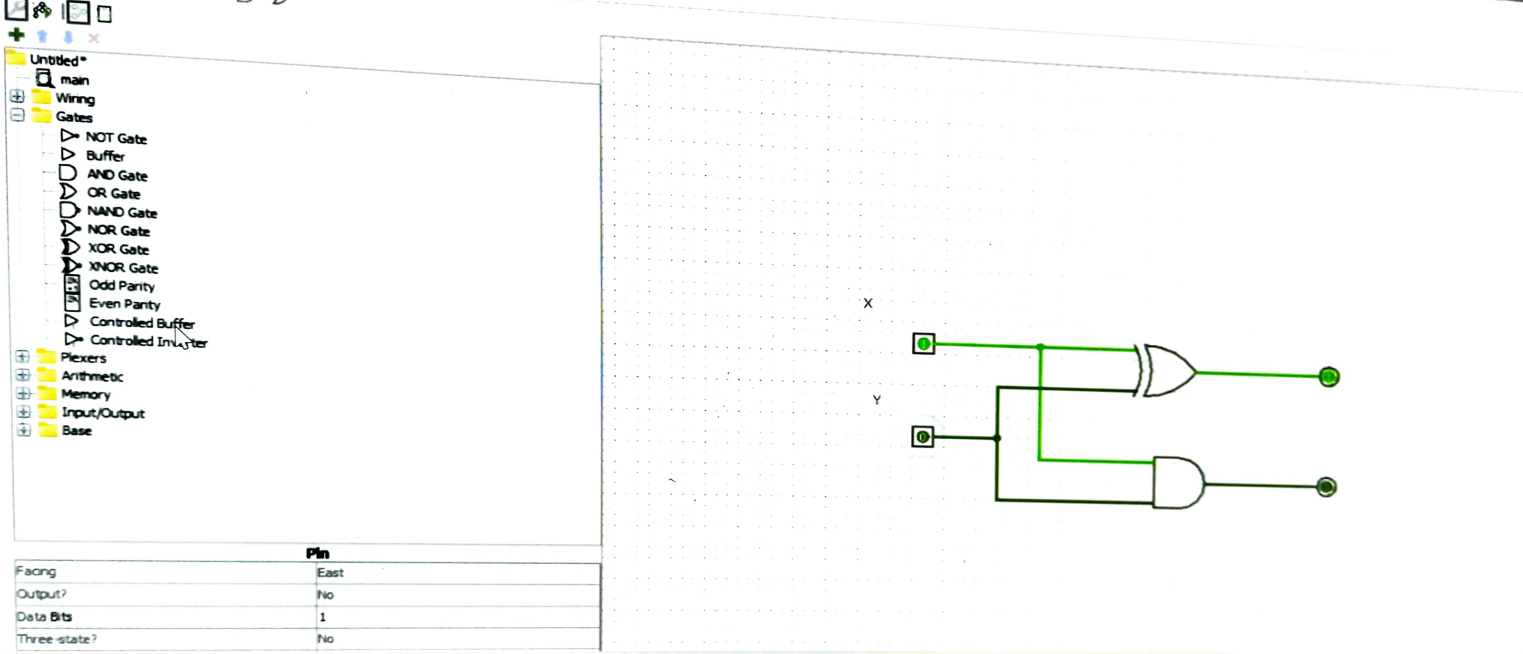
Untitled*
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Memory
Input/Output
Base
X
Y
Pin
Facing
East
Output?
No
Data Bits
1
Three-state?
No