# Experiment 6: Study of Flip-Flops

**Objective:**

1. To become familiar with flip-flops.

2. To implement and observe the operation of different flip-flops.

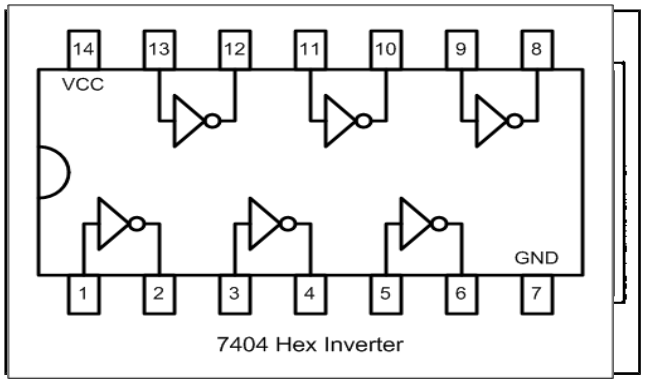
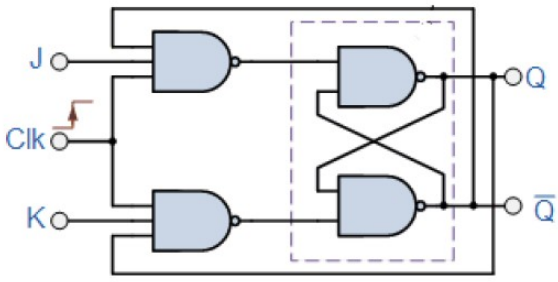



Fig.1. Pin Diagram for 74LS76

Fig.2. Pin Diagram for 7404

1. **2. JK FLIP-FLOP:**
2. The JK flip flop (JK means Jack Kilby, a Texas instrument engineer, who invented it) is the most versatile flip-flop, and the most commonly used flip flop. Like the RS flip-flop, it has two data inputs, J and K, and an EN/clock pulse input (CP). Note that in the following circuit diagram NAND gates are used instead of NOR gates. It has no undefined states, however. The fundamental difference of this device is the feedback paths to the AND gates of the input, i.e. Q is AND-ed with K and CP and Q' with J and CP.
3. 

**Circuit Diagram:**



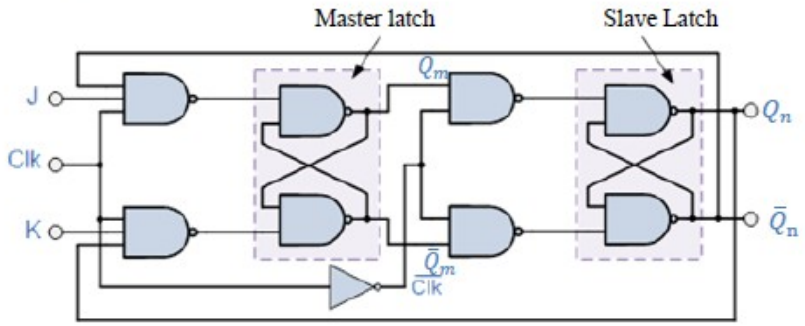

**Characteristic Table:**

| $Q_n$ | J | K | $Q_{n+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1(Toggle,$\bar{Q}_n$) |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0(Toggle,$\bar{Q}_n$) |

4. 
5. Fig.4. Circuit Diagram and Characteristic Table of JK Flip-Flop
6. 
7. The JK flip-flop has the following characteristics:
8. If one input (J or K) is at logic 0, and the other is at logic 1, then the output is set or reset (by J
9. and K respectively), just like the RS flip-flop.

10. If both inputs are 0, then it remains in the same state as it was before the clock pulse occurred;
11. again like the RS flip flop. CP has no effect on the output.
12. If both inputs are high, however the flip-flop changes state whenever a clock pulse occurs; i.e.,
13. the clock pulse toggles the flip-flop again and again until the CP goes back to 0 as shown in the shaded rows of the characteristic table above. Since this condition is undesirable, it should be eliminated by an improvised form of this flip-flop as discussed in the next section.
14.
15. **3. MASTER-SLAVE JK FLIP-FLOP:**
16. Although JK flip-flop is an improvement on the clocked SR flip-flop it still suffers from timing problems called "race" if the output Q changes state before the timing pulse of the clock input has time to go "OFF", so the timing pulse period (T) must be kept as short as possible (high frequency). As this is sometimes not possible with modern TTL IC's the much improved Master-Slave J-K Flip-Flop was developed. This eliminates all the timing problems by using two SR flip-flops connected together in series, one for the "Master" circuit, which triggers on the leading edge of the clock pulse and the other, the "Slave" circuit, which triggers on the falling edge of the clock pulse.
17.
18. The master-slave JK flip flop consists of two flip flops arranged so that when the clock pulse enables the first, or master, it disables the second, or slave. When the clock changes state again (i.e., on its falling edge) the output of the master latch is transferred to the slave latch. Again, toggling is accomplished by the connection of the output with the input AND gates.
19.

**Circuit Diagram:**




20.
21. Fig.5 Slave JK Flip-Flop

24. Characteristic Table:

| CP | J | K | $Q_m$ | $\bar{Q}_m$ | $Q_n$ | $\bar{Q}_n$ |
|---|---|---|---|---|---|---|
| 0→1 | 0 | 0 | Hold | | Hold | |
| 1→0 | 0 | 0 | Hold | | Hold | |
| 0→1 | 0 | 1 | 0 | 1 | Hold | |
| 1→0 | 0 | 1 | Hold | | 0 | 1 |
| 0→1 | 1 | 0 | 1 | 0 | Hold | |
| 1→0 | 1 | 0 | Hold | | 1 | 0 |
| 0→1 | 1 | 1 | Toggle | | Hold | |
| 1→0 | 1 | 1 | Hold | | Toggle | |

**27.**

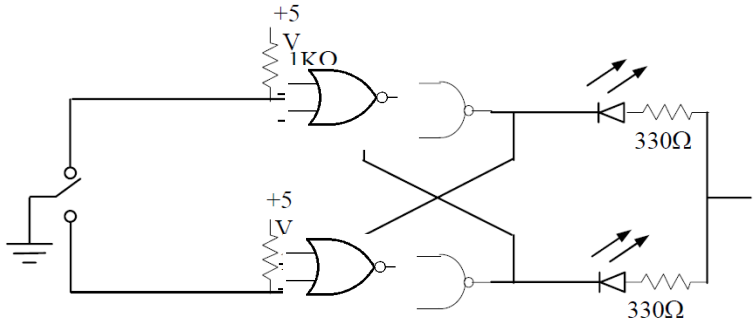
**28.**

**29.**

**30. Laboratory Work:**

**31. a)** In the Lab, Build the RS latch shown in Fig.6. Use switches as a bouncing switch. Q and Q' Outputs are connected to LED's. Verify the truth table experimentally.

**32.**

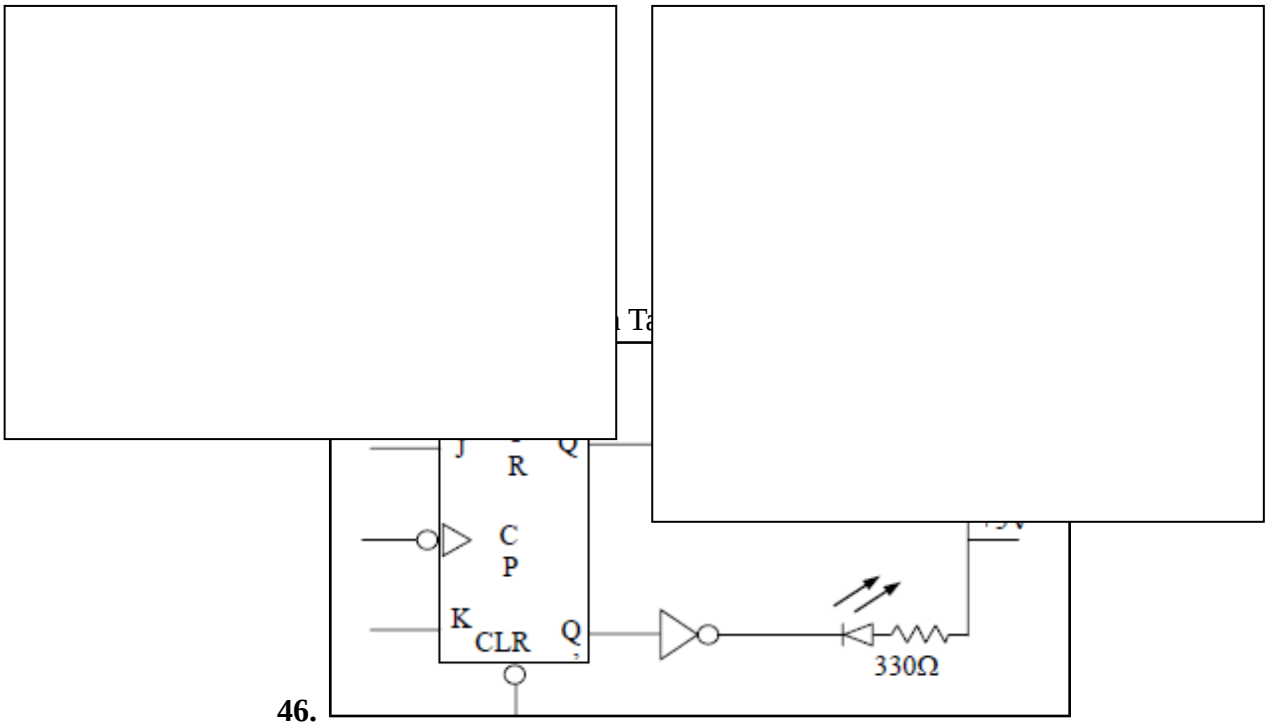



**33.**

**34.** Fig.6. RS Latch Circuit.

**35. b)** In the Lab, Construct the circuit of Fig 8. Look at the data sheet for the 74LS76 and determine the inactive logic required at the PRE and CLR inputs.

**36.**




**46.**

**47.**

**48.** Fig.8. JK Flip-Flop Circuit

**49. Pre-Lab.:**

- Explain the difference between latch and flip-flop.
- What is the difference between 7476 and 74LS76 IC's?

**50. Overview:**

So far you have encountered with *combinatorial logic*, i.e. circuits for which the output depends only on the inputs. In many instances it is desirable to have the next output depending on the current output. A simple example is a *counter*, where the next number to be output is determined by the current number stored. Circuits that remember their current output or state are often called *sequential logic* circuits. Clearly, sequential logic requires the ability to store the current state. In other words, *memory* is required by sequential logic circuits, which can be created with boolean gates. If you arrange the gates correctly, they will remember an input value. This simple concept is the basis of RAM (random access memory) in computers, and also makes it possible to create a wide variety of other useful circuits.

Memory relies on a concept called **feedback**. That is, the output of a gate is fed back into the input. The simplest possible feedback circuit using two inverters is shown below (Fig.2):

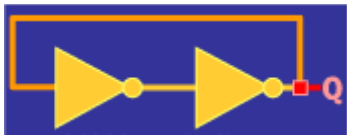


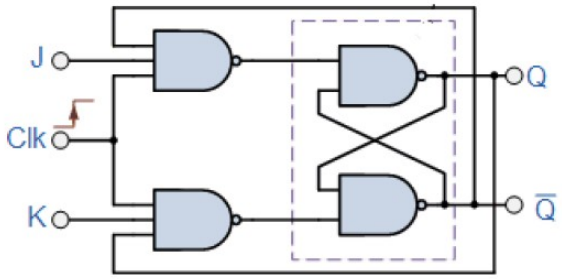

Fig.2: Simplest realization of feedback circuit

If you follow the feedback path, you can see that if Q happens to be 1 (or 0), it will always be 1 (or 0). Since it's nice to be able to control the circuits we create, this one doesn't have much use -- but it does let you see how feedback works. It turns out that in "real" sequential circuits, you can actually use this sort of simple inverter feedback approach. The memory elements in these circuits are called *flip-flops*.

**2. JK FLIP-FLOP:**

The JK flip flop (JK means Jack Kilby, a Texas instrument engineer, who invented it) is the most versatile flip-flop, and the most commonly used flip flop. Like the RS flip-flop, it has two data inputs, J and K, and an EN/clock pulse input (CP). Note that in the following circuit diagram NAND gates are used instead of NOR gates. It has no undefined states, however. The fundamental difference of this device is the feedback paths to the AND gates of the input, i.e. Q is AND-ed with K and CP and Q' with J and CP.

**Circuit Diagram:**




**Characteristic Table:**

| $Q_n$ | J | K | $Q_{n+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1(Toggle,$\bar{Q}_n$) |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0(Toggle,$\bar{Q}_n$) |

Fig.4. Circuit Diagram and Characteristic Table of JK Flip-Flop

The JK flip-flop has the following characteristics:

- If one input (J or K) is at logic 0, and the other is at logic 1, then the output is set or reset (by J

and K respectively), just like the RS flip-flop.

- If both inputs are 0, then it remains in the same state as it was before the clock pulse occurred;

again like the RS flip flop. CP has no effect on the output.

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the clock pulse toggles the flip-flop again and again until the CP goes back to 0 as shown in the shaded rows of the characteristic table above. Since this condition is undesirable, it should be eliminated by an improvised form of this flip-flop as discussed in the next section.

## 3. MASTER-SLAVE JK FLIP-FLOP:

Although JK flip-flop is an improvement on the clocked SR flip-flop it still suffers from timing problems called "race" if the output Q changes state before the timing pulse of the clock input has time to go "OFF", so the timing pulse period (T) must be kept as short as possible (high frequency). As this is sometimes not possible with modern TTL IC's the much improved Master-Slave J-K Flip-Flop was developed. This eliminates all the timing problems by using two SR flip-flops connected together in series, one for the "Master" circuit, which triggers on the leading edge of the clock pulse and the other, the "Slave" circuit, which triggers on the falling edge of the clock pulse.

The master-slave JK flip flop consists of two flip flops arranged so that when the clock pulse enables the first, or master, it disables the second, or slave. When the clock changes state again (i.e., on its falling edge) the output of the master latch is transferred to the slave latch. Again, toggling is accomplished by the connection of the output with the input AND gates.

**Circuit Diagram:**

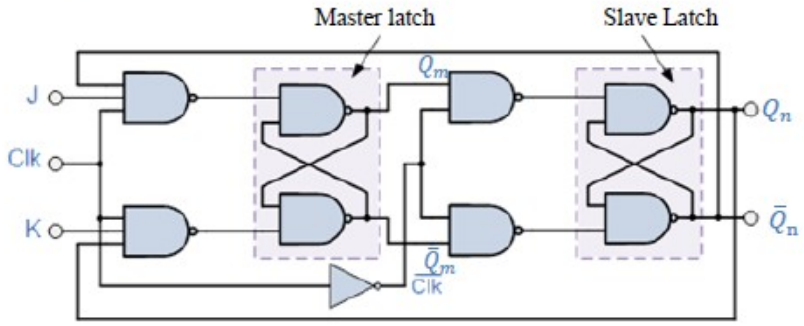


Fig.5. Circuit Diagram of Master-Slave JK Flip-Flop

Characteristic Table:

| CP | J | K | $Q_m$ | $\bar{Q}_m$ | $Q_n$ | $\bar{Q}_n$ |
|---|---|---|---|---|---|---|
| 0→1 | 0 | 0 | Hold | | Hold | |
| 1→0 | 0 | 0 | Hold | | Hold | |
| 0→1 | 0 | 1 | 0 | 1 | Hold | |
| 1→0 | 0 | 1 | Hold | | 0 | 1 |
| 0→1 | 1 | 0 | 1 | 0 | Hold | |
| 1→0 | 1 | 0 | Hold | | 1 | 0 |
| 0→1 | 1 | 1 | Toggle | | Hold | |
| 1→0 | 1 | 1 | Hold | | Toggle | |

**51. Laboratory Work:**

**a)** In the Lab, Build the RS latc tches as a bouncing switch. Q and Q' Outputs are connected to LED's. mentally.

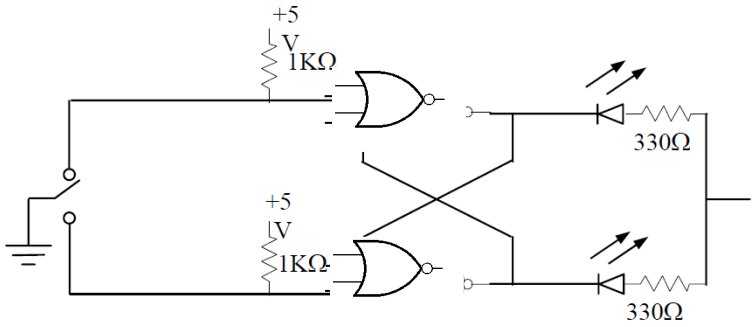


Fig.6. RS Latch Circuit.

**b)** In the Lab, Construct the circuit of Fig 8. Look at the data sheet for the 74LS76 and determine the inactive logic required at the PRE and CLR inputs.

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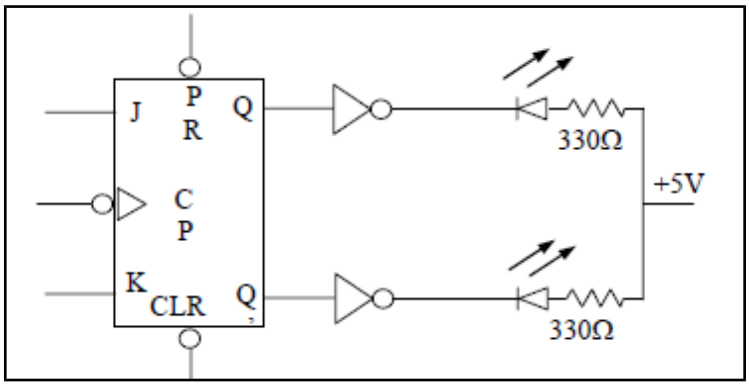


Fig.8. JK Flip-Flop Circuit