

DB18
Johnson Counter

Operating Manual
Ver.1.1

An ISO 9001 : 2000 company



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A handwritten signature in black ink, appearing to read 'Kamlesh'.

Bangalore, 2007-11-21

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**Johnson Counter
DB18**

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RoHS Compliance



Sciencetech Products are RoHS Complied.

RoHS Directive concerns with the restrictive use of Hazardous substances (Pb, Cd, Cr, Hg, Br compounds) in electric and electronic equipments.

Sciencetech products are “Lead Free” and “Environment Friendly”.

It is mandatory that service engineers use lead free solder wire and use the soldering irons upto (25 W) that reach a temperature of 450°C at the tip as the melting temperature of the unleaded solder is higher than the leaded solder.

Introduction

DB18 is a compact, ready to use **Johnson Counter** experiment board. This experiment board has been designed to study the operation of 4 Bit Johnson Counter which can be shown with the help of LED's at the output. It can be used as stand alone unit with external power supply and pulse generator or can be used with **Sciencetech Digital Lab, ST2611** which has built in power supply, pulse generator, pulser switches, 8 bits data switches, logic probe, digital display, 8 bits LED display.

List of boards :

Model	Name
DB01	Logic Gates
DB02	Universal Gate- NAND/NOR
DB03	EX-OR Gate Implementation
DB04	Demorgan's Theorem
DB05	EX-OR Gate Application
DB06	Code Conversion (Binary to Gray & Gray to Binary)
DB07	Code Conversion (BCD to Excess-3 code)
DB08	Binary Adder -Subtractor
DB09	Encoder – Decoder
DB10	Multiplexer – Demultiplexer
DB11	Flip-Flops (R-S, D, J-K, T)
DB12	Shift Register (4 bit SIPO)
DB13	4 Bit Synchronous Binary Counter
DB16	Digital to Analog Converter (R-2R ladder)
DB15	BCD to 7- Segment Decoder
DB17	3 Digit Event Counter
DB21	Fiber Optic Digital Link
DB22	Analog to digital converter (Counter Type)
DB27	Digital to Analog Converter (R-2R ladder)
DB28	Monostable Multivibrator
DB29	CMOS and Crystal Oscillator
DB31	Decoder/Demultiplexer
DB32	Modulo-N programmable counter
DB35	4 BIT Shift Register

.....and many more

Theory

Almost any complex digital system contains several *counters*. A counter's job is the obvious one of counting events or periods of time or putting events into sequence. Counters also do some not so obvious jobs such as dividing frequency, addressing, and serving as memory units.

A counter is probably one of the most useful and versatile subsystems in a digital system. A counter driven by a clock can be used to count the number of clock cycles. Since the clock pulses occur at known intervals, the counter can be used as an instrument for measuring time and therefore period or frequency.

There are basically two different types of counters :

1. Synchronous,
2. Asynchronous.

The Asynchronous : or Ripple counter is simple and straightforward in operation and construction and usually requires a minimum of hardware. Each flip-flop is triggered by the previous flip-flop, and thus the counter has a cumulative settling time. In other words, the clock pulse (CP) inputs of all flip-flops (except the first) are triggered not by the incoming pulses but rather by the transition that occurs in other flip-flops. Counter such as these are also known as Serial Counters.

The asynchronous counter is the simplest to build, but there is a limit to its highest operating frequency. As each flip-flop has delay time and in a asynchronous counter these delay times are additive, and the total 'settling' time for the counter is approximately the delay time times the total number of flip-flops. Further more there is a possibility of glitches occurring at the output of decoding gates used with these counters. Both of these problems can be overcome by the use of a synchronous or parallel counter.

An increase in speed of operation can be achieved by use of a Parallel or Synchronous counter. Here every flip-flop is triggered by the clock (in synchronism), and thus settling time is simply equal to the delay time of a single flip-flop. The increase in speed is usually obtained at the price of increased hardware. Serial and parallel counters can be used in combination to compromise between speed of operation and hardware count.

A Synchronous counter : in contrast to an *asynchronous counter*, is one whose output bits change state simultaneously, with no ripple. What is the use of synchronous counter when asynchronous counter are simplest to build? Why are we increasing the complexity of our counter? A ripple counter may be simplest to build, but there is a limit to its highest operating frequency. As we know that each flip flop has a delay time; in ripple counter these delay time are additive i.e. all the delay time added together. and this make total 'settling time' for the counter equal to delay time multiply with number of flip flop in counter. Furthermore there is the possibility of glitches occurring at the output of decoding gates used with ripple counter. Both of these problems can be overcome by the use of a Synchronous counter or Parallel

counter. The main difference between an asynchronous and synchronous counter is that, that in synchronous counter every flip flop is triggered in synchronism with clock i.e. same clock is feed into all the flip flop. The only way we can build such a counter circuit from J-K flip-flops is to connect all the clock inputs together, so that each and every flip-flop receives the exact same clock pulse at the exact same time:

A Johnson counter :

Johnson counter is one of the simplest examples of a *synchronous counter* i.e. a counter in which all the outputs change simultaneously. A Johnson counter is generally used to produce moving light displays. It differs from a ripple counter in that

- it is based on a clocked D latch
- all the clock inputs are fed from the same clock
- the NOT Q output of the final latch is used as the input to the first

An example of a Johnson counter is shown below.

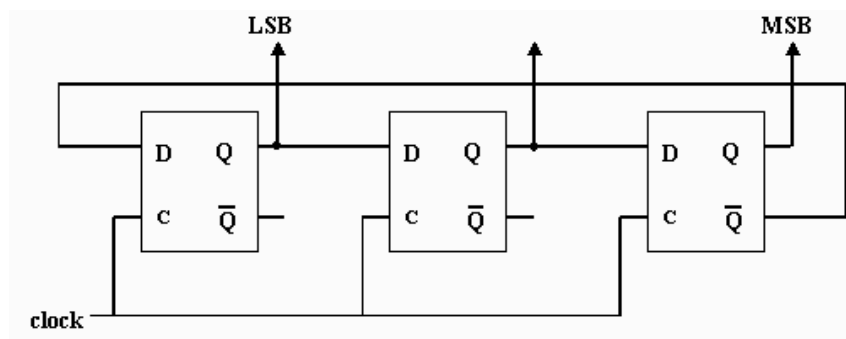


Figure 1

If the output of the last flip flop shift register was connected back to the control input of the first flip flop in the register. This arrangement resulted in a ring counter and the technique is called *direct feedback*. But if the output of the last flip flop and first crossed over and then connected back to the control inputs of the first flip flop i.e. D is fed in to A and D is fed in to A. The technique is called the inverse feedback. The connection results in a counter that has some very unique characteristics and its called **Johnson or Shift counter :**

If all the inputs start at 0 then all the outputs Q will be 0, but the NOT Q from the third D latch will be 1. Thus the input to the first latch will now be 1 and on the first negative clock pulse the output of the first D latch will change to 1. This now makes the input to the second latch 1, and its output will now change to 1 on the second clock pulse, making the input to the third latch 1. The third latch will therefore have an output of 1 on the third clock pulse at which time the NOT Q output (and the input to the first latch) will become 0. At this point the 0's propagate through the sequence on successive clock pulses. The timing diagram looks as shown below.

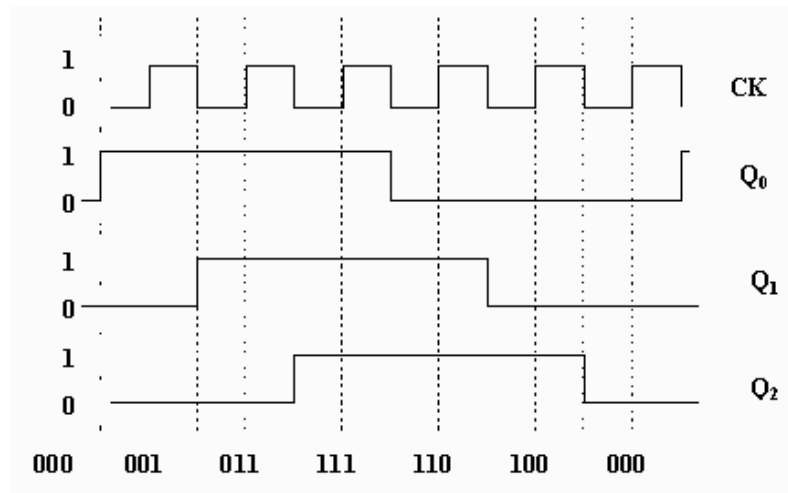


Figure 2

The 4 Bit Master slave flip flops are connected in a standard shift register as shown in Figure 3. In addition, the outputs of the last flip flop are crossed over and then connected back to the inputs of the first flip flop. Specifically, D is connected to 'K' input of \bar{A} , and \bar{D} is connected to 'J' input of A.

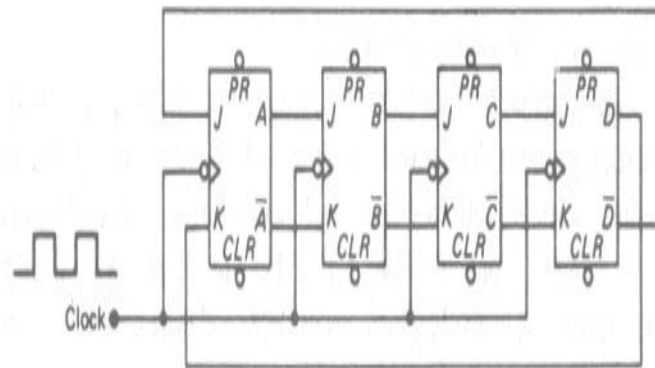


Figure 3

Now assume that all flip flops are in reset condition and the clock is allowed to run since \bar{D} is high and D is low. Thus at first 1 is set to flip flop A during the first cycle of the clock. At the same time; B, C and D remains low since their J inputs are low and K inputs are high. During the second cycle of the clock, remains high since \bar{D} is still high due to D remains low. AT the same time, B is set high since A is now high, C and D remains unchanged i.e. low during this period.

During the third clock period A and B remains high whilst setting C also high; But D remains low.

At Forth clock period A, B and C remains high and it set D also high. So at forth clock cycle the all four flip flop have been changed from the low states to high states.

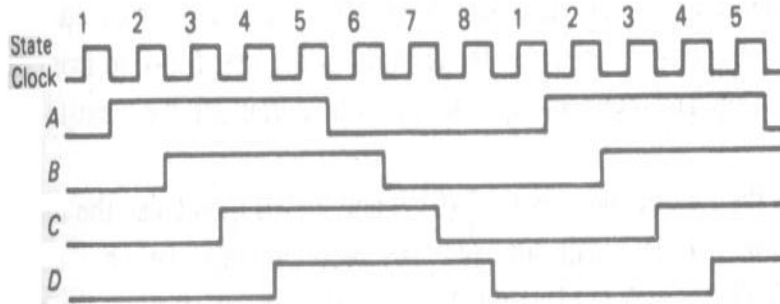


Figure 4

During the fifth clock period, D is low and D is high; therefore, A is reset to low state and B, C and D remains high.

At sixth clock period A remains low and reset B to low while C and D are still high.

At Seventh cycle clock C also reset due to B is low now just D is high and D is low.

At the eight cycle of clock A, B, C and D all become low while setting D as high.

For the Ninth clock period the process will be same as it was for first clock cycle.

Thus this shift register inverse feed back has progress through a complete cycle of counts in eight clock period. Figure 4 shows the progress of a Johnson Counter with a negative clock triggering.

A truth table can be use to verify the output of Johnson counter.

Table 1

D	C	B	A	State	Binary equivalent
0	0	0	0	1	0
0	0	0	1	2	1
0	0	1	1	3	3
0	1	1	1	4	7
1	1	1	1	5	15
1	1	1	0	6	14
1	1	0	0	7	12
1	0	0	0	8	8
0	0	0	0	1	0

Experiment

Objective :

To study counting process of 4-Bit Johnson Counter

Apparatus required :

1. Digital board, **DB37**.
2. DC Power Supply of +5V.
3. Pulse generator.

Logic diagram :

(Logic 1 = +5V & Logic 0= GND)

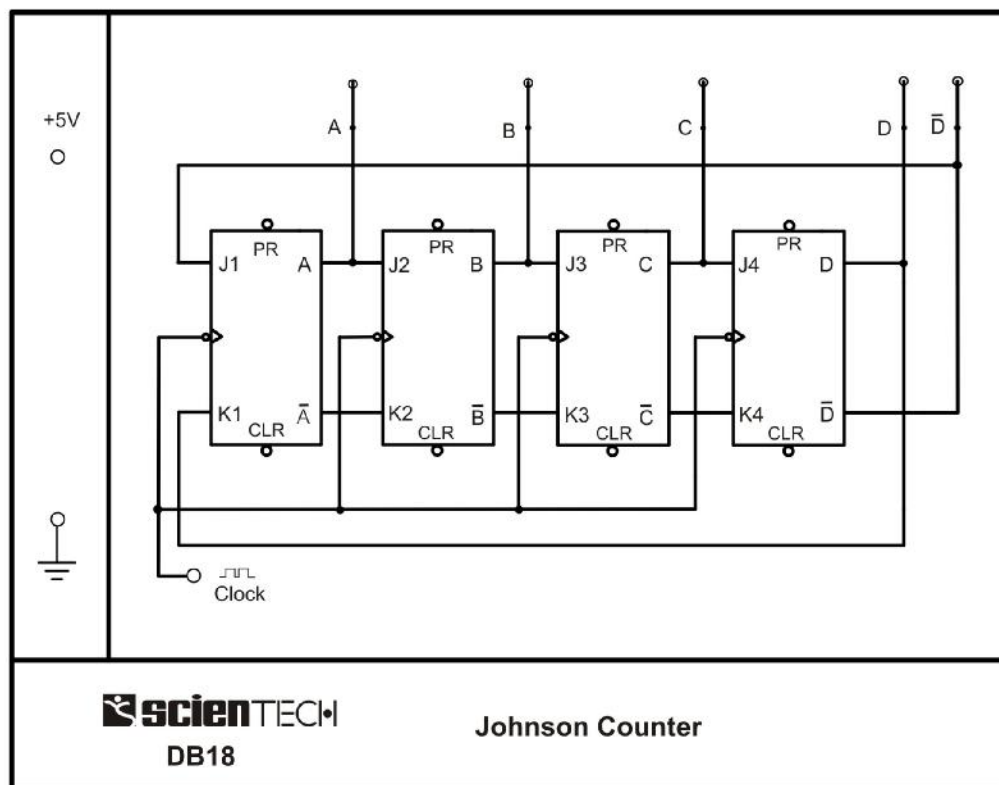


Figure 5

DB18

Procedure :

- To Study the counting procedure of Johnson counter precede as follow :
- 1. Connect +5V and ground to their indicated position on **DB18** experiment board from DC power supply.
- 2. Connect TTL clock pulse of 1Hz ($T=1\text{sec}$) from the pulse generator to the socket 'CLK'.
- 3. Switch ON the power supply and pulse generator.
- 4. Observe output on LED and match it with the truth table Table1 given in the theory.
- 5. Vary the frequency to observe the difference in the LED output. As the frequency increase the time difference will decrease.
- 6. Repeat above steps 4-8 to repeat the process.

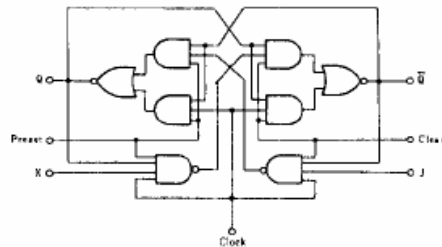
Observation Table :

S. No.	A	B	C	D	<u>D</u>
1	0	0	0	0	1
2					
3					
4					
5					
6					
7					
8					
9					

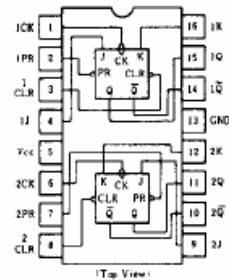
Datasheet

HD74LS76A • Dual J-K Flip-Flops (with Preset and Clear)

BLOCK DIAGRAM(1/2)



PIN ARRANGEMENT

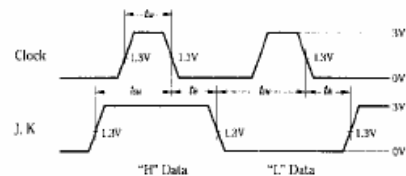


RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	Clock High	20	—	—	ns
	Clear Preset Low	25	—	—	ns
Setup time	"H" Data	20↓	—	—	ns
	"L" Data	20↓	—	—	ns
Hold time	t_h	0↓	—	—	ns

Note) ↓: The arrow indicates the falling edge.

TIMING DEFINITION



ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item		Symbol	Test Conditions	min	typ*	max	Unit
Input voltage		V_{IH}		2.0	—	—	V
		V_{IL}		—	—	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-400\mu\text{A}$	2.7	—	—	V
		V_{OL}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$ <div>$I_{OL}=8\text{mA}$ $I_{OL}=4\text{mA}$</div>	—	—	0.5 0.4	V
Input current	J, K	I_{IH}	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	—	—	20	μA
	Clear			—	—	60	
	Preset			—	—	60	
	Clock			—	—	80	
	J, K	I_{IL}^{**}	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	—	—	-0.4	mA
	Clear			—	—	-0.8	
	Preset			—	—	-0.8	
	Clock			—	—	-0.8	
	J, K	I_I	$V_{CC}=5.25\text{V}, V_I=7\text{V}$	—	—	0.1	mA
	Clear			—	—	0.3	
	Preset			—	—	0.3	
	Clock			—	—	0.4	
Short-circuit output current		I_{OS}	$V_{CC}=5.25\text{V}$	-20	—	-100	mA
Supply current ***		I_{CC}	$V_{CC}=5.25\text{V}$	—	4	6	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75\text{V}, I_{IH}=-18\text{mA}$	—	—	-1.5	V

* $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$

** I_{IL} should not be measured when preset and clear inputs are low at same time.

*** With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

HD74LS76A

FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	\downarrow	L	L	Q_0	\bar{Q}_0
H	H	\downarrow	H	L	H	L
H	H	\downarrow	L	H	L	H
H	H	\downarrow	H	H	Toggle	
H	H	H	X	X	Q_0	\bar{Q}_0

Notes) H; high level, L; low level, X; irrelevant

\downarrow ; transition from high to low level

Q_0 ; level of Q before the indicated steady-state input conditions were established.

\bar{Q}_0 ; complement of Q_0 or level of \bar{Q} before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by \downarrow .

*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

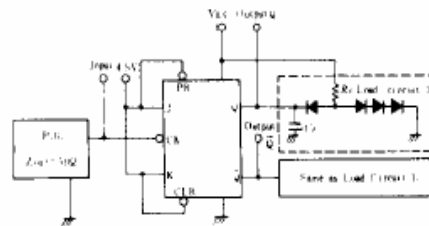
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}				30	45	—	MHz
Propagation delay time	t_{PLH}	Clear	Q, \bar{Q}	$C_L=15pF$, $R_L=2k\Omega$	—	15	20	ns
	t_{PHL}	Preset			—	15	20	ns

TESTING METHOD

1) Test Circuit

1.1) f_{max} , t_{PLH} , t_{PHL} (Clock \rightarrow Q, \bar{Q})

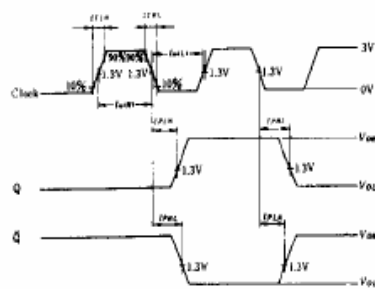


Notes) 1. Test is put into the each flip-flop

2. All diodes are 1S2074 Φ .

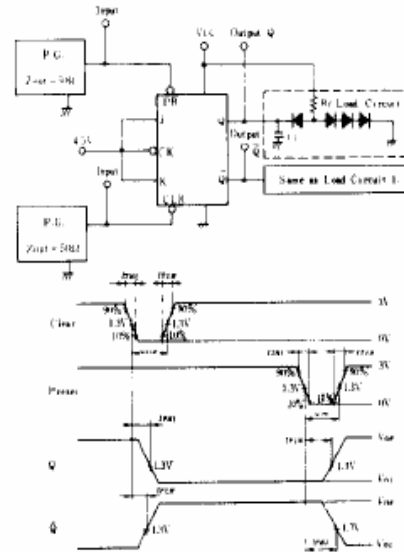
3. C_L includes probe and jig capacitance.

Waveform



Note) Clock input pulse; $t_{PLH} \leq 15ns$, $t_{PHL} \leq 6ns$, $PRR=1MHz$, duty cycle=50% and: for f_{max} , $t_{PLH} = t_{PHL} \leq 2.5ns$.

1.2) t_{PHL} , t_{PLH} (Clear, Preset \rightarrow Q, \bar{Q})



Note) Clear and preset input pulse; $t_{PLH} \leq 15ns$, $t_{PHL} \leq 6ns$, $PRR=1MHz$

Warranty

1. We guarantee the product against all manufacturing defects for 24 months from the date of sale by us or through our dealers. Consumables like dry cell etc. are not covered under warranty.
2. The guarantee will become void, if
 - a) The product is not operated as per the instruction given in the operating manual.
 - b) The agreed payment terms and other conditions of sale are not followed.
 - c) The customer resells the instrument to another party.
 - d) Any attempt is made to service and modify the instrument.
3. The non-working of the product is to be communicated to us immediately giving full details of the complaints and defects noticed specifically mentioning the type, serial number of the product and date of purchase etc.
4. The repair work will be carried out, provided the product is dispatched securely packed and insured. The transportation charges shall be borne by the customer.

For any Technical Problem Please Contact us at service@scientech.bz

List of Accessories

1. 2mm patch cord (Red) 16"..... 1 No.
2. 2mm patch cord (Black) 16"..... 1 No.
3. 2mm patch cord (Blue) 16". 1 No.
4. e-manual 1 No.

Updated 18-05-2009