Traffic Light Controller

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Abstract – As name suggests the project aims at controlling a traffic signal. The main purpose is to control the traffic of a lane and change the signals according to it.

Index Terms – Introduction, Working Principle, Circuit Diagram, VHDL Code, Simulation Results, RTL Schematic , Technology Schematic, Hardware Implementation, Results, Conclusion.

The following are the specifications needed for the Xilinx Simulation:

Family : Spartan 3

Device : XC3S400

Simulator: ISE simulator(VHDL)

I. INTRODUCTION

Traffic Light controller project consist of 2 inputs namely clock and sensor and 3 outputs, the Green , Yellow and Red light. This project is implemented using Xilinx Simulator and also Xilinx FPGA kit.

Property Name	Value
Product Category	All
Family	Spartan3
Device	XC3S400
Package	PQ208
Speed	-5
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISE Simulator (VHDL/Verilog)
Preferred Language	VHDL
Enable Enhanced Design Summary	☑
Enable Message Filtering	☑
Display Incremental Messages	☑

Fig a Xilinx Specifications

II. Circuit Explanation

The circuit shown in fig. is explained as follows showing the operation of each component:

The working of this is quite simple.

As seen above what we have is only 2 input's present:

1. Clock
2. Sensor

The working of this system is explained as below:

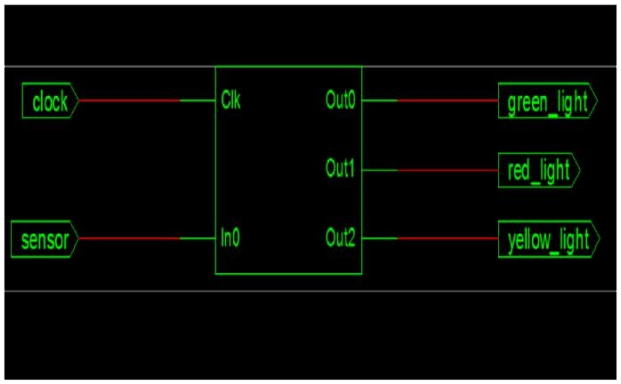
1. We give a continuous clock input to the system.
2. Then after a fixed amount of delay the led's at the output i.e. at the traffic lamp start glowing once we sense the traffic by the sensor input.
3. This delay can be adjusted by the designer by setting the clock frequency.
4. Now, the special case in the system is the Sensor input.
5. Whenever the sensor input is high the system operates under normal conditions.
6. But, when the SENSOR pin input's a low signal this indicates that the lane as to be stop immediately.
7. Thus when Sensor = 0 the Red LED glows at the traffic lamp
8. This is how the system operates.

III. VHDL CODE

The code that was written of the above circuit implementation is as follows:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL; use
IEEE.STD_LOGIC_ARITH.ALL; use
IEEE.STD_LOGIC_UNSIGNED.ALL;
entity traffic_light is port(sensor,clock:in
std_logic;
red_light,green_light,yellow_light:out
std_logic);
end traffic_light;
architecture fsm of traffic_light
is type t_state is
(red,green,yellow); signal
ps,ns:t_state; begin
process(ps,sensor)
begin
case ps is
when green=>
ns<=yellow;
red_light='0';
green_light='1';
yellow_light='0';
when red=>
red_light='1';
green_light='0';
yellow_light='0';
if(sensor='1') then
ns<=green;
else
ns=>red;
end if;
when yellow=>
red_light='0';
green_light='0';
yellow_light='1';
ns<=red;
end case;
end process;
process
begin
wait untilclock'event and clock='1';
ps<=ns;
end process;
end fsm;
```

IV. RTL Schematic of Given Design



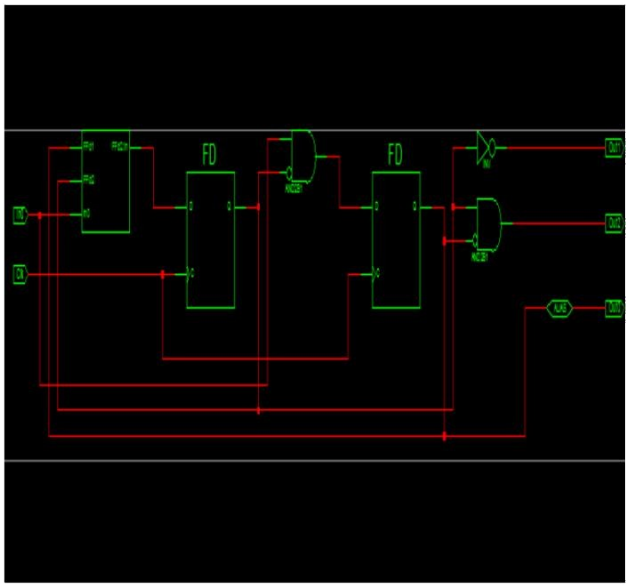


Fig b. RTL schematics

V. Technology Schematics

The figure shown below is an Technology Schematic :

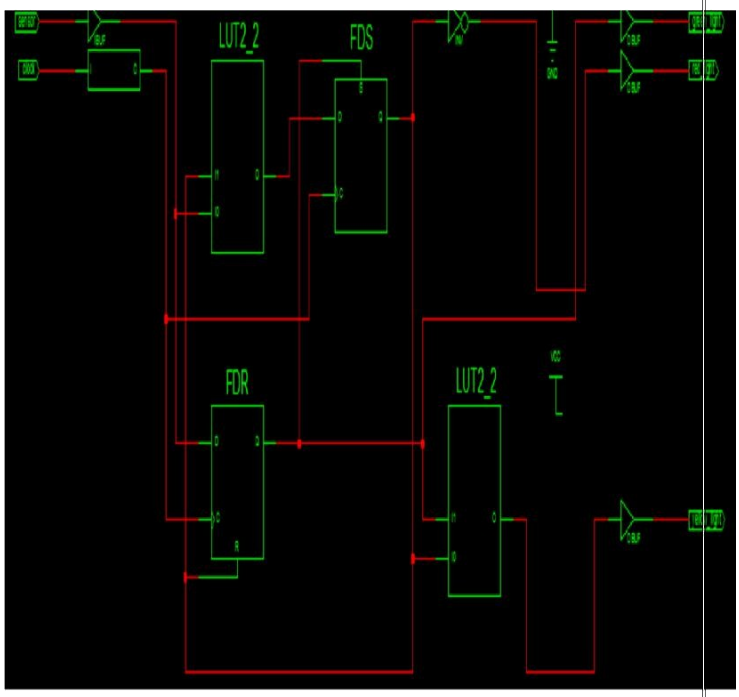
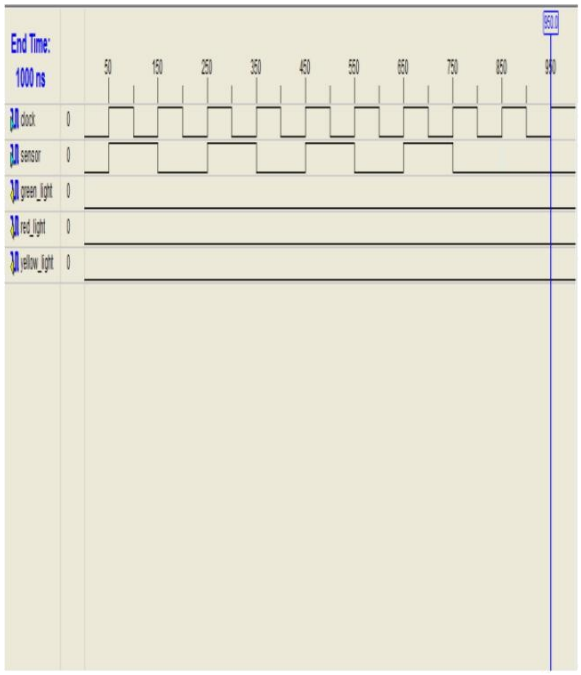
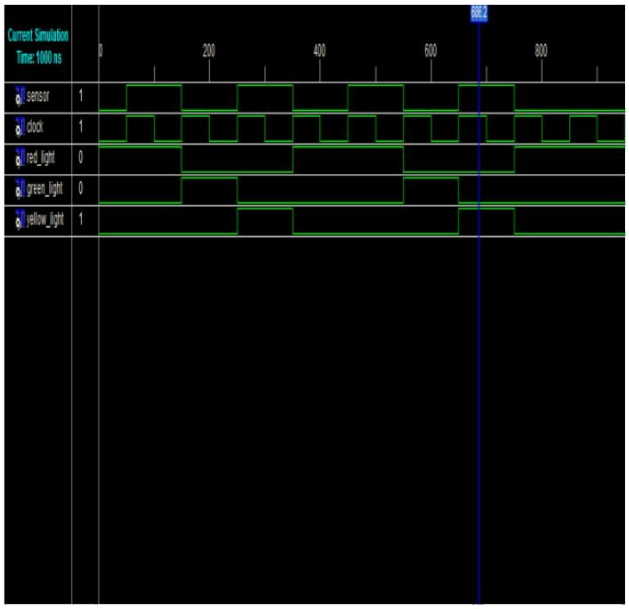


Fig c. Technology Schematic

VI. Results

The results of the simulation were seen to be as follows:





VII. Hardware Implementation

The circuit was implemented on a FPGA kit having several extra peripherals.

What we connected is a clock generated by the FPGA to the input pin assigned and a sensor that can be connected to +Vcc or ground.

By changing the conditions of traffic i.e. the sensor input we observe different Traffic signal status.

The following were the steps followed while implementing the code on hardware:

1. The FPGA kit was connected to the PC via Parallel port slot.
2. Supply was given to the FPGA kit.
3. The program code was copied into the Xilinx folder.
4. Then the project was opened in the Xilinx simulator.
5. Process Synthesize XST was carried out
6. Then In User Constraints Process the pin name and numbers of input and output are defined i.e. UCF file is created.
7. Then Process Implement Design was Carried Out.
8. Program file was generated.
9. Then the Process was Run on the FPGA kit.
10. At last, input conditions are changed and respective output pins were observed.

VIII. Pin Configuration

The following were the pins used and the pin numbers were assigned as follows:

Fig c **Table Of Pin configuration**

Pin Name	Pin Number	Pin Function
clock	2	Input
sensor	3	Input
green_light	4	Output
yellow_light	5	Output
red_light	7	Output

IX. CONCLUSION

Thus the Above circuit of Traffic Light Controller was successfully implemented and simulated too on the Xilinx Software as well as successfully hardware tested on Xilinx FPGA kit.

X. REFERENCES

The following were some of the references used in getting the desired project successfully implemented

1. FPGA Prototyping by VHDL Examples: *Xilinx* Spartan-3 Version By Pong Chu
2. Digital System and Design By R.P Jai