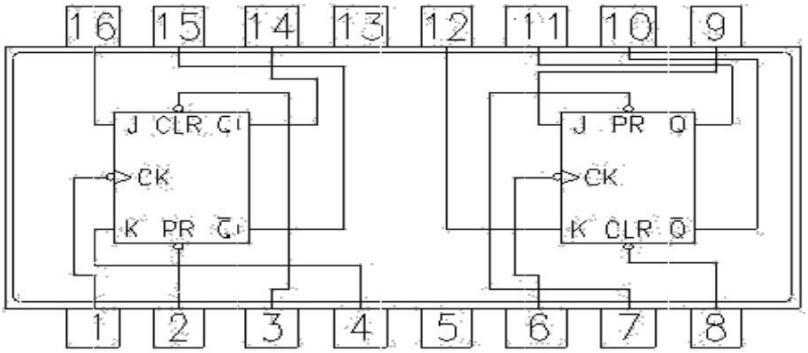
Aim: – Design , and Ver ify the 4- Bit Synch ronous Co unter

APPARATUS R EQUIRED : Digital tr ainer kit and 4 JK flip flop each IC 7 476 (i.e dua l JK flip flop) and two AND gates IC 740 8.

BRI EF THEOR Y: Counter is a circui t which cyc le through state sequenc e. Two types of counter, Sync hronous counter (e.g. parallel) and Asynchrono us counter (e .g. ripple). In Ripple counter s ame flip-flo p output to be used as clock signal source for other flip-flop. Synchronous cou nter use the same clock signal for all flip-flop.

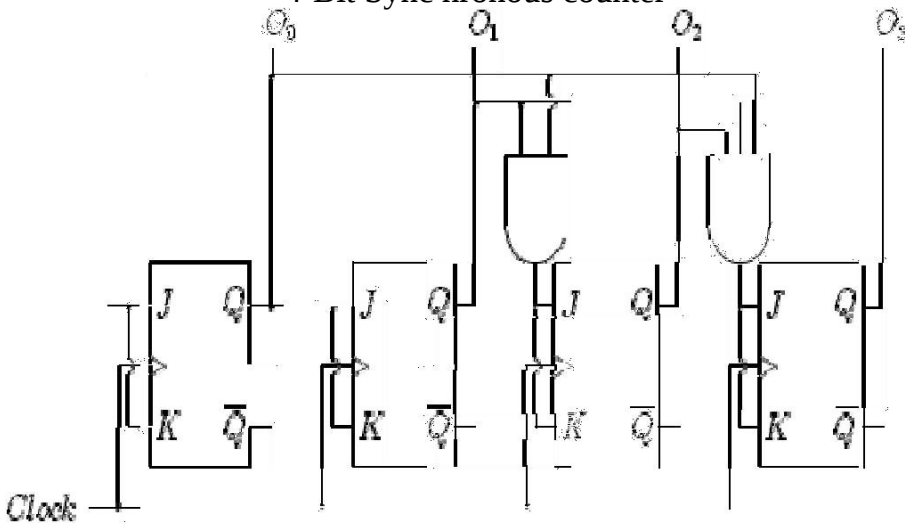
PIN CONFIGURATION:

Dual JK Master Slave F lip Flop w ith clear & preset



LOG IC DIAGR AM:

4-Bit Sync hronous counter



Pin Number	Description
1	Clock 1 Input
2	Preset 1 Input
3	Clear 1 Input
4	J1 Input
5	Vcc
6	Clock 2 Input
7	Preset 2 Input
8	Clear 2 Input
9	J2 Input
10	Complement Q2 Output
11	Q2 Output
12	K2 Input
13	Ground
14	Complement Q1 Output
15	Q1 Output
16	K1 Input

OBSERVATION TABLE:

Truth Table

States				**Count**
0_4	0_3	0_2	0_1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6

0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

PROCEDURE:

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

RESULT: 4-bit synchronous counter studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 What do you understand by counter?
Ans. Counter is a register which counts the sequence in binary form. Q.2What is asynchronous counter?
Ans. Clock input is applied to LSB FF. The output of first FF is connected as clock to next FF.
Q.3What is synchronous counter?
Ans. Where Clock input is common to all FF.
Q.4Which flip flop is used in asynchronous counter? Ans. All Flip-Flops are toggling FF.
Q.5Which flip flop is used in synchronous counter? Ans. Any FF can be used.
Q.6 What do you understand by modulus?
Ans. The total no. of states in counter is called as modulus. If counter is modulus-n, then it has n different states.
Q.7 What do you understand by state diagram?

Ans. State diagram of counter is a pictorial representation of counter states directed by arrows in graph.

Q.8 What do you understand by up/down counter?

Ans. Up/Down Synchronous Counter: two way counter which able to count up or down.

Q.9 Why Asynchronous counter is known as ripple counter?

Ans. Asynchronous Counter: flip-flop doesn't change condition simultaneously because it doesn't use single clock signal Also known as ripple counter because clock signal input as ripple through counter.

Q.10 which type of counter is used in traffic signal? Ans. Down counters.