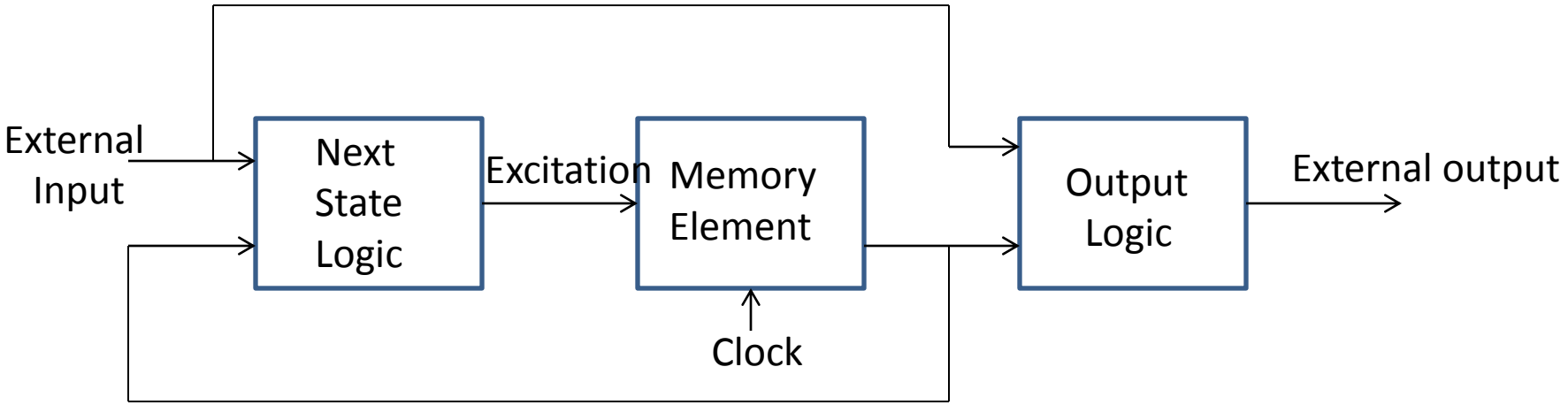
Sequential Logic Design

Flip Flops

By Prof. Sujata Wakchaure

Introduction

- The major aspect of digital system is analysis and design of sequential circuits



Introduction (Contd..)

- Memory Element is some medium in which one bit of information (0 or 1) can be stored
- Present content of memory elements referred to as **Present State** of memory element
- The new content of the memory element referred to as the **Next State**

Flip Flops

- Flip flop is a basic digital circuit
- It has 2 stable states
  - 1 State
  - 0 State
- It is obtained by using NAND & NOR gate

- What is the difference between flip flop and latch?

Flip Flops (Contd..)

- **Fundamental circuit for flip flop**

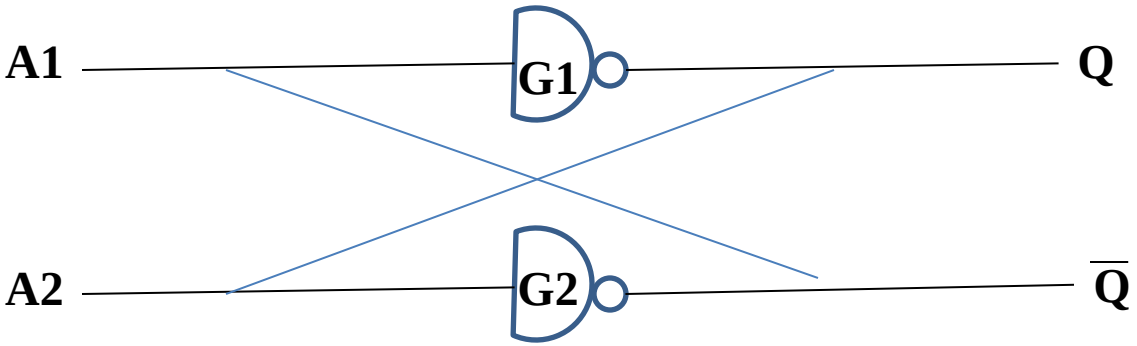


Fig 1: Cross Coupled Inverters as a Memory Element

- If o/p of G1 to be **Q=1** (but Q is I/p to G2) therefore the o/p of G2 will be $\overline{Q}$**=0**

- Similarly if Q=0 then $\overline{Q}$=1

Flip Flops (Contd..)

- From above discussion, we note the following points:

1. The outputs Q & $\overline{Q}$ are always complementary

2. The ckt has 2 stable states, in one of the stable state Q=1 which is referred to as the 1 state (or set state)
   - Whereas in other stable state Q=0 which is referred to as 0 state (or reset state)

3. If the ckt is in 1 state, it continues to remain in this state & similarly if it is in 0 state, it continues to remain in this state

- This property of ckt is referred to as Memory i.e. it can store 1-bit of digital information
- Since this information is locked or latched in this ckt, therefore, this ckt is known as a latch

Flip Flops (Contd..)

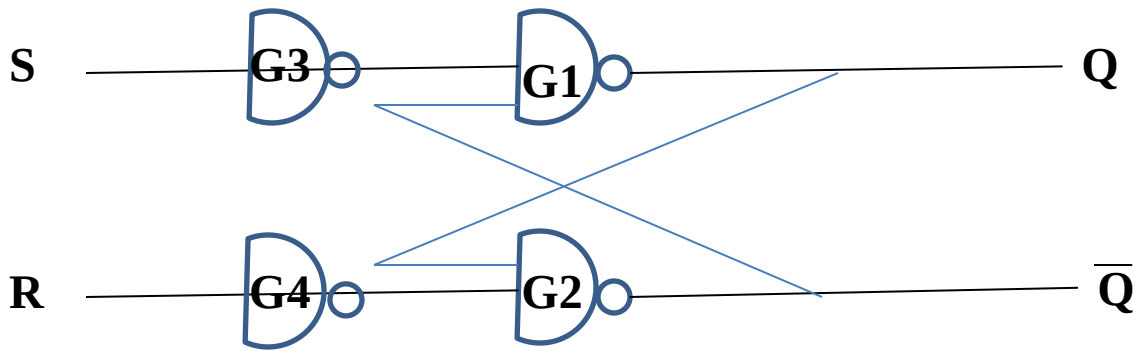


Fig 2: The memory cell with provision for entering data

- Here if we replace inverters G1 & G2 with 2 i/p NAND gates, the other terminals of NAND gates can be used to enter the desired digital information

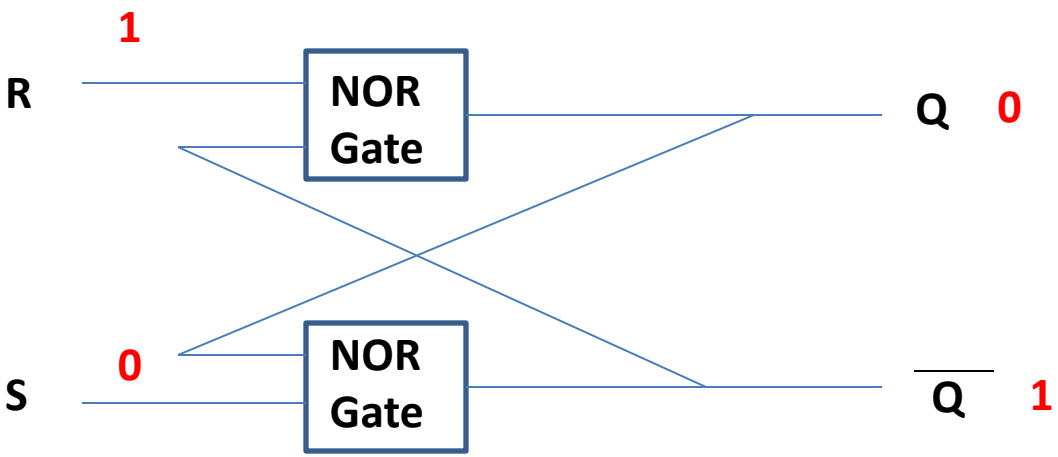
Flip Flops (Contd..)

- If S=0 & R=0, the ckt is exactly same as that of fig1
- If S=1 & R=0, the o/p of G3 will be 0 & the o/p of G4 will be 1
- Since one of the I/P of G1 is 0, its o/p will certainly be 1
- Consequently both the i/p of G2 will be 1 giving an o/p $\overline{Q}$=0
- Hence for this i/p condition, Q=1 & $\overline{Q}$=0
- Similarly if S=0 & R=1, then o/p will be Q=0 & $\overline{Q}$=1
- The 1st of these 2 I/P conditions (S=1,R=0) makes Q=1 i.e. Set State
- Whereas the 2nd I/P condition (S=0, R=1) makes Q=0 i.e. Reset or Clear State

S-R Latch

NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



Case 1:

If S=0 , R=1 => Q=0 , $\overline{Q}$=1

If S=0 , R=0 => Q=0 , $\overline{Q}$=1

The outputs are same, that's why this condition is called as Memory

S-R Latch (Contd..)

Case 2:

If S=1 , R=0 => Q=1 , $\overline{Q}$=0

If S=0 , R=0 => Q=1 , $\overline{Q}$=0

The outputs are same, that's why this condition is called as Memory

Case 3:

If S=1 , R=1 => Q=0 , $\overline{Q}$=0

If S=0 , R=0 => Q=0 , $\overline{Q}$=1

OR

Q=1 , $\overline{Q}$=0

But Q =$\overline{Q}$ it's not true

They must be complement to each other

A	B	Q	$\overline{Q}$
0	0	Memory	
0	1	0	1
1	0	1	0
1	1	Not Used	

- So for same configuration when S=0 , R=0, we have different o/p
- That's why S=1 , R=1 is not used case

S-R Flip Flop

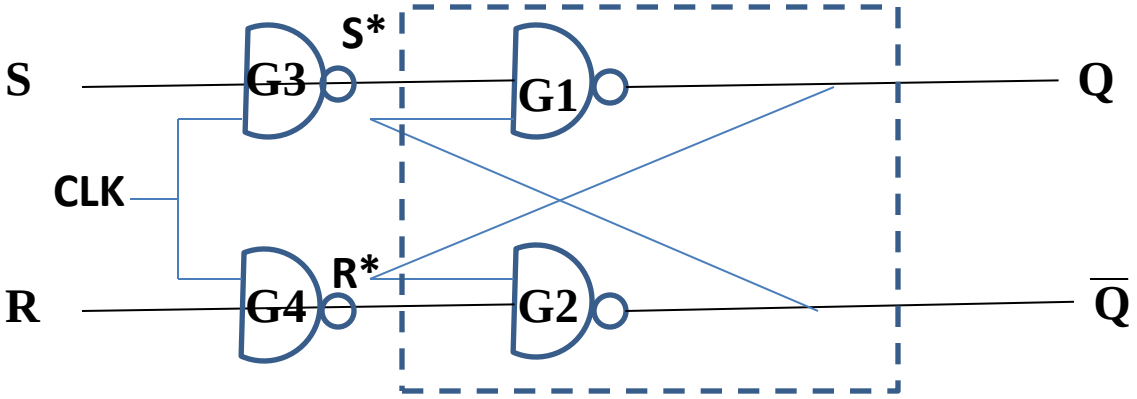


Fig 3: Clocked S-R Flip Flop

- In this ckt if clock pulse is present (CLK=1), its operation is same as that of fig 2

- If CLK=0, the gate G3 & G4 are inhibited, i.e. Their o/p are 1 irrespective of the values of S-R
- In other words, the ckt responds to the I/P S&R only when the clock is present.

•Assuming that i/p do not change during the presence of the clock pulse, we can express the operation of flip flop in form of truth table for S-R flip flop

S-R Flip Flop (Contd..)

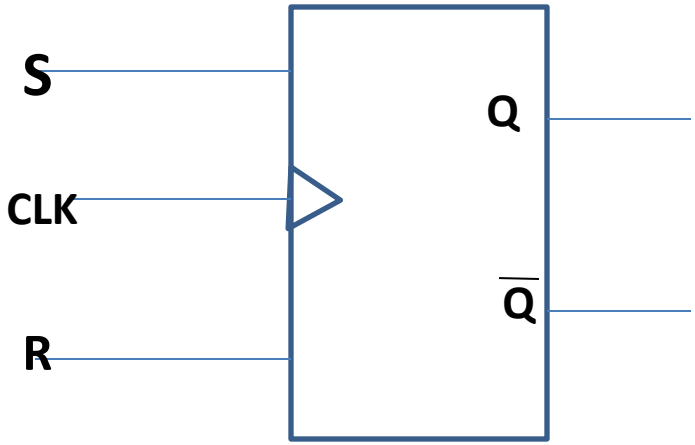
- When S*=0 , R*=0 the Q & $\overline{Q}$ can't be determined, it will be contradictory case, that's why not used case

A	B	Q	$\overline{Q}$
0	0	Not Used	
0	1	1	0
1	0	0	1
1	1	Memory	

- Why we used clock in this ckt, because we don't want our i/p to change accidently, we only wants to change the i/p, when want for that purpose clock is used

S-R Flip Flop (Contd..)

- $S^* = \overline{(S \cdot CLK)} = \overline{S} + \overline{CLK}$
- $R^* = \overline{(R \cdot CLK)} = \overline{R} + \overline{CLK}$



Case 1:

CLK = 0

Then S*=1 $S^* = \overline{S} + \overline{CLK}$

R*=1 $R^* = \overline{R} + \overline{CLK}$

Here value of $\overline{S}$ & $\overline{R}$ doesn't matter, that means x x (don't care terms)

So from previous truth table you can see when S*=1 & R* = 1, we are having the memory i.e. previous state is stored here

S-R Flip Flop (Contd..)

- Case 2:

  If CLK = 1 $\overline{S}=0$ $\overline{R}=0$

  Then $S^* = \overline{S} + \overline{CLK}$

  $R^* = \overline{R} + \overline{CLK}$

  It means $S^* = \overline{S} = 1$

  $R^* = \overline{R} = 1$

Again the last case i.e. 1 1=> memory

- Case 3:

  If CLK = 1 S= 0 R=1

  Then $S^*=1$

  $R^*=0$

  From previous truth table => 1 0 => 0 1

S-R Flip Flop (Contd..)

- Case 4:

  If CLK = 1 S= 1 R=0

  Then S*=0

  R*=1

  From previous truth table =>
  0 1 => 1 0

- Case 5:

  If CLK = 1 S= 1 R=1

  Then S*=0

  R*=0

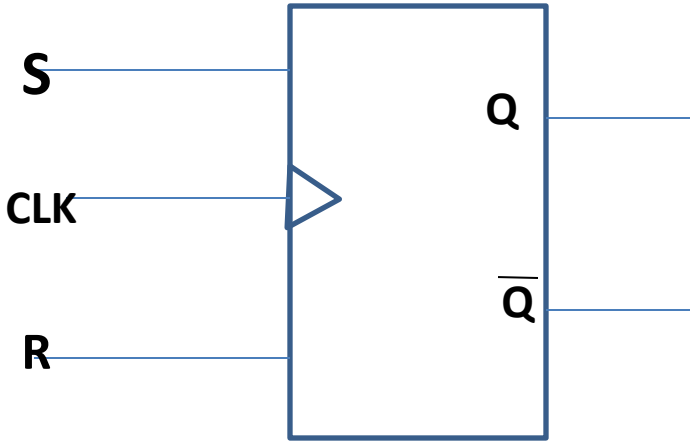
  From previous truth table =>
  0 0 => Not used

CLK	S	R	Q	Q
0	X	X	Memory	
1	0	0	Memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Not Used	

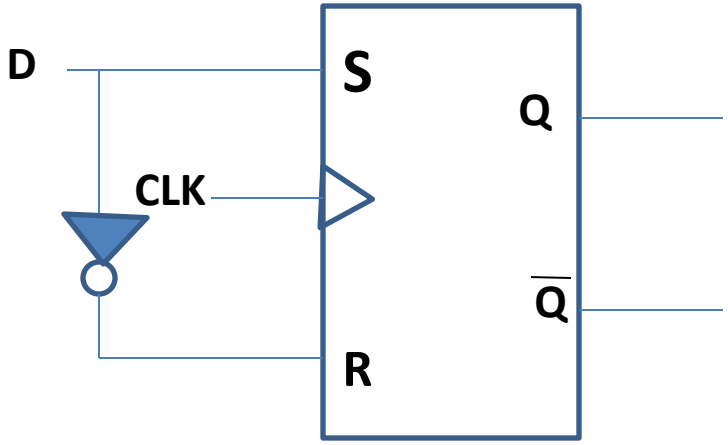
D Flip Flop

Truth Table for SR Flip Flop

CLK	S	R	Qn+1
0	X	X	Memory
1	0	0	Memory
1	0	1	0
1	1	0	1
1	1	1	Not Used

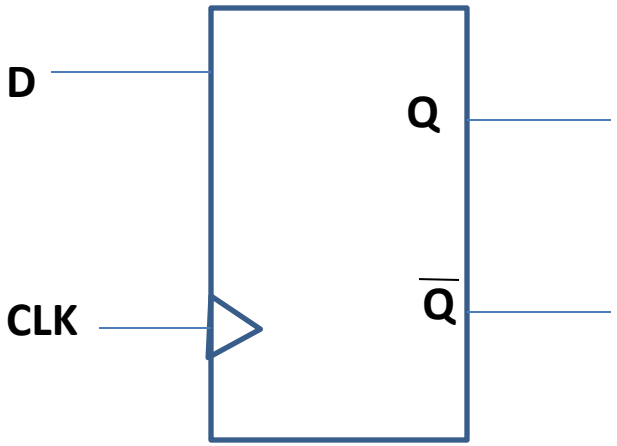


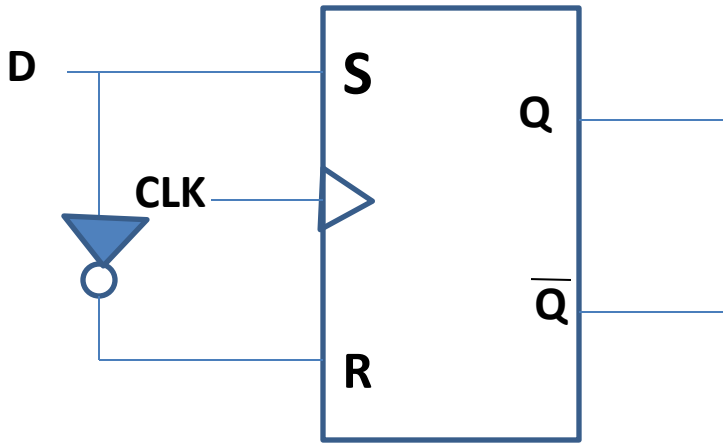
S & R are always complementary of each other



When D=0 (S=0), then R=1 that means 0 1
D=1 (S=1), then R=0 that means 1 0

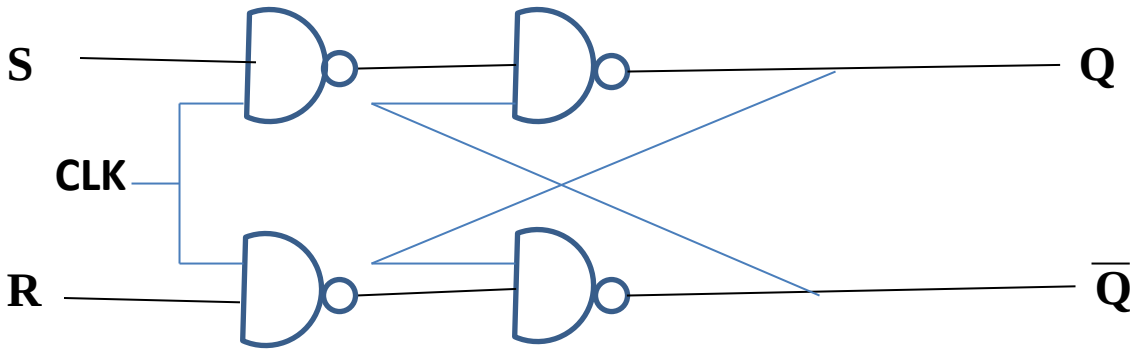
D Flip Flop (Contd..)





CLK	D	Q
0	X	Memory
1	0	0
1	1	1

JK Flip Flop

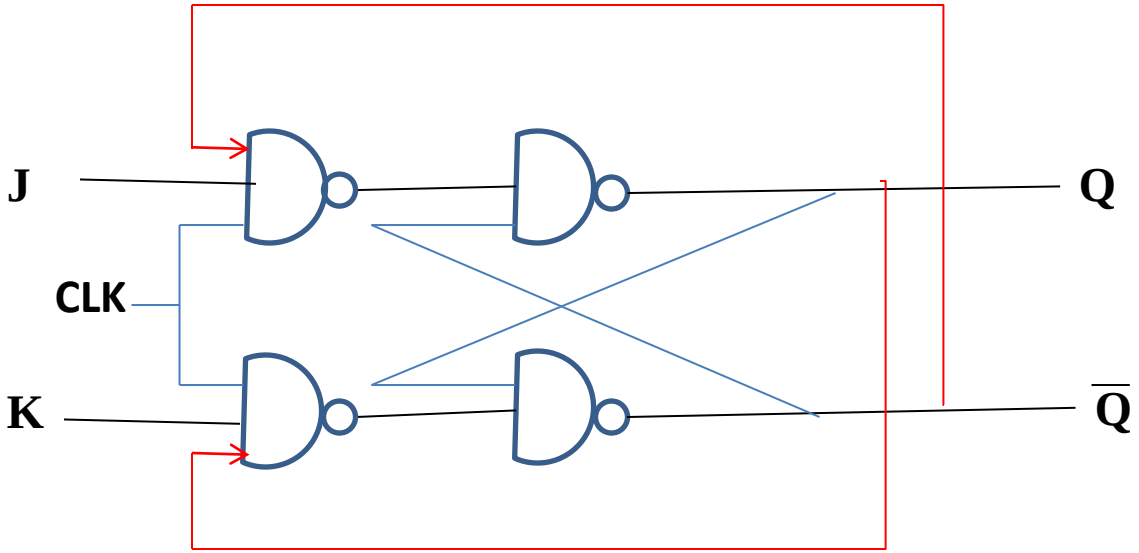


Truth Table for SR Flip Flop

CLK	S	R	Qn+1
0	X	X	Memory
1	0	0	Memory
1	0	1	0
1	1	0	1
1	1	1	Not Used

JK Flip Flop (Contd..)

- Disadvantage of SR Flip Flop is the last case i.e. 1 1 1 = Not used case



JK Flip Flop (Contd..)

- Working of JK Flip Flop

➢ Case 1:

CLK=0 J=X K=X

➢ Case 2:

CLK=1 J=1 K=0

Q=1 $\overline{Q}$=0

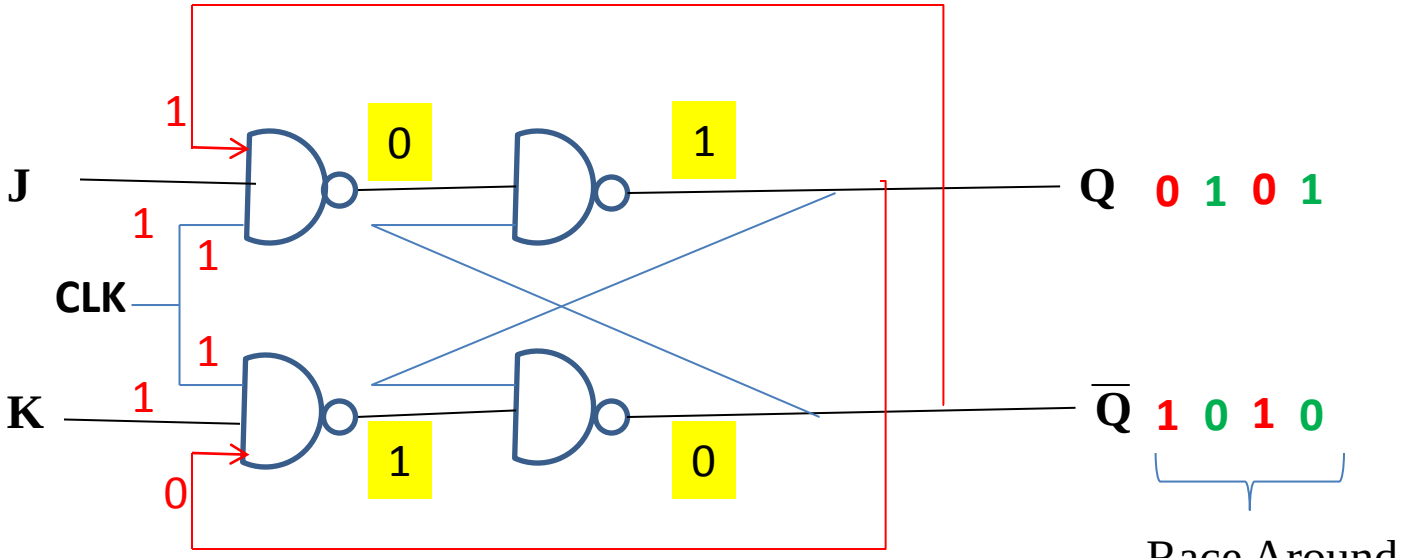
➢ Case 3:

CLK=1 J=0 K=1

Q=0 $\overline{Q}$=1

CLK	J	K	Qn+1
0	X	X	Memory
1	0	0	Memory
1	0	1	0
1	1	0	1
1	1	1	$\overline{Qn}$

JK Flip Flop (Contd..)



Case 4:

CLK=1 J=1 $\overline{K}$=1

assume Q=0 $\overline{Q}$=1

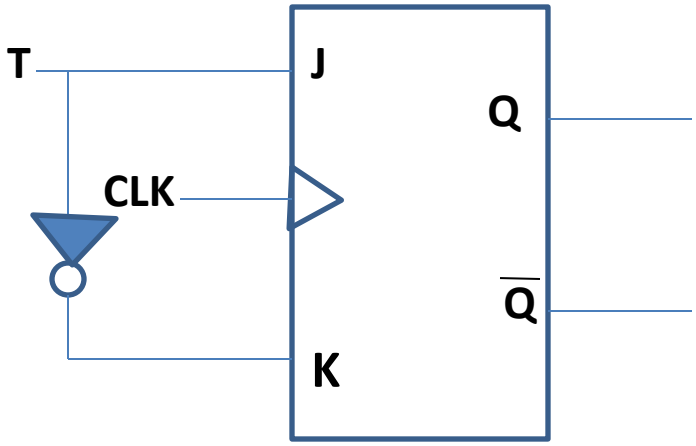
When Q=0 it will become 1 and again it become 0

That means It is the complement of previous state

Therefore whatever with the value for Qn we are having o/p as $\overline{Qn}$ (Toggling)

T Flip Flop

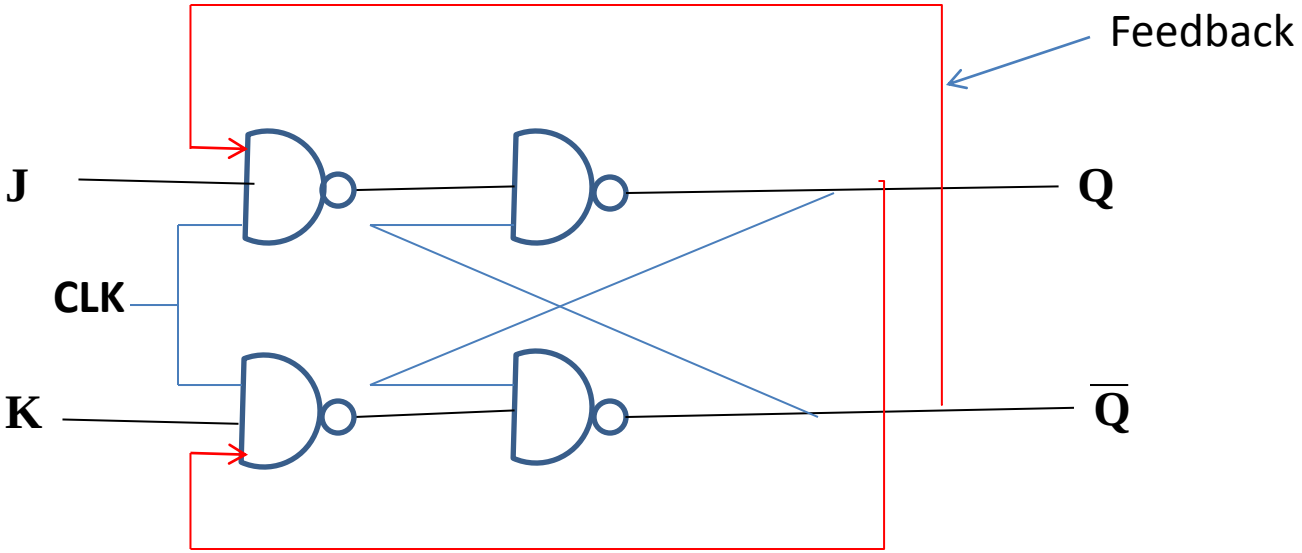
- Toggling is the controlled change of o/p from 0 to 1 and 1 to 0



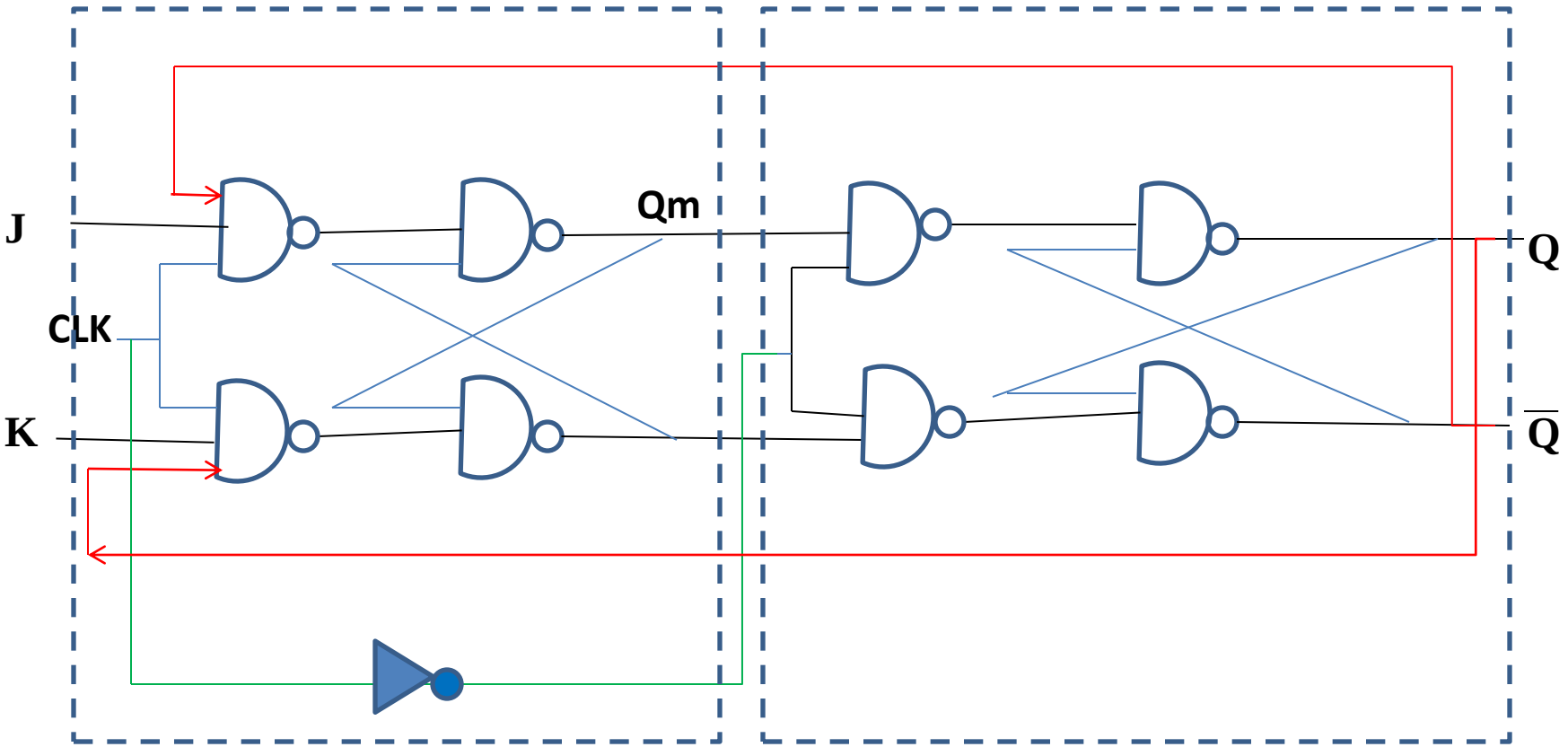
CLK	T	Qn+1
0	X	Memory
1	0	Memory
1	1	1

When T=0 (J=0), then K=0 that means 0 0 => Memory (From TT of JK FF)
T=1 (J=1), then K=1 that means 1 1 => $\overline{Qn}$ (From TT of JK FF)

Master Slave Flip Flop



Master Slave Flip Flop (Contd..)



Master Slave Flip Flop (Contd..)

- Master Slave ckt can be implemented for SR and D flip flop also
- Important things in Master Slave flip flop
  - Feedback
  - Clock
- When Clock =1 => Master will operate
- When Clock =0 => Slave will operate

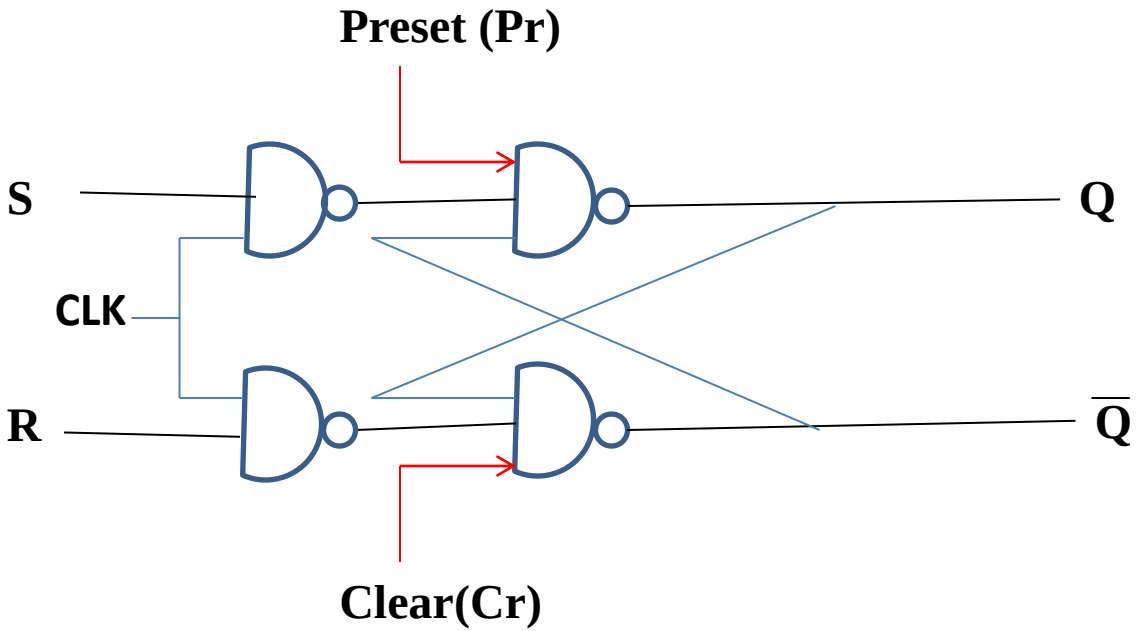
- When clk=1, Qm will change and Q remains same

- When clk=0, Q will change but when Q changes we are having feedback here, but the clock is low, therefore master will not operate, so there is no effect of feedback

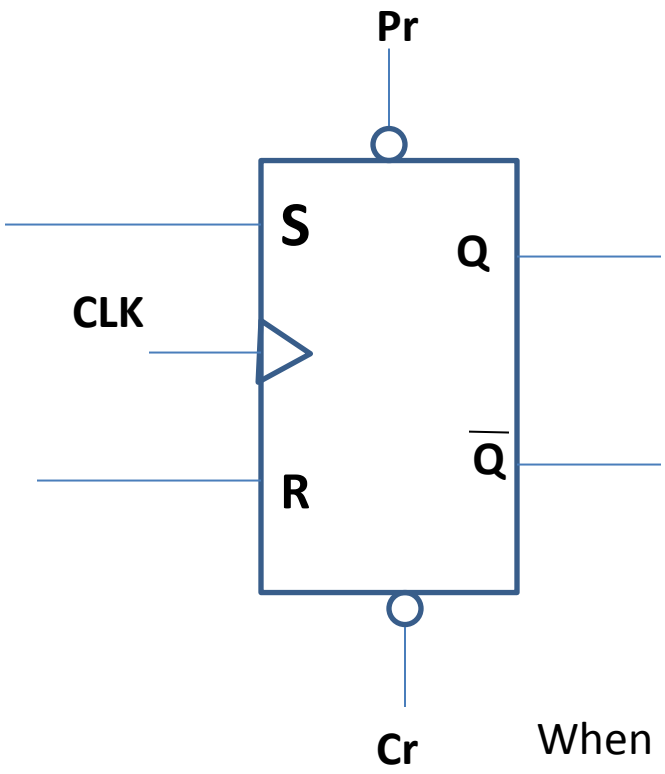
Preset And Clear

- They are direct I/P or Overriding I/P or Asynchronous I/P
- While S, R, J, K, D and T are Synchronous I/P
- Whenever Preset and Clear comme into the picture they will change the O/P. i.e. Qn will change directly irrespective of Synchronous I/P

Preset And Clear (Contd..)



Preset And Clear (Contd..)



Preset	Clear	Qn
0	0	Not Used
0	1	1
1	0	0
1	1	Normal

When Pr=0 the O/P=1 i.e. Q=1 $\overline{Q}$=0

When Cr=0 the O/P=1 i.e. Q=0 because $\overline{Q}$=1

Characteristic Table & Excitation Table For SR Flip Flop

Truth Table for SR Flip Flop

CLK	S	R	Q	Q
0	X	X	Memory	
1	0	0	Memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Not Used	

Characteristic Table & Excitation Table For SR Flip Flop (Contd..)

Characteristic Table

Qn	S	R	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

Excitation Table

Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Characteristic Table & Excitation Table For D Flip Flop

Truth Table for SR Flip Flop

CLK	D	Qn+1
0	X	Qn
1	0	0
1	1	1

Characteristic Table & Excitation Table For D Flip Flop (Contd..)

Characteristic Table

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

D=0 Qn+1=0

D=1 Qn+1=1

Qn+1=D

Excitation Table

Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

Characteristic Table & Excitation Table For JK Flip Flop

Truth Table for SR Flip Flop

CLK	J	K	Qn+1
0	X	X	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	$\overline{Qn}$

Memory

Characteristic Table & Excitation Table For JK Flip Flop (Contd..)

Characteristic Table

Qn	J	K	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	**1**
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	**0**

Excitation Table

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$Qn+1 = \overline{Qn} \cdot J + Qn \cdot \overline{K}$

$J = Qn+1 \qquad K = \overline{Qn+1}$

Characteristic Table & Excitation Table For T Flip Flop

Truth Table for SR Flip Flop

CLK	T	Qn+1
0	X	Qn
1	0	Qn
1	1	$\overline{Qn}$

Characteristic Table & Excitation Table For T Flip Flop (Contd..)

Characteristic Table

Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

Odd 1's Detector

Excitation Table

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

$Q_{n+1} = Q_n \oplus T$

Flip Flop Conversions

- **Steps:**

1. Identify available & required Flip Flop
2. Make characteristic table of required flip flop
3. Make Excitation table for available flip flop
4. Write Boolean expression for available flip flop
5. Draw the circuit

JK Flip Flop to D Flip Flop

- Step 1: Available Flip Flop = JK FF

  Required Flip Flop = D FF
- Step 2: Characteristic table of Required FF=> D FF

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

Qn+1 = D

JK Flip Flop to D Flip Flop (Contd..)

- Step 3: Excitation table of available FF=> JK FF

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

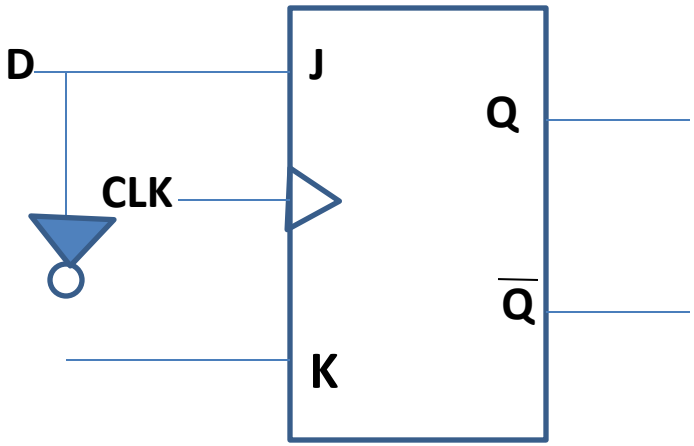
Qn	D	Qn+1	J	K
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

JK Flip Flop to D Flip Flop (Contd..)

- **Step 4:** Boolean expression for available FF=> JK FF

  J=D K=$\overline{D}$

- **Step 5:** Draw Circuit



T Flip Flop to D Flip Flop

- Step 1: Available Flip Flop = T FF

  Required Flip Flop = D FF
- Step 2: Characteristic table of Required FF=> D FF

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

Qn+1 = D

T Flip Flop to D Flip Flop (Contd..)

- Step 3: Excitation table of available FF=> T FF

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

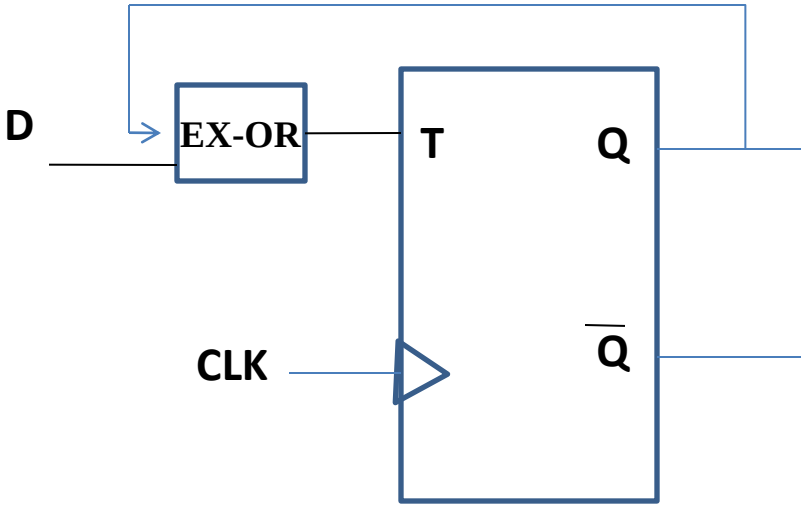
Qn	D	Qn+1	T
0	0	0	0
0	1	1	1
1	0	0	X
1	1	1	X

T Flip Flop to D Flip Flop (Contd..)

- **Step 4:** Boolean expression for available FF=> T FF

  $T = D \oplus Qn$

- **Step 5:** Draw Circuit



SR Flip Flop to JK Flip Flop

- Step 1: Available Flip Flop = SR FF

  Required Flip Flop = JK FF
- Step 2: Characteristic table of Required FF=> JK FF

Qn	J	K	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	**1**
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	**0**

SR Flip Flop to JK Flip Flop (Contd..)

- **Step 3:** Excitation table of available FF=> SR FF

Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

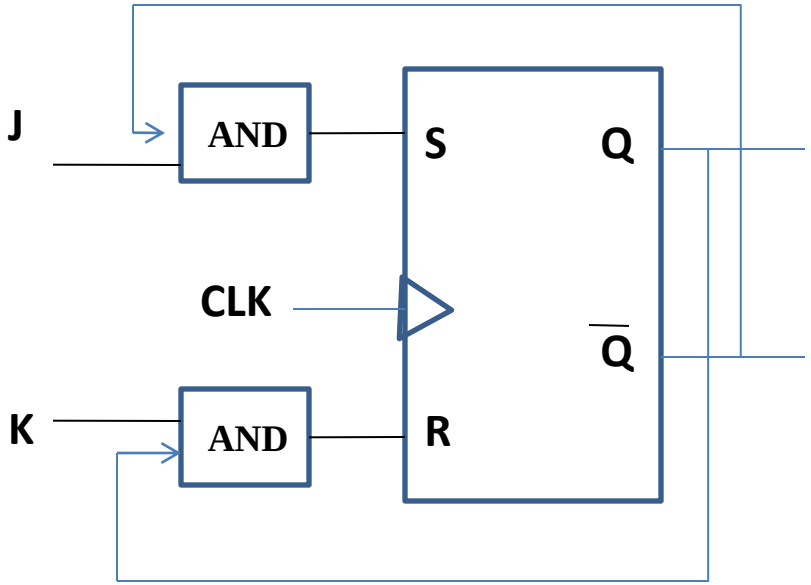
Qn	J	K	Qn+1	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	**1**	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	**0**	0	1

SR Flip Flop to JK Flip Flop (Contd..)

- **Step 4:** Boolean expression for available FF=> T FF

  $S = \overline{Qn} \cdot J \qquad R = Qn \cdot K$

- **Step 5:** Draw Circuit



SR Flip Flop to T Flip Flop

- Step 1: Available Flip Flop = SR FF

  Required Flip Flop = T FF
- Step 2: Characteristic table of Required FF=> T FF

Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

SR Flip Flop to T Flip Flop (Contd..)

- **Step 3:** Excitation table of available FF=> SR FF

Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

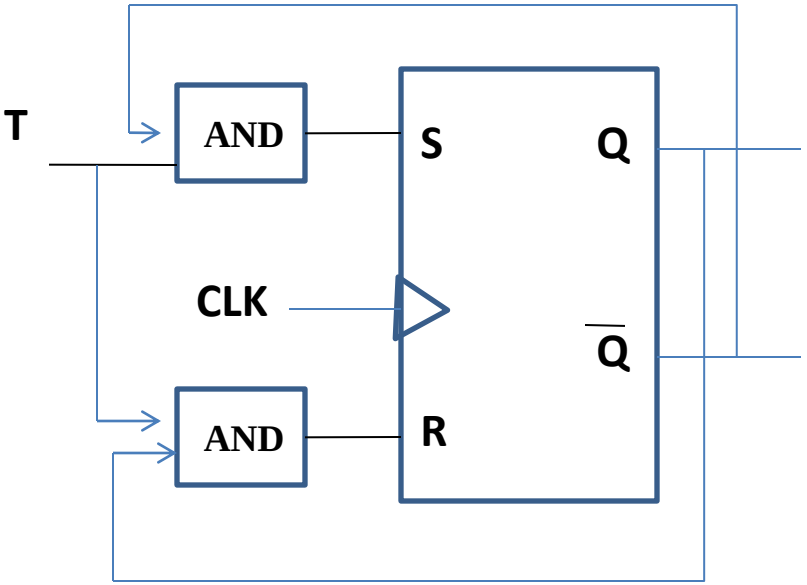
Qn	T	Qn+1	S	R
0	0	0	0	X
0	1	1	1	0
1	0	1	X	0
1	1	0	0	1

SR Flip Flop to JK Flip Flop (Contd..)

- **Step 4:** Boolean expression for available FF=> T FF

  $S = \overline{Qn} \cdot T \qquad R = Qn \cdot T$

- **Step 5:** Draw Circuit



Home Work

1. Convert JK Flip Flop into SR Flip Flop

2. Convert T Flip Flop into SR Flip Flop