

Counters

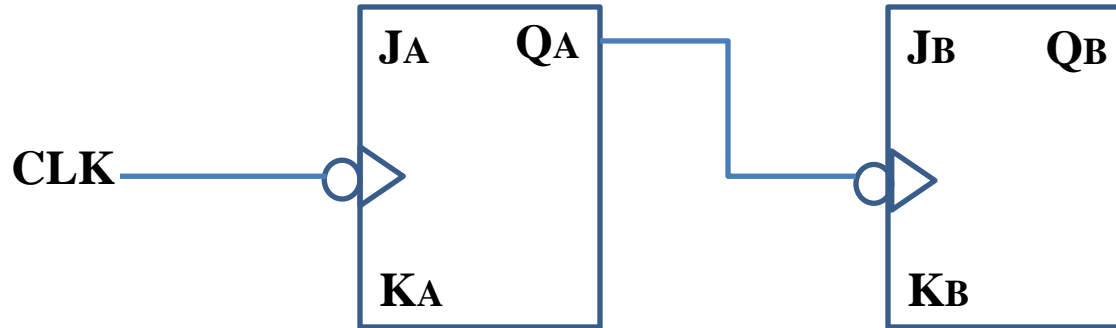
by

Prof. Sujata Wakchaure

Introduction

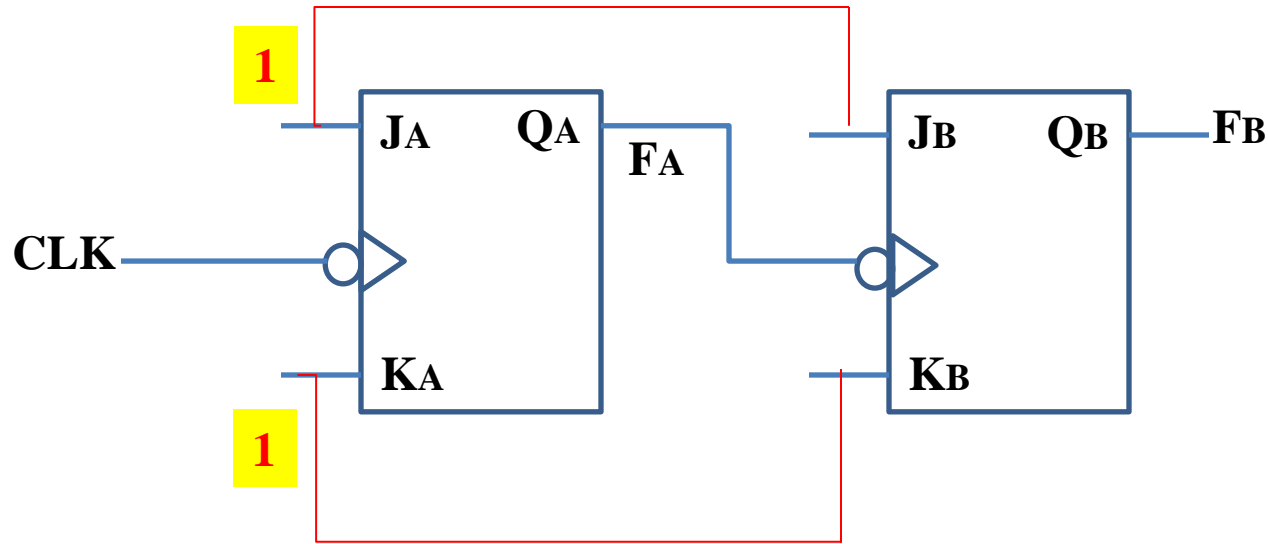
- In digital logic and computing, a **counter** is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal
- Counters are a specific type of sequential circuit
- Counters can act as simple clocks to keep track of “time.”
- Counters are special case of a finite state machine
- Applications: System Clock, Timer, Watches, Alarms, Protocols, Frequency Division, etc.

Working of Counter



- It is a flipflop as divide by 2 circuit
- Clock is not same here

Working of Counter (Contd..)



- Now $J_A = K_A = J_B = K_B = 1$
- That means there is **Toggling**.
- Toggling is very imp in counters

Working of Counter (Contd..)

Given to
1st FF only

Clock

T_C

0

1

2

3

4

T_A

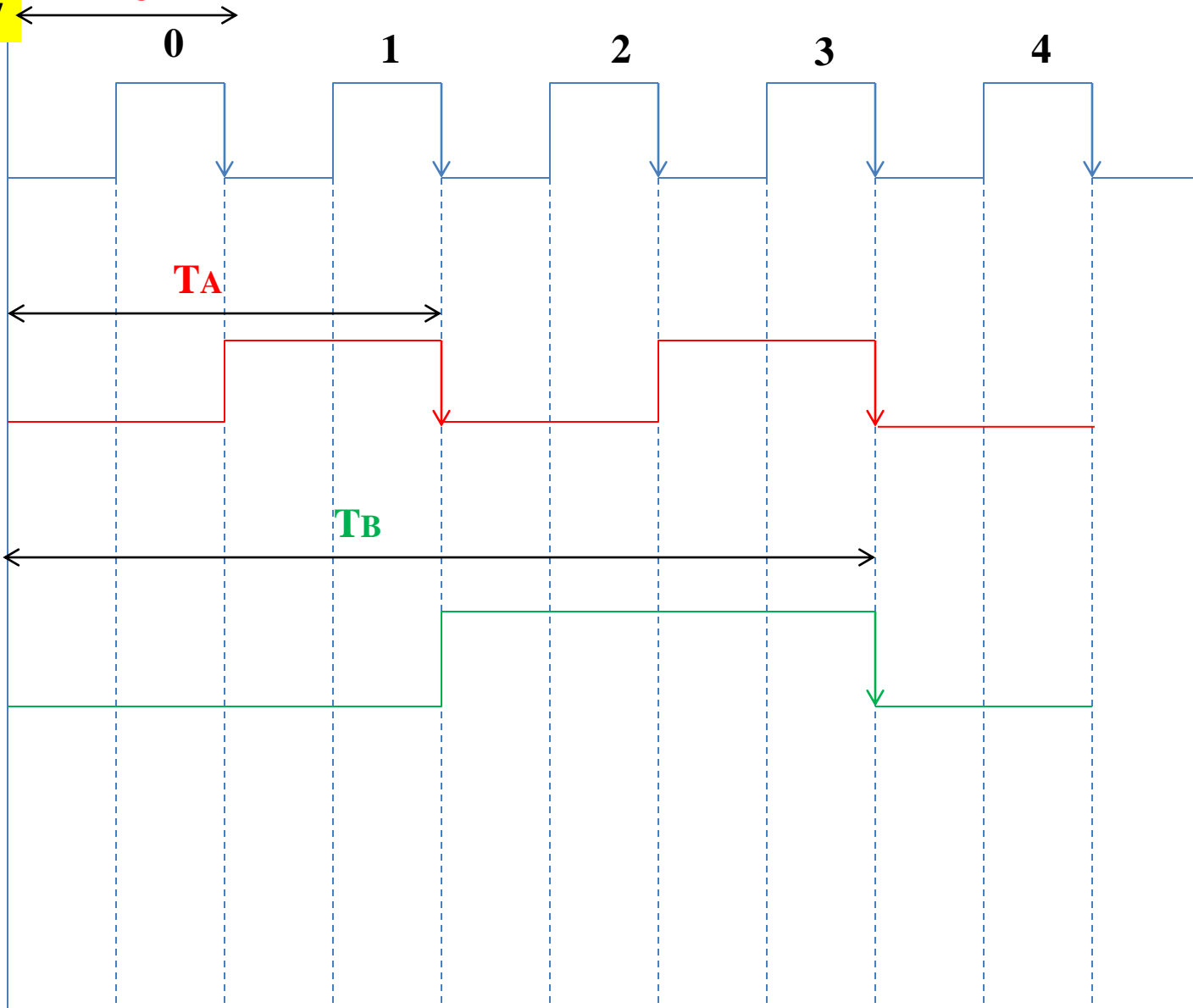
Q_A

Clk to
2nd FF

T_B

Q_B

O/P of
2nd FF



Working of Counter (Contd..)

- Initially $Q_A = 0$
- As Toggling is there Q_A will become as follows:
 $Q_A = 1$
- Then for next interval 1 will become 0
 $Q_A = 0$
- Now Q_A is acting as a **Clock** for next FF

Working of Counter (Contd..)

- So now consider Q_B as **Low**

$$Q_B = 0$$

- **Frequency (fc) :**
 - Time Period T_C is for Clock
 - Time Period T_A is for Q_B
 - Here T_A is Twice of T_C

$$T_A = 2T_C$$

Working of Counter (Contd..)

- Relation between Time Period and Frequency:

$$\mathbf{F = 1/T}$$

- I can write as,

$$T_A = 1/F_A$$

$$\mathbf{T_A = 2/f_c}$$

Now Frequency is half

OR $\mathbf{F_A = f_c/2}$

- Similarly we can check for $\mathbf{F_B}$

$$\mathbf{T_B = 2T_A}$$

$$\mathbf{1/F_B = 2/F_A}$$

OR $F_B = F_A/2 = F_c/4$

$$\mathbf{F_B = F_c/4}$$

Working of Counter (Contd..)

- This particular circuit is counting from 0 to 3

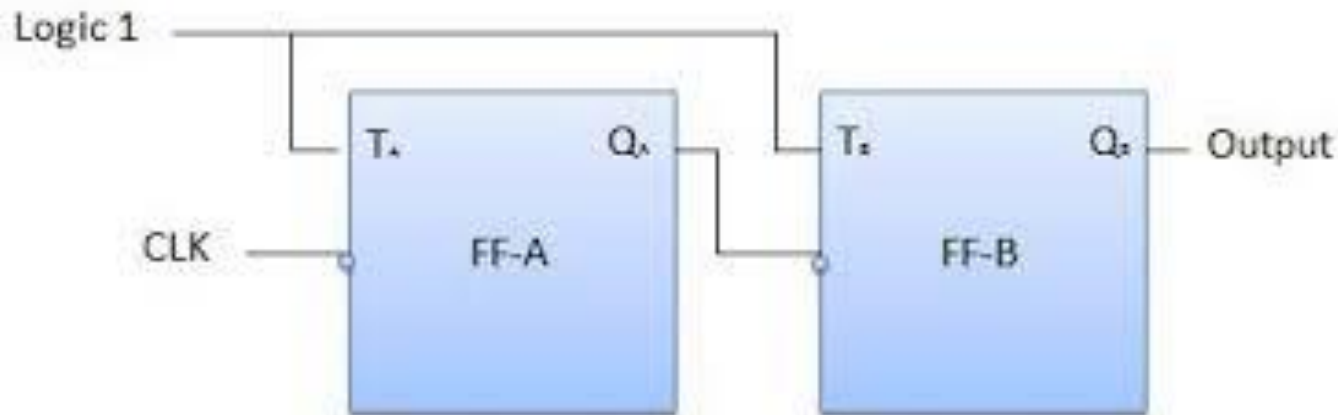
CLK	Q _B	Q _A
0	0	0
1	0	1
2	1	0
3	1	1

Types of Counters

1. Asynchronous Counter (Ripple Counter)
2. Synchronous Counter

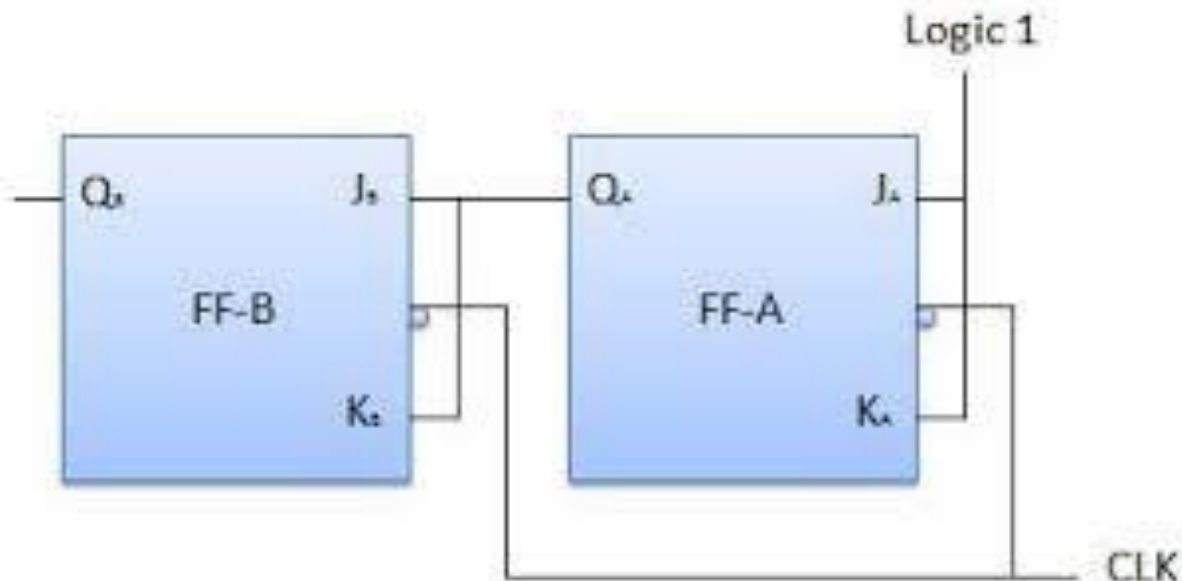
Asynchronous Counter (Ripple Counter)

- Here only the 1st Flip-Flop is clocked by external clock
- All the subsequent flip-flops are clocked by the O/P of the preceding flip-flop



Synchronous Counters

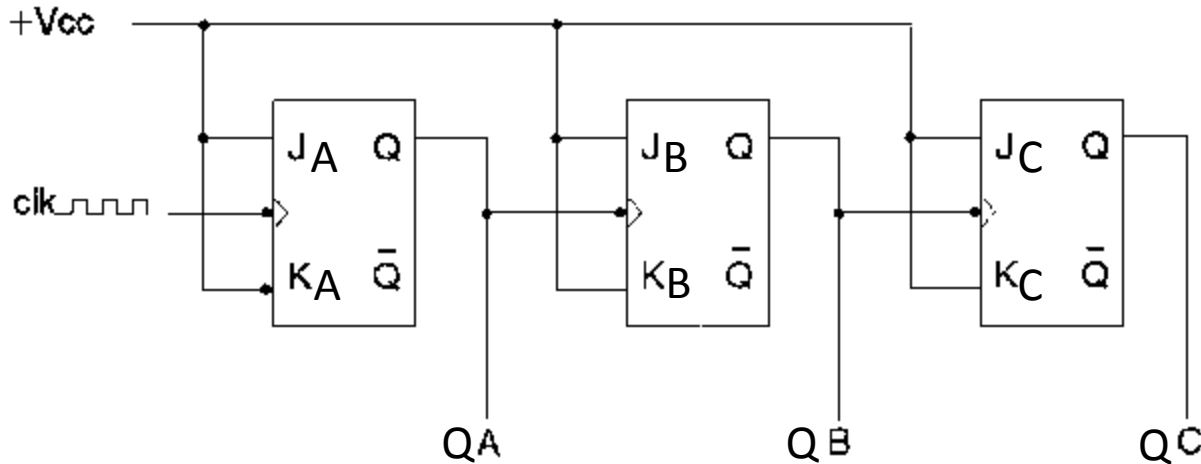
- All the flip-flop receive the external clock pulse simultaneously



Asynchronous Vs. Synchronous Counter

Asynchronous Counter	Synchronous Counter
Flip-flops are connected in such a way that the O/P of 1 st ff drives the clock of next ff	There is no connection between O/P of 1 st ff & clock of the next ff
FF are not clocked simultaneously	FF are clocked simultaneously
FF ckt is simple for more no. of states	Ckt becomes complicated as no. of states increases
Speed is slow as clock is propagated through no. of stages	Speed is high as clock is given at a same time

3-Bit Asynchronous Up Counter

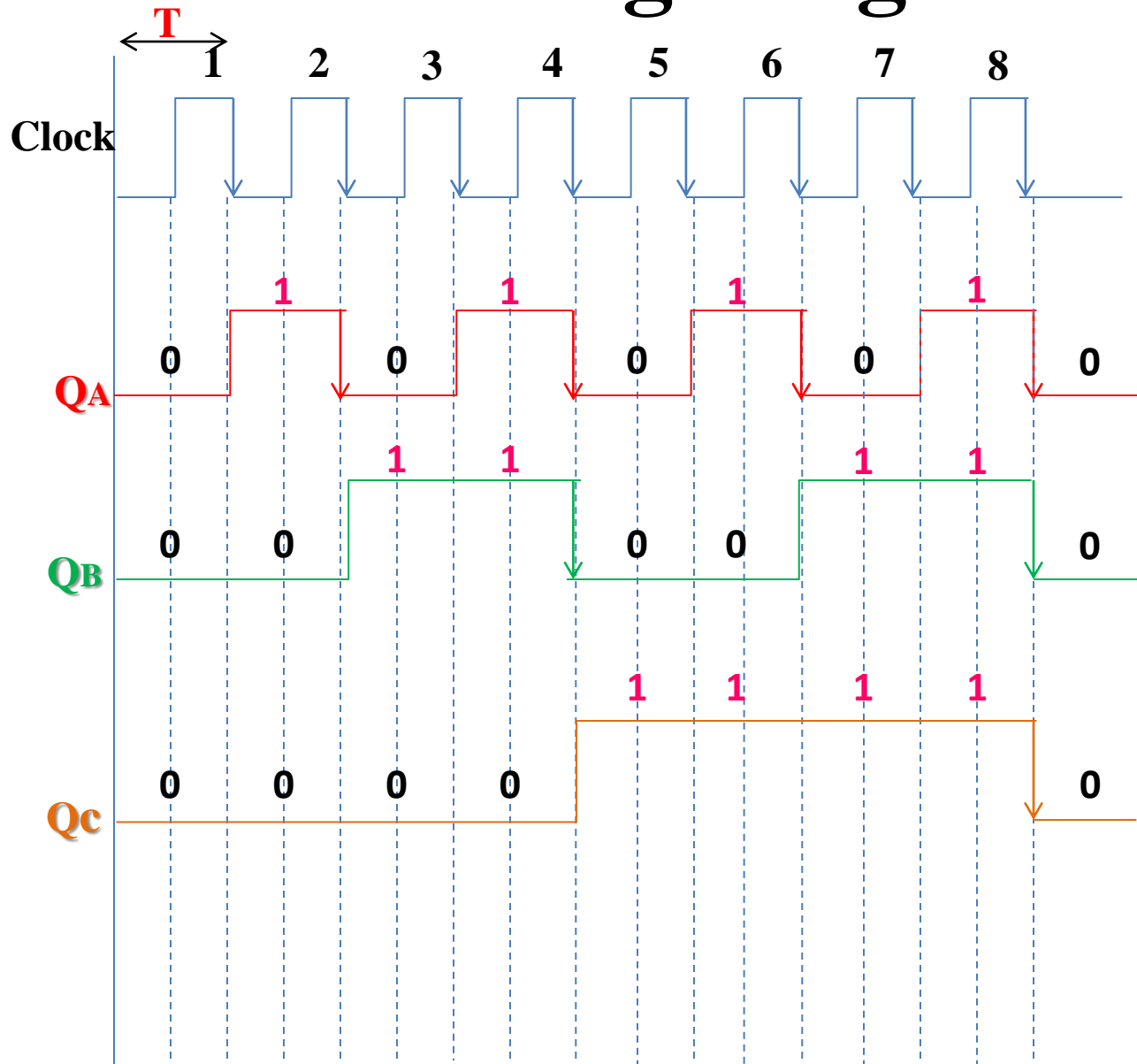


- Up counter Means, it will start counting from lower value (0-1-2-....) i.e. 000

111

- for **Toggling** we have to make $J_A = K_A = J_B = K_B = J_C = K_C = 1$

Timing Diagram



Timing Diagram (Contd..)

Clock	QC	QB	QA	Decimal Equivalent
Initially	0	0	0	0
1 st ↓	0	0	1	1
2 nd ↓	0	1	0	2
3 rd ↓	0	1	1	3
4 th ↓	1	0	0	4
5 th ↓	1	0	1	5
6 th ↓	1	1	0	6
7 th ↓	1	1	1	7
8 th ↓	0	0	0	0

- Total 8 States

$$2^n = 2^3 = 8$$

Where, n = No. of flip-flops

- **Maximum Count = $2^n - 1$**
 $= 8 - 1$
 $= 7$

Synchronous Counter

- **How to design Synchronous Counter?**
- Step 1: Decide Type of FF and No. of FF
- Step 2: Excitation Table of FF
- Step 3: State diagram & ckt excitation table
- Step 4: Obtain simplified equation using K-Map
- Step 5: Draw the logic diagram

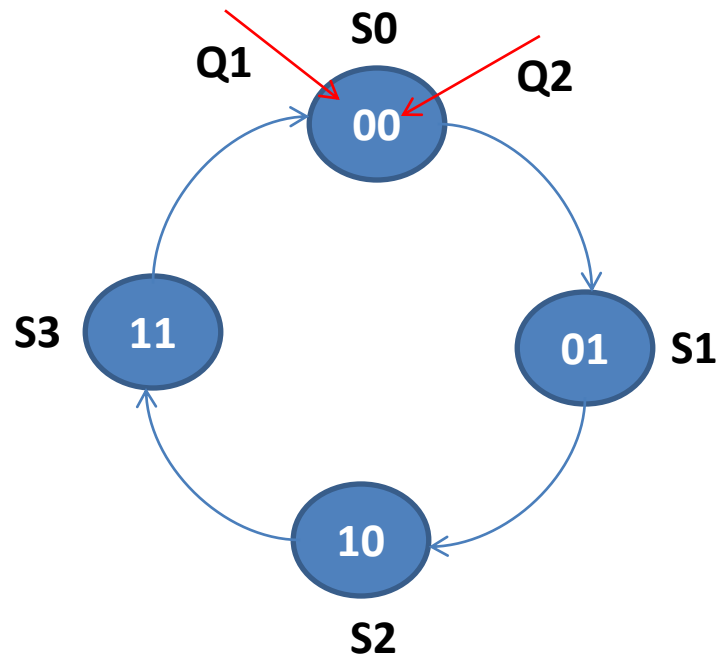
2 – Bit Synchronous Up Counter

- Step 1: Decide Type of FF and No. of FF
 » i.e. JK FF
- Step 2: Excitation table of JK FF

Q _n	Q _{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

2 – Bit Synchronous Up Counter (Contd..)

- Step 3: State dia and ckt Excitation table
 - » $2^n = 2^2 = 4$
 - » Max Count = $2^n - 1 = 4 - 1 = 3$



2 – Bit Synchronous Up Counter (Contd..)

- Circuit Excitation Table:

Present State		Next State					
Q1	Q2	Q1*	Q2*	J1	K1	J2	K2
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

- Step 4: Obtain simplified equation using K-Map

$$J1 = Q2$$

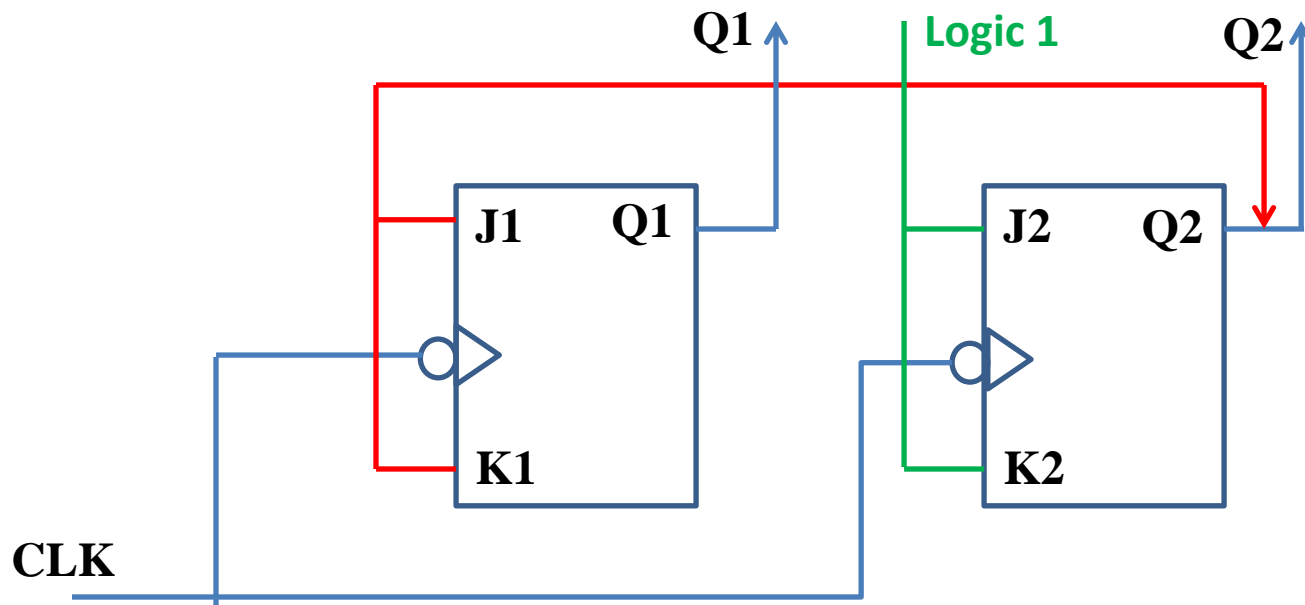
$$J2 = 1$$

$$K1 = Q2$$

$$K2 = 1$$

2 – Bit Synchronous Up Counter (Contd..)

- Step 5: Draw the Logic Diagram:



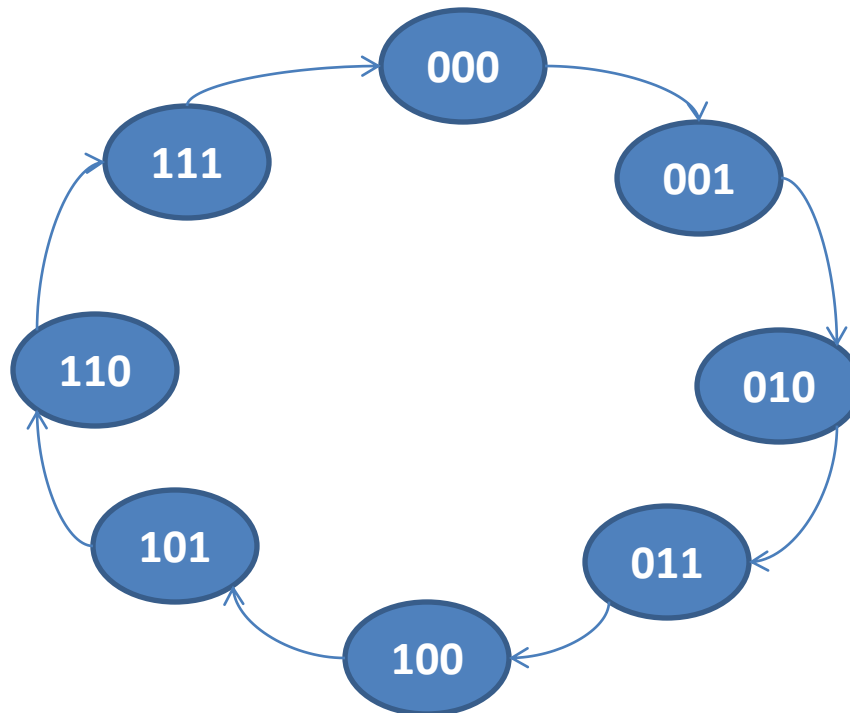
3 – Bit Synchronous Up Counter

- Step 1: Decide Type of FF and No. of FF
 - » 3-Bit => 3 FF => T FF
- Step 2: Excitation table of T FF

Q _n	Q _{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

3 – Bit Synchronous Up Counter (Contd..)

- Step 3: State dia and ckt Excitation table
 - » $2^n = 2^3 = 8$
 - » Max Count = $2^n - 1 = 8 - 1 = 7$



3 – Bit Synchronous Up Counter (Contd..)

- Circuit Excitation Table:

Present State			Next State					
QC	QB	QA	QC*	QB*	QA*	TC	TB	TA
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

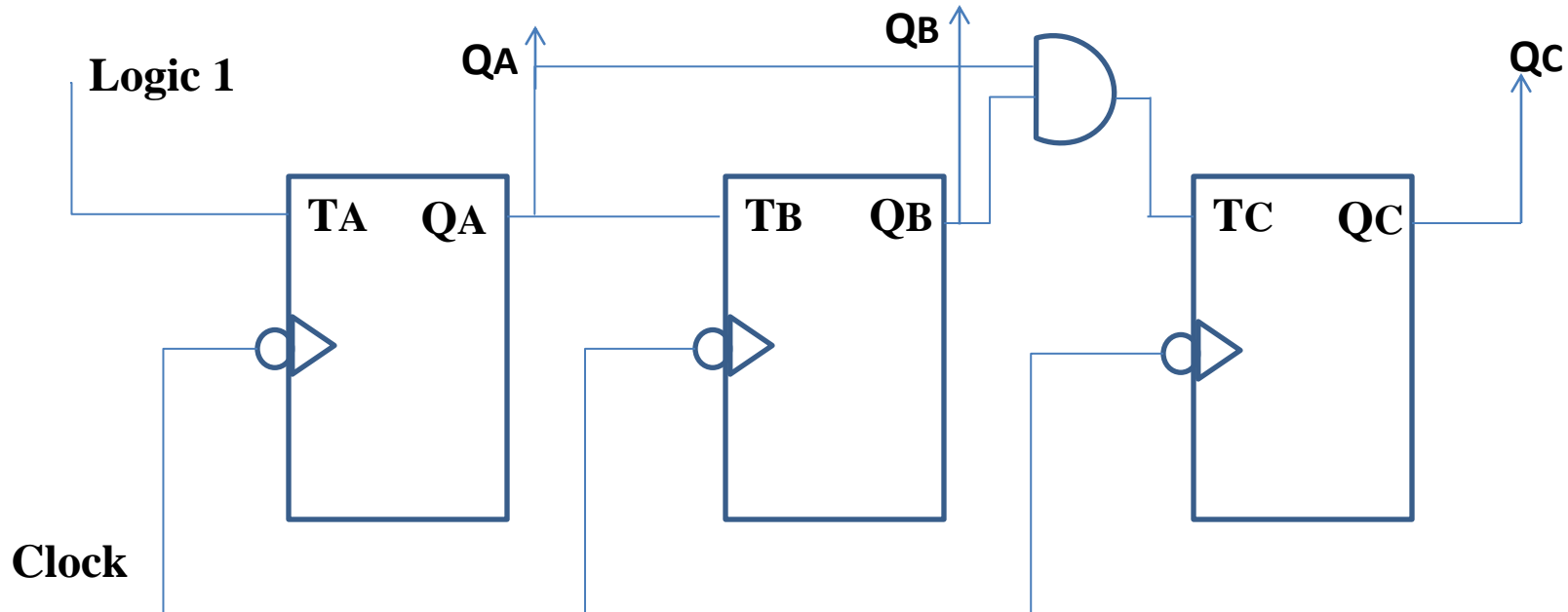
$$T_C = Q_B Q_A$$

$$T_B = Q_A$$

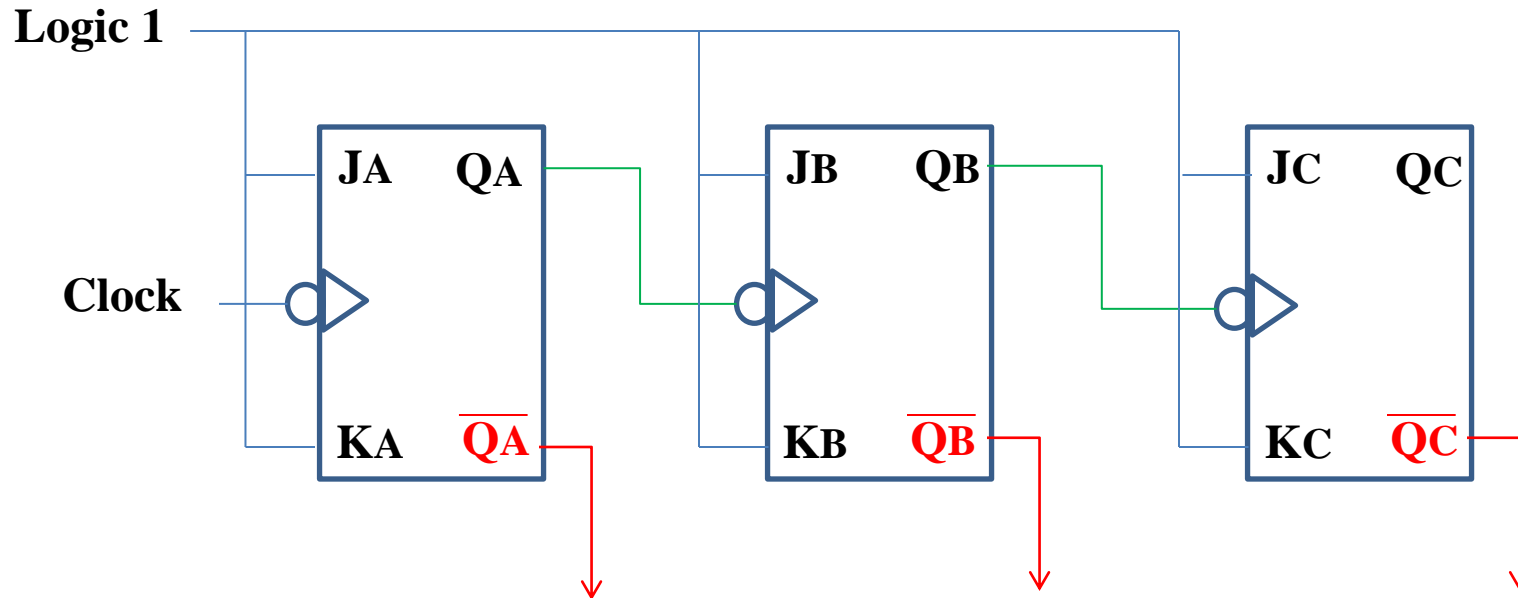
$$T_A = 1$$

3 – Bit Synchronous Up Counter (Contd..)

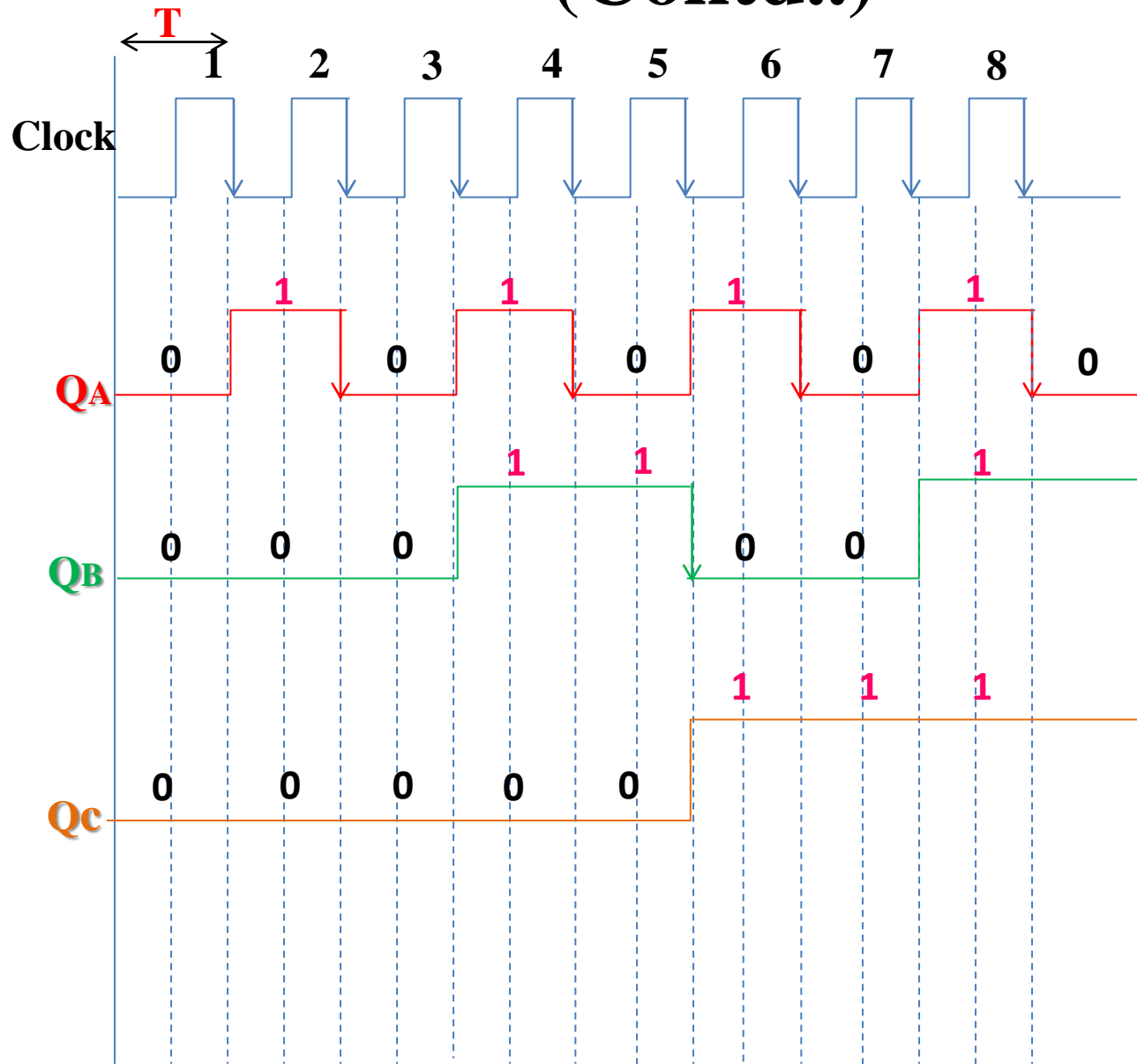
- Step 5: Logic Diagram



3 – Bit Asynchronous Down Counter



3 – Bit Asynchronous Down Counter (Contd..)



3 – Bit Asynchronous Down Counter (Contd..)

Clock	Up Counting			Down Counting			Decimal Equivalent
	QC	QB	QA	QC	QB	QA	
Initially	0	0	0	1	1	1	7
1 st	0	0	1	1	1	0	6
2 nd	0	1	0	1	0	1	5
3 rd	0	1	1	1	0	0	4
4 th	1	0	0	0	1	1	3
5 th	1	0	1	0	1	0	2
6 th	1	1	0	0	0	1	1
7 th	1	1	1	0	0	0	0

3 – Bit Asynchronous Down Counter (Contd..)

