1. In the circuit shown, the clock frequency must be 12Khz and the output we should get 15Khz, i.e., the frequency of the Clk signal, is 12 kHz.The frequency of the signal at $Q_2$ is _____ KHz.

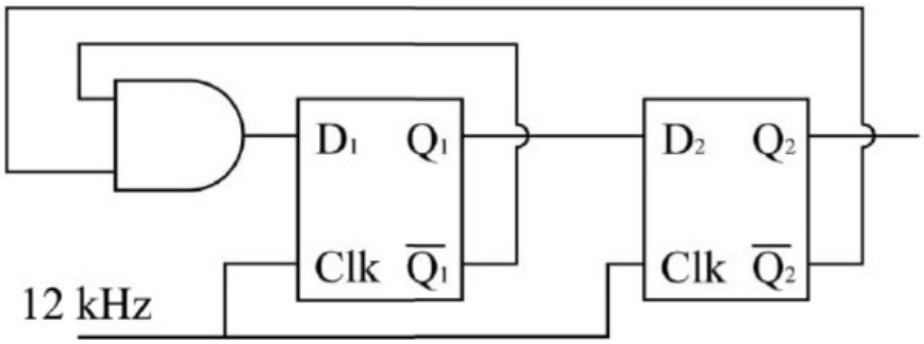


Figure 1