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End-to-End Time Synchronization Performance Measurement in Heterogenous TSN Networks

Susruth Sudhakaran and Christopher Hall

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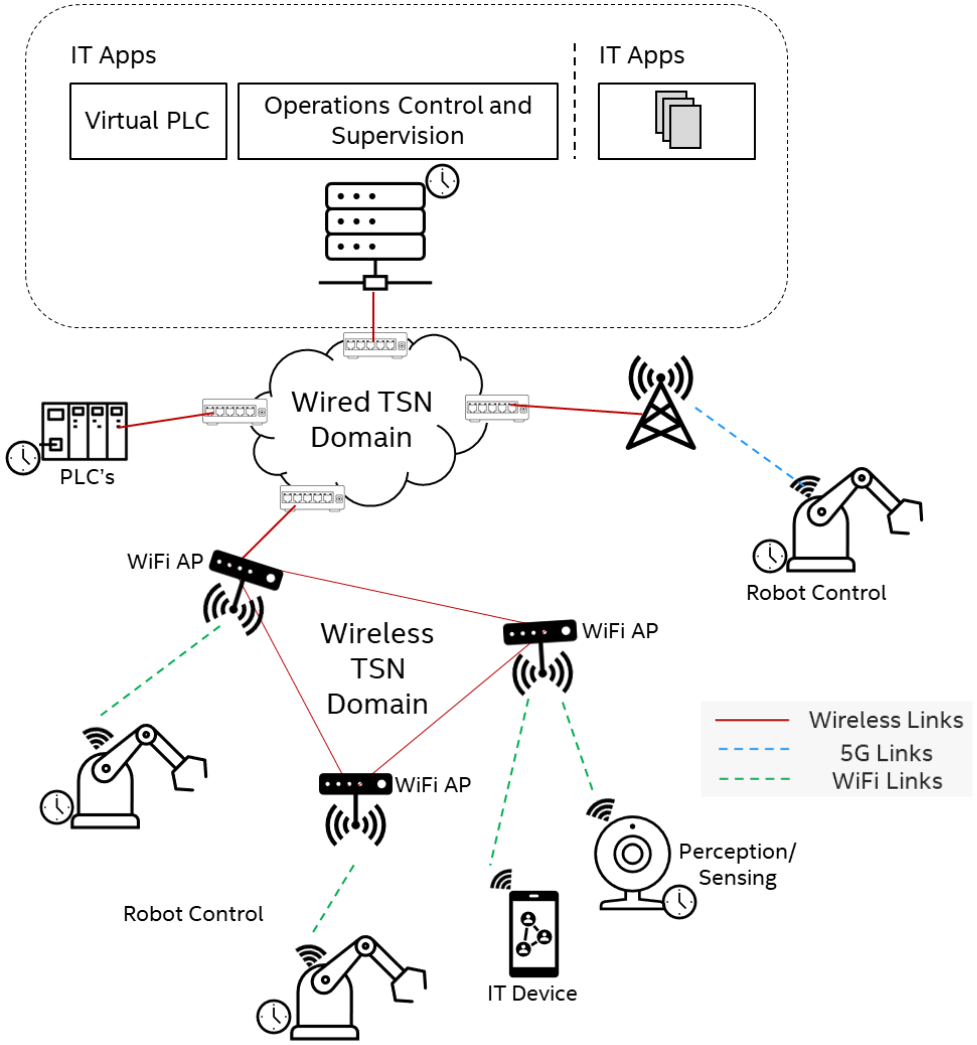
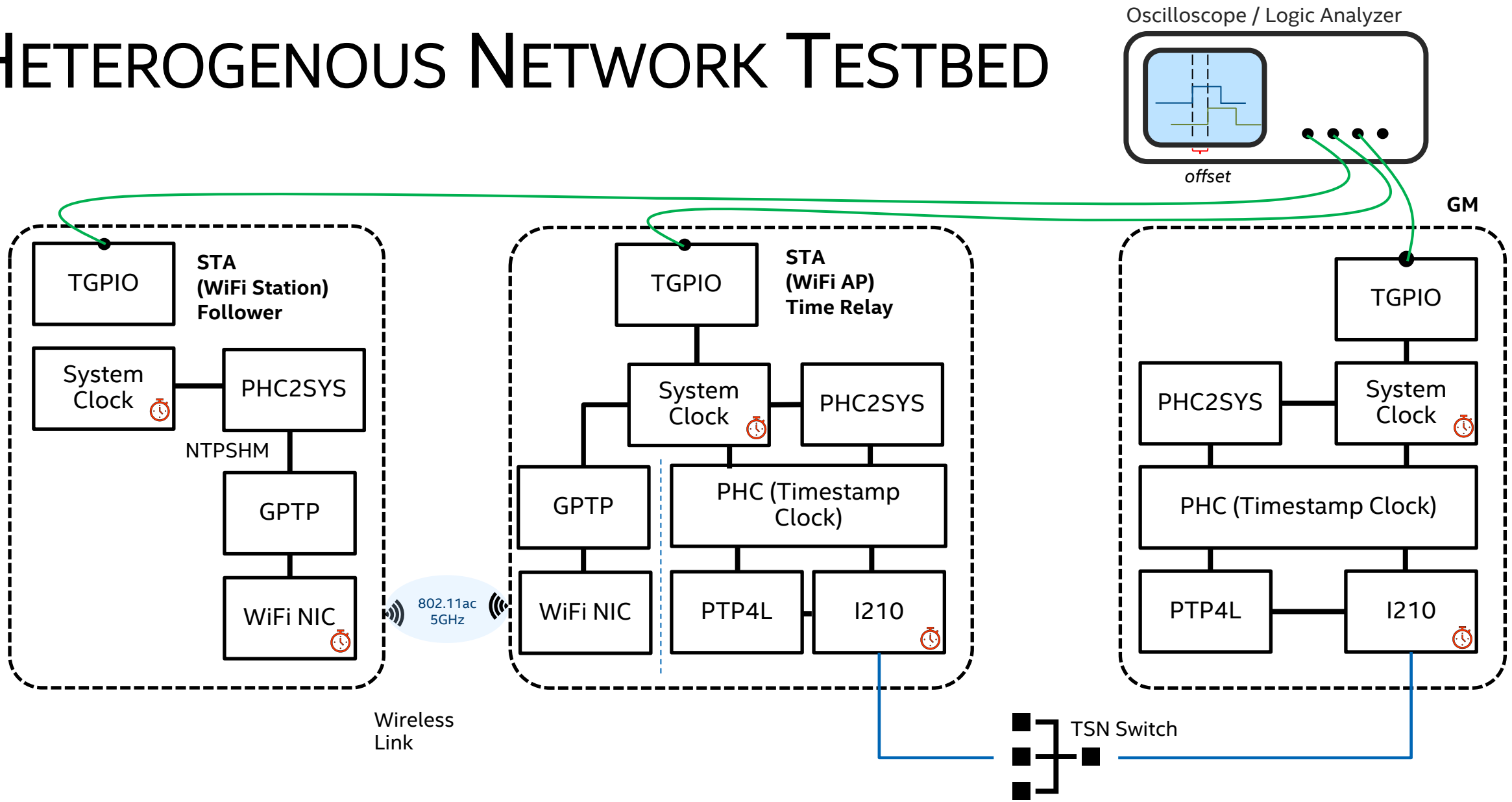
HETEROGENOUS TSN NETWORK

- Heterogenous networks include standards-based Ethernet, Wi-Fi, and 5G networks
- Support for heterogeneous networks are a core requirement for Industry 4.0 enabling
- TSN support is a requirement for Industrial use cases
- Precise Time Synchronization is a key requirement for industrial use cases providing common time base for coordinated control applications and deterministic network access



Industry 4.0 requires TSN and we need a testbed and measurement methodology to assess time synchronization accuracy over heterogenous networks

HETEROGENOUS NETWORK TESTBED

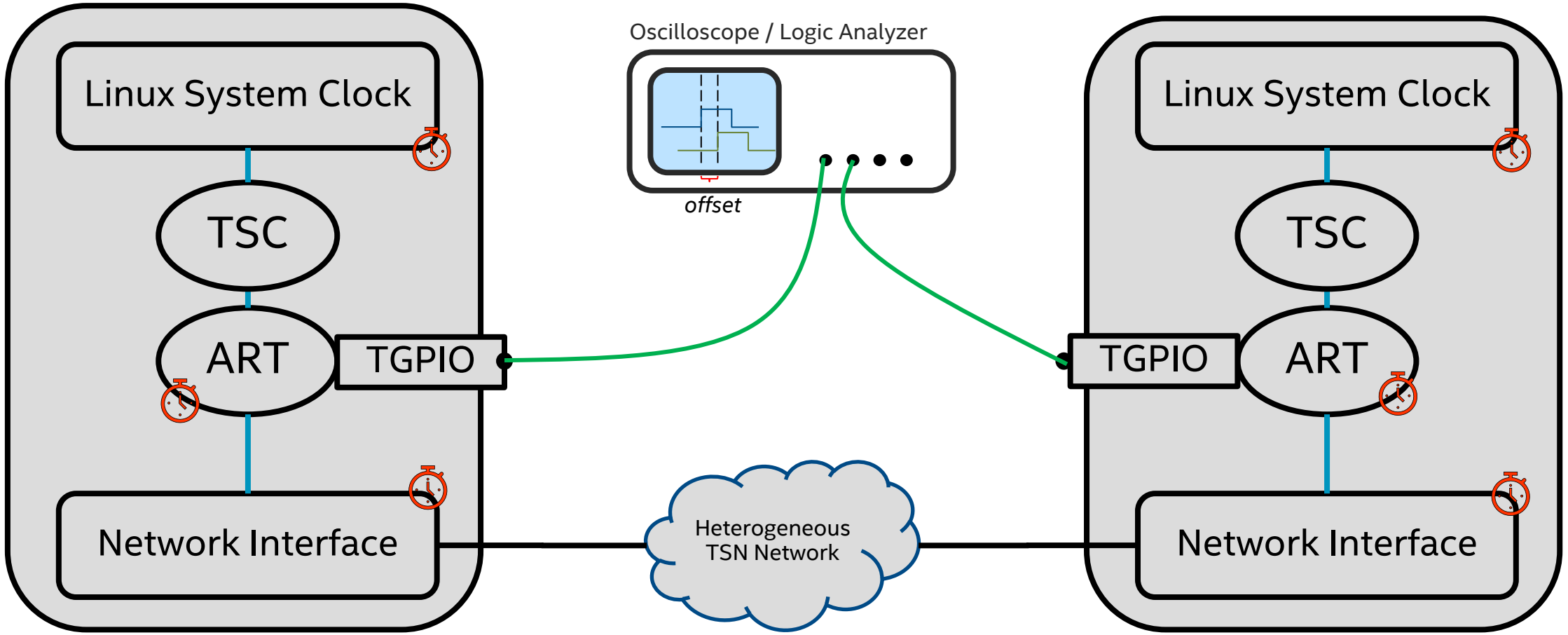


We developed a representative testbed and time synchronization measurement methodology

Hardware Overview

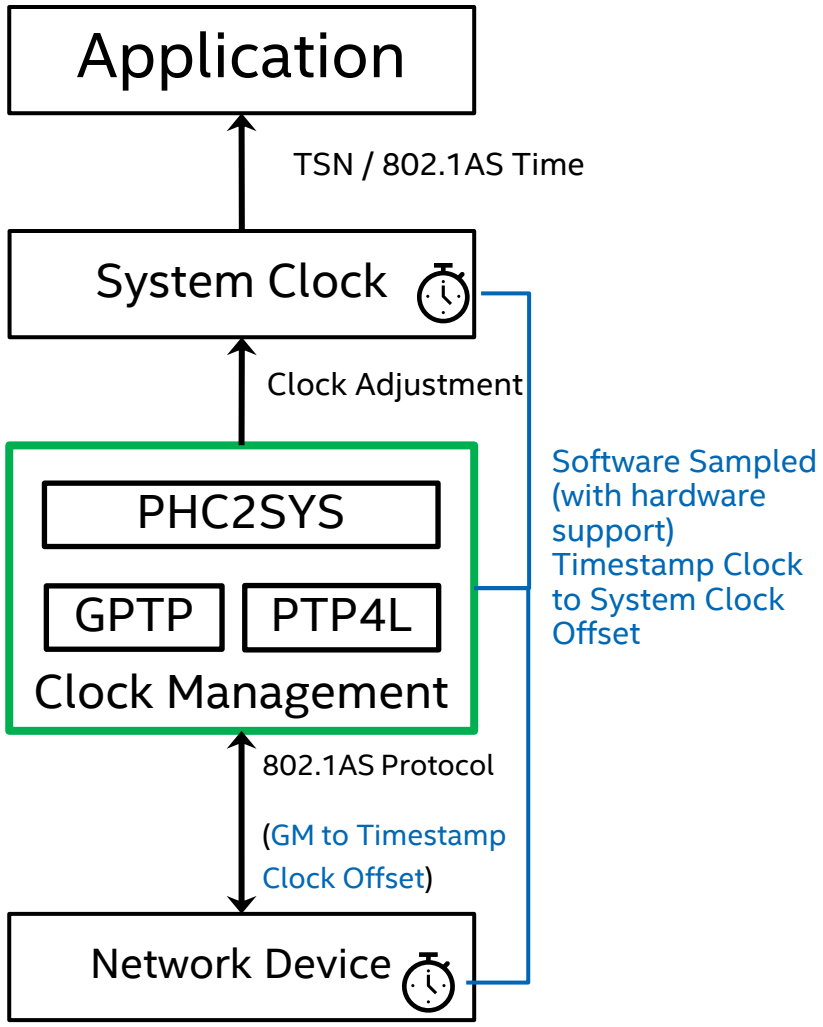
The ART (platform) clock is used to relate the network interface timestamp clock with the system clock using hardware cross-timestamp

The Time-Aware GPIO (TGPIO) output is triggered in hardware by the Always Running Timer (ART)



The ART clock provides a common timebase for all supported (e.g PCIe, integrated NICs) devices connected to the platform. Clock management software uses the hardware cross-timestamp to relate clocks on the platform.

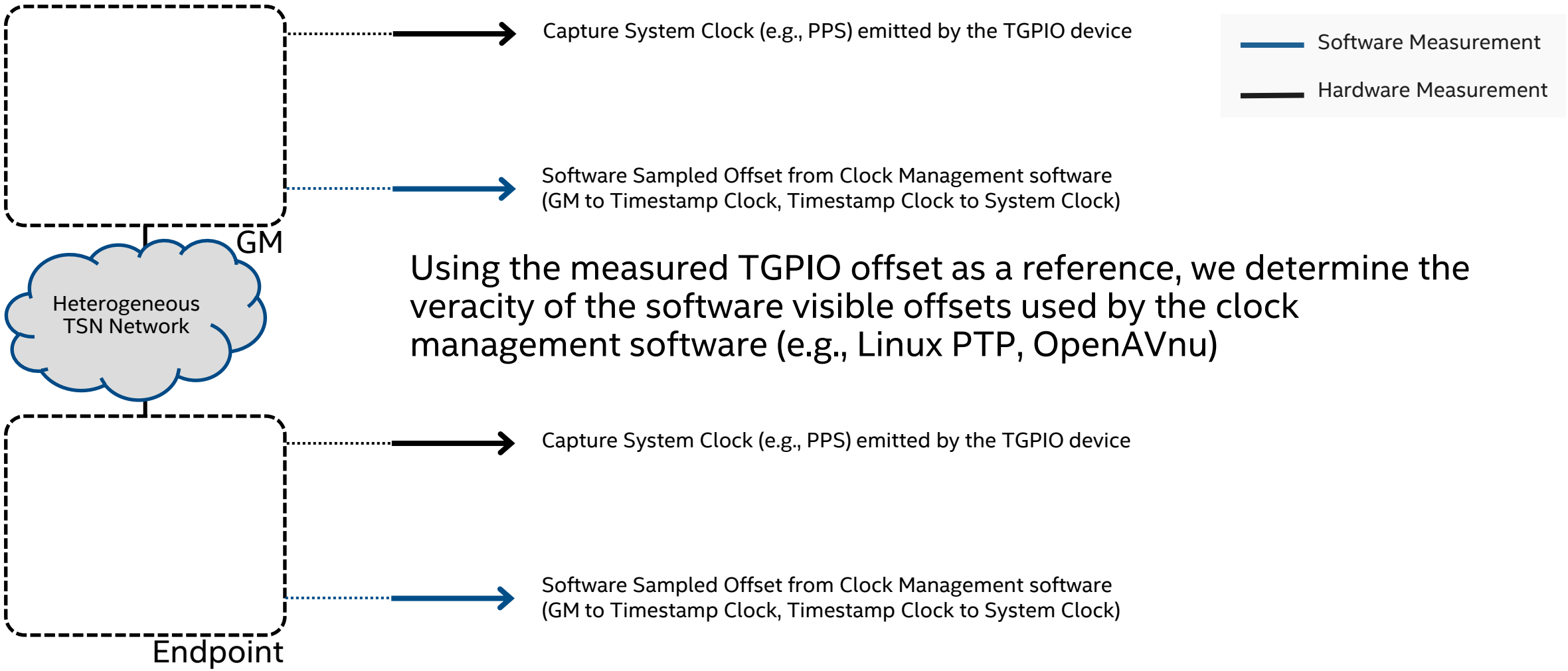
Time Synchronization Software Overview



- On Ethernet links, the clock management software components are the PTP4L and PHC2SYS utilities provided by Linux PTP
- For WiFi media, the clock management software components are the OpenAvnu time sync daemon and PHC2SYS (Linux PTP)

The Clock Management software component replicates the GM clock locally using the 802.1AS-derived GM to network clock offset and the intra-platform cross-timestamp

Measurement Methodology



Using the measured TGPIO offset as a reference, we determine the veracity of the software visible offsets used by the clock management software (e.g., Linux PTP, OpenAVnu)

We concurrently capture the software derived offsets and hardware-based system clock output (e.g., PPS) using a common timebase

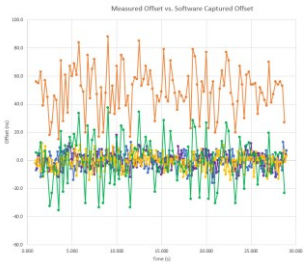
Measurement Scenarios

We measure each the time synchronization performance of each media separately combine them for the end-to-end measurement.

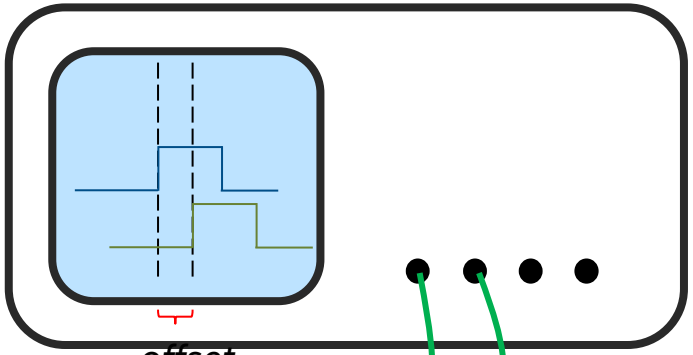
- Ethernet only
- Wi-Fi Only
- Wi-Fi and Ethernet (End-to-End)

Ethernet-Only Measurement

We simultaneously capture the software derived offsets and hardware-based system clock output (e.g., PPS) using a common time base. The data is presented on the following two slides



Oscilloscope / Logic Analyzer



Follower

TGPIO

System Clock

PHC2SYS

PHC (Timestamp Clock)

NIC

PTP4L

Logger

GM

TGPIO

PHC2SYS

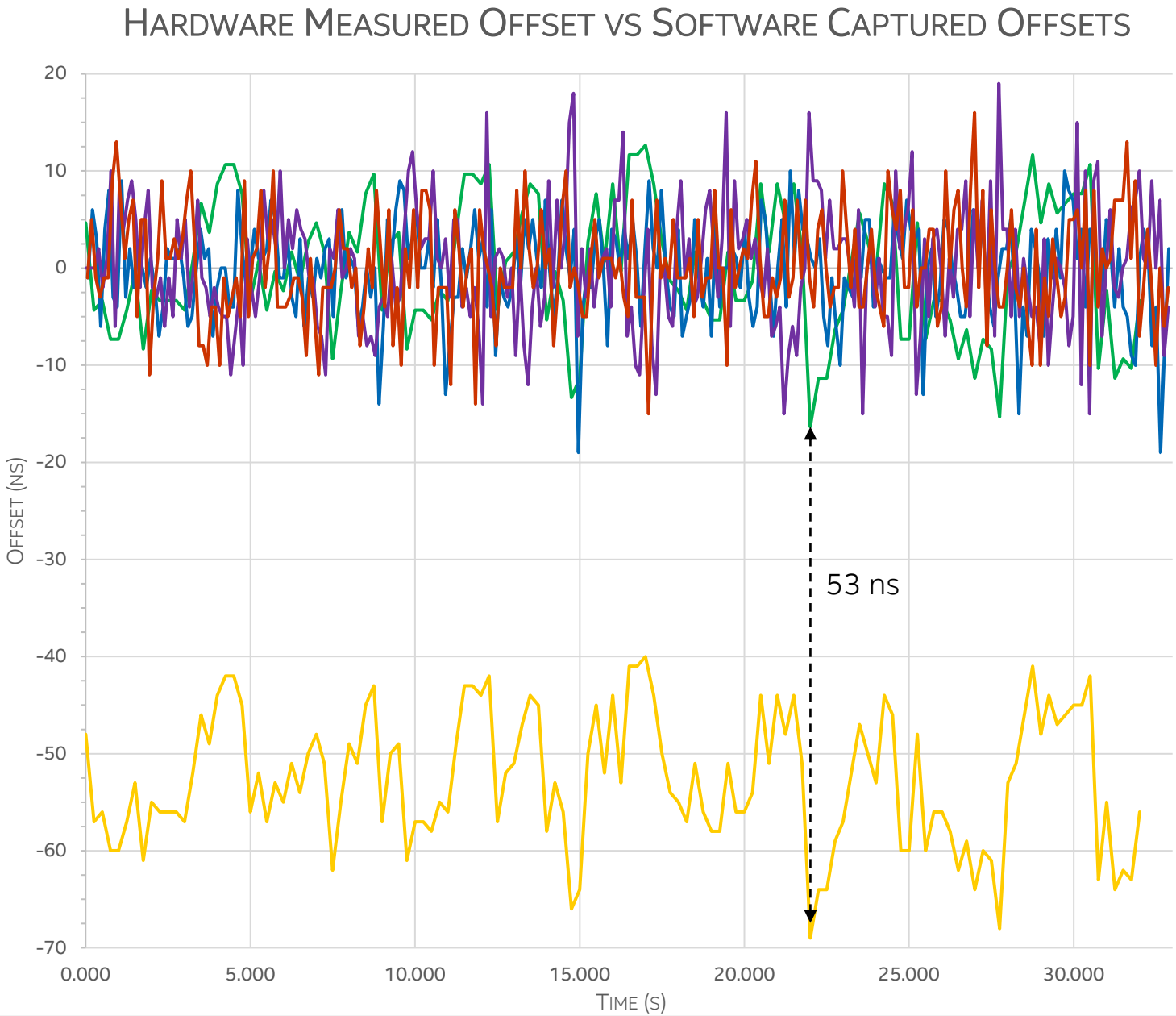
System Clock

PHC (Timestamp Clock)

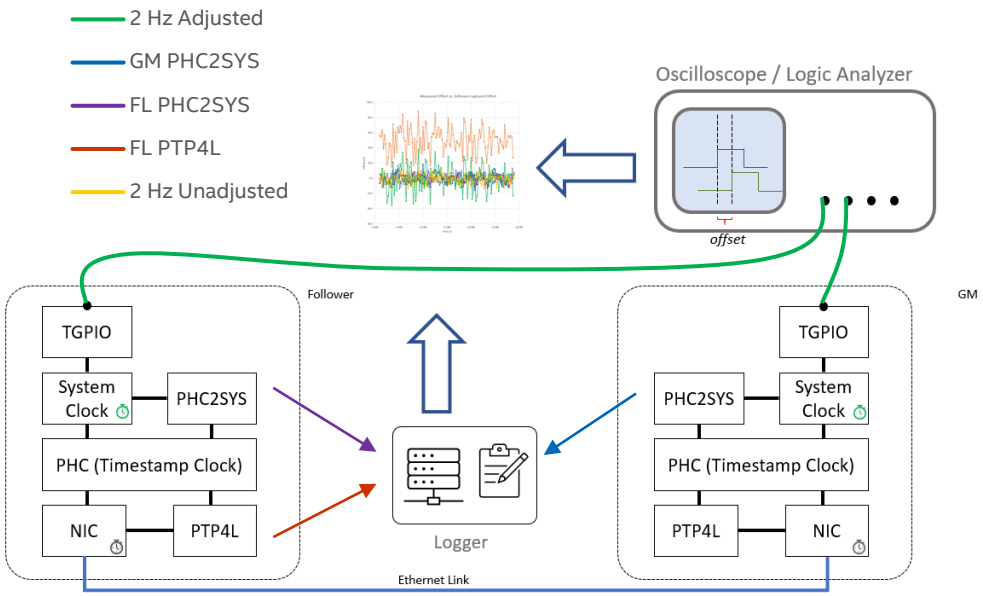
PTP4L

NIC

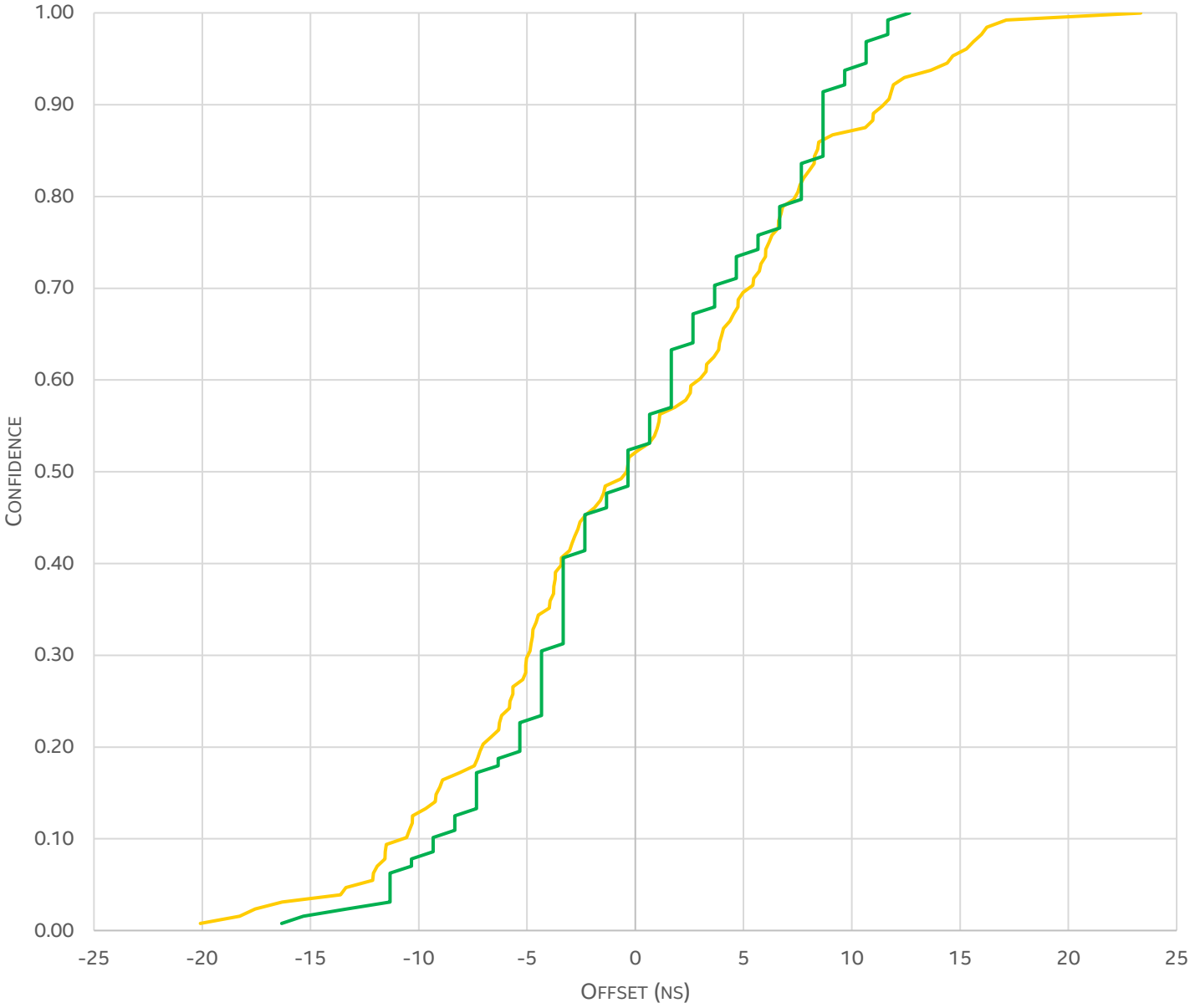
Ethernet Link



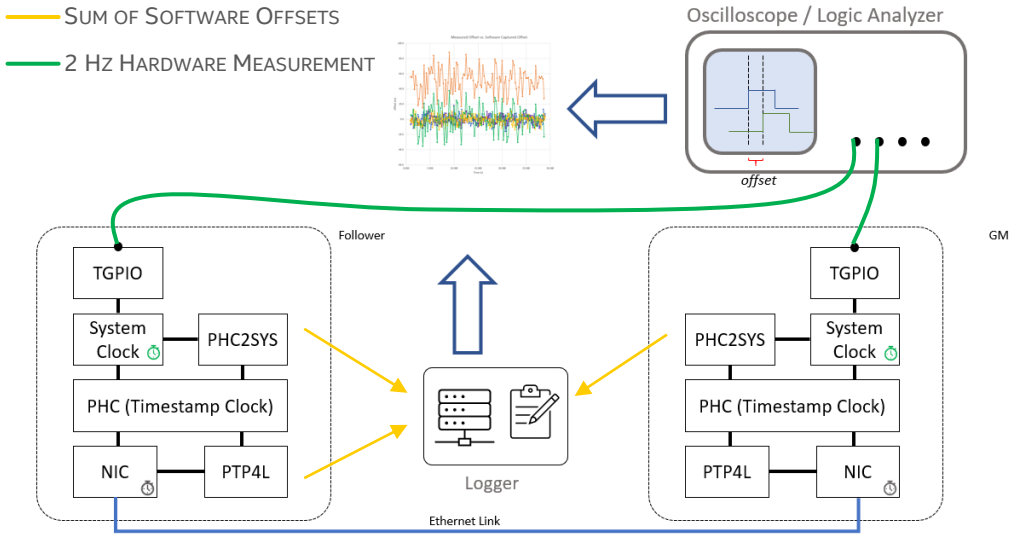
- We concurrently captured the software derived offsets and measured the hardware offsets generating a time series plot
- There is a bias due to PTP path asymmetry that isn't software visible. We adjust the hardware measured timestamps to compensate for this and the TGPIO scheduling error.
- Next, we see how well the software derived and hardware measured offsets agree



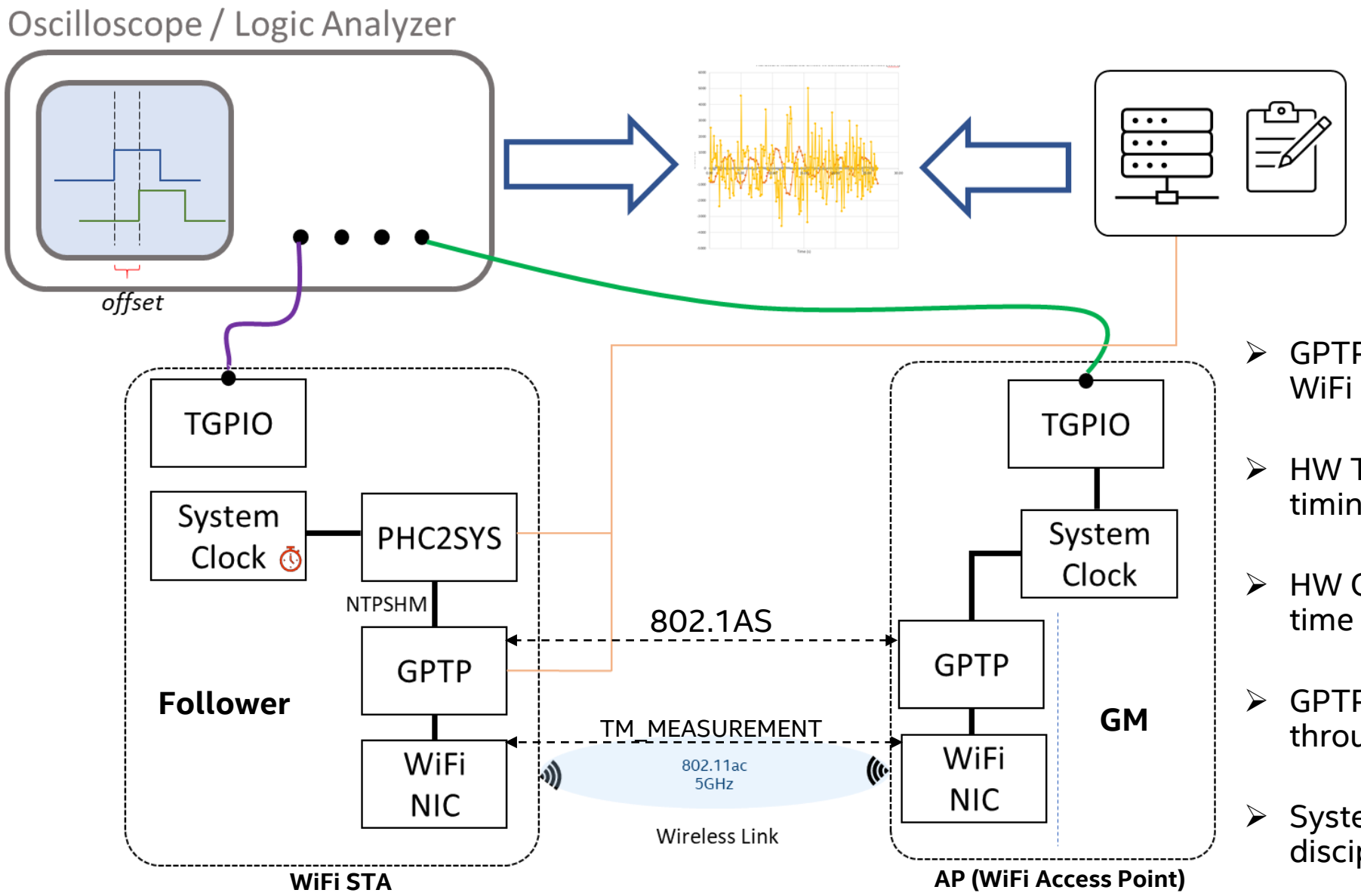
CDF: Sum of SW Derived Offsets vs 2Hz Hardware Offset Measurement



- 85%+ of the hardware measured offsets are within 20 ns (+/- 10) of the GM clock
- 74%+ of the software measured offset are within 20 ns (+/- 10) of the GM clock
- The hardware measured offsets exhibit less variance than the software measured offsets due to filtering and the PI controller
- **88%+ of the software measured offsets and within 4 ns of the hardware measured offsets**

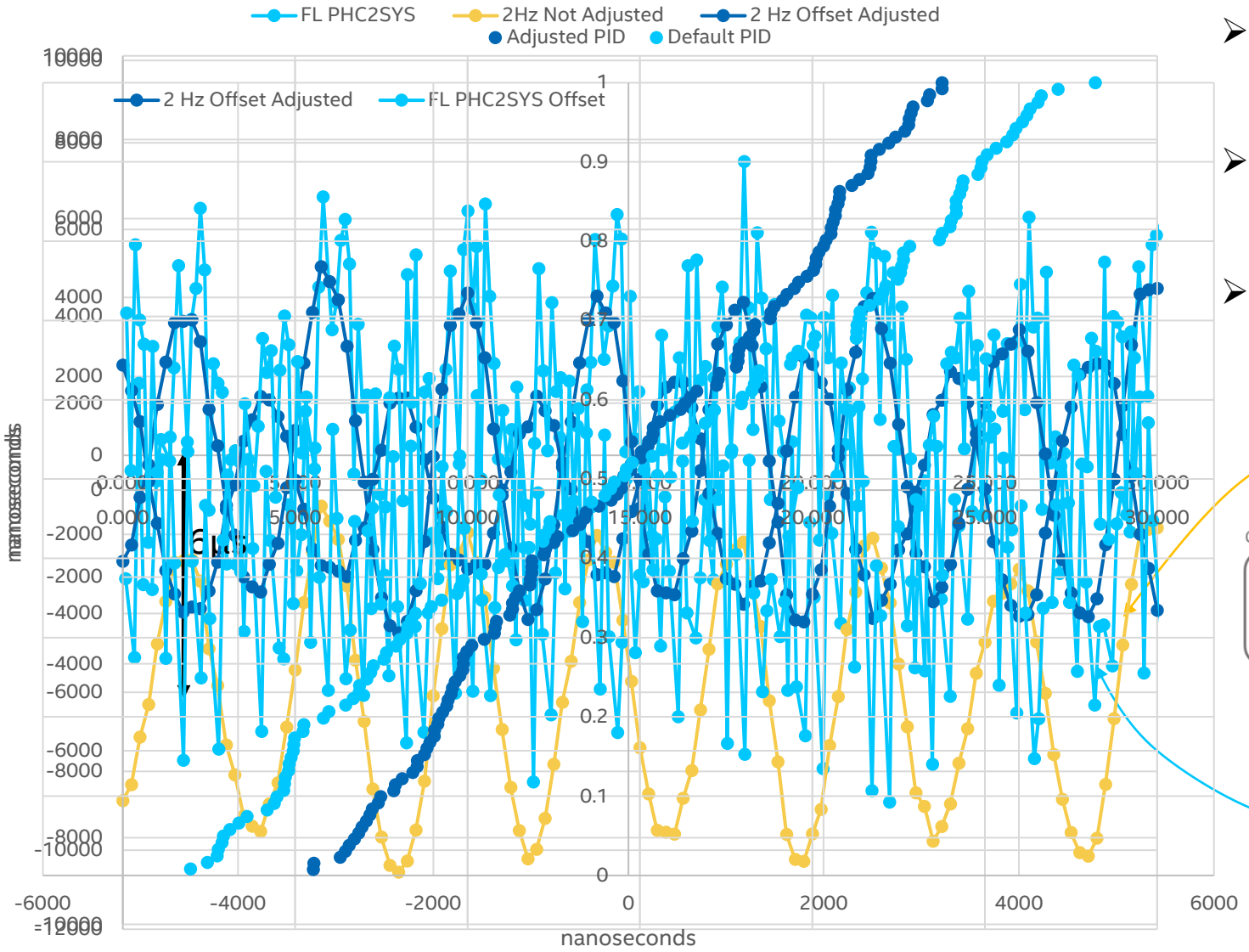


MEASUREMENT : WIRELESS (WIFI) - SETUP

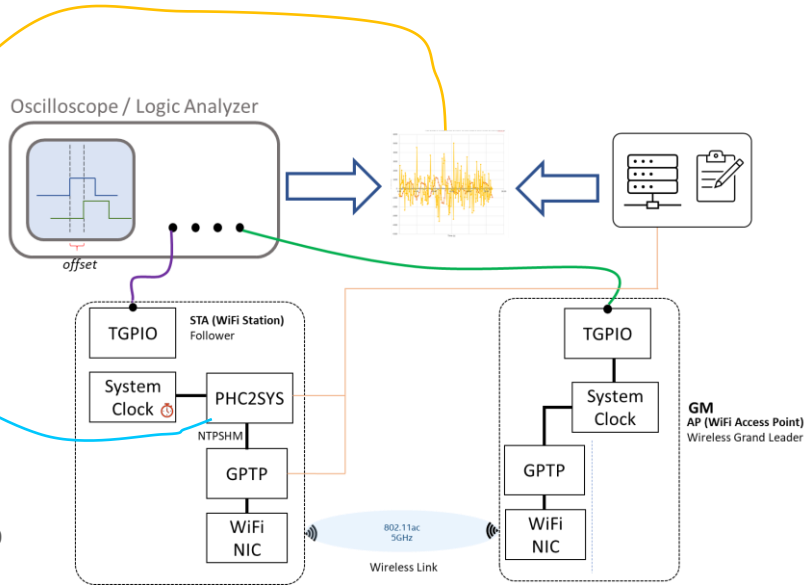


- GPTP Implementing 802.1AS over WiFi
- HW Timestamping of 802.11 timing measurement frames
- HW Cross Timestamp maps device time to system time
- GPTP to PHC2SYS interface through NTPSHM
- System clock at Follower disciplined by PHC2SYS

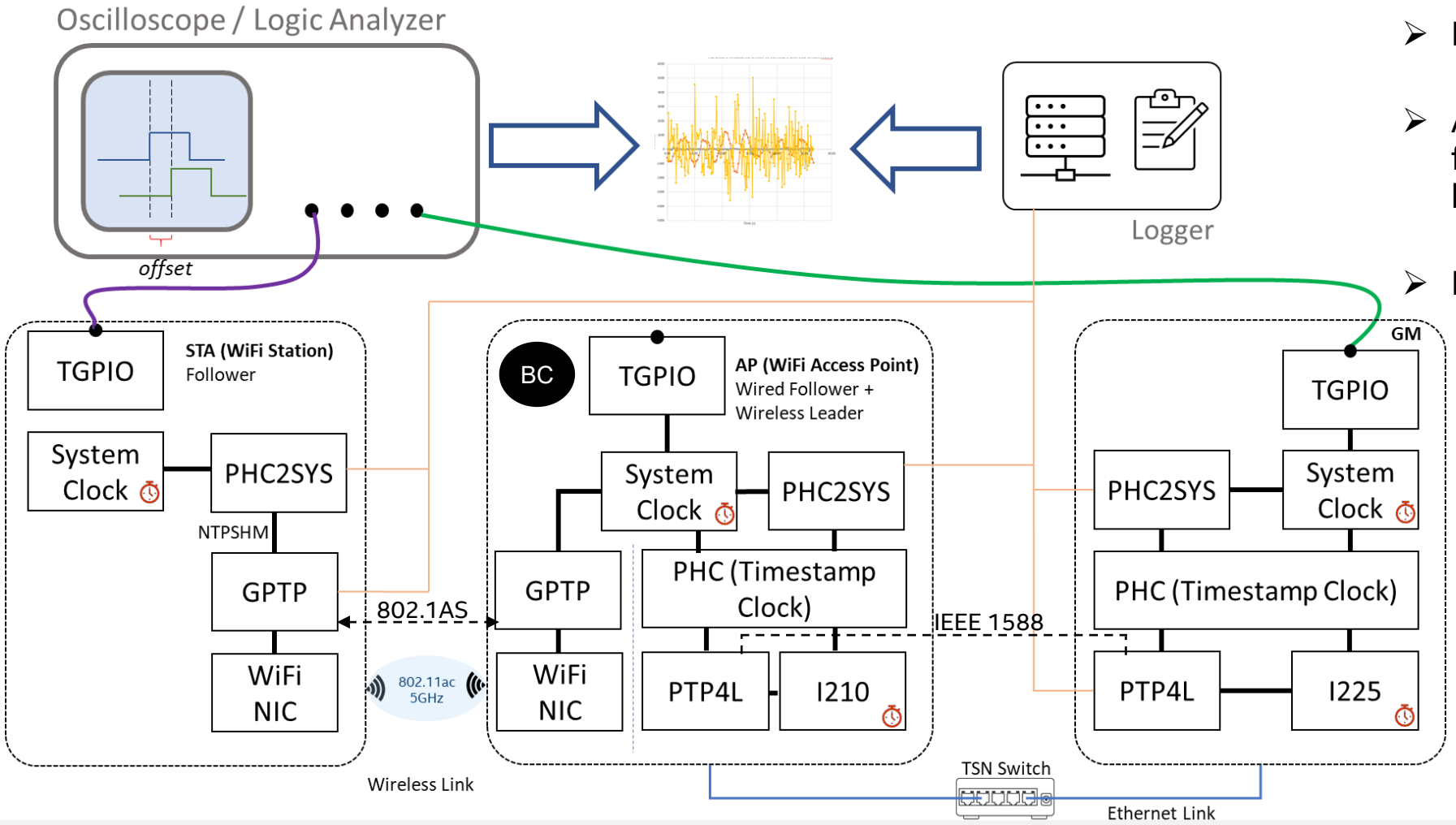
MEASUREMENT : WIRELESS (WIFI) - RESULTS



- Any bias due to path asymmetry can be detected and removed as a calibration step
- PID tuning can be used to reduce the effect of transient variations in perceived software offsets
- 90% of end-to-end time synch error achieved is within +/-2us

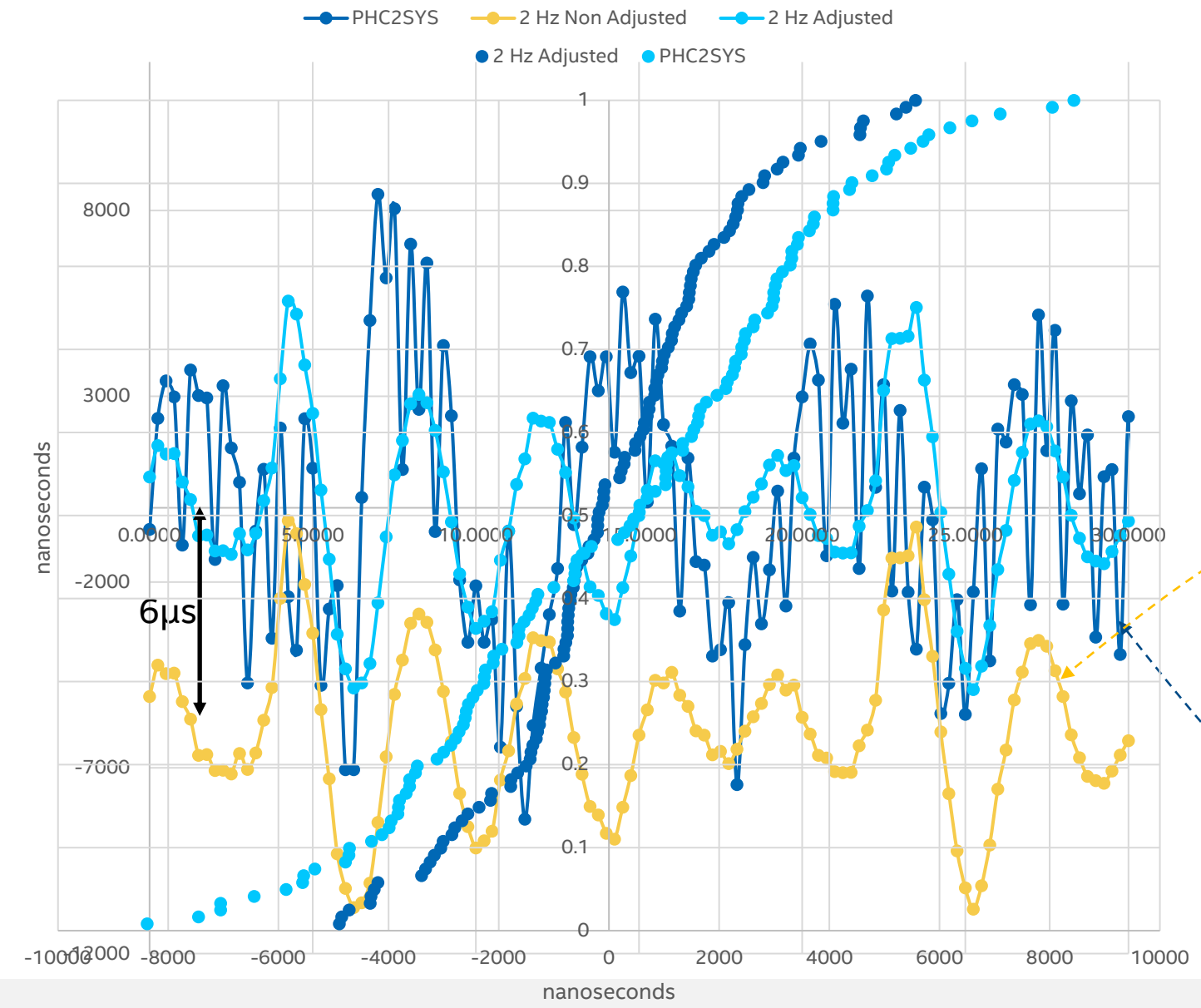


MEASUREMENT : END-TO-END (WIRED + WIRELESS) - SETUP

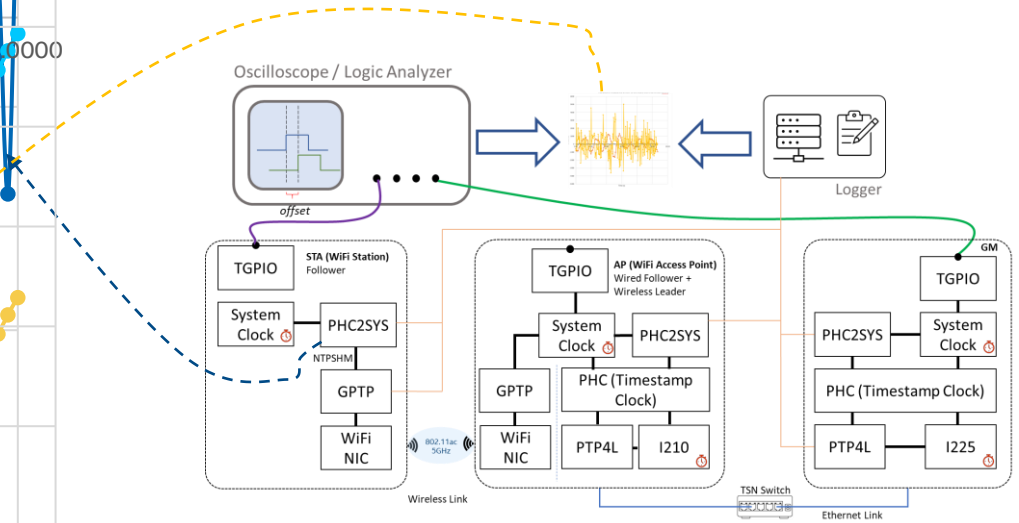


- TSN Switch bridges wired node to wireless segment
- IEEE1588 between GM and AP
- AP implements a Boundary Clock function using System Clock as a bridge
- IEEE 802.1AS from AP to STA/s

MEASUREMENT : END-TO-END (WIRED + WIRELESS) - RESULTS



- Constant bias from WiFi is still present and can be removed as part of calibration.
- PID tuning can be used to reduce the effect of transient variations in perceived software offsets
- 90% of offsets between system times is within +/-2.5µ



Conclusion

- Hardware-triggered output PPS based on CPU-Time provides ground truth for end-to-end synchronization (system-clock to system-clock)
- Hardware Time-Aware GPIO PPS measurements demonstrate the veracity software derived offsets
- Heterogeneous (Ethernet and Wi-Fi) end-to-end single-domain 802.1AS time synchronization achieves the expected accuracy given:
- Current Wi-Fi timestamp accuracy: 1 µs (end-to-end 2 µs)
- Hardware cross-timestamp allows system clock to act as accurate time-aware (Ethernet-to-Wi-Fi) relay

Next Steps

- Extend test bed with 5G network segment
- Perform measurements with Wi-Fi Fine Timing Measurement (FTM)
- Add frequency perturbation to GM simulating environments where heat or voltage variations affect the oscillator frequency
- Extend testbed and measurements to incorporate more network paths
- Add multiple PTP domains to the test bed, implementing multi-path and/or multiple GM redundancy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