Image Processing Application Implemented Using Xilinx System Generator

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ABSTRACT

This paper discusses about the new concept of image processing using Xilinx system generator which is embedded in MATLAB® named SIMULINK. Recent advances in synthesis tools for SIMULINK suggest a feasible high-level approach to algorithm implementation for embedded DSP systems. The top model - based visual development process of SIMULINK facilitates host side simulation and validation, as well as synthesis of target specific code, furthermore, legacy code written in MATLAB or ANCI C can be reused in custom blocks. However, the code generated for DSP platforms is often not very efficient. It is discussed that Image processing application can be easily made and they can be implemented on VLSI targeted board.

Keywords: Digital Image Processing, Matlab, Xilinx System Generator, simulink, model based design

I. INTRODUCTION

The handling of digital images has become in recent decades a subject of widespread interest in different areas such as medical and technological application, among others. We may cite lots of examples where image processing helps to analyze infer and make decision. The main objective of image processing is to improve the quality of the images for human interpretation or the perception of the machines independent of the images for human interpretation or the perception of the machines independently. This paper focuses in the processing pixel to pixel of an image and in the modification of pixel neighbourhoods and of course the transformation can be applied to the whole image or only a partial region. The need to process the image in real time, leading to the implementation level hardware, which offers parallelism, thus significantly reduces the processing time, which was why decided to use Xilinx System Generator, a tool with graphical interface under the Matlab/Simulink based blocks which makes it very easy to handle with respect to other software for hardware description. And design based on simulink tool is called model, so it is very efficient way to create model based design. In addition to offering all the tools for easy graphical simulation level. This article presents architecture of image processing application generator, which is an extension of Simulink and consists of a bookstore called “Blocks Xilinx”, which are mapped architectures, entities, signs, ports and attributes, which script file to produce synthesis in FPGAs, HDL simulation and development tools. The tool retains the hierarchy of Simulink when it is converted into VHDL.

II. XILINX SYSTEM GENERATOR

Xilinx System Generator (XSG) is an integrator design environment (IDE) for FPGAs, which uses Simulink, as a development environment and is presented in the form of block set. It has an integrated design flow, to move directly to the configuration file (*.bit) necessary for programming the FPGA. One of the most important features of Xilinx System Generator is possessed abstraction arithmetic, which is working with representation in fixed point with a precision arbitrary, including quantization and overflow. You can also perform simulation both as a fixed point double precision. XSG automatically generates VHDL code and a draft of the ISE model being developed. Make hierarchical VHDL synthesis, expansion and mapping hardware, in addition to generating a user constraint file (UCF), simulation and test bench and test vectors among other things. Xilinx System Generator was created primarily to deal with complex Digital signal processing (DSP) applications, but it has other application like the theme of this work. The blocks in Xilinx System Generator operate with Boolean values or arbitrary values in fixed point, for a better approach to hardware implementation. In contrast Simulink works with numbers of double-precision floating point. The connection between blocks, Xilinx system generator and Simulink Blocks are gateway blocks In figure 1 shows the broad flow design Xilinx System Generator. As already mentioned, you can then move to the configuration file to program the FPGA.

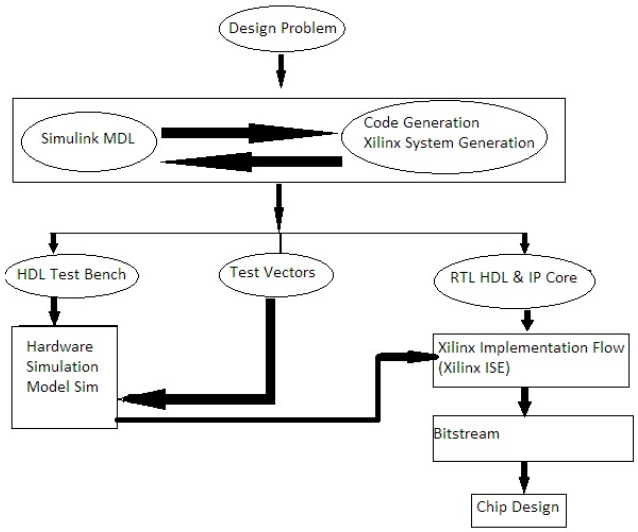


Figure 1 Design flow in Xilinx System Generator

III BASIC MODEL BASED DESIGN

Edge detection is the process of identifying sharp changes in image brightness [1]. This is important because it detects physical changes in the objects imaged. The image formation process in many applications such as seismology, photography, radar, microscopy and ultrasound is such that changes in acquired image brightness can relate to severe changes in depth or distance, discontinuities in surface orientation, changes in material properties, variation on scene illumination and boundaries of an object this identifying edge can lead to better image understanding while reducing data volume for more efficient subsequent processing [2].

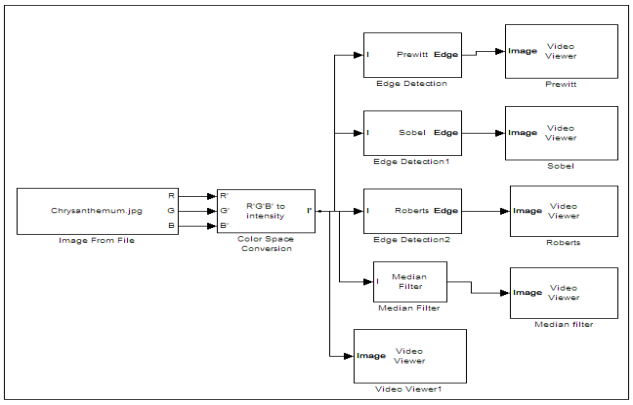
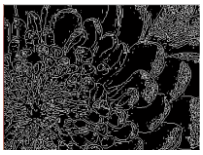


Figure 2. Model Based Edge Detection of Image

A. RESULTS

Figure A Original Image Figure B Original Image



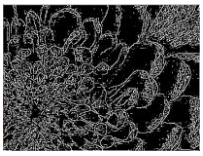
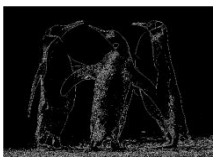
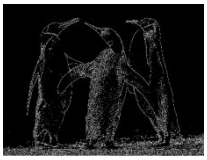


Figure A1 Prewitt Figure A2 Robert Figure A3 Sobel





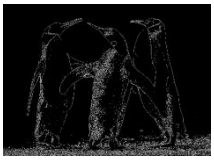


Figure B1 Prewitt Figure B2 Robert Figure C3 Sobel

IV READING IMAGE AND PROCESSING IN XILINX SYSTEM GENERATOR

A. READING IMAGE

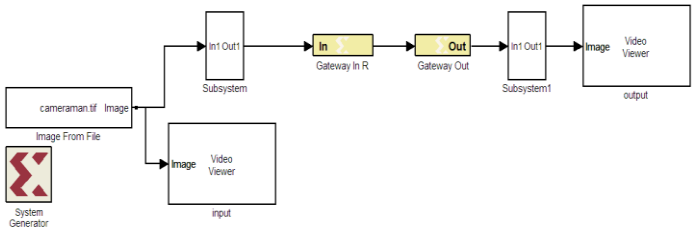
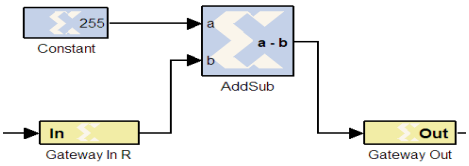


Figure 3. Image Reading in XSG

B. GRAY SCALE IMAGE NEGATIVE



Input image Output Image Negative

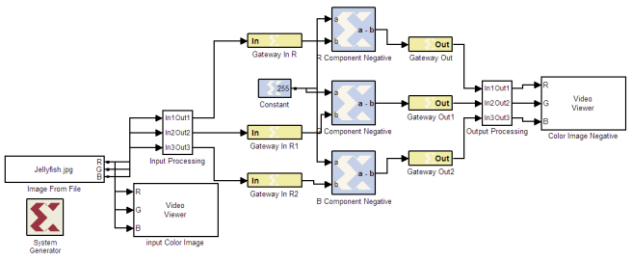
Figure 4 Gray scale Image Negative

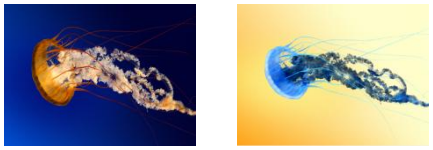
C. COLOR IMAGE RGB EXTRACT

Input Image

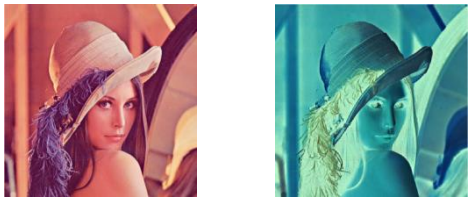
R Component G Component B Component

D. COLOR IMAGE NEGATIVE





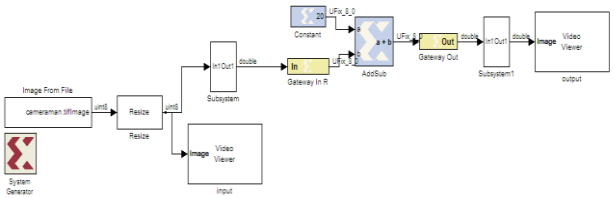
Input Image Output Image



Input Image Output Image

Figure 5 Color Image Negative

D. IMAGE ENHANCEMENT



Input Image Output Image

Figure 6 Color Image Negative

Section A represent how image is read from the directory and processed in simulink. All the image processing is done between FPGA boundaries gateway in and gateway out. Image read is in Simulink is basic block for reading the image from the directory and gateway out the image output as per the block specified under Xilinx FPGA boundaries. Section B represents how gray scale image is inverted using simple block insertion which reflect image negative at output side, note that the block required to calculate negative is connected within the FPGA Gateway IN/OUT boundaries. Section C shows the color image can be extracted in to its R-G-B components. Section D represents the required block to calculate color image negative, each color component is treated as individual signal and individual image negative blocks required to make all component negative and output of each is given to the R-G-B video viewer. The result is shown in figure 5 for two input test images. In addition to this in section D it is shown that how image can be enhanced by adding a constant to each pixel values [3,4] Image filtering can also be done using model based design different filtering architecture can be defined and Xilinx block can be created [6].

V FUTURE WORK

Our future work is oriented for multimedia authentication system using digital watermarking, in which we are going to apply the combination of DCT, DWT,SVD using simulink. We will test all these possibilities and compare with each other. By doing this we can achieve the advantage of both DCT, DWT and SVD. Than the simulink (.mdl) file will be converted to

(.hdl) using XSG and this authentication system will be implemented on one of the VLSI targeted board.[5]

VI CONCLUSION

The Xilinx System Generator tool is a new application in image processing, and offers a friendly environment design for the processing, because processing units are designed by blocks. This tool support software simulation,but the most important is that can synthesize in FPGAs hardware, with the parallelism, robust and speed, this features are essentials in image processing.

In this paper we have presented the basic idea how image processing can be done in model based approach, we have demonstrated some of the image processing application which is done under SIMULINK and this can be implement using Xilinx System Generator (XSG). In this paper we have shown how image can be read, image edge detectors, image enhancement, gray scale color image negative, R-G-B component extraction from color image and color image negative very efficiently and we have taken two test images for the color image negative to give better idea.

VII REFERENCES

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