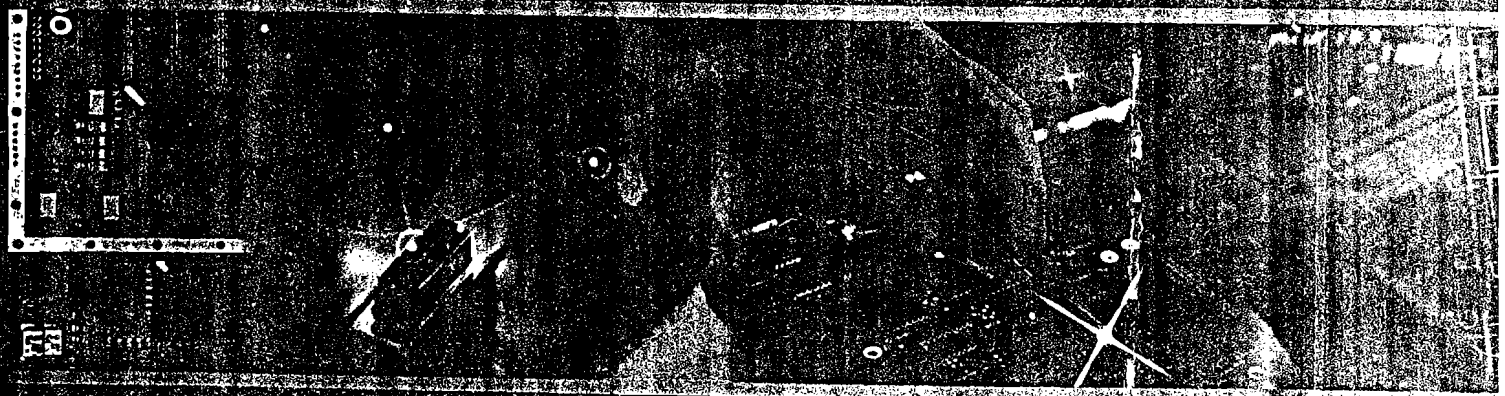
International Conference

On

"Emerging Techniques in Electronics, Computing Embedded System & VLSI Design in ICEVD - 08"



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Design of Switch-Capacitor Regulator for System on Chip Applications

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Abstract

Switch-Cap Regulators are available as discrete devices and are used for obtaining higher efficiency when compared to the low-efficiency linear regulators. In this paper, we present a Switch-Cap Regulator specifically designed for System on Chip applications. The designed regulator should meet some stringent requirements to be able to be incorporated in System on Chip , some of them being able to limit the startup current to a safe value and obey the EMC requirements of electrical devices.

Subject Areas
Low power VLSI design
Nanotechnology

Design of Switch-Capacitor Regulator for System on Chip Applications

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Abstract:

Switch-Cap Regulators are available as discrete devices and are used for obtaining higher efficiency when compared to the low-efficiency linear regulators. In this paper, we present a Switch-Cap Regulator specifically designed for System on Chip applications. The designed regulator should meet some stringent requirements to be able to be incorporated in System on Chip , some of them being able to limit the startup current to a safe value and obey the EMC requirements of electrical devices.

1. Introduction

The need of voltage regulators is indispensable. In the near distance past, linear power converters were the mainstay of power conversion and voltage regulation. Switching power converters were still an unexplored technology mainly consigned to low-volume, high-cost, commercial or military applications. These advances have allowed power converters to increase their electrical and thermal performance while decreasing their size and cost by utilizing switching power conversion techniques.

Both types of regulators, however, have their benefits and problems. The advantages of using linear regulators are low parts count, excellent regulation characteristics, low output noise, no generated EMI and excellent transient response. The disadvantages include single outputs, no "step-up" designs, low power density and poor efficiency. Switching voltage regulators exploit the energy storage characteristics of passive magnetic and capacitive circuit elements. Unlike the linear regulator, whose pass element continuously transfers energy from the input voltage source to the load, the switching regulator takes discrete packets of energy from the input voltage source. It temporarily stores the energy as a magnetic field in an inductor or as an electric field in a capacitor and then transfers the energy to the load.

There are both advantages and disadvantages of using switched capacitor techniques rather than inductor-based switching regulators. First advantage is the elimination of the inductor and the related magnetic design issues. Second advantage is that, converters typically have relatively low noise and minimal radiated EMI. Application circuits are simple, and only two or three external capacitors are required. Because there is no need for an inductor, the final PCB component height can be made smaller than a comparable switching regulator. This is important in many applications such as display panels.

Switch-Cap Regulators have the problem of very high start-up a current, that flow to charge the external capacitors, exists. Switch-Cap Regulators as discrete devices can still tolerate these currents as they are external to a system. However in an SoC application, such high currents can be detrimental to the entire system. So the designed Switch-Cap Regulator should have a mechanism to limit the start-up current to a safe value.

For a regulator to be designed on chip, it is necessary that it obey the EMC requirement of the electrical devices i.e. it doesn't interfere with the normal functioning of other neighboring blocks. So certain design and layout requirements should exist for such regulators. Another very important thing for a block in an SoC is low inductive noise. The inductive coupling is directly related to the rate of change of current through the inductor, that in-turn would depend upon the switching speed. So in order to have low inductive noise, the slew of the switching clocks should be low enough. This asks for a higher delay in the clock edges to make them non-overlapping.

2. Basic Architecture and Operation

Shown in the Figure 1, above is the block diagram of the Switched-Cap Regulator circuit designed in 0.18μ technology. The Regulator is designed to provide a constant voltage of 1.8V with a maximum load of 200mA. It also

- Amplitude
- Edge Rate
- Duty Cycle
- Edge Discontinuity
- Ringing

For above mentioned reasons the clock transitions are kept very slow so that the current rises slowly and the spike generated is lesser in amplitude and frequency components. Under typical conditions the Clock Frequency is 250KHz with a rise/fall time of 100ns. An estimate of Frequency spectrum generated in the SC regulator can be done for this clock frequency. The fundamental frequency would be 250KHz with cutoff frequency of f_{cutoff} 3.5MHz which is well below the 30MHz mark.

Also from Antenna Theory we can estimate about the loop length required to transmit the Electromagnetic waves, e.g. to transmit EMI at a frequency of 30MHz, the loop length required is 5 meters. Such high antenna lengths are very impractical in design and can be taken care by multiple connections and decoupling. The Conducted Noise can be minimized by proper layout having good guard rings and ground shields.

3.2. Startup Current considerations

If the switching action of the switched-cap regulator were to start from the very beginning when all the nodes are uncharged, then in the first clock cycle only when the switch S1 is ON, a huge amount of current of the order of 5 Amperes can flow through the PMOS S1 and into the entire matrix. Such high currents can be harmful for the entire chip as they can even result in the burning of the supply rails due to electro-migration and heating effect, and should be thus avoided in an SoC. For that very purpose, a BYPASS MOS has been used in the circuit which charges all the intermediate nodes in the switchcap matrix with a limited amount of current prior to the actual switching action, with switches S2 and S3 in ON state and S1 and S4 in OFF state. Now when the switching begins, all the nodes are previously charged to some potential resulting in lower startup currents.

3.3. Load internal to an SoC

For a load internal to an SoC i.e. if the load current of 200mA (max.) has to be drawn by a block inside the chip, then it need a separate pad for the same as already discussed and shown in Figure 2. The output has to be redirected to the input through this extra pad. Shown below in Figures 3 and 4 are the two ways in which the internal load can be supplied by the designed Regulator. Here Iload represents the Internal load. In Figure 3, Iload is supplied by the Regulator in one cycle and by the tank cap C2 in the next cycle. So in Pad1 inductor, the current keeps on changing resulting in undesirable spikes in the voltage across Iload. Whereas with the scheme used in Figure 4, the voltage across Iload will not exhibit spikes because the current through the Pad2 inductor will always flow irrespective of the clock sequence. In this way the scheme used in Figure 4 becomes indispensable for an SoC.

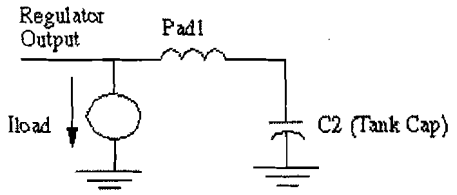

Figure 3. Internal Load without an extra Pad

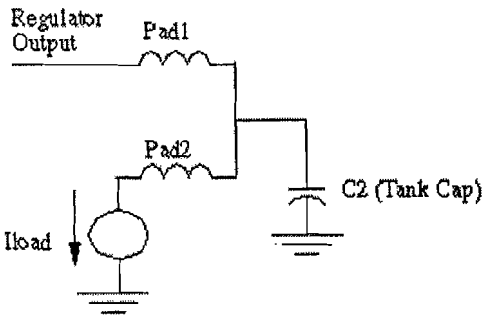

Figure 4. Internal Load with an extra Pad

4. Design

4.1. Oscillator

The oscillator is a simple ring oscillator. Also instead of ring oscillator, a back-to-back combination of NOR gates can be used for faster convergence. The first stage decides the frequency of the oscillator because it is this stage that introduces the delay in the loop with the help of current and capacitance controlled delay. The current is obtained from the bandgap reference. The oscillator is oscillate at 4 MHz so that the capacitance value required is reduced and hence the area. The clock obtained at 4MHz can then be suitably divided by 16 to give a clock oscillating at a frequency of 250 KHz. Figure 5 shows the basic architecture of the oscillator designed.

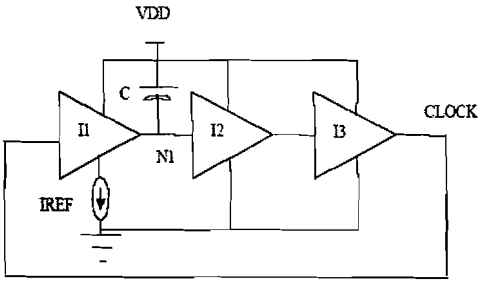

Figure 5. Design of Oscillator

The counter following the oscillator is a conventional 4-bit asynchronous counter whose final output will be oscillating at a frequency 1/16 times that of the input clock.

4.2. Clock Generator

This block generates non-overlapping clocks from a single clock. It is obtained by delaying the original clock and performing a NAND operation between the original and the delayed version shown in Figure 6. The non-overlapping time to be 0.1μs. So we would actually need a delay element of 0.2μs. Clock C and Clock D shown in Figure 6 are non-overlapping clocks separated by 0.1μs. Such a huge amount of delay cannot be achieved using simple inverter chains. The structure of the delay element is shown in Figure 7. Here most of the delay is again in the first stage. Both the R and the C of the first RC circuit are increased by introducing MOS switches with high lengths and capacitances respectively. The advantage of introducing the high L-MOSes lies in reducing the area consumption significantly for the same delay that would otherwise have been attained with much higher capacitances.

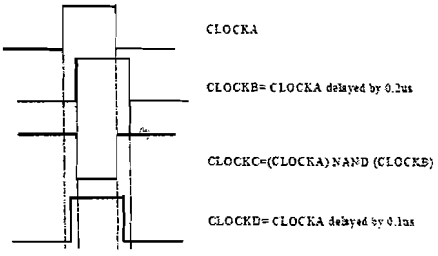

Figure 6. Generation of Non-Overlapping Clocks

4.3. Delay_5u

This block is used to prevent the flow of very high currents in the switches during the startup of the bandgap and thus again very important for an SoC. What actually happens is that due to the overshoot in the bandgap voltage the resistance of the switches is reduced drastically resulting in very high currents through the switches of the order of 1-2A, due to the comparator action. In order to avoid this, the bandgap voltage should have settled to its steady state value when the switching action begins. For this the Power-up of the bandgap should actually come nearly 5μs (settling time of the bandgap voltage) before the Power-up of rest of the circuit. So in effect we had to delay the Power-up of the rest of the circuit by nearly 5μs in order to prevent the flow of very high currents through the switches. This was achieved by this delay circuit. The circuit again has most of the delay in the first stage only (Figure 8). The consequent stages are used for smoothing operation. Here also an RC circuit is made. A very high R is introduced by a very high L-PMOS only. No similar NMOS is used because the delay is needed only in the falling edge of the Power-down signal.

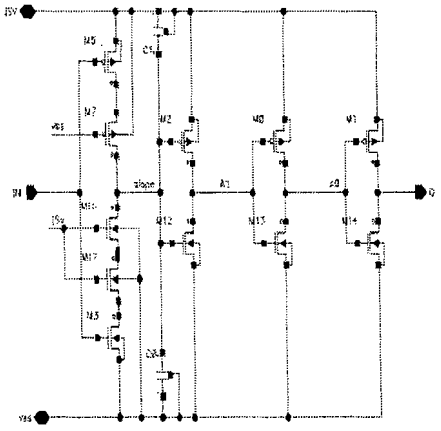

Figure 7. Clock Generator Delay

4.4. Power On Reset

The startup of the switch-cap regulator is very crucial. In the unfortunate event of the startup failing, very high startup currents of the order of 5A can flow in the switch matrix that can be detrimental for the chip due to electromigration.

To prevent this, a bypass MOS that would provide a charging current within the safe limits till the nodes have settled to close to their final value. But for the detection of startup, we would need a Power on Reset circuit that would give us a one shot pulse as soon as the supply is switched on. This one shot pulse would be used to turn ON the

bypass MOS with the help of suitable logic. So here lies the utility of the POR circuit. Figure 9 shows the POR outputs as the supply is varied.

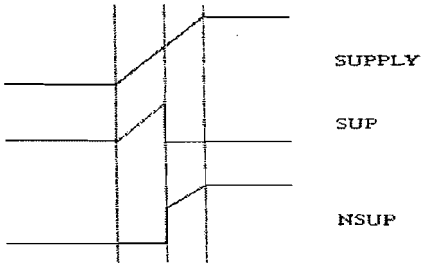

Figure 9. Power on Reset Outputs

4.5. Startup logic

With the help of SUP and NSUP signals the STARTUP signal is turned ON, when the supply is turned ON. This STARTUP signal is then passed to the BYPASS node as shown in Figure 10, which forms the gate of the bypass MOS. After this the startup mode begins where the switches S2 and S3 are turned ON, whereas S1 and S4 are turned OFF and the bypass MOS of a smaller limited size starts charging all the nodes of the switch cap matrix almost linearly, so that when the switching action takes place for the first time, the matrix is not subjected to very high startup currents. This startup mode continues till the time the output voltage increases to 1.8V, after which the STARTUP signal becomes 0, thereby switching OFF the bypass MOS, and turning ON the oscillator, counter and the clock generator for the normal switching operation of the circuit.

An important design aspect here is that although the PWRGD signal becomes available after the output has reached 1.75V, yet the startup is not finished because at this point the resistance of the switches controlled by the feedback is very low and hence if switching were to start at this point, the non-uniformity of clocks in the beginning can result in the flow of very huge short circuit currents, although momentarily. So it's better to wait for some more time during which the output voltage further rises and the switch resistance increases, resulting in relatively smaller short circuit currents in the beginning. Once the normal operation has begun, the startup will again begin, once the output voltage falls below 1.65V i.e. the PWRGD signal falls to 0 and the startup mode will continue again till the output has reached 1.8V.

4.6. Feedback Amplifier

To compare the output and the bandgap voltage, a class AB amplifier is used to provide a rail-to-rail output with good output swing capability. The output of this amplifier is used to control the resistances of two of the switches and provide regulation. This output acts as the supply for the drivers driving those two switches. That is why the quiescent current of the second stage is kept to be very high of the order of 400∝A to enable faster responses.

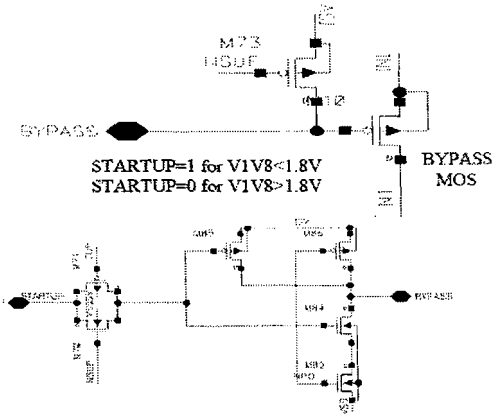

Figure 10. Logic used in startup block

The differential amplifier is a P-DIFF amplifier owing to its lower input offset voltage compared to the N-DIFF, when used in this configuration, because here we have an offset voltage corresponding to the second mirroring action also. Moreover the stability of this amplifier is not an issue here as it is used in an open loop configuration. So it's the complete loop that should be stable and not necessarily this amplifier. Figure 11 shows the circuit of the class AB amplifier used.

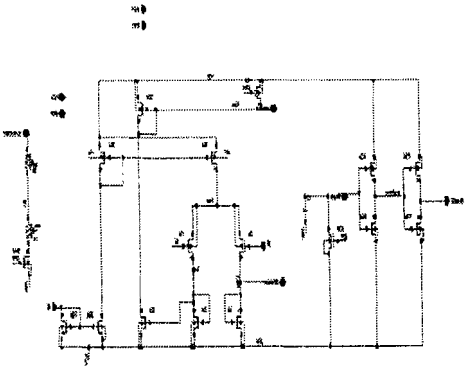

Figure 11. Feedback Amplifier