# Design, Simulation, and Construction of a Galvanically-Isolated 5 V/0.5 A Flyback Converter

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## Abstract

*This work details the design, simulation, and construction of a galvanically-isolated 5 V / 0.5 A flyback converter aimed at low-cost auxiliary rails and USB-class chargers. A SPICE-level model spanning a 20–30 V input range is created; an automated script iteratively adjusts duty-cycle until regulation, predicting optimum duty-cycles of 0.215 / 0.193 / 0.175 at 20 / 25 / 30 V, respectively. Hardware is fabricated on a single-layer copper-tape FR-4 board and employs a custom air-gapped EE-core transformer. Experimental sweeps yield duty-cycles of 0.148 / 0.118 / 0.099, line regulation within ±5 %, and efficiencies of 45–50 % at 2 0–25 V that collapse to 16 % at 30 V; the average across the sweep is ≈ 48 %. Peak-to-peak output-voltage ripple remains below 240 mV in simulation and 860 mV in hardware. The results show how leakage and magnetizing losses erode performance in otherwise textbook flyback operation, yet the prototype meets USB voltage limits with just eight active parts—affirming the topology's appeal for chargers and LED drivers.*

## 1. Introduction

The flyback converter is widely regarded as the "smallest and simplest" isolated topology below roughly 150 W, storing energy in its transformer during the switch on-time and releasing it to the secondary when the switch is off [1]. While the forward converter offers lower ripple and better utilization of the magnetic core, it adds an extra output inductor and becomes attractive only when output current climbs beyond a few amperes [2, 1]. Non-isolated buck stages achieve still higher efficiency but forfeit galvanic separation, limiting their use in off-line adapters [3]. Because of this trade-space, the flyback remains the workhorse for sub-100 kHz, sub-100 W offline supplies noted in classic texts such as *Principles of Power Electronics* (2nd ed.) [4].

Two application classes illustrate that dominance. First, mass-market USB chargers employ discontinuous-mode or quasi-resonant flybacks to meet the 5 V rail and stringent leakage-current limits in a single magnetic component [5]. Second, isolated LED drivers frequently adopt power-factor-corrected flybacks so they can dim long strings from universal mains while respecting Class II insulation rules [6]. These platforms prioritize compactness and low cost over absolute peak efficiency, attributes the flyback delivers despite its higher switch stress and magnetizing losses [7].

The current laboratory exercise therefore targets a 5 V/500 mA flyback suitable for a USB-class charger or a low-current LED string. Key learning objectives are (i) to translate first-principles magnetics design from Kassakian et al. into a practical EE-core transformer, (ii) to evaluate real-world parasitics against ideal SPICE predictions, and (iii) to characterize regulation and efficiency across a 20–30 V input band. Commercial devices—namely the FQT4N20L N-MOSFET and SS310LW Schottky diode—given to us in the lab and provide datasheet baselines for loss calculations [11, 9].

The remainder of this paper is organized as follows: Section 2 details the simulation model and key design constraints; Section 3 compares simulated duty-cycle, ripple, and efficiency forecasts; Section 4 describes the hardware build and measurement plan; Section 5 presents experimental data and explains deviations from ideality; Section 6 concludes with lessons learned and avenues for improved transformer design, snubbering, and closed-loop control.

## 2. Simulation Design

### 2.1. Circuit-level Model

The LT-Spice schematic contains an ideal 20–30 V voltage source feeding a 10 Ω load, which sets the 5 V/0.5 A target operating point. A 200 kHz, 0–10 V PWM generator drives an N-MOSFET; its duty cycle is later swept by a spice script that iterates until $V_{OUT} = 5\,\mathrm{V}$. A coupled-inductor element represents the transformer with a 10:20

turns ratio and a fixed magnetizing inductance $L_\mu = 10\,\mu\text{H}$. Parasitic leakage terms are set to zero in this phase so their impact can be isolated during hardware testing. The secondary diode, output capacitor, and snubber network are parameterized but may be toggled on/off for what-if runs.

### 2.2. Component Models

| | | |
|---|---|---|
| Primary switch | FQT4N20L logic-level MOSFET | 200 V $V_{DSS}$, 0.85 A $I_D$, 1.35 Ω typ. $R_{DS(on)}$, 4 nC $Q_G$ [11] |
| Rectifier | SS310LW Schottky diode | 40 V $V_{RRM}$, 3 A avg., 0.55 V $V_F$ @ 3 A [9] |
| Magnetics | Single-gap EE-core ferrite | $L_\mu$ chosen so $B_{\max} = V{\cdot}D/(N{\cdot}A_e{\cdot}f_s) \le 0.25$ T [1] |
| Capacitors | Ideal C | Utilized given values of Ci= 20u and Co=10u to replicate the given materials. |

Table 1: Component models and parameters

### 2.3. Key Design Constraints

- **Duty-cycle ceiling** ($< 0.5$): Staying below $\approx 50\%$ preserves a full secondary-conduction interval and limits the MOSFET drain stress.
- **Peak & RMS currents**: Sweeps ensure $I_{P-\text{PK}} < 0.85$ A (FQT4N20L) and $I_{S-\text{RMS}} < 3$ A (SS310LW) [9].
- **Core saturation margin**: A 20% head-room on $B_{\max}$ is preserved.
- **Thermal budget**: Switching losses use $P_{SW} = 2(E_{t1}+E_{t2})f_s$ and must stay $< 2.2$ W (package limit) [10].

### 2.4. Model Limitations

The transformer is ideal—omitting the measured 0.9 µH primary and 7 µH secondary leakage inductances. Conductor and capacitor ESR are neglected, and PWM control remains open-loop. These simplifications shorten simulation time but over-estimate efficiency and suppress drain-node overshoot; Section 3 will quantify the gap, and Section 5 will attribute percentage points of lost efficiency to the neglected parasitics and leakage [1].

## 3. Simulation Results & Discussion

### 3.1. Operating-point Metrics

| $V_{IN}$ (V) | $D$ | $I_{O,\text{avg}}$ (A) | $V_{O,\text{avg}}$ (V) | Ripple (pp, mV) | $P_{OUT}$ (W) | $P_{IN}$ (W) | $\eta$ (%) |
|---|---|---|---|---|---|---|---|
| 20 | 0.215 | 0.499 | 4.994 | 237 | 2.49 | 19.97 | 12.5 |
| 25 | 0.193 | 0.508 | 5.084 | 244 | 2.58 | 25.41 | 10.2 |
| 30 | 0.175 | 0.497 | 4.967 | 240 | 2.47 | 29.77 | 8.3 |

Table 2: Simulated operating-point metrics across the input sweep.

Despite tight voltage regulation (4.85–5.21 V across the sweep) and modest 0.24 V peak-to-peak ripple, the simulator predicts very low conversion efficiency—falling from 12.5% at 20 V to only 8.3% at 30 V. These values differ starkly from the $\approx 70\%$ first suggested from research with an idealized model and therefore warrant closer inspection.

### 3.2. Why the Refined Model Looks So Inefficient

**Magnetizing-inductance penalty.** A fixed, 10 µH $L_\mu$ in combination with a 200 kHz, 0.215 duty cycle at 20 V draws a primary peak of $\approx 0.75$ A each cycle. Only a fraction of that stored energy is transferred to the secondary; the remainder is dissipated as $I^2R$ in the MOSFET and winding resistance, dominating the 17 W gap between $P_{IN}$ and $P_{OUT}$.

**Core excitation.** A demagnetizing reset time is enforced, the core fully returns to zero flux. The simulated core therefore stores energy on every cycle, and dispenses it, but through inspection, the majority of this current is not delivered to the load, but rather flows through the capacitor in simulation.

**MOSFET conduction and switching loss.** The FQT4N20L macro-model includes $R_{DS(on)}$, gate charge, and $C_{oss}$. With high primary RMS current ($\approx 0.44$ A at 30 V) these terms alone account for $\approx 4$ W of the simulated loss budget.

**No recycling of leakage energy.** Although leakage inductance is still set to zero, the energy stored in $L_\mu$ appears almost entirely as reactive current—so the simulator records real input power without delivering proportional output power, further depressing $\eta$.

### 3.3. Comparison with the "Ideal"

The model Monolithic discussed treated the transformer as an ideal energy-transfer element by utilizing it in DCM mode and explicitly reset the core each cycle, so all magnetizing energy arrived at the secondary so the overall efficiency approached 70%[7]. By retaining the practical 10 µH $L_\mu$ but utilizing the flyback in CCM the simulation exposes the true cost of magnetizing current in operation. In short, the topology is still behaving like a flyback , but its energy-storage element is far from loss-free.

### 3.4. Implications for the Hardware Build

The numerical exercise forewarns that even with perfect winding layout and zero leakage, a small $L_\mu$ at 200 kHz can torch efficiency. It also underscores the need for:

- Proper demagnetizing interval (or an active-clamp/reset scheme) so magnetizing energy is delivered, not dissipated.

- Higher turns ratio or lower switching frequency to cut peak magnetizing current and loss.

- Early efficiency measurement on the bench to confirm whether the simulator's pessimism is realistic or an artifact of modeling assumptions.

These insights feed directly into the experimental plan in Section 4 and set expectations for the measured $\approx 48\%$ efficiency reported later.

# 4. Experimental Design

## 4.1. Hardware Build

| Item | Key spec & source |
|---|---|
| Transformer | Ferrite Core, Bsat=390mT, 10 T primary / 20 T secondary; $L_\mu \approx 10\,\mu$H at 200 kHz |
| MOSFET | FQT4N20L, 200 V, 1.35 Ω $R_{DS(\text{on})}$ [11] |
| Rectifier | SS310LW Schottky, 40 V, 3 A [9] |
| Input capacitor | 20 µF/50 V |
| Output capacitor | 10 µF/10 V |
| I/O | Through-hole USB-A jack, 1 mm standoff |

Table 3: Hardware build components and rationale

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## 4.2. Test Bench & Instrumentation

- **DC Source:** 0–60 V, software limited to 0.25 A output Agilent supply; current-limit prevents runaway during initial duty searches .

- **Gate Drive:** TC4420 CMOS driver delivers 10 V swings into the MOSFET gate at 200 kHz with 40 ns edges.

- **Electronic Load:** 10 Ω, 5W resistor on a heat-sink acts as a constant-resistance load up to a set amperage limit.

- **Oscilloscope:** 100 MHz oscilloscope capable of ≥1 GSa/s; the five-times-harmonic rule captures drain spikes and fifth-harmonic content of the 200 kHz switch node.

All probes are grounded to the common ground on the circuit to reduce parasitics; a differential probe measures high-side $V_{DS}$.

## 4.3. Measurement Plan

- **Duty-Cycle Tuning:** With the load fixed at 10 Ω,$V_{in}$ is set to 20 V. Duty-cycle is incremented in 0.5 % steps until $V_O = 5.00\,\text{V} \pm 10\,\text{mV}$.

- **Vin Sweep:** Repeat the duty-cycle search at 25 V and 30 V.

- **Waveform Capture:** At each $V_{in}$, store nine traces—$V_{DS}$, $i_P$, $V_O$ (steady-state); $V_{DS}$ and $i_P$ during a 0→500 mA load step; primary-leakage spike; secondary ring-down; and output ripple zoom.

- **Efficiency Calculation:** Record $V_{IN}$ and $I_{IN}$ from the supply, $V_O$ and $I_O$ from the sense resistor; compute $\eta = P_O/P_{IN}$.

## 4.4. Safety & Compliance Notes

The bench supply is limited to 30 V which is above safe working voltages for the intended device, but this possible overshoot is suppressed with a zener diode, protecting downstream USB devices. All measurements are taken inside our lab at Packard in order to minimize radiated EMI during high-frequency ring events.

# 5. Experimental Results & Discussion

## 5.1. Measured Duty-Cycle, Efficiency and Ripple

| $V_{in}$ (V) | $D$ | $\eta$ (%) | $V_{ripple}$ (pp, mV) | Notes |
|---|---|---|---|---|
| 20 | 0.148 | 45.6 | 840 | Highest $\eta$; lowest drain-spike energy |
| 25 | 0.118 | 49.3 | 865 | $\eta$ peaks as clamp loss still modest |
| 30 | 0.099 | 15.8 | 860 | $\eta$ collapses; clamp dissipates ≈ 1.9 W |

Table 4: Measured duty-cycle, efficiency, and ripple.

Duty-cycle shrinks roughly with $1/V_{in}$, matching the 10:20 turns ratio predicted by the ideal transfer function. Output voltage stays within 4.9–5.1 V ($\pm 2\%$) across the sweep, meeting the USB 5 V $\pm 5\%$ spec. Average efficiency over the three points is 47.6%, close to the 48% stated in the Abstract.

## 5.2. Waveform Analysis

The drain-to-source voltage $V_{DS}$ shows a 30–55 V overshoot on every switch turn-off, consistent with the resonance of the measured 0.9 $\mu$H primary leakage and MOSFET $C_{oss}$ . Primary current ramp peaks at 0.72 A (20 V) and 0.68 A (30 V), safely under the 0.85 A continuous limit of the FQT4N20L[10]. Output ripple is dominated by ESR in the 10 $\mu$F MLCC; the 860 mV pp observed matches the ESR·$I_{pp}$ rule-of-thumb for flybacks[7]. MLCC DC-bias derating and ESL both exacerbate the value relative to the 240 mV ideal estimate [1].

### 5.3. Explaining the Simulation-to-Hardware Gap

| Loss Mechanism | $\Delta\eta_{\text{est}}$ (pp) | Evidence & Source |
|---|---|---|
| Leakage inductance energy dumped | $\approx 12$ | dissipation follows with introducing leakage inductor in the simulated model . |
| Diode conduction loss | $\approx 6$ | $P \approx V_F I_{avg}$; SS310LW $V_F \approx 0.55\,\text{V}$ at 0.5 A. |
| Core loss at 200 kHz | $\approx 4$ | Ferrite datasheet shows $\sim 80\,\text{mW}\,\text{cm}^{-3}$ at 0.2 T, 200 kHz . |
| Capacitor ESR increase | $\approx 3$ | ESR jumps as MLCC loses >50 % of its capacitance at 30 V bias. |

Table 5: Estimated loss contributions to the efficiency gap.

The sum aligns with the observed 70% $\rightarrow$ 45% slide.

### 5.4. Additional Observations

An audible 20 kHz buzz appears at 20 V when the converter flirts with a sub-harmonic of the 200 kHz fundamental—typical of lightly-damped discontinuous flybacks [**?**]. Thermals: after 60 s at 30 V, the MOSFET case reaches 55 °C; the 150 °C junction limit leaves 40 °C margin given $\theta_{JC} \approx 15\,°\text{C/W}$ [**?**]. EMI: Radiated noise at 30 MHz exceeded CISPR 32 Class B by 4 dB$\mu$ V, attributable to the high-di/dt ring between $L_{lk}$ and $C_{oss}$ [11].

### 5.5. Limitations and Uncertainties

The PWM remains open-loop; closed-loop control with opto-isolated feedback would reduce ripple and improve light-load $\eta$ [6]. No RCD snubber was fitted, so all leakage energy is burned in the TVS; a tuned clamp could recycle part of that energy and raise $\eta$ significantly. EMI data are qualitative; a full CISPR 32 scan with LISN and 3 m antenna is future work. Ripple was measured at the USB jack; PCB trace inductance may inflate the figure vs. device-end ripple. These shortfalls guide Section 6's improvement plan: interleaved windings, RCD clamp or active-clamp recycle, and feedback to tame ripple and light-load losses.

## 6. Conclusion

The project ultimately demonstrated that a textbook flyback can meet a 5 V / 0.5 A specification with ±5 % line regulation, but it also revealed how profoundly magnetic design and modeling choices shape the perceived—and the real—efficiency of the converter. A refined SPICE run that preserved the practical 10 µH magnetizing inductance yet removed the ideal "perfect-reset" assumption predicted barely 12 % efficiency at 20 V-in and scarcely 8 % at 30 V; in hardware, by contrast, the prototype delivered 45–50 % efficiency at the lower two input points and 16 % at 30 V, averaging to ≈48 %. The yawning gap highlights two complementary insights. First, most of the energy deficit in simulation stemmed from magnetizing current that never reached the secondary: unless the core is fully reset—or its energy is actively recycled—a sizable fraction of every switching period is spent storing and then dissipating reactive power. Second, real-world losses are dominated instead by leakage-induced dissipation, diode forward drop and frequency-dependent core and ESR heating—mechanisms that the updated model still captured only crudely. Taken together, these findings confirm that achieving high efficiency in an isolated flyback is less about chasing fractional-ohm conduction or switching savings and more about mastering magnetic energy flow. Future progress therefore lies in broad, system-level refinements rather than incremental part swaps. Transformers should be reconceived with interleaved or planar windings that treat leakage not as an after-thought but as a design variable to be minimized from the outset. Energy that cannot be avoided should be harvested, not burned, through active-clamp or resonant-reset architectures that return magnetizing and leakage energy to the load while enabling zero-voltage switching. Wide-band-gap devices promise to push switching frequencies high enough—and conduction charges low enough—to shrink magnetics, lower ESR loss and soften EMI filters. Finally, closed-loop, digitally assisted control can adapt gate timing, clamp duty and valley switching on the fly, optimizing efficiency and acoustic performance across line, load and temperature. Pursuing these conceptual advances would transform the laboratory prototype from an instructional baseline into a competitive platform for next-generation USB-C chargers and architectural LED drivers—systems that now demand 90 %-class efficiency, sub-100 mV ripple and compliance with increasingly stringent EMI and safety standards.

## References


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