

# CMOS Circuit Design and SPICE Simulation using SKY130 Technology Workshop



## Brief Description of the course:

This is focused towards CMOS circuit design and SPICE simulation using SKY130 technology organized by VLSI System Design. The content of the workshop is divided across the five days in a smart way which allows the learner to grasp all the concepts if the workshop is attended dedicatedly. On the first day of the workshop the emphasis was on the basics of NMOS Drain current ( $I_d$ ), Drain-to-source Voltage ( $V_{ds}$ ) and the plot between the two of them. The second day focuses primarily on velocity saturation and basics of CMOS inverter VTC and the plots between  $I_d$  and  $V_{gs}$  and the plot for determining the value of  $V_t$ . The third was concentrated on CMOS switching threshold and dynamic simulations, where a lot of equations were derived to find the relationships between the (W/L) ratios of the PMOS and NMOS and the switching threshold voltage ( $V_m$ ). On the fourth day of the workshop, Noise margins and CMOS inverter robustness with respect to them was discussed. On the fifth and final day of the workshop the emphasis was on Power supply variation and Device variation. In the power supply variation, the effects of using various power supplies on the inverter were observed and we discussed the advantages and disadvantages of using a small power supply and the reason that it is not used. In the device variation, the impact of manufacturing processes on a single inverter and inverter chain were discussed.

## Tools Covered:

- NGSpice + SKY130 PDK – Open-source SPICE simulator with accurate 130 nm device models.
- NGSpice Built-in Plotter – For waveform visualization.
- VS Code / Vim – Netlist editing with syntax highlighting.
- Bash & Make Scripts – Automating multi-corner sweeps and parameter studies.
- Git & GitHub – Version control, sharing lab results, reproducibility.

## Projects Covered:

1. Design & Characterization of a CMOS Inverter
  - Sizing PMOS/NMOS pairs
  - Generating VTC plots
  - Optimizing switching threshold and rise/fall delays
2. Noise-Margin & Delay Analysis of an Inverter Chain

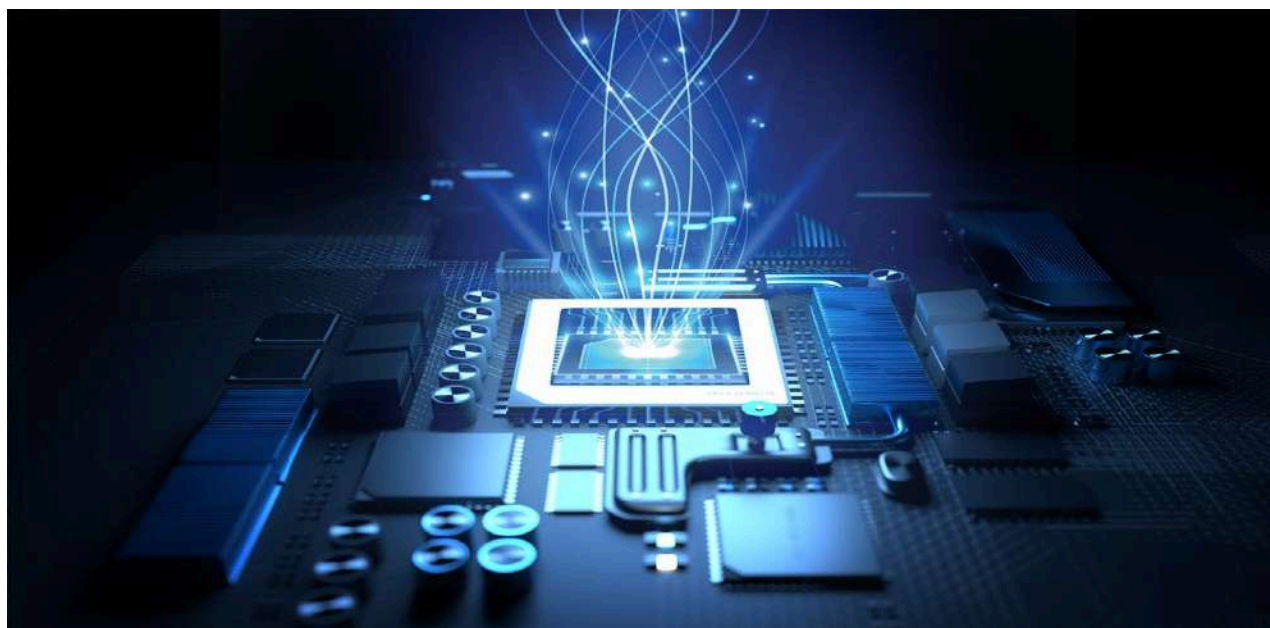
- Evaluating NMH/NML
  - Timing analysis through TT/SS/FF corners
  - Sub-1 V supply sweeps
3. PVT-Aware Low-Power Standard Cell
- Building process-tolerant library cells
  - Parametric sweeps using scripts
  - Documenting guard-band guidelines for tape-out

## What I Learned

- Setting up the SKY130 PDK and NGSpice for CMOS simulations.
- Extracting  $I_d$ - $V_{ds}$  and  $I_d$ - $V_{gs}$  curves, understanding channel-length modulation,  $\mu$ ,  $\lambda$ , and  $C_{ox}$ .
- Designing CMOS inverters and deriving switching-threshold equations.
- Analyzing noise margins (NMH/NML) and robustness under glitches.
- Performing transient simulations to measure rise/fall delays and power consumption.
- Sweeping VDD for low-power design and running PVT corner simulations.
- Using Bash/Make automation for large-scale SPICE sweeps.
- Integrating SPICE-verified designs into OpenLane/VSDFlow for digital implementation.
- Applying learned concepts to create silicon-ready, low-power, robust designs.

# INDEX:

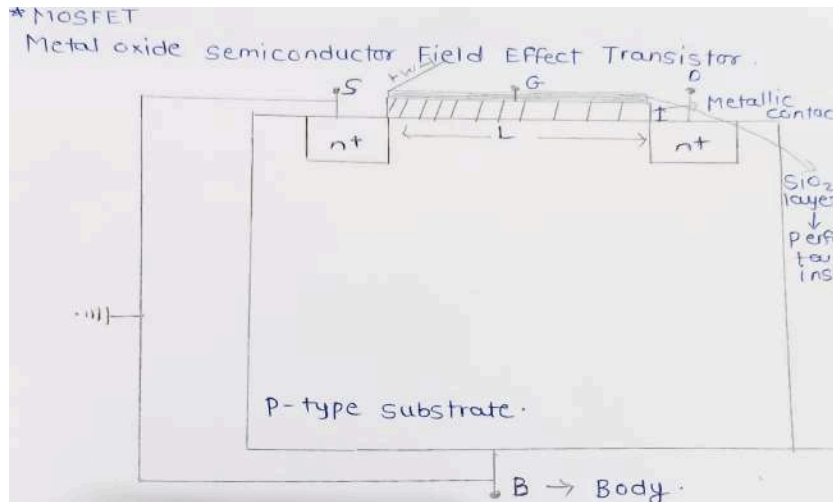
1. Basics of MOSFET
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  - o Depletion Mode
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4. Transconductance  $g_m$  in triode vs saturation
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# MOSFET

Full Form: Metal Oxide Semiconductor Field Effect Transistor

- S: Source
- D: Drain
- G: Gate (metallic contact with  $\text{SiO}_2$  insulation layer)
- B: Body (p-type substrate for n-MOS)
- L: Channel length
- W: Channel width
- $t_{\text{ox}}$ : Oxide thickness
- $\text{SiO}_2$  acts as a perfect insulator



Why it is called Field Effect Transistor?

In MOSFET, the current that flows between Drain (D) and Source (S) terminals is controlled by an electric field which is perpendicular to the direction of the current flow.

- This perpendicular control is why it is called a Field Effect Transistor (FET).
- The Gate (G) terminal is separated from the channel by a perfect insulating layer ( $\text{SiO}_2$ ), hence no current (negligible) flows through the gate terminal.

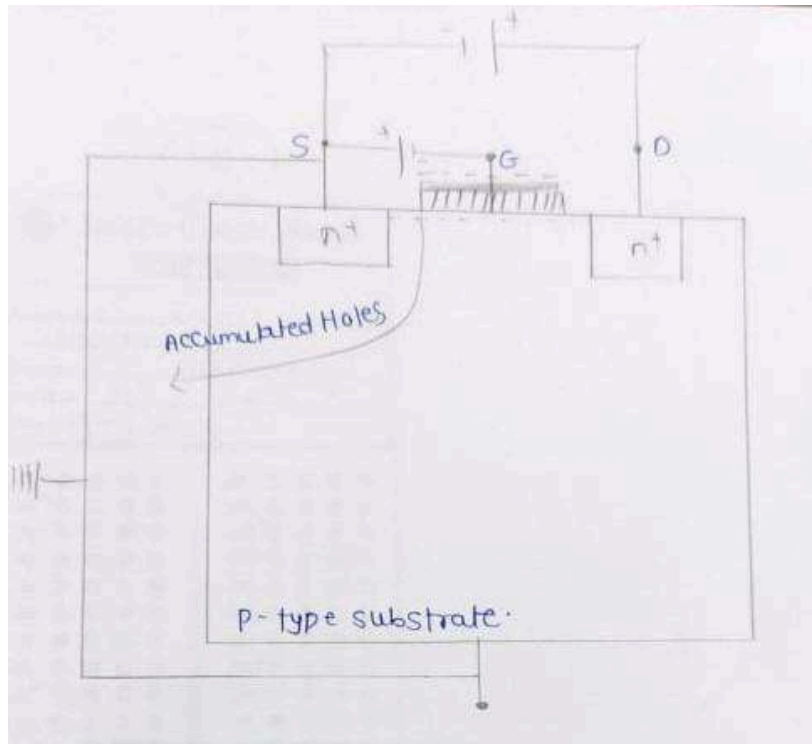
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## Regions (Modes) of Operation

### 1. Enhancement MOSFET:

1. Accumulation Mode
  2. Depletion Mode
  3. Inversion Mode
-

## 1. Accumulation Mode



Condition:  $V_{GS} < 0$  (for n-MOS)

Where:

$$V_{GS} = V_G - V_S$$

Explanation:

- Gate connected to negative voltage  $\Rightarrow$  negative charges develop on the metallic gate plate.
- These negative charges attract holes (majority carriers in p-type substrate) toward the Si-oxide interface.
- This increases hole concentration near the surface  $\Rightarrow$  Accumulation Mode.

Capacitor Analogy:

- MOS structure behaves like a parallel plate capacitor:
  - o Negative charge on Gate plate.
  - o Positive charge (holes) on semiconductor plate.

Capacitance in accumulation mode:

$$C_{MOS} = \frac{\epsilon_{ox} \cdot A}{t_{ox}}, A = W \cdot L$$

Equilibrium:

When fully charged,

$$Q_{-}(Gate) = Q_{+}(SC - plate)$$

$$Q = C_{MOS} \cdot V_{GS}$$

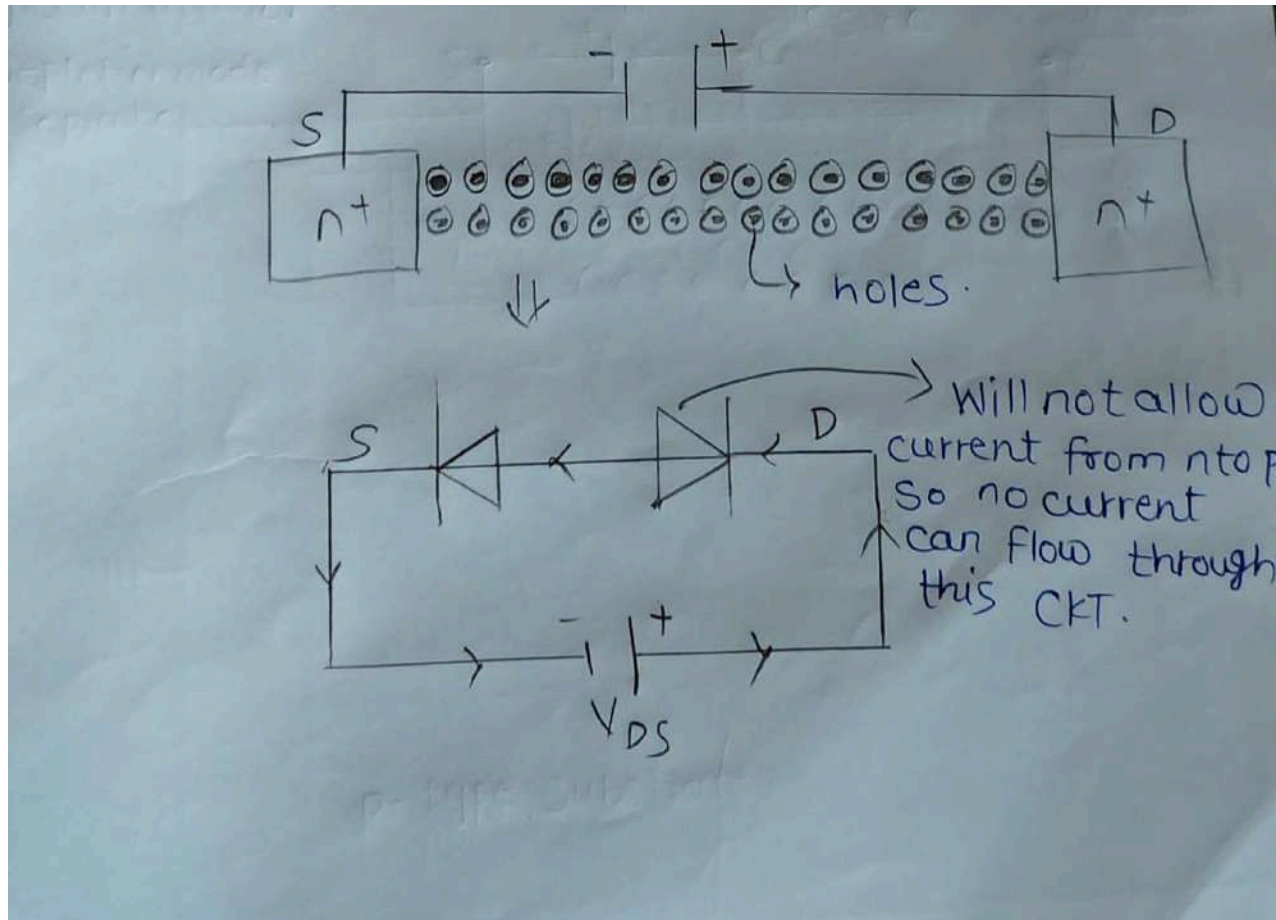
If  $V_{DS} > 0$ :

- Accumulated holes form a barrier between source and drain.
- This barrier prevents conduction  $\Rightarrow$

$$I_{DS} = 0 \text{ for any applied } V_{DS}$$

For n-type MOSFET:

$V_{GS} < 0 \Rightarrow$  Accumulation Mode,  $I_{DS} = 0$



## 2. Depletion Mode

Condition:  $V_{GS} > 0$  (small positive voltage, below threshold)

Explanation:

- Positive charges develop on the Gate plate.
- These positive charges repel holes from p-type substrates near the Si-oxide interface.
- This creates a depletion region containing:
  - o Negative acceptor ions (fixed)
  - o Minority carriers (electrons)
- As  $V_{GS}$  increases  $\Rightarrow$  depletion region width ( $W_{dep}$ ) increases.

Capacitor Analogy:

- Stored charges:
  - o +ve on Gate metallic plate
  - o -ve (acceptor ions & electrons) in depletion region
- Equivalent capacitance:

$$C_{MOS} = \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}}$$



Where:

$$C_{ox} = \frac{\epsilon_{ox} \cdot A}{t_{ox}}, C_{dep} = \frac{\epsilon_{sc} \cdot A}{W_{dep}}$$

Observation:

- In depletion mode,  $C_{MOS} < C_{MOS}$  (in accumulation mode)
- As  $V_{GS} \uparrow \Rightarrow W_{dep} \uparrow, C_{dep} \downarrow$ , hence  $C_{MOS} \downarrow$
- MOS capacitance here behaves as a voltage-variable capacitor (VVC).

If  $V_{DS} > 0$ :

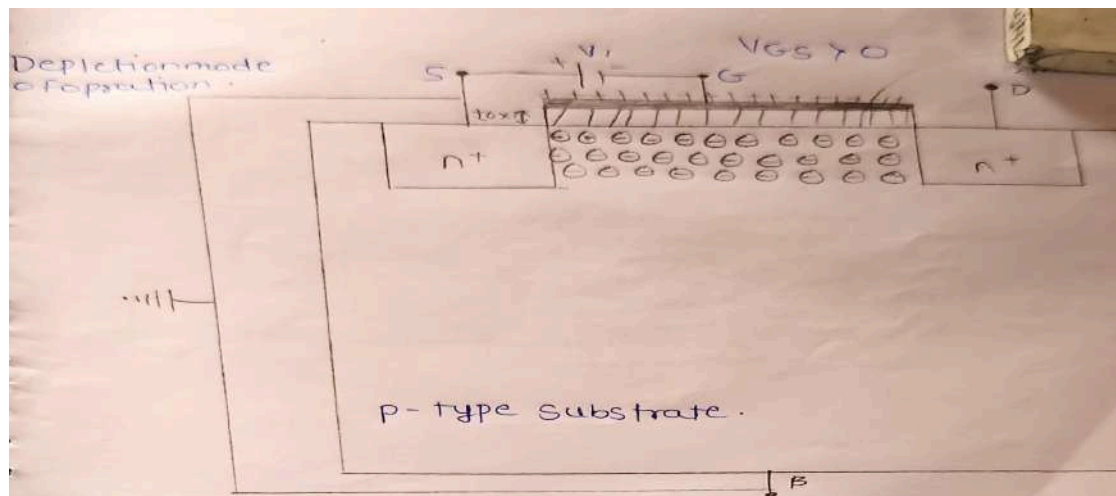
- Depletion region has high resistance between source and drain  $\Rightarrow$  negligible current:

$$I_{DS} \approx 0$$

Thus,

$$V_{GS} \text{ in depletion mode: } C_{MOS} = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}}, I_{DS} \approx 0$$

### Depletion Mode of Operation



### Structure and Bias

- Consider an n-MOS structure with p-type substrate (Body B), n+ Source (S), n+ Drain (D), Gate (G) over oxide of thickness  $t_{ox}$ , and channel geometry  $W \times L$ .
- Apply a small positive gate bias:  $V_{GS} > 0$  (but below threshold  $V_{th}$ ).

### Physical Process

- Positive charge on the metallic gate plate repels holes (majority carriers) from the p-type substrate near the Si-oxide interface, creating a depletion region containing mainly negative acceptor ions and some minority electrons.
- As  $V_{GS}$  increases above 0V, more positive charge forms on the gate, repelling more holes; depletion width  $W_{dep}$  increases with  $V_{GS}$ .

### Capacitor Analogy and Charge Balance

- The MOS structure behaves like a capacitor where positive charge is stored on the gate plate and corresponding negative charge (fixed acceptor ions + minority electrons) appears in the semiconductor (SC) plate.
- At electrostatic equilibrium:  $Q_{+}(\text{gate}) = |Q_{-}|(\text{semiconductor})$ .
- Voltage across the MOS capacitor equals the applied  $V_{GS}$  in quasi-static consideration (ignoring flat-band/work-function differences as per the note's context).



### Capacitance in Depletion

- The effective MOS capacitance in depletion is the series combination of oxide and depletion capacitances:  

$$C_{MOS} = (C_{ox} \cdot C_{dep}) / (C_{ox} + C_{dep})$$

$$C_{ox} = \epsilon_{ox} \cdot A / t_{ox}, \text{ with } A = W \cdot L$$

$$C_{dep} = \epsilon_{sc} \cdot A / W_{dep}$$
- Observations with increasing  $V_{GS}$  (below  $V_{th}$ ):
  - $W_{dep} \uparrow \Rightarrow C_{dep} \downarrow \Rightarrow C_{MOS} \downarrow$
  - CMOS in depletion is less than CMOS in accumulation
  - MOS capacitance behaves as a voltage-variable capacitor (VVC)

### Conduction with Applied VDS in Depletion

- If a potential difference is applied between drain and source ( $V_{DS} > 0$ ) while in depletion, the depletion region presents a high resistance path; current between drain and source is negligible:  $I_{DS} \approx 0$  for any applied VDS in depletion mode.

### Transition Toward Inversion and Threshold

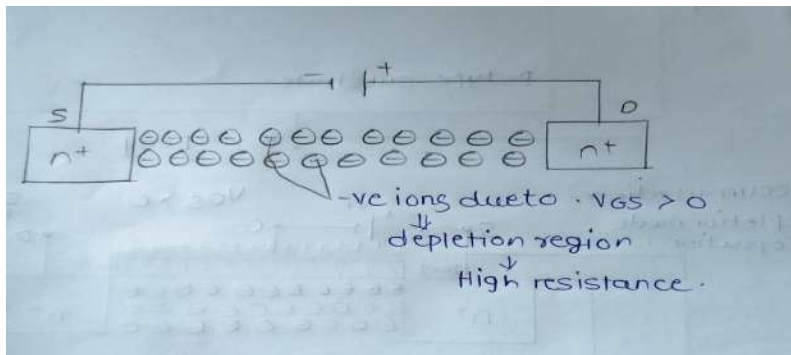
#### Minority Electron Attraction

- As  $V_{GS}$  increases further above 0V, in addition to hole repulsion, minority electrons are increasingly attracted toward the Si-oxide interface.<sup>[2][11]</sup>
- The continued electron attraction accompanies depletion-region growth until a point where electron concentration at the surface becomes significant.<sup>[1][12]</sup>

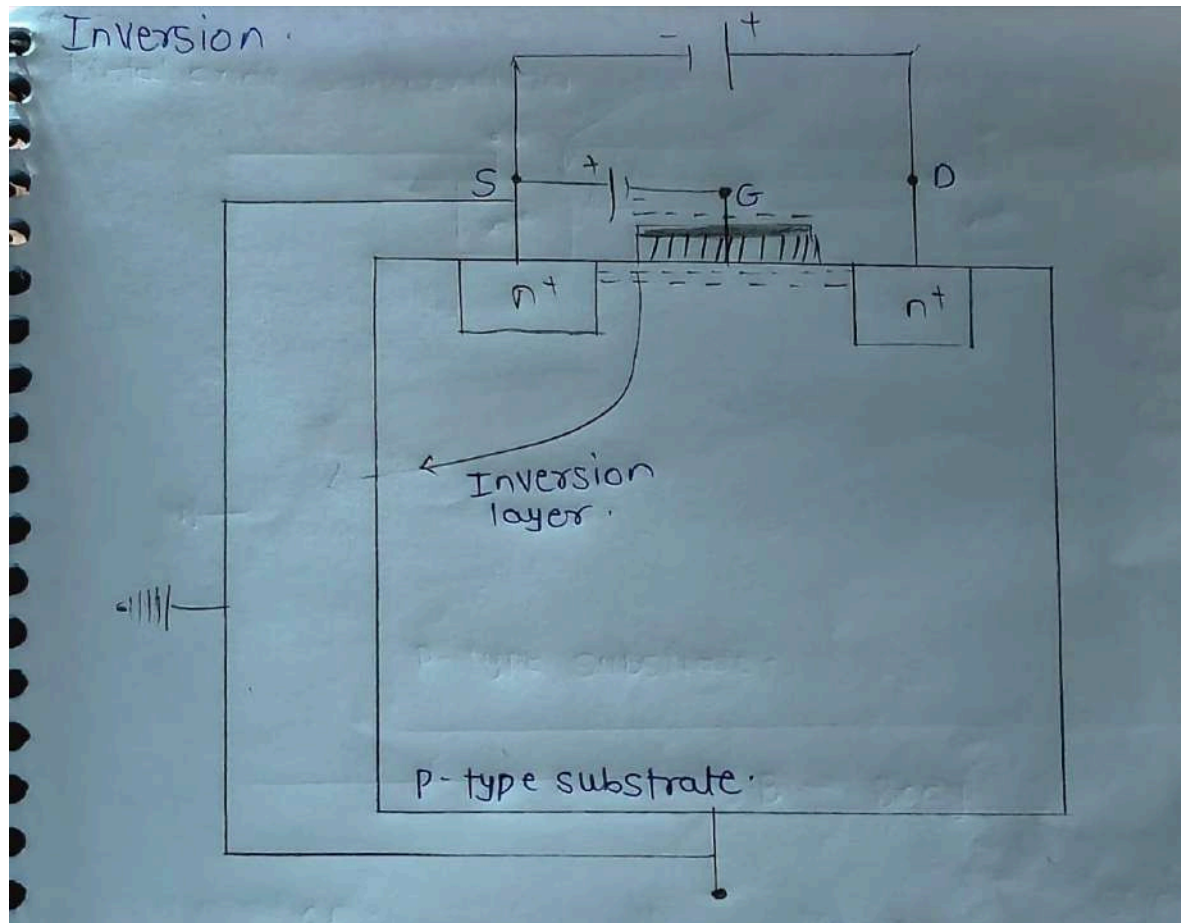
#### Threshold Voltage and Inversion Onset

- At  $V_{GS} = V_{th}$ , depletion width reaches approximately its maximum, and a very thin inversion layer of electrons forms at the interface such that electron concentration at the surface equals the hole concentration in the p-type bulk (strong inversion condition).
- At  $V_{GS} = V_{th}$ , the inversion layer thickness is extremely small, so its conductive cross-sectional area  $A \rightarrow 0$ ; channel resistance  $R \propto 1/A \rightarrow \infty$ ; hence  $I_{DS}$  tends to zero for any applied VDS at the exact threshold point.
- Around this point, the minimum MOS capacitance can be described by the series combination with the minimum depletion capacitance:  

$$C_{MOS(min)} = C_{ox} \cdot C_{dep(min)} / (C_{ox} + C_{dep(min)})$$



### 3. Inversion Mode ( $V_{GS} > V_{th}$ ):



#### Channel Formation and Capacitance

- For  $V_{GS} > V_{th}$ , repelling additional holes becomes progressively harder, while attracting more electrons becomes easier; thus, the inversion-layer (n-type channel) thickness increases with  $V_{GS}$ .
- Depletion width ceases to increase appreciably with further  $V_{GS}$  in strong inversion (approximately at its maximum), so the small-signal MOS capacitance in inversion becomes dominated by the oxide:  $C_{MOS} \approx C_{ox}$  (independent of  $V_{GS}$ ).  
 $C_{ox} = \epsilon_{ox} \cdot A / t_{ox}$

#### Finite Channel Resistance and Current Flow

- With  $V_{GS} > V_{th}$  and  $V_{DS} > 0$  applied, the inversion layer has finite thickness and finite cross-sectional area; hence, finite channel resistance and nonzero drain current flow from drain to source through the n-type inversion channel.

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#### Channel Potential, Reverse-Biased Junctions, and Tapering

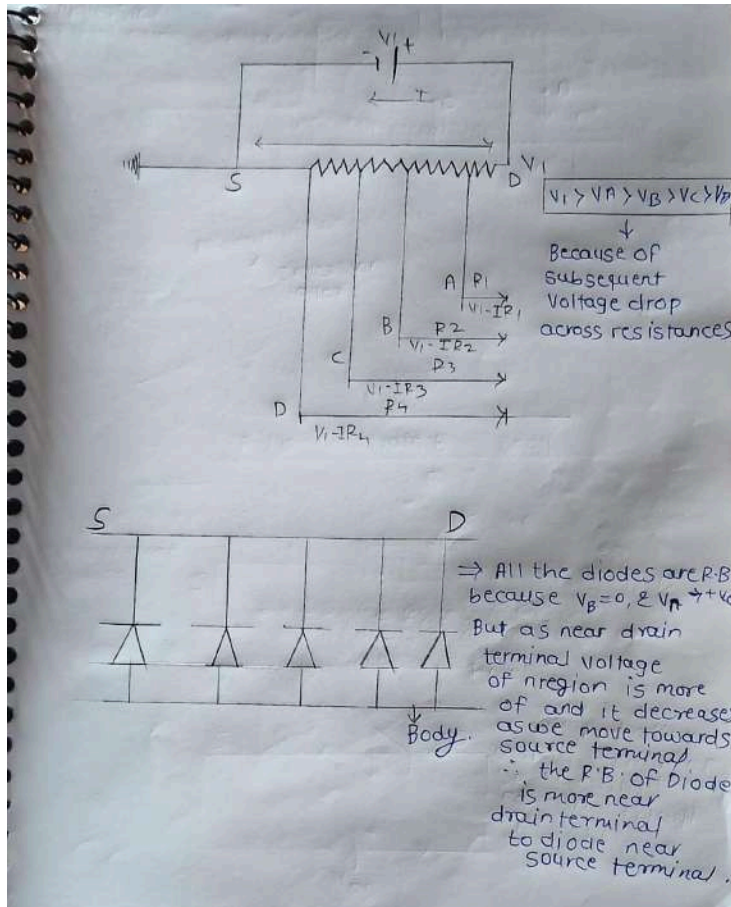
#### Body Diodes and Reverse Bias

- The p-n junctions (body-to-source and body-to-drain) are reverse-biased in normal operation (with body at 0V and positive potentials near n-regions), causing depletion penetration into both p and n sides.

- The local potential along the channel decreases from the drain toward the source ( $V_D > V_B > V_C > V_S$ ), so reverse bias is greater near the drain than near the source.

#### Depletion Penetration and Channel Shape

- Due to stronger reverse bias near the drain, depletion extends more into the n-type inversion layer near the drain than near the source, making the channel cross-section taper: thicker near source, thinner near drain.
- As  $V_{DS}$  increases from 0V, current increases while the channel's tapering intensifies, reducing the effective cross-sectional area and increasing channel resistance; current still rises with  $V_{DS}$  but with decreasing incremental rate.



#### Pinch-Off and Saturation Condition

##### Pinch-Off Criterion

- With increasing  $V_{DS}$  at fixed  $V_{GS} > V_{th}$ , the channel thickness at the drain end keeps reducing; at  $V_{DS} = V_{GS} - V_{th}$ , the channel thickness at the drain approaches zero (pinch-off at the drain end).
- At pinch-off, the incremental resistance at the drain end tends to infinity (local area  $\rightarrow 0$ ), and the incremental current gain with further increases in  $V_{DS}$  tends to zero.

##### Beyond Pinch-Off

- For  $V_{DS} > V_{GS} - V_{th}$ , the pinch-off point shifts slightly toward the source; the effective channel length shortens, but the incremental current remains approximately unchanged, leading to a near-constant  $I_{DS}$  (current saturation).

## Conclusion from all Modes

- $V_{GS} < 0 \rightarrow$  Accumulation mode  $\rightarrow I_{DS}=0$  for any applied  $V_{DS}$
  - $V_{GS} < V_{th} \rightarrow$  Depletion mode  $\rightarrow I_{DS}=0$  for any applied  $V_{DS}$
  - $V_{GS} > V_{th} \rightarrow$  Inversion mode; for  $0 < V_{DS} < (V_{GS} - V_{th})$ , a conductive channel (inversion layer) forms between D and S and  $I_{DS}$  flows from drain to source, increasing with  $V_{DS}$  (triode region)
- 

### Triode Region (Linear Region) Behavior:

- Condition:  $V_{GS} > V_{th}$  and  $0 < V_{DS} < (V_{GS} - V_{th})$
  - Drain current equation in triode region:  
 $I_{DS} = K_n [2(V_{GS} - V_{th}) \cdot V_{DS} - V_{DS}^2]$ , where  $K_n = \mu_n \cdot C_{ox} \cdot W/L$
  - Alternative form (emphasizing aspect ratio and parameters):  
 $\mu_n$ : electron mobility;  $C_{ox}$ : oxide capacitance per unit area ( $= \epsilon_{ox}/t_{ox}$ );  $W/L$ : aspect ratio;  $V_{ov} = (V_{GS} - V_{th})$ : overdrive voltage
  - $I_{DS}$  increases with  $V_{DS}$  with diminishing incremental gain as  $V_{DS}$  grows (due to the  $-V_{DS}^2$  term)
- 

### Saturation Region and Pinch-Off:

- Pinch-off condition:  $V_{DS} = V_{GS} - V_{th}$
  - At  $V_{DS} \geq (V_{GS} - V_{th})$ , incremental current with further  $V_{DS}$  is approximately zero; current becomes nearly constant  $\rightarrow$  saturation region
  - Saturation boundary is the common point between triode and saturation regions:  $V_{DS} = V_{GS} - V_{th}$ <sup>[3]</sup>
  - Drain current at the boundary (from triode equation) gives the saturation current expression:  
 $I_{DS(sat)} = K_n (V_{GS} - V_{th})^2$
  - For any  $V_{DS}$  greater than  $(V_{GS} - V_{th})$ , current remains at approximately  $I_{DS(sat)}$  and is largely independent of  $V_{DS}$  (ideal long-channel model, ignoring channel-length modulation)
- 

### Practical Notes on Entering Saturation

- For smaller  $V_{GS}$  values just above  $V_{th}$ , only a small  $V_{DS}$  is required to reach saturation; thus, probability of operating in saturation is high
  - For higher  $V_{GS}$  values, a larger  $V_{DS}$  is required to reach saturation; probability of being in saturation is lower at the same  $V_{DS}$
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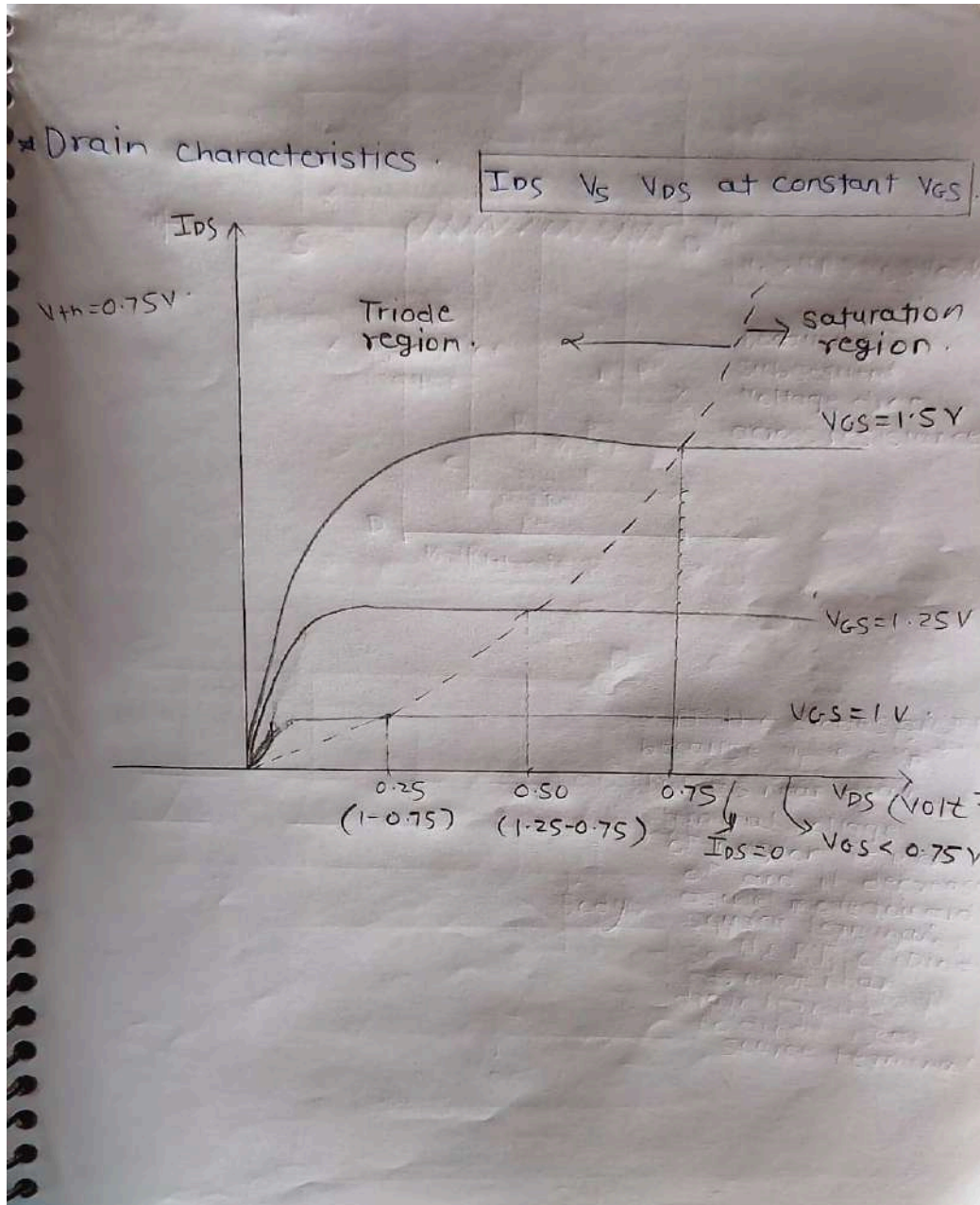
## Characteristics of N channel MOSFET and GRAPHS:

### Drain Characteristics ( $I_{DS}$ vs $V_{DS}$ at constant $V_{GS}$ ):

- Example threshold noted:  $V_{th}=0.75V$
- Regions:
  - o  $V_{GS} < 0.75V \rightarrow I_{DS}=0$  (cutoff)
  - o For  $V_{GS} > V_{th}$ :
    - $0 < V_{DS} < (V_{GS} - V_{th}) \rightarrow$  triode (linear) region
    - $V_{DS} \geq (V_{GS} - V_{th}) \rightarrow$  saturation region
- Qualitative plots show increasing  $I_{DS}$  curves for higher  $V_{GS}$ , with linear-like behavior at very small  $V_{DS}$  and saturation plateaus beyond pinch-off
- In triode region and for very small  $V_{DS}$ ,  $I_{DS}-V_{DS}$  is approximately linear with nearly constant conductance (i.e., resistance roughly constant), but the slope depends on  $V_{GS}$ ; hence the device behaves as a VVR (voltage-variable resistor)

Formulas emphasized in this context:

- $I_{DS} \approx K_n \cdot 2(V_{GS} - V_{th}) \cdot V_{DS}$  for very small  $V_{DS}$  (linear approximation)
- VVR interpretation:  $V_{DS} = R(V_{GS}) \cdot I_{DS}$ , where  $R$  varies with  $V_{GS}$



Drain Characteristics of MOSFET

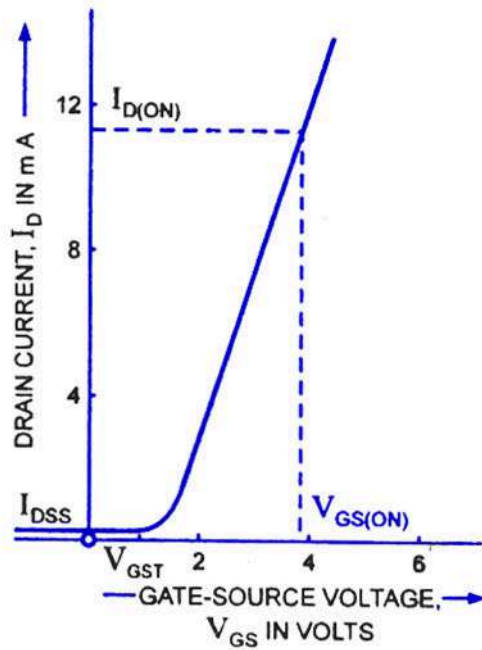
#### Transfer Characteristics ( $I_{DS}$ vs $V_{GS}$ at constant $V_{DS}$ , with device in saturation)

- Consider  $V_{DS}$  sufficiently large so MOSFET remains in saturation across the sweep
- $I_{DS}$ - $V_{GS}$  curve is non-linear and parabolic in saturation according to  $I_{DS(sat)} = K_n (V_{GS} - V_{th})^2$
- Indicates how effectively input voltage  $V_{GS}$  controls output current  $I_{DS}$

- At smaller  $V_{GS}$  (just above  $V_{th}$ ), changes in  $V_{GS}$  produce relatively small  $I_{DS}$  changes; at higher  $V_{GS}$ , small  $V_{GS}$  changes produce large  $I_{DS}$  changes

Transconductance:

- $g_m = \partial I_{DS} / \partial V_{GS}$  in saturation  $= 2 \cdot K_n \cdot (V_{GS} - V_{th})$
- This  $g_m$  expression is valid in saturation region



*Transfer Characteristic*

#### Key Parameters and Notation

- $\mu_n$ : mobility of electrons
- $C_{ox}$ : oxide capacitance per unit area ( $= \epsilon_{ox}/t_{ox}$ )
- $W/L$ : aspect ratio
- $K_n = \mu_n \cdot C_{ox} \cdot W/L$ : conduction parameter
- $V_{ov} = (V_{GS} - V_{th})$ : overdrive voltage

Recap: Saturation Region (n-MOS)

- $I_{DS(sat)} = K_n [V_{GS} - V_{th}]^2$
- Transconductance in saturation:  
 $g_m = \partial I_{DS} / \partial V_{GS} = 2K_n [V_{GS} - V_{th}]$   
 $\Rightarrow g_m \propto \sqrt{I_{DS}}$  since  $I_{DS} = K_n(V_{GS} - V_{th})^2 \Rightarrow g_m = 2\sqrt{K_n \cdot I_{DS}}$
- As  $V_{GS} \uparrow \Rightarrow I_{DS} \uparrow$  and  $g_m \uparrow$ ; and vice versa.

Where  $K_n = \mu_n \cdot C_{ox} \cdot W/L$ , and  $C_{ox} = \epsilon_{ox}/t_{ox}$ .



### Transfer Characteristics in Triode Region (n-MOS):

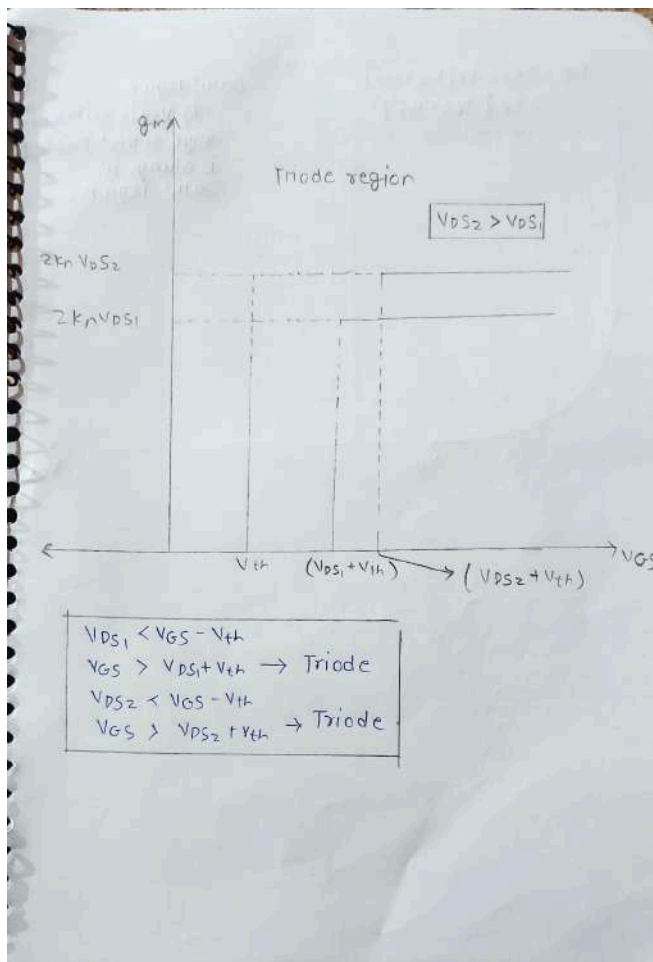
- Condition:  $V_{GS} > V_{th}$  and  $0 < V_{DS} < (V_{GS} - V_{th})$
- Drain current:  

$$I_{DS} = K_n [2(V_{GS} - V_{th}) \cdot V_{DS} - V_{DS}^2]$$
- For small-signal slope with respect to  $V_{GS}$  at constant  $V_{DS}$ :  

$$g_m = \partial I_{DS} / \partial V_{GS} = 2K_n \cdot V_{DS}$$
  - Note: In triode,  $g_m$  depends on  $V_{DS}$  (not on  $V_{GS}$  directly), so at fixed  $V_{DS}$ ,  $g_m$  is constant versus  $V_{GS}$ .
- Linearized form ( $y = m x + c$ ) at constant  $V_{DS}$  treating  $I_{DS}$  vs  $V_{GS}$ :  
 $y \equiv I_{DS}, x \equiv V_{GS}$   
 $m = 2K_n \cdot V_{DS}$   
 $c = -2K_n \cdot V_{th} \cdot V_{DS} - K_n \cdot V_{DS}^2$ 
  - Slope increases with  $V_{DS}$ ; intercept set by  $V_{th}$  and  $V_{DS}^2$  term.

Graphical notes:

- For  $V_{GS} > V_{th}$ ,  $I_{DS}$ - $V_{GS}$  in triode is an affine line at fixed  $V_{DS}$  with slope  $2K_n \cdot V_{DS}$ .
- $I_{DS}$ - $V_{DS}$  in triode is approximately linear at very small  $V_{DS}$ , then curves downward due to  $-V_{DS}^2$  term.



### Comparing $g_m$ in Regions (n-MOS)

- Triode ( $0 < V_{DS} < V_{GS} - V_{th}$ ):  
 $g_m = 2K_n \cdot V_{DS} \Rightarrow$  independent of  $V_{GS}$  at fixed  $V_{DS}$
- Saturation ( $V_{DS} \geq V_{GS} - V_{th}$ ):  
 $g_m = 2K_n(V_{GS} - V_{th}) \Rightarrow$  increases linearly with  $V_{GS}$  and equals  $2\sqrt{K_n \cdot I_{DS}}$



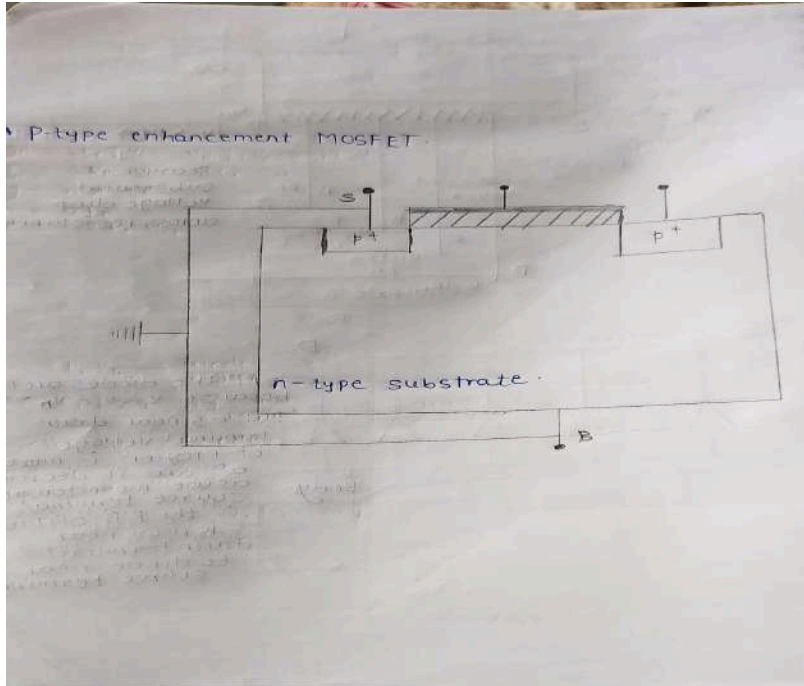
Key takeaways:

- In saturation, both  $I_{DS}$  and  $g_m$  depend on  $V_{GS}$ .
- In triode,  $I_{DS}$  depends on  $V_{GS}$ , but  $g_m$  at constant  $V_{DS}$  does not depend on  $V_{GS}$ ; it depends on  $V_{DS}$ .

Region conditions (n-MOS):

- Triode:  $V_{DS} < V_{GS} - V_{th}$
- Saturation:  $V_{DS} \geq V_{GS} - V_{th}$

## p-Type Enhancement MOSFET (pMOS, enhancement type):



Convention used: body at reference; source at higher potential than drain; for pMOS,  $V_{SD} > 0$ ,  $V_{DS} < 0$ ; use  $V_{SG} = -V_{GS} \geq 0$ .

Modes:

- Accumulation (pMOS):  $V_{GS} > 0$  (i.e.,  $V_{SG} < 0$ )
  - Gate positive w.r.t. source de-accumulates holes; with the provided note convention, the accumulation/depletion labeling mirrors nMOS text but keep sign conventions consistent in equations below.
- Depletion:  $V_{th} < V_{GS} < 0$  (i.e.,  $0 < V_{SG} < |V_{TP}|$ )
  - Effective depletion, no conduction channel; CMOS in depletion is series:  
 $CMOS = (C_{dep} \cdot C_{ox}) / (C_{dep} + C_{ox})$
  - At  $V_{GS} = V_{th}$  ( $V_{SG} = |V_{TP}|$ ), CMOS reaches minimum:  
 $CMOS(min) = (C_{dep(min)} \cdot C_{ox}) / (C_{dep(min)} + C_{ox})$
- Inversion (ON):  $V_{GS} < V_{th} \Leftrightarrow V_{SG} > |V_{TP}|$ 
  - Channel forms; current flows for applied source-drain bias.
  - For pMOS in normal operation: source at higher potential, drain at lower  $\Rightarrow V_{SD} > 0$  and  $V_{SG} > 0$ .

Capacitance references:

- $CMOS(inversion) \approx C_{ox} = \epsilon_{ox} \cdot A / t_{ox}$  (strong inversion)
- $CMOS(accumulation) \approx C_{ox}$
- Depletion uses series formula above.

pMOS conduction (using pMOS-friendly variables):

- ON condition:  $V_{SG} > |V_{TP}|$
- Triode (linear) region:  $0 < V_{SD} < (V_{SG} + V_{TP})$   
 $I_{SD} = K_p [2(V_{SG} + V_{TP}) \cdot V_{SD} - V_{SD}^2]$
- Saturation:  $V_{SD} \geq (V_{SG} + V_{TP})$   
 $I_{SD}(\text{sat}) = K_p [V_{SG} + V_{TP}]^2$
- Parameter:  $K_p = \mu_p \cdot C_{ox} \cdot W / (2L)$

Notes:

- Drain characteristics  $I_{SD}$ – $V_{SD}$  mirror nMOS with variable substitutions:  
 $V_{DS} \leftrightarrow V_{SD}, (V_{GS} - V_{th}) \leftrightarrow (V_{SG} + V_{TP})$
- Transfer characteristic in saturation ( $I_{SD}$  vs  $V_{SG}$  at sufficiently large  $V_{SD}$ ):  
 $I_{SD} = K_p [V_{SG} + V_{TP}]^2 = K_p [-V_{GS} + V_{TP}]^2$   
 This is a mirror image of nMOS transfer characteristics.

pMOS region conditions summary:

- OFF:  $V_{SG} < |V_{TP}| \Rightarrow I_{SD} = 0$  (no inversion)
- Triode:  $V_{SG} > |V_{TP}|$  and  $V_{SD} < (V_{SG} + V_{TP})$
- Saturation:  $V_{SG} > |V_{TP}|$  and  $V_{SD} \geq (V_{SG} + V_{TP})$

Transconductance for pMOS:

- Triode (constant  $V_{SD}$ ):  $g_m = \partial I_{SD} / \partial V_{SG} = 2K_p \cdot V_{SD}$
- Saturation:  $g_m = \partial I_{SD} / \partial V_{SG} = 2K_p (V_{SG} + V_{TP}) = 2\sqrt{(K_p \cdot I_{SD})}$

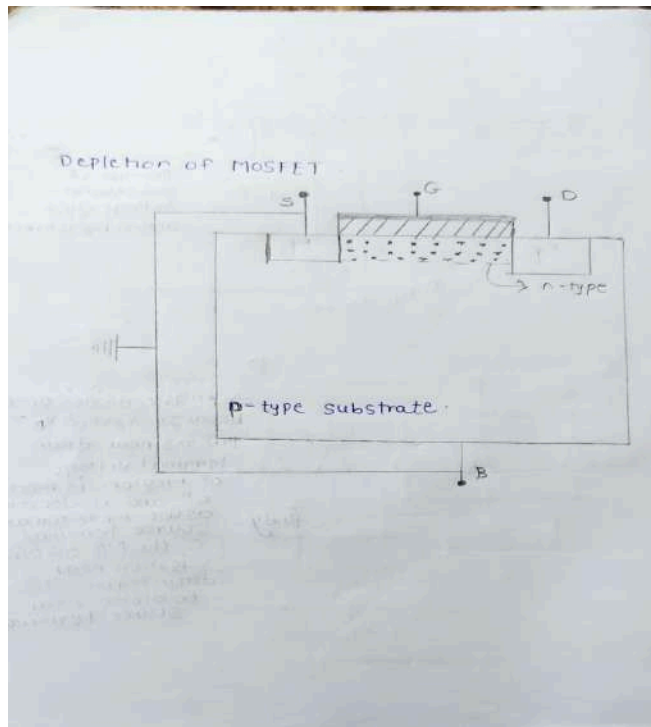
Sign conventions reminder:

- For pMOS, typical signs:  $V_{SG} \geq 0, V_{SD} \geq 0, V_{TP} < 0$  (magnitude  $|V_{TP}|$ ).
- Mapping to nMOS forms: replace  $(V_{GS} - V_{th})$  with  $(V_{SG} + V_{TP})$ .

## Quick Equation Box:

- nMOS triode:  $I_{DS} = K_n [2(V_{GS} - V_{th}) \cdot V_{DS} - V_{DS}^2]$
- nMOS saturation:  $I_{DS} = K_n (V_{GS} - V_{th})^2$
- nMOS  $g_m$ :
  - o Triode:  $g_m = 2K_n \cdot V_{DS}$
  - o Saturation:  $g_m = 2K_n(V_{GS} - V_{th}) = 2\sqrt{(K_n \cdot I_{DS})}$
- pMOS triode:  $I_{SD} = K_p [2(V_{SG} + V_{TP}) \cdot V_{SD} - V_{SD}^2]$
- pMOS saturation:  $I_{SD} = K_p (V_{SG} + V_{TP})^2$
- pMOS  $g_m$ :
  - o Triode:  $g_m = 2K_p \cdot V_{SD}$
  - o Saturation:  $g_m = 2K_p(V_{SG} + V_{TP}) = 2\sqrt{(K_p \cdot I_{SD})}$

## 2. Depletion MOSFET Basics



### n-Type Depletion MOSFET

- n-type channel exists even at  $V_{GS} = 0 \rightarrow$  current flows for  $V_{DS} > 0$ .
- Applying  $-ve$   $V_{GS}$  repels electrons  $\rightarrow$  channel width reduces (depletion).
- At  $V_{GS} = V_{th}$  (negative)  $\rightarrow$  channel fully depleted  $\rightarrow I_{DS} = 0$  for any  $V_{DS}$ .
- $V_{th}$  is negative for n-type depletion MOSFET.
- Modes:
  - o  $V_{GS} < V_{th} \rightarrow$  OFF (no channel)
  - o  $V_{GS} > V_{th}$ ,  $V_{DS} < (V_{GS} - V_{th}) \rightarrow$  Triode
  - o  $V_{GS} > V_{th}$ ,  $V_{DS} \geq (V_{GS} - V_{th}) \rightarrow$  Saturation

### Equations:

- Triode:

$$I_{DS} = K_n [2(V_{GS} - V_{th})V_{DS} - V_{DS}^2]$$

- Saturation:

$$I_{DS} = K_n (V_{GS} - V_{th})^2$$

- With positive  $V_{GS}$ , electron density in the channel increases  $\rightarrow$  enhancement mode.
- Drain characteristics:
  - o  $V_{GS} < 0 \rightarrow$  depletion mode curves
  - o  $V_{GS} > 0 \rightarrow$  enhancement mode curves  
(similar to enhancement MOSFET but  $V_{th}$  is negative)

### p-Type Depletion MOSFET

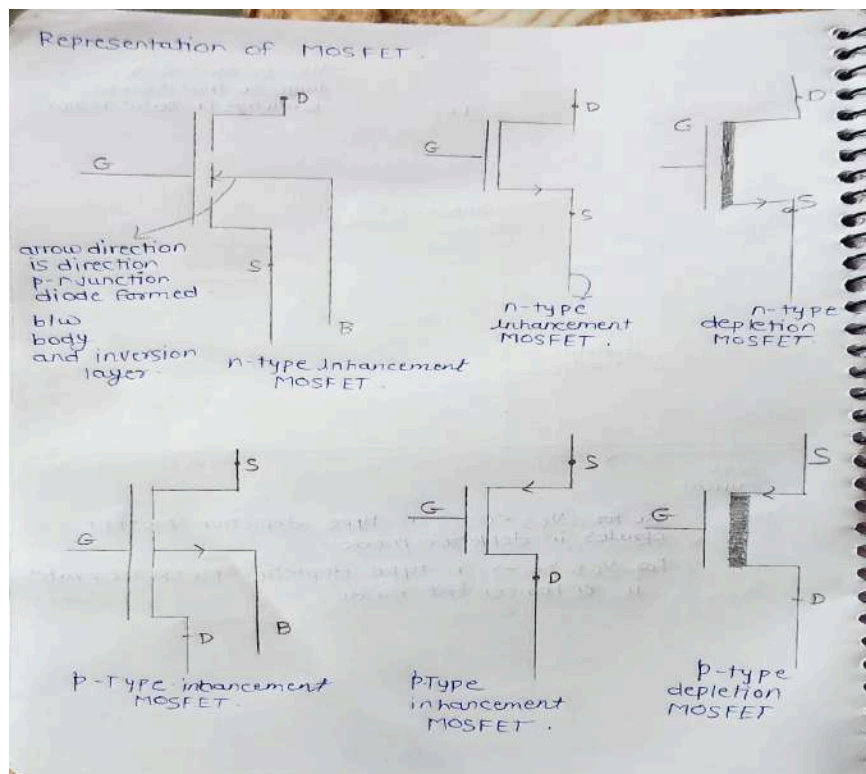
- $V_{th}$  positive.
  - Modes:
    - o  $V_{GS} > 0 \rightarrow$  Depletion mode
    - o  $V_{GS} < 0 \rightarrow$  Enhancement mode
  - Transfer characteristic = mirror image (about y-axis) of n-type.
- 

## Enhancement vs Depletion MOSFET:

- Enhancement type: Normally OFF at  $V_{GS} = 0$  (needs inversion to conduct).
- Depletion type: Normally ON at  $V_{GS} = 0$  (already has channel).
- n-type enhancement:  $V_{th} > 0$
- n-type depletion:  $V_{th} < 0$
- p-type enhancement:  $V_{th} < 0$
- p-type depletion:  $V_{th} > 0$

### 2. MOSFET Symbol Representation

- Arrow shows p-n junction direction between body and inversion layer.
- Symbol variations for:
  - o n-type enhancement
  - o n-type depletion
  - o p-type enhancement
  - o p-type depletion



## 3. Non-Ideal Effects

### 3.1 Channel Length Modulation ( $\lambda$ )

- In saturation ( $V_{DS} \geq V_{GS} - V_{th}$ ):
  - Increasing  $V_{DS}$  moves pinch-off point toward source, reducing effective channel length.
  - Leads to slight increase in  $I_{DS}$  with  $V_{DS}$  instead of constant (ideal).
- Ideal:  $\lambda = 0 \rightarrow I_{DS}$  flat in saturation.
- Practical: small positive  $\lambda \rightarrow I_{DS}$  slope in saturation region.

Modified Saturation Current Equation:

$$I_{DS} = I_{DS0} [1 + \lambda V_{DS}]$$

where

$$I_{DS0} = K_n (V_{GS} - V_{th})^2$$

- $\lambda$ : channel-length modulation parameter ( $V^{-1}$ ), very small in long-channel devices.

Key Summary Table

Type	Vth Sign	At VGS=0	Modes Possible
n-Enhancement	+ve	OFF	Enhancement only
n-Depletion	-ve	ON	Depletion & Enhancement
p-Enhancement	-ve	OFF	Enhancement only
p-Depletion	+ve	ON	Depletion & Enhancement

#### 1. Channel Length Modulation

- In Saturation Region:  
If we increase

$$V_{DS} > (V_{GS} - V_{th})$$

the zero-point (where channel thickness  $\rightarrow 0$ ) shifts toward the Source terminal, thus the effective channel length decreases.

- This decrease in effective channel length with increase in  $V_{DS}$  (above  $V_{GS} - V_{th}$ ) is called Channel Length Modulation.

#### Ideal vs Practical

- Ideal assumption: In saturation, for  $V_{DS} > (V_{GS} - V_{th})$ ,  $I_{DS}$  stays constant.
- Practical: With increase in  $V_{DS}$  above  $(V_{GS} - V_{th})$ ,  $I_{DS}$  increases slightly  $\rightarrow$  drain characteristics have slope in saturation instead of flat.

Equations:

- Ideal saturation current:

$$I_{DS0} = K_n [V_{GS} - V_{th}]^2$$

- With channel length modulation:

$$I_{DS} = I_{DS0} [1 + \lambda \Delta V_{DS}]$$

where:

$\lambda$  = channel length modulation parameter ( $V^{-1}$ , very small in long-channel MOSFETs)

$$\Delta V_{DS} = V_{DS} - (V_{GS} - V_{th})$$


---

Output Resistance

- Ideal:  $\lambda = 0 \Rightarrow r_o \rightarrow \infty$
- Practical:  $\lambda > 0 \Rightarrow$  finite but high  $r_o$

$$r_o = \frac{1}{\lambda I_{DS0}}$$


---

Modified Current Expression (including  $\lambda$ ):

$$I_{DS} = K_n [V_{GS} - V_{th}]^2 \cdot [1 + \lambda(V_{DS} - (V_{GS} - V_{th}))]$$

Effect on  $g_m$ :

- Ideal:  $g_m = 2K_n(V_{GS} - V_{th})$ , independent of  $V_{DS}$  in saturation.
  - Practical: In saturation, as  $V_{DS} \uparrow \Rightarrow \Delta V_{DS} \uparrow \Rightarrow I_{DS} \uparrow \Rightarrow g_m \uparrow$ .
- 

Also: Due to channel length modulation, effective  $V_{th}$  decreases slightly with  $V_{DS}$ .

---

## 2. Body Effect:

- Normally Body (B) and Source (S) are connected  $\Rightarrow V_{SB} = 0$ .
- When they are not connected  $\Rightarrow V_{SB} \neq 0 \Rightarrow$  threshold voltage changes  $\Rightarrow$  Body Effect.

Equation:

$$V_{TN} = V_{TN0} + \gamma \left[ \sqrt{V_{SB} + 2\phi_f} - \sqrt{2\phi_f} \right]$$

Where:

- $V_{TN}$  = threshold voltage with body effect
  - $V_{TN0}$  = threshold voltage when  $V_{SB} = 0$
  - $\gamma$  = body effect parameter
  - $\phi_f$  = Fermi potential
  - Due to body effect, magnitude of  $V_{th}$  increases.
-

### 3. Threshold Voltage Dependence:

1. Oxide thickness ( $t_{ox}$ ):

$$C_{ox} = \frac{\epsilon_{ox} \cdot A}{t_{ox}}$$

$$t_{ox} \downarrow \Rightarrow C_{ox} \uparrow \Rightarrow V_{th} \downarrow$$

$$t_{ox} \uparrow \Rightarrow C_{ox} \downarrow \Rightarrow V_{th} \uparrow$$

2. Substrate doping ( $N_s$ ):

- o  $N_s \uparrow \Rightarrow$  more charge needed for inversion  $\Rightarrow V_{th} \uparrow$

$$N_s \downarrow \Rightarrow V_{th} \downarrow$$

3. Temperature (T):

$$T \uparrow \Rightarrow V_{th} \downarrow$$

$$T \downarrow \Rightarrow V_{th} \uparrow$$

---

Temperature Effect on IDS

$$I_{DS} = K_n (V_{GS} - V_{th})^2 \text{ with}$$

$$K_n = \frac{\mu_n C_{ox} W}{2L}$$

- As  $T \uparrow$ :
    - o  $V_{th} \downarrow \Rightarrow$  tends to increase IDS
    - o  $\mu_n \downarrow \Rightarrow K_n \downarrow \Rightarrow$  tends to reduce IDS
  - Net effect: Reduction in IDS with temperature  $\Rightarrow$  thermal runaway not a problem in MOSFETs.
- 

### 4. Subthreshold Conduction:

- Ideal: For  $V_{GS} < V_{th} \Rightarrow I_{DS} = 0$
- Practical: For  $V_{GS} < V_{th} \Rightarrow$  a small current (off-state current) flows.

Graph:  $\sqrt{I_{DS}}$  vs  $V_{GS}$

- Ideal: intercept at  $V_{th}$ , zero below
- Practical: slope continues below  $V_{th}$ , nonzero IDS

Equation (ideal strong inversion):

$$\sqrt{I_{DS}} = \sqrt{K_n} (V_{GS} - V_{th})$$

---

Cause: Weak inversion region – small diffusion current between source/drain even when  $V_{GS} < V_{th}$ .

- Off-state current increases slightly due to channel length modulation.



## Key Points Recap:

- Channel Length Modulation  $\Rightarrow$  IDS slope in saturation, finite  $r_o$ ,  $g_m$  depends slightly on  $V_{DS}$ .
- Body Effect  $\Rightarrow$  higher  $V_{th}$  when  $V_{SB} > 0$ .
- Threshold Voltage Dependence  $\Rightarrow$  affected by  $t_{ox}$ , doping  $N_s$ , temperature  $T$ .
- Subthreshold Conduction  $\Rightarrow$  small IDS for  $V_{GS} < V_{th}$  (off-state current).

# Introduction SPICE:

SPICE (Simulation Program with Integrated Circuit Emphasis) is a general-purpose electronic circuit simulator used to mathematically predict how circuits behave before building hardware. It models components (resistors, capacitors, inductors, diodes, BJTs, MOSFETs, sources, transmission lines) and solves the circuit's equations to perform common analyses:

## Why SPICE simulations are needed:

SPICE predicts circuit behavior mathematically before hardware is built, enabling early fault finding, faster iteration, and lower cost by reducing prototype spins and optimizing component values and tolerances. SPICE supports DC, AC, and transient analyses—as well as noise, distortion, and temperature sweeps—so performance and reliability can be verified across operating conditions. It is industry-standard at both board and transistor levels to check design integrity and account for parasitics and tolerances that are hard to validate on breadboards.

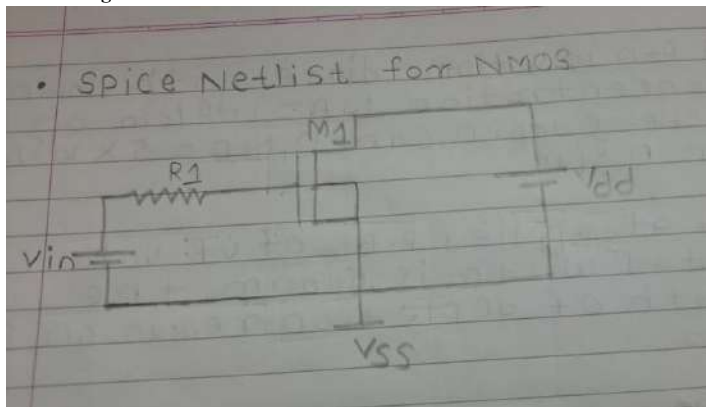
## What SPICE is used for in CMOS:

- Verify transistor-level operation and operating points in analog/mixed-signal CMOS blocks using DC/AC/transient analyses.
- Validate designs before fabrication where breadboarding integrated circuits is impractical and mask costs are high.
- Model and analyze subcircuits common in CMOS (switches, current mirrors, references, amplifiers) using MOS device models and small-signal parameters.

## Why SPICE is used for in MOSFETs:

- Evaluate I–V behavior, switching dynamics, and power dissipation using vendor and PDK MOSFET models.
- Capture parasitics and temperature effects with advanced, temperature-dependent MOSFET models for accurate transient and thermal behavior.
- Accelerate design by simulating MOSFET choices and gate-drive conditions to optimize efficiency and ensure safe operating area before hardware

## CODE Diagram:



The snap shot of SPICE netlist of the above NMOS

$R1$  resistance is added as it is not desired that the current from  $V_{in}$  would be directly fed to the gate of  $M1$ .

Definition of nodes and the method to identify them

A node is can be defined as a point connecting two terminals. If two terminals of a single device are short circuited then the node is said to be in between these two terminals. But most of the times a node connects two different devices.

The method to identify nodes is to identify the SPICE netlist for the device and all the wires connecting different components have one node on them.

## **SPICE syntax:**

SPICE netlist code for our NMOS

\*Model Description

.param temp=27

\*Including sky130 library files

.lib "sky130\_fd\_pr/models/sky130.lib.spice" tt

### **\*Netlist Description**

XM1 Vdd n1 0 0 sky130\_fd\_pr\_\_nfet\_01v8 w=5 l=2

R1 n1 in 55

Vdd vdd 0 1.8V

Vin in 0 1.8V

\*simulation commands

.op

.dc Vdd 0 1.8 0.1 Vin 0 1.8 0.2

.control

run

display

setplot dc1

.endc

.end

## **There are five types of process corners available for use:**

tt -> Typical corner

sf -> Slow-fast corner

ff -> Fast-fast corner

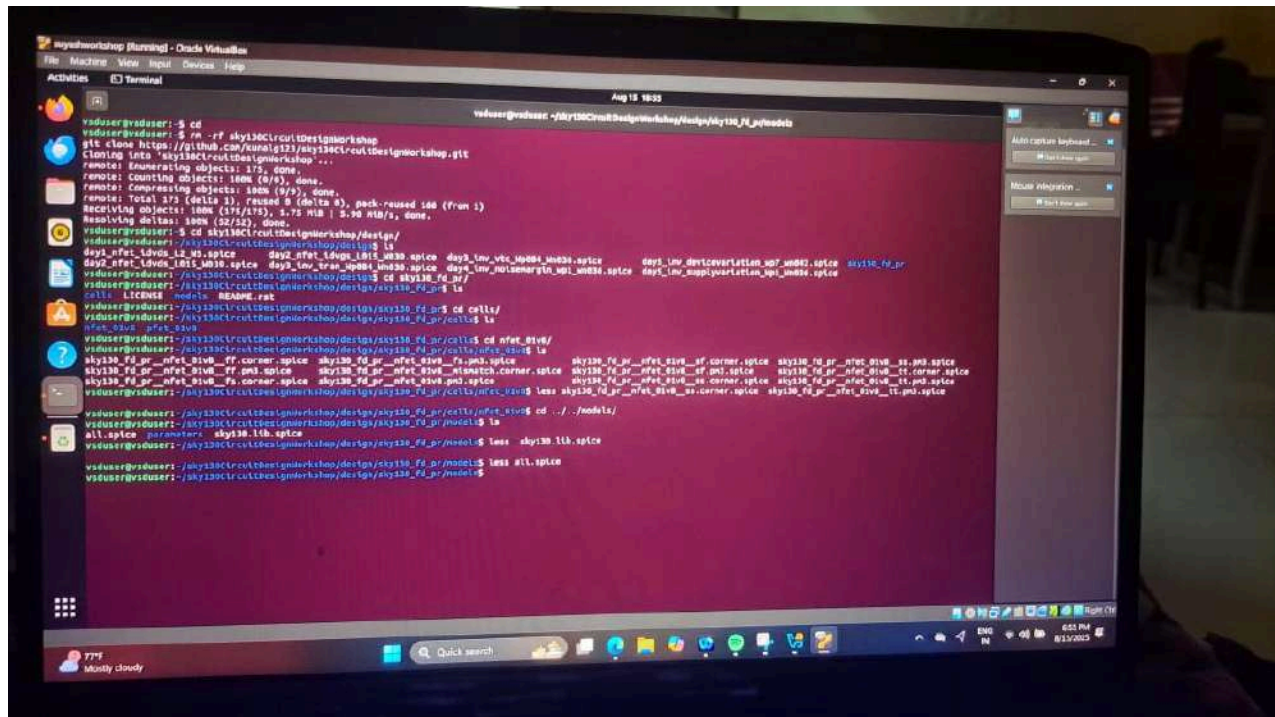
ss -> Slow-slow corner

fs -> Fast-slow corner

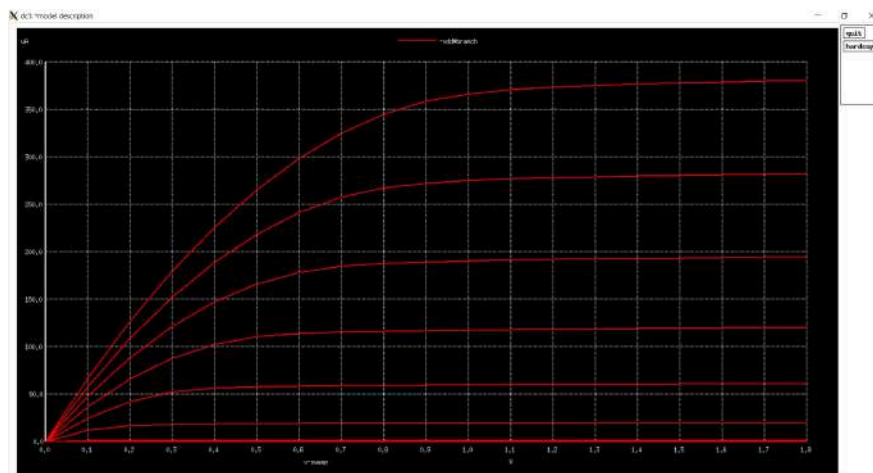
In the Lab activity, the corner is used. The corner can be changed by changing the word 'tt' in the line .lib "sky130\_fd\_pr/models/sky130.lib.spice" tt with any valid process corner

Method to save SPICE model

## Method to write code for SPICE simulation



The snap shot of the terminal window of NGSPICE Simulation:



## Velocity Saturation and basics of CMOS inverter VTC:

### 1. Velocity Saturation:

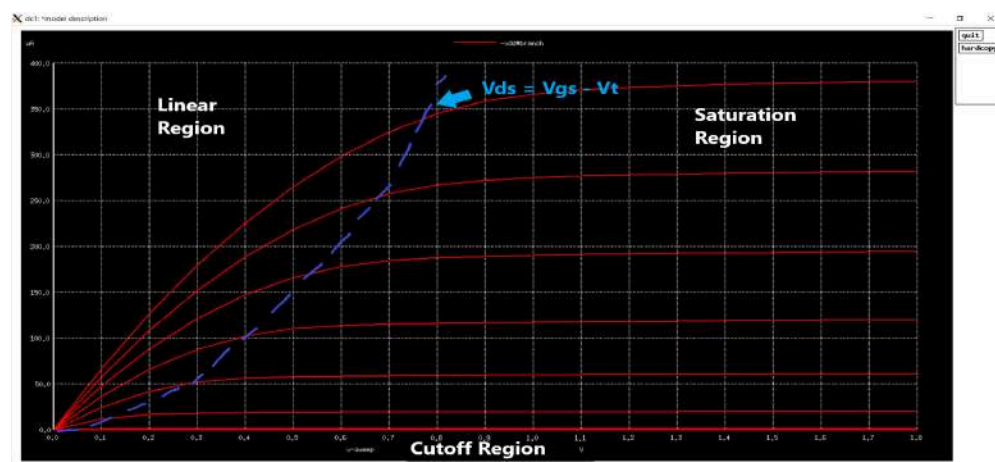
In short-channel MOSFETs, as the electric field in the channel becomes very high, carrier velocity stops increasing linearly with field and reaches a maximum (saturation velocity). This limits the drain current, affects transconductance, and is a key factor in modern deep-submicron device behavior.

### CMOS Inverter VTC (Voltage Transfer Characteristic):

The VTC shows how the output voltage of a CMOS inverter changes with its input voltage. From the curve, you can identify switching threshold ( $V_m$ ), noise margins (NMH, NML), and inverter gain — all critical for ensuring robust digital logic operation.

SPICE simulation for lower nodes and the characteristics for long channel and short channel devices were observed. The velocity saturation at lower and higher electric fields and the velocity saturation drain current model were also observed.

MOSFET as a switch and the characteristics of the CMOS inverter were taught.



The snap shot of various regions of operation of NMOS on graphs plotted between  $I_{ds}$  and  $V_{ds}$ .

The plot overlapping with the 'x' axis is at  $V_{gs}=0V$  and that is because there is 0 drain current at that point of time and the reason is that when  $V_{gs}=0V$  the nmos is not turned 'ON' so, there is no channel present.

The theory about the cut-off region of NMOS.

When  $V_{gs} < V_t$  the region of operation of the NMOS is said to be the cut-off region

Cut-off region is a region where the device has been cut-off or it is 'OFF'

Short channel effect

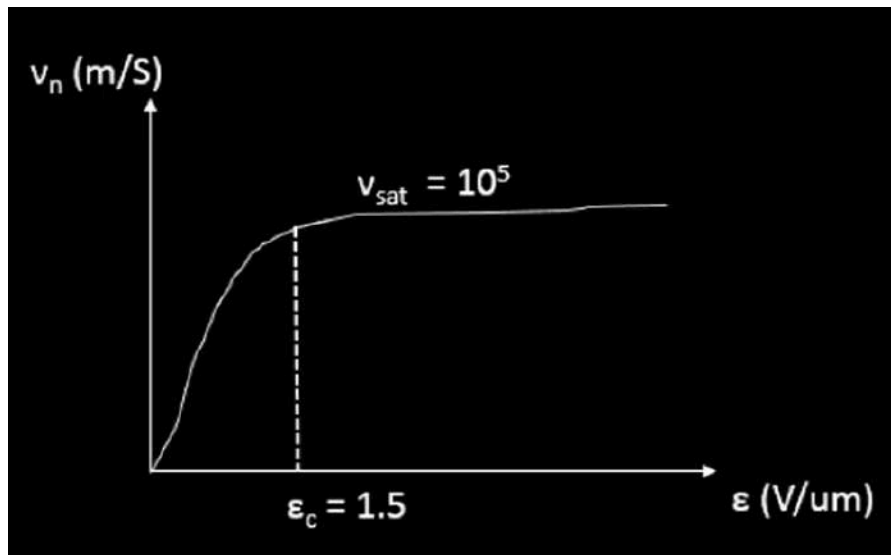
### Velocity Saturation effect

For the lower values of the electric field, the velocity tends to be a linear function of the electric field. But, after a certain point (cut-off) the velocity just saturates. This point of saturation is represented by  $\epsilon_c$  (critical electric field)

$V_n(\text{m/S}) = \text{linear for } \epsilon \leq \epsilon_c$

$V_n(\text{m/S}) = \text{constant for } \epsilon \geq \epsilon_c$

$$V_n(\text{m/S}) = \frac{\mu_n \epsilon}{1 + \frac{\epsilon}{\epsilon_c}} \text{ for } \epsilon \leq \epsilon_c$$
$$= V_{sat} \text{ for } \epsilon \geq \epsilon_c$$



The snap shot of the graph of velocity saturation effect

The modes of operation for long channel ( $>250\text{nm}$ ) devices and short channel ( $<250\text{nm}$ ) devices.

**The modes of operation for long channel devices are:**

Cut-off region

Resistive region

Saturation region

**The modes of operation for short channel devices are:**

Cut-off region

Resistive region

Velocity Saturation region

Saturation region

$V_{dsat}$  is a technology parameter saturation voltage i.e voltage at which device velocity saturates and is independent of  $V_{gs}$  or  $V_{ds}$

### **The various modes when the value of $V_{min}$ is different:**

When  $V_{gt}$  is the minimum of  $V_{gt}$ ,  $V_{ds}$ ,  $V_{dsat}$  the device is in the saturation region.

When  $V_{ds}$  is the minimum of  $V_{gt}$ ,  $V_{ds}$ ,  $V_{dsat}$  the device is in the resistive region.

When  $V_{dsat}$  is the minimum of  $V_{gt}$ ,  $V_{ds}$ ,  $V_{dsat}$  the device is in the velocity saturation region.

It looks like current should increase at lower nodes.

Velocity Saturation causes device to saturate early

For plotting the graph between  $I_{ds}$  and  $V_{ds}$  for short channel devices we need to write the following

## **SPICE code To Drain Characteristics:**

\*Model Description

.param temp=27

\*Including sky130 library files

.lib "sky130\_fd\_pr/models/sky130.lib.spice" tt

\*Netlist Description

XM1 Vdd n1 0 0 sky130\_fd\_pr\_\_nfet\_01v8 w=0.39 l=0.15

R1 n1 in 55

Vdd vdd 0 1.8V

Vin in 0 1.8V

\*simulation commands

.op

.dc Vdd 0 1.8 0.1 Vin 0 1.8 0.2

.control

run

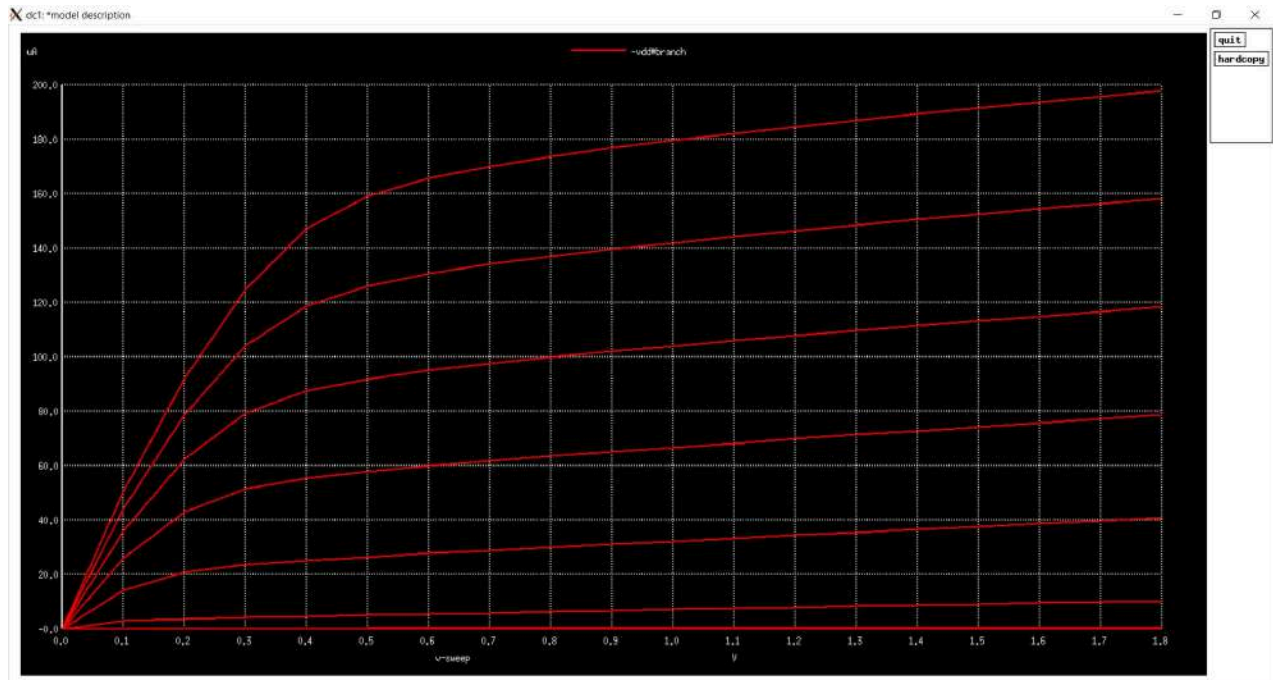
display

setplot dc1

.endc

.end





Drain Characteristics of MOSFET on NGSPICE

The snap shot of output window for plot between  $I_d$  and  $V_d$  for short channel device

To observe the value of  $I_d$  at any point on the curve, then left click on the point on the curve to be observed.

Now on the terminal window, some values of  $x_0$  and  $y_0$  should appear.

The value of  $I_d$  corresponds to the value of  $y_0$  in ampere.

To calculate Threshold voltage for  $I_d$  versus  $V_{gs}$  curve, the following SPICE code is required:

## SPICE code For Transfers Characteristics:

\*Model Description

```
.param temp=27
```

\*Including sky130 library files

```
.lib "sky130_fd_pr/models/sky130.lib.spice" tt
```

\*Netlist Description

```
XM1 Vdd n1 0 0 sky130_fd_pr__nfet_01v8 w=0.39 l=0.15
```

```
R1 n1 in 55
```

```
Vdd vdd 0 1.8V
```

```
Vin in 0 1.8V
```

\*simulation commands

```
.op
```

```
.dc Vin 0 1.8 0.1
```

```
.control
```

```
run
```

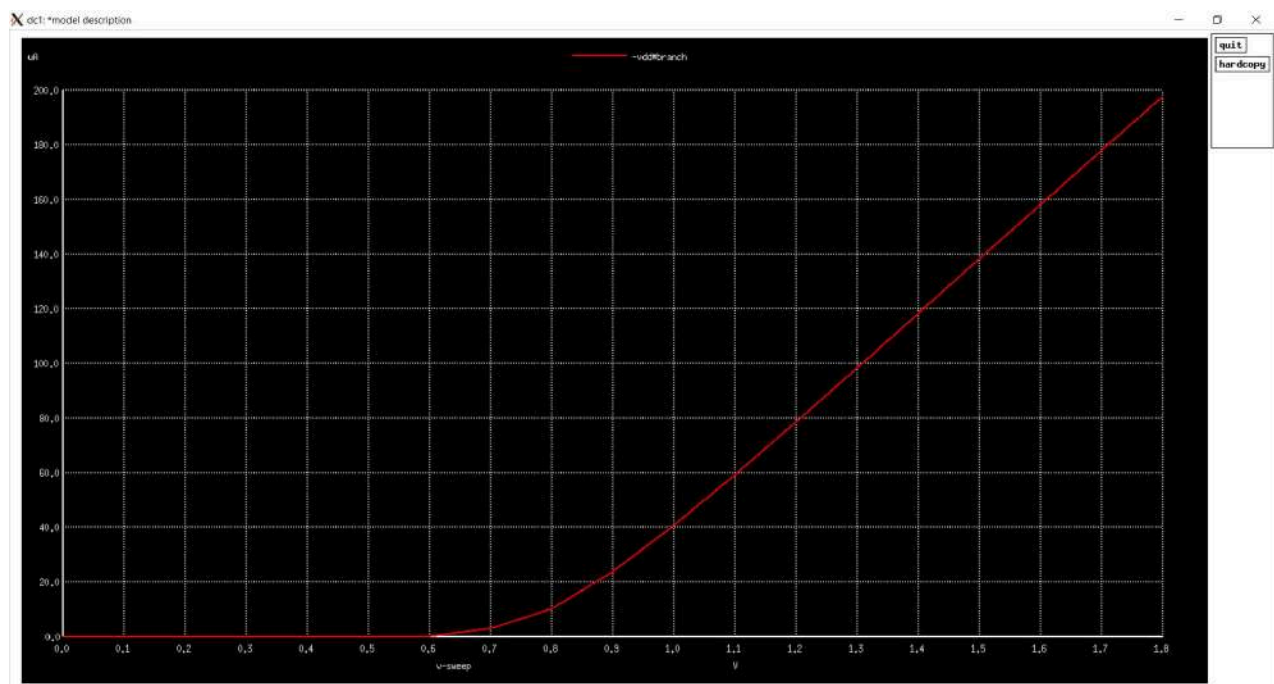
```
display
```

```
setplot dc1
```

```
.endc
```

```
.end
```

The snap shot of terminal window for plot between  $I_{ds}$  and  $V_{ds}$  for short channel device without the sweep for vdd



Transfer Characteristics of MOSFET ON NGSPICE

## 2.CMOS voltage transfer characteristics (VTC):

What was learnt:

### CMOS WORKING:

Transistor as a switch

With infinite 'Off' resistance when  $|V_{gs}| < |V_t|$

With finite 'On' resistance when  $|V_{gs}| > |V_t|$

The working of CMOS inverter

What happens when  $V_{in}$  is 'high' and equal to 'vdd'

PMOS turns 'OFF'

NMOS turns 'ON'

What happens when  $V_{in}$  is 'low' and equal to '0V'

PMOS turns 'ON'

NMOS turns 'OFF'

The flow of current when  $V_{in}$  is 'high' and when  $V_{in}$  is 'low'

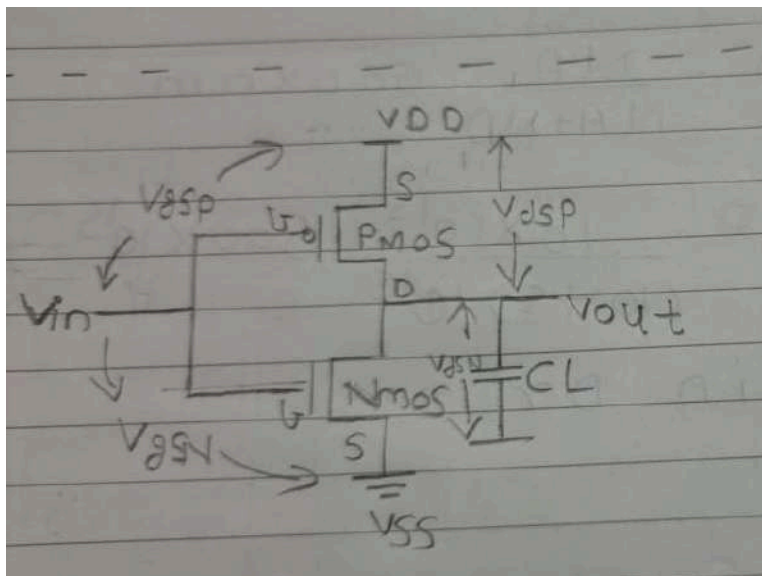
When  $V_{in} = V_{dd}$

Direct path exists between  $V_{out}$  and  $V_{ss}$  resulting in  $V_{out} = 0V$

When  $V_{in} = 0V$

Direct path exists between  $V_{dd}$  and  $V_{out}$ , resulting in  $V_{out} = V_{dd}$

Defined terminologies in CMOS inverter



Circuit Diagram of CMOS Inverter

### Derivation CMOS voltage transfer characteristics (VTC):

For the NMOS voltage equations

$$V_{gsN} = V_{in}$$

$$V_{dsN} = V_{out}$$

For the PMOS voltage equations

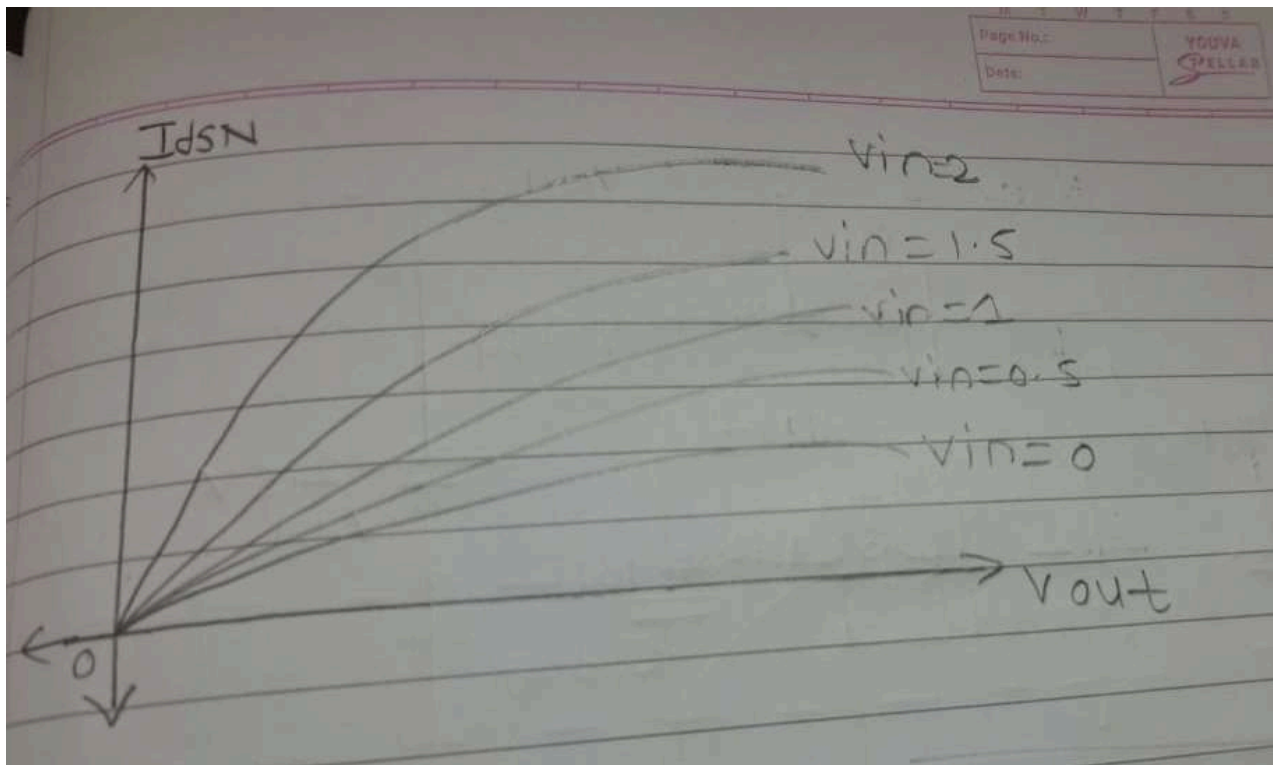
$$V_{gsP} = V_{in} - V_{dd}$$

$$V_{dsP} = V_{out} - V_{dd}$$

For the relationship between the currents

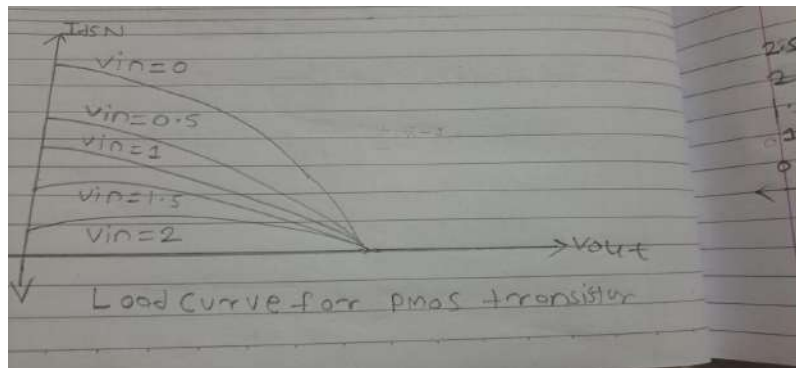
$$I_{dsP} = -I_{dsN}$$

Load curve for PMOS transistor in CMOS inverter



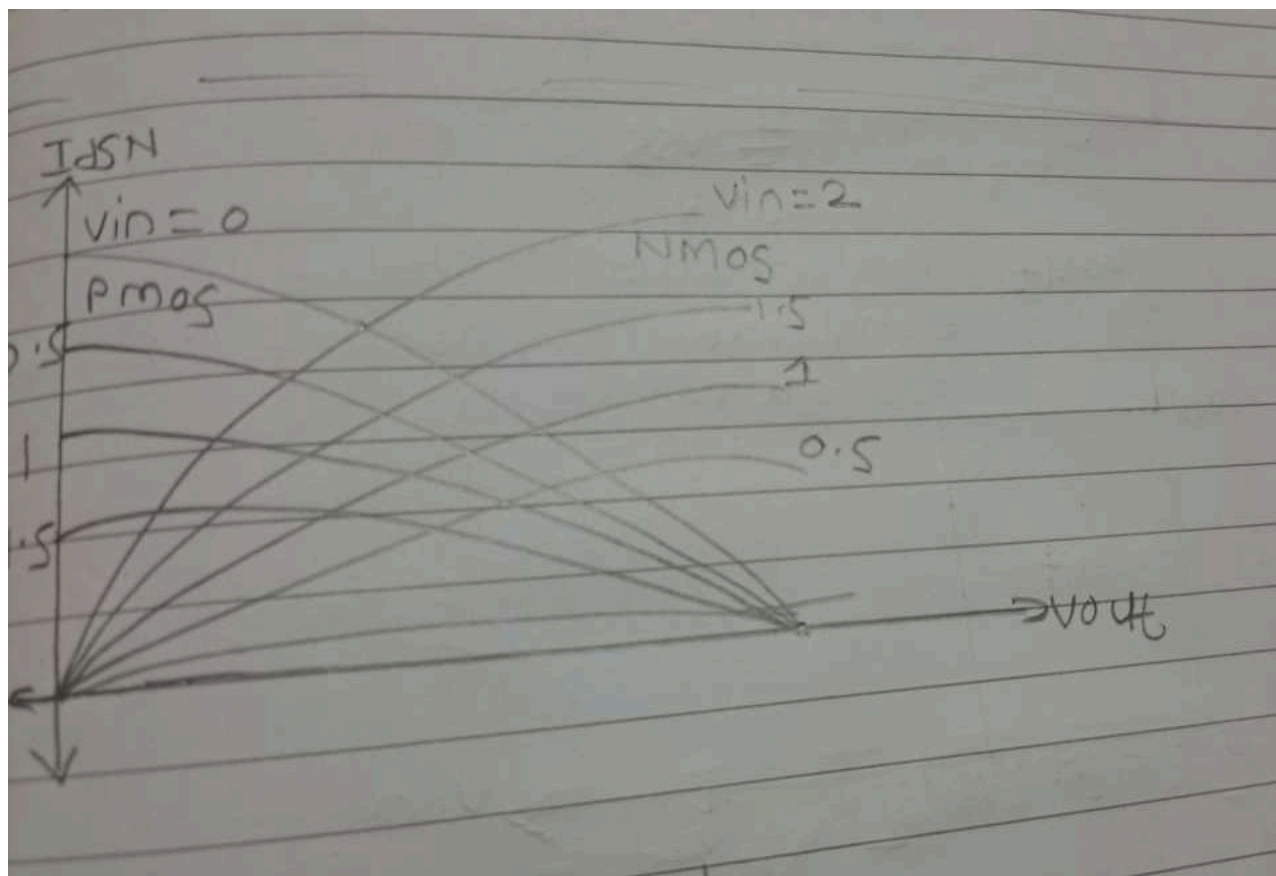
The snap shot of load curve for PMOS transistor in CMOS inverter

Load curve for NMOS transistor in CMOS inverter



The snap shot of load curve for NMOS transistor in CMOS inverter

Superimposing the load curve of NMOS on the load curve of PMOS and plotting  $V_{IN}$  vs  $V_{OUT}$  from the graph obtained



The snap shot of superimposed load curve of NMOS and load curve of PMOS

## Voltage transfer characteristics and SPICE simulations:

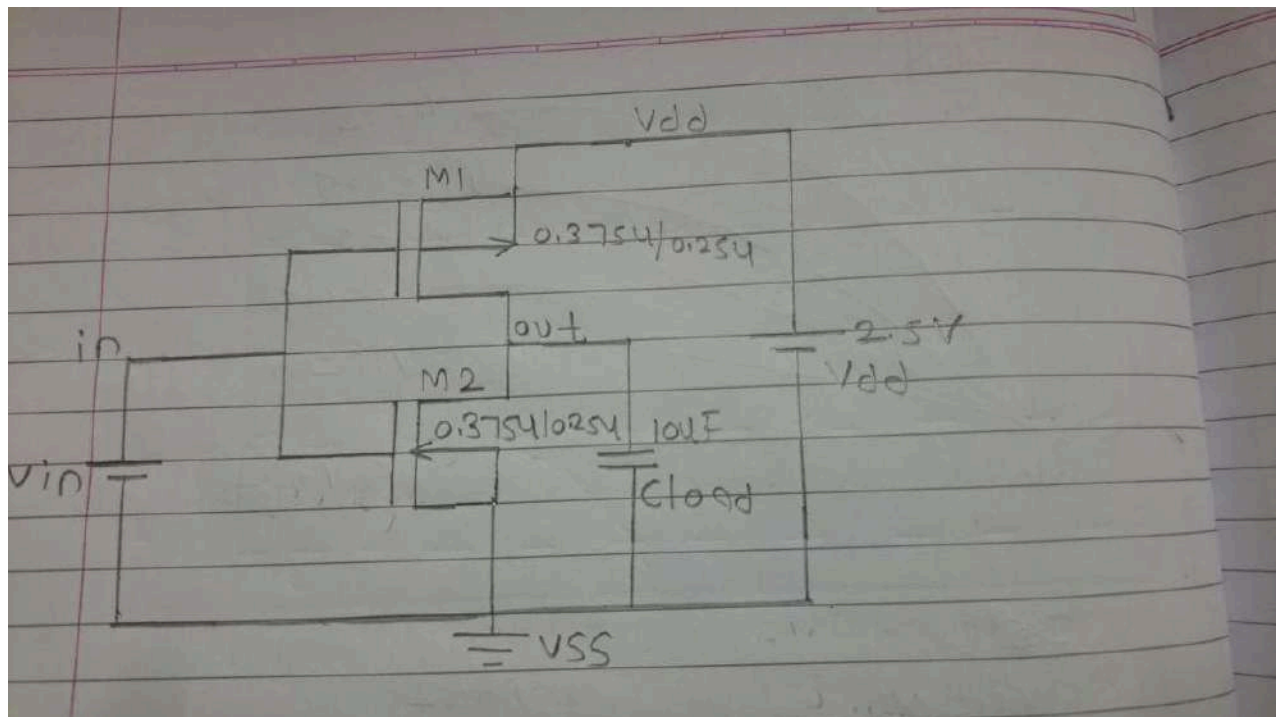
The various components of a SPICE deck:

Component connectivity

Component values

Identification of 'nodes'

Naming 'nodes'



The snap shot of the SPICE netlist considered

**The SPICE code for the above netlist looks something like following:**

\*\*\*MODEL Description\*\*\*

\*\*\*NETLIST Description\*\*\*

M1 out in vdd vdd pmos W=0.375u L=0.25u

M2 out in 0 0 nmos W=0.375u L=0.25u

load out 0 10f

Vdd vdd 0 2.5

Vin in 0 2.5

\*\*\*SIMULATION Commands\*\*\*

.op

```
.dc Vin 0 2.5 0.05

***.include tsmc_025um_model.mod***

.LIB "tsmc_025um_model.mod" CMOS_MODELS

.end
```

Lab Activity:

For plotting the Vtc characteristics of CMOS inverter, the following code is needed:

```
*Model Description

.param temp=27

*Including sky130 library files

.lib "sky130_fd_pr/models/sky130.lib.spice" tt

*Netlist Description

XM1 out in vdd vdd sky130_fd_pr__pfet_01v8 w=0.84 l=0.15

XM2 out in 0 0 sky130_fd_pr__nfet_01v8 w=0.36 l=0.15

Cload out 0 50fF

Vdd vdd 0 1.8V

Vin in 0 1.8V

*simulation commands

.op

.dc Vin 0 1.8 0.01

.control

run

setplot dc1

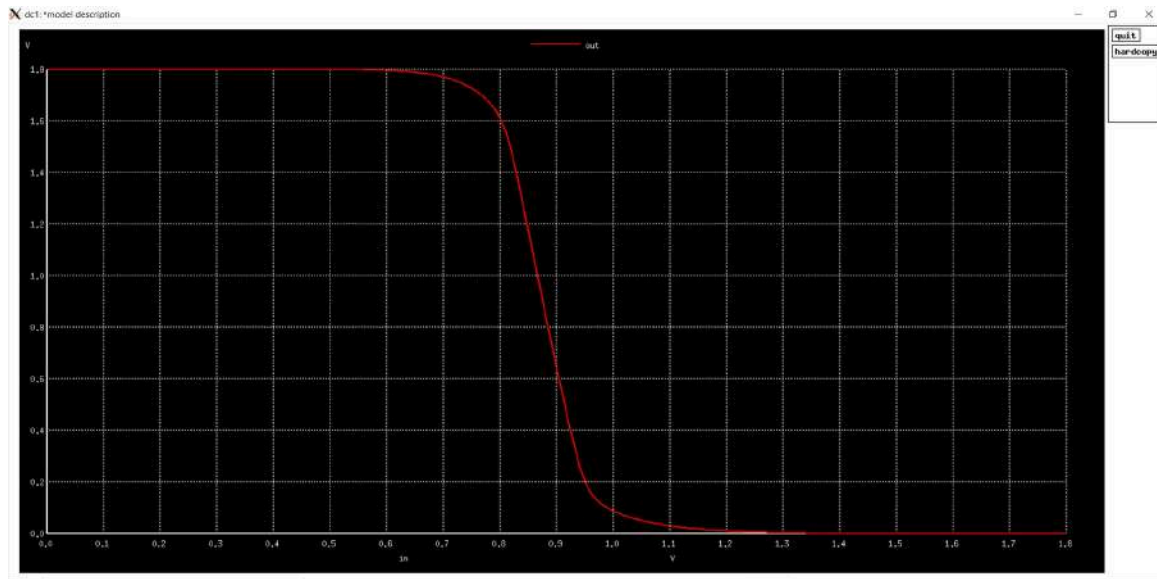
display

.endc

.end
```



The snap shot of the terminal window for plotting the Vtc characteristics of CMOS inverter



### output window for plotting the Vtc characteristics of CMOS inverter on NGSPICE

To find the switching threshold voltage ( $V_m$ ), it is known that  $V_{out} = V_{in}$  so zoom in on the plot where roughly  $V_{out} = V_{in}$  by selecting the area of the plot by right clicking on the screen and dragging it to select the area.

Zoom twice or thrice until the point where  $V_m$  lies becomes almost certain.

Left click roughly on the point on the curve where  $V_m$  should approximately lie.

Values of  $x_0$  and  $y_0$  will now appear on the terminal window.

Since we are finding  $V_m$ , therefore  $x_0 \sim y_0$  and hence  $x_0 = y_0 = V_m$ .

### For performing the transient analysis, the following code is required:

\*Model Description

.param temp=27

\*Including sky130 library files

.lib "sky130\_fd\_pr/models/sky130.lib.spice" tt

\*Netlist Description

XM1 out in vdd vdd sky130\_fd\_pr\_\_pfet\_01v8 w=0.84 l=0.15

XM2 out in 0 0 sky130\_fd\_pr\_\_nfet\_01v8 w=0.36 l=0.15

Cload out 0 50fF

Vdd vdd 0 1.8V

Vin in 0 PULSE(0V 1.8V 0 0.1ns 0.1ns 2ns 4ns)

\*simulation commands

```
.tran 1n 10n
```

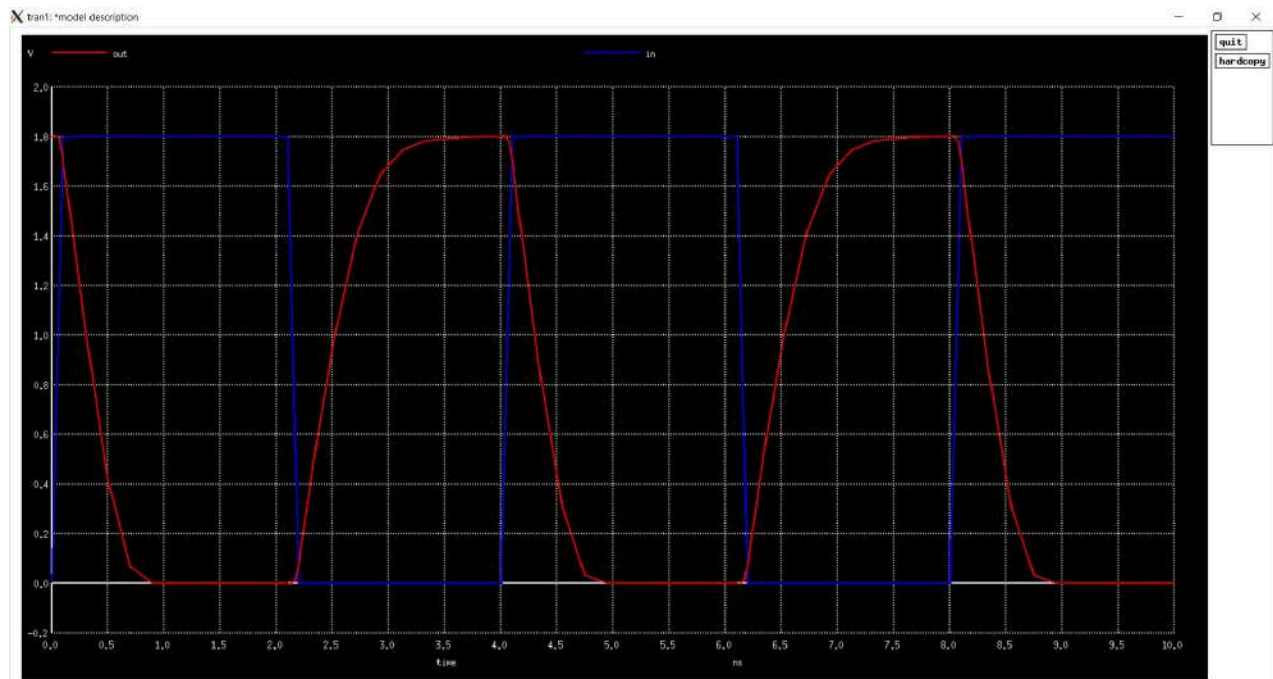
```
.control
```

```
run
```

```
.endc
```

```
.end
```

The snap shot of the terminal window for performing the transient analysis



**The snap shot of the output window for performing the transient analysis on NGSPICE**

To calculate the rise delay:

Zoom on the part of the curve having fall of the input pulse and rise of the output pulse around voltage of  $(V_{dd}/2)$  by right clicking on the screen and dragging it to select the area.

Now, left click on the rising edge of the output curve at  $(V_{dd}/2)$  to get a point  $x_0, y_0$  on the terminal.

Similarly, get the point at  $(V_{dd}/2)$  for falling edge of the input curve.

The difference between the x-coordinate of the rising edge of the output curve and the falling edge of the input curve is the rise delay.

To calculate the falling delay:

Zoom on the part of the curve having rise of the input pulse and fall of the output pulse around voltage of  $(V_{dd}/2)$  by right clicking on the screen and dragging it to select the area.

Now, left click on the falling edge of the output curve at  $(V_{dd}/2)$  to get a point  $x_0, y_0$  on the terminal.

Similarly, get the point at  $(V_{dd}/2)$  for rising edge of the input curve.

The difference between the x-coordinate of the falling edge of the output curve and the rising edge of the input curve is the fall delay.

# Static Behavior Evaluation - CMOS Inverter Robustness: Switching threshold

A CMOS inverter is a robust device because the shape of its input versus output curve remains the same for all different values of (W/L) ratios.

1. Static Behavior Evaluation: CMOS Inverter Robustness
2. Switching Threshold
3. Noise Margin
4. Power Supply Variation
5. Device Variation

## 1.CMOS Inverter Robustness:

CMOS inverter robustness refers to its ability to operate correctly under **real-world variations and disturbances** without producing logic errors. Key factors include:

- **Noise Margins (NMH/NML)** – Measure tolerance to unwanted voltage noise at logic levels.
- **PVT Variations** – Process, Voltage, and Temperature changes can shift switching thresholds and delay.
- **Glitch Immunity** – Ability to reject short transient pulses on the input.
- **Load Variations** – Stable operation despite changes in capacitive or resistive loading.
- **Supply Scaling** – Maintaining functionality when VDD changes, especially for low-power design.

A robust inverter maintains correct logic levels, adequate noise margins, and predictable timing **across all operating conditions**, ensuring reliability in large digital systems.

## 2.Switching Threshold (Vm)

The **switching threshold** of a CMOS inverter is the **input voltage** at which the inverter's **output voltage equals its input voltage**.

- At **Vm**, both the PMOS and NMOS transistors conduct significant current.
- It's the point where the inverter transitions from output HIGH to output LOW.
- Ideally, Vm is set near **VDD/2** for balanced noise margins and symmetrical switching speed.
- In the VTC (Voltage Transfer Characteristic) curve, it's the **midpoint of the steep transition region**.

### Formula :

For matched NMOS/PMOS parameters:

$$V_m \approx V_{DD} \cdot \frac{1}{2} \quad V_m \approx \frac{V_{DD}}{2}$$

but in real designs, Vm is influenced by **W/L ratios**, threshold voltages (Vt), and mobility differences between electrons and holes.

### Derivation FOR CMOS SWITCHING THRESHOLD(VM):

Vm when (Wp/Lp) is 1.5 is approximately equal to 0.98V and when (Wp/Lp) is 3.75 it is approximately equal to 1.2V

Wp and Lp in the above section are Width of PMOS channel and Length of PMOS channel

At Vm, both PMOS and NMOS are turned 'ON' because Vgs almost crossed the threshold region for both of them.

A few observations can be made from the information stated above,

Therefore,  $V_{gs} = V_{ds}$

$I_{dsP} = -I_{dsN}$  which means that  $I_{dsP} + I_{dsN} = 0$

We know the equations for  $I_{dsN}$  and  $I_{dsP}$  which are as stated below:

$$I_{dsN} = k_n \cdot \left[ ([V_m - V_t] \cdot V_{dsatN}) - \frac{V_{dsatN}^2}{2} \right]$$

$$I_{dsP} = k_p \cdot \left[ ([V_m - V_{dd} - V_t] \cdot V_{dsatP}) - \frac{V_{dsatP}^2}{2} \right]$$

We ignore the  $1+\lambda V_{ds}$  because the term is very small and it makes the equations very difficult for hand calculations.

Since,  $I_{dsP} + I_{dsN} = 0$

Therefore, the equations can be re-written as:

$$k_p \cdot \left[ ([V_m - V_{dd} - V_t] \cdot V_{dsatP}) - \frac{V_{dsatP}^2}{2} \right] + k_n \cdot \left[ ([V_m - V_t] \cdot V_{dsatN}) - \frac{V_{dsatN}^2}{2} \right] = 0$$

$$k_n \cdot \left[ ([V_m - V_t] \cdot V_{dsatN}) - \frac{V_{dsatN}^2}{2} \right] = k_p \cdot \left[ ([-V_m + V_{dd} + V_t] \cdot V_{dsatP}) - \frac{V_{dsatP}^2}{2} \right]$$

$$\therefore k_n \cdot V_{dsatN} \left[ ([V_m - V_t]) - \frac{V_{dsatN}}{2} \right] = k_p \cdot V_{dsatP} \left[ ([-V_m + V_{dd} + V_t]) - \frac{V_{dsatP}}{2} \right]$$

$$\therefore \frac{k_p \cdot V_{dsatP}}{k_n \cdot V_{dsatN}} = \frac{(V_m - V_t) - \frac{V_{dsatN}}{2}}{(-V_m + V_{dd} + V_t) + \frac{V_{dsatP}}{2}}$$

$$\therefore \frac{\left(\frac{W_P}{L_P}\right) \cdot k'_p \cdot V_{dsatP}}{\left(\frac{W_N}{L_N}\right) \cdot k'_n \cdot V_{dsatN}} = \frac{(V_m - V_t) - \frac{V_{dsatN}}{2}}{(-V_m + V_{dd} + V_t) + \frac{V_{dsatP}}{2}}$$

$$\therefore \frac{\left(\frac{W_P}{L_P}\right)}{\left(\frac{W_N}{L_N}\right)} = \frac{k'_n \cdot V_{dsatN} \cdot \left[(V_m - V_t) - \frac{V_{dsatN}}{2}\right]}{k'_p \cdot V_{dsatP} \cdot \left[(-V_m + V_{dd} + V_t) + \frac{V_{dsatP}}{2}\right]}$$

Here,

$W_P$  is the width of the channel in PMOS

$L_P$  is the length of the channel in PMOS

$W_N$  is the width of the channel in NMOS

$L_N$  is the length of the channel in NMOS

$k_n'$  is the process transconductance of the NMOS

$k_p'$  is the process transconductance of the PMOS

$V_{dsatn}$  is the  $V_{dsat}$  of the NMOS

$V_{dsatp}$  is the  $V_{dsat}$  of the PMOS

$V_m$  is the switching threshold voltage

$V_t$  is the threshold voltage

$V_{dd}$  is the supply voltage

**We experimented with the sizes of the PMOS with respect to the sizes of NMOS and came up with the following conclusions**

( $W_p/L_p$ )     $\times$  ( $W_n/L_n$ )    Rise Delay    Fall Delay

( $W_p/L_p$ )    1. ( $W_n/L_n$ )    148pS        71pS        0.99V

( $W_p/L_p$ )    2. ( $W_n/L_n$ )    80pS        76pS        1.2V

( $W_p/L_p$ )    3. ( $W_n/L_n$ )    57pS        80pS        1.25V

( $W_p/L_p$ )    4. ( $W_n/L_n$ )    45pS        84pS        1.35V

( $W_p/L_p$ )    5. ( $W_n/L_n$ )    37pS        88pS        1.4V

We can make some conclusions from the above table:

When ( $W_p/L_p$ ) = 2. ( $W_n/L_n$ ), there is an approximately equal rise-fall delay

Due to the equal rise-fall delay, ( $W_p/L_p$ ) = 2. ( $W_n/L_n$ ) create typical characteristics for a clock inverter/buffer

The conditions other than ( $W_p/L_p$ ) = 2. ( $W_n/L_n$ ) can still be used as regular inverters/buffers and these can be preferred for data path

Switching threshold for ( $W_p/L_p$ ) = 2. ( $W_n/L_n$ ) and ( $W_p/L_p$ ) = 3. ( $W_n/L_n$ ) is very small. Similarly, switching threshold for ( $W_p/L_p$ ) = 4. ( $W_n/L_n$ ) and ( $W_p/L_p$ ) = 5. ( $W_n/L_n$ ) is also very small

When  $W_p/L_p$  is increased, the rise delay is significantly reduced because time required for the output capacitor to charge decreases significantly and the reason is the availability of a bigger area to charge the capacitor.

$R_{on}(PMOS) \sim 2.5 * R_{on}(NMOS)$

### 3.CMOS Noise Margin Robustness:

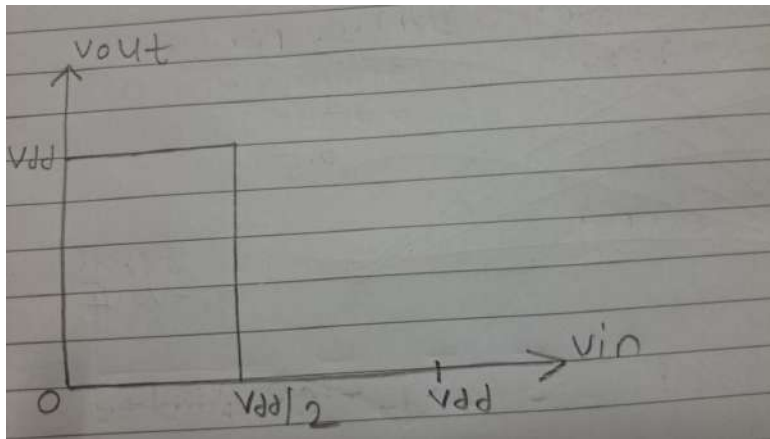
#### CMOS Noise Margin Robustness :

Noise margin robustness is the CMOS inverter's **ability to tolerate unwanted voltage noise** on its input without misinterpreting logic levels.

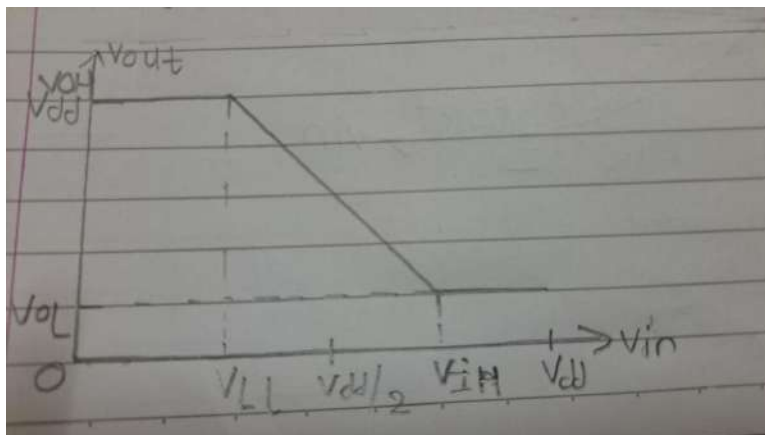
- **NMH (Noise Margin High)** → Max noise voltage a HIGH input can withstand before being seen as LOW.
- **NML (Noise Margin Low)** → Max noise voltage a LOW input can withstand before being seen as HIGH.
- Larger NMH/NML = more robust against interference, supply ripple, and crosstalk.
- Achieved by **balancing switching threshold** and designing for steep VTC slope.

Static Behavior Evaluation - CMOS Inverter Robustness: Noise Margin

The ideal and actual Input-Output characteristics of an inverter were observed



**ideal Input-Output characteristics of an Inverter**



**actual Input-Output characteristics of an Inverter with finite slope**

In the above diagram, the terms stated are explained as follows:

$V_{IL}$  is Input Low Voltage ( $V_{IL}$  could be  $V_{DD}/4$ )

Any input voltage level between 0 and  $V_{IL}$  will be treated as logic '0'

$V_{OH}$  is Output High Voltage ( $V_{OH} < V_{OH} \leq V_{DD}$ )

Any output voltage level between  $V_{OH}$  and  $V_{DD}$  will be treated as logic '1'

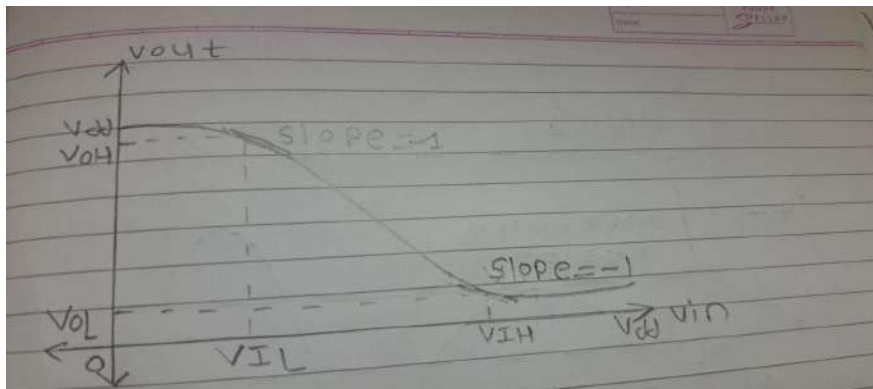
$V_{IH}$  is Input High Voltage ( $V_{IH}$  could be  $3.V_{DD}/4$ )

Any input voltage level between  $V_{IH}$  and  $V_{DD}$  will be treated as logic '1'

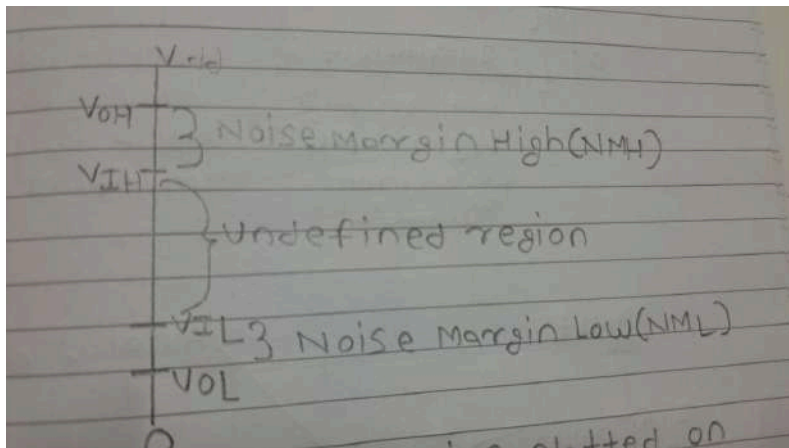
$V_{OL}$  is Output Low Voltage ( $0 \leq V_{OL} < V_{IL}$ )

Any output voltage level between 0 and  $V_{OL}$  will be treated as logic '0'

Actual Input-Output characteristics on an inverter were observed and they were plotted on a scale



#### Actual Input-Output characteristics of an Inverter



#### Noise induced bump characteristics at different noise margin levels

For any signal to be considered as logic '0' and logic '1', it should be in the NML and NMh ranges, respectively. - If the height of the bump lies in between  $V_{OL}$  and  $V_{IL}$  then it's not hazardous because it still lies in the range of logic '0'. Any glitch that occurs in this region is a safe glitch because it will still be considered as logic '0'. - If the height of the bump lies in the "undefined region" then it is potentially hazardous because it can acquire

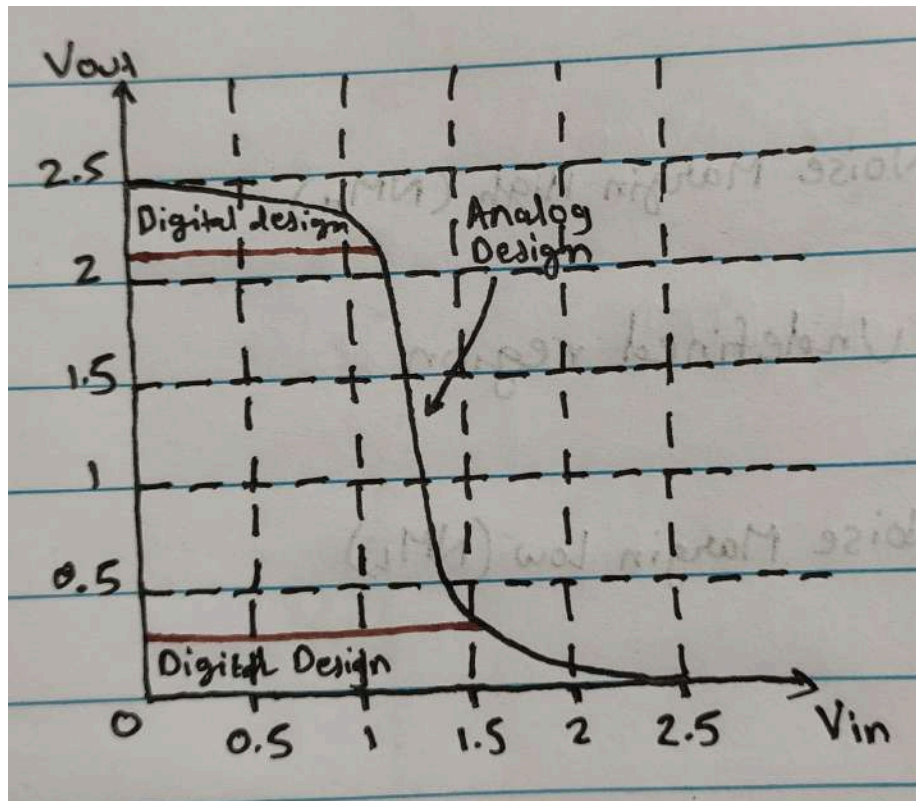
logic '1' which can be fatal. Any glitch in this region is unsafe because it is unclear if it will go to logic '1' or fall to logic '0'. - If the height of the bump lies in between  $V_{ih}$  and  $V_{oh}$  then it will definitely be considered as logic '1'. These kinds of glitches are the glitches that need to be fixed.

**Conclusions of noise margins of the inverter at different values of  $W_p/L_p$  were observed and they were as follows:**

$(W_p/L_p)$	$x.(W_n/L_n)$	NMh	NMl	$V_m$
$(W_p/L_p)$	$1.(W_n/L_n)$	0.3	0.3	0.99V
$(W_p/L_p)$	$2.(W_n/L_n)$	0.35	0.3	1.2V
$(W_p/L_p)$	$3.(W_n/L_n)$	0.4	0.3	1.25V
$(W_p/L_p)$	$4.(W_n/L_n)$	0.42	0.27	1.35V
$(W_p/L_p)$	$5.(W_n/L_n)$	0.42	0.27	1.4V

A few conclusions can be inferred from the above table: - When  $(W_p/L_p) = 2.(W_n/L_n)$  there is a rise at the NMh because PMOS is responsible for holding the charges on the capacitance. When the size of PMOS is increased, a low-resistance path from supply to the capacitance is formed and as a result of that, the capacitance is able to retain the charge for a longer amount of time resulting in an increased NMh. - When  $(W_p/L_p) = 4.(W_n/L_n)$  there is a drop at the NMl because the NMOS has now become weaker than the PMOS - When  $(W_p/L_p) = 5.(W_n/L_n)$  the NMh almost comes to a static point. - In the above table, NMl is not affected much but NMh has increased by 120mV but this range is still acceptable and this proves the CMOS inverter robustness with respect to the Noise Margin. - Finally, the areas that can be used for digital and analog applications are stated in the figure below:

**GRAPH Areas Fitted for digital and analog Designs:**



Vout versus Vin curve showing the areas that can be used for digital and analog applications



Lab Activity:

For performing the Day 4 Lab Activity we need the following code

\*Model Description

```
.param temp=27
```

\*Including sky130 library files

```
.lib "sky130_fd_pr/models/sky130.lib.spice" tt
```

\*Netlist Description

```
XM1 out in vdd vdd sky130_fd_pr__pfet_01v8 w=1 l=0.15
```

```
XM2 out in 0 0 sky130_fd_pr__nfet_01v8 w=0.36 l=0.15
```

```
Cload out 0 50fF
```

```
Vdd vdd 0 1.8V
```

```
Vin in 0 1.8V
```

\*simulation commands

```
.op
```

```
.dc Vin 0 1.8 0.01
```

```
.control
```

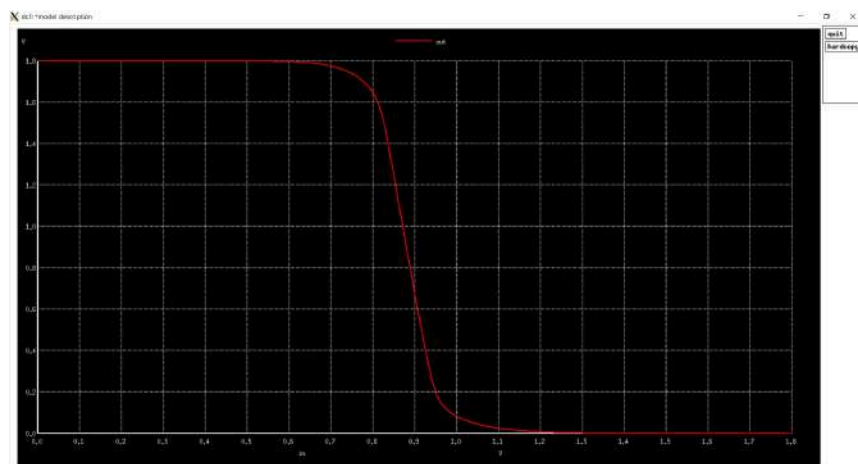
```
run
```

```
setplot dc1
```

```
display
```

```
.endc
```

```
.end
```



The snap shot of the output window for calculating the Noise Margins

Method to calculate the Noise Margins from the plot:

Run the ngspice command and open the plot

left click on the point towards the top of the graph where the curvature seems to be '-1'

In this case it was  $x_0 = 0.766667$ ,  $y_0 = 1.71351$

Now, left click on the point towards the bottom of the graph where the curvature seems to be '-1'

In this case it was  $x_0 = 0.977333$ ,  $y_0 = 0.110811$ . Let's consider these points as  $x_1$  and  $y_1$  thus making the coordinates  $x_1 = 0.977333$ ,  $y_1 = 0.110811$

For noise margin high we need  $V_{oh}-V_{ih}$  and in this case  $V_{oh}=y_0$  and  $V_{ih}=x_1$

For noise margin low we need  $V_{il}-V_{ol}$  and in this case  $V_{il}=x_0$  and  $V_{ol}=y_1$

Therefore, we get  $NM_h = 0.736177$  and  $NM_l = 0.655856$

## 4.CMOS Power supply:

- **Power-Supply Variations (VDD changes)**
  - Fluctuations in supply voltage (e.g., from 1.8 V down to 0.6 V in low-power designs).
  - Can affect switching threshold, noise margins, delay, and power consumption.
  - A robust design ensures functionality across the expected VDD range.

Whenever we move from 250nm nodes to lower nodes like 20nm or so on, we scale our supply voltage as well. For example, if things were working at 1V sometime back, now they will be operating at 0.7V

A CMOS inverter can be operated at 0.5V as well and it has its own advantages and disadvantages:

### **Advantages of using 0.5V supply:**

There is a significant increase in gain (close to 50% improvement)

There is a significant reduction in energy consumption (close to 90% improvement)

### **Disadvantages of using 0.5V supply:**

Performance impact (0.5V supply rising and falling edge is insufficient to completely charge or discharge the load capacitance)

Lab Activity:

To perform the lab activity for power supply scaling, we need the following code:

\*Model Description

.param temp=27

\*Including sky130 library files

.lib "sky130\_fd\_pr/models/sky130.lib.spice" tt

\*Netlist Description

XM1 out in vdd vdd sky130\_fd\_pr\_\_pfet\_01v8 w=1 l=0.15

XM2 out in 0 0 sky130\_fd\_pr\_\_nfet\_01v8 w=0.36 l=0.15

Cload out 0 50fF

Vdd vdd 0 1.8V

Vin in 0 1.8V

.control

let powersupply = 1.8

alter Vdd = powersupply

let voltagesupplyvariation = 0

dowhile voltagesupplyvariation < 6

dc Vin 0 1.8 0.01

let powersupply = powersupply - 0.2

```
alter Vdd = powersupply
```

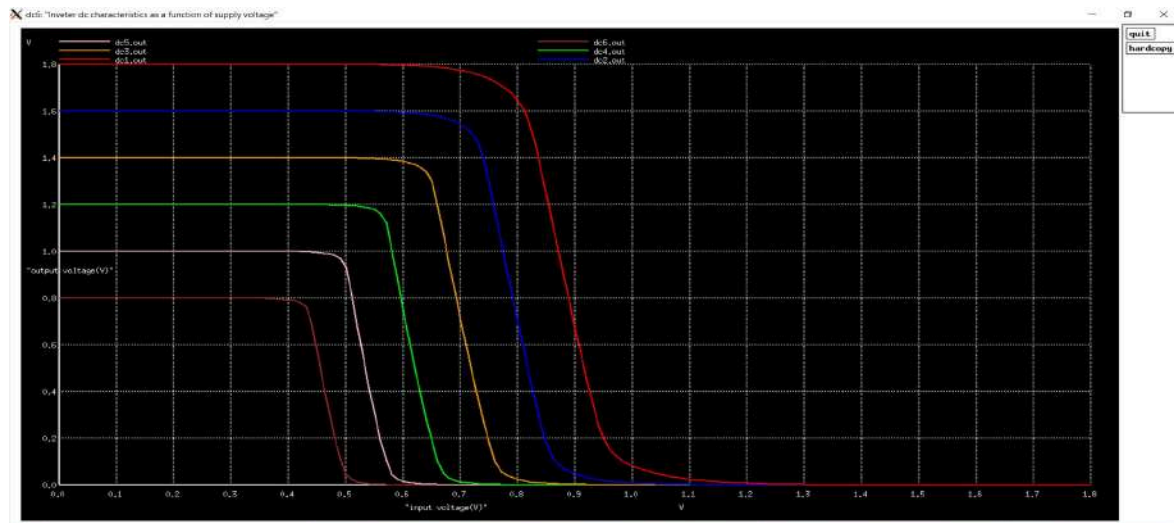
```
let voltagesupplyvariation = voltagesupplyvariation + 1
```

```
end
```

```
plot dc1.out vs in dc2.out vs in dc3.out vs in dc4.out vs in dc5.out vs in dc6.out vs in xlabel "input voltage(V)" ylabel "output voltage(V)" title "Inveter dc characteristics as a function of supply voltage"
```

```
.endc
```

```
.end
```



### The snap shot of the output window to observe the power supply variation

To calculate the gain for the given plot:

Select the curve for which the gain is to be calculated (In this case, we chose the plot for 1.8V Vdd)

Left click on the point where the slope of the curve is almost changing toward the top of the plot

The point obtained was  $x_0 = 0.766667$ ,  $y_0 = 1.71351$

Now, left click on the point where the slope of the curve is almost changing toward the bottom of the plot

The point obtained was  $x_0 = 0.982667$ ,  $y_0 = 0.1$  but for our convenience let us consider the coordinates of the point to be  $x_1$ ,  $y_1$

Therefore, the point becomes  $x_1 = 0.982667$ ,  $y_1 = 0.1$

Subtract  $y_1$  from  $y_0$ . So,  $y_0 - y_1 = 1.61351$

Subtract  $x_1$  from  $x_0$ . So,  $x_0 - x_1 = -0.216$

Now,  $\text{gain} = (y_0 - y_1) / (x_0 - x_1)$

Hence,  $\text{Gain}(g) = |(1.61351) / (-0.216)| = |-7.46995| = 7.46995$

## 5. Device Variation:

What was learnt:

**There are two sources for device variation:**

### 1. Etching Process Variation:

The etching process will define the structures in the layout of the CMOS inverter.

Etching is a very important fabrication step

It is the process that defines the structure (width and the height)

Based on the structures that get defined by the process, it directly impacts the delay

In layout of the CMOS inverter we have:

P-diffusion region which is indicated by green color.

Poly-silicon area which is indicated by red color.

Metal layer which is indicated by blue color.

N-diffusion region indicated by yellow color.

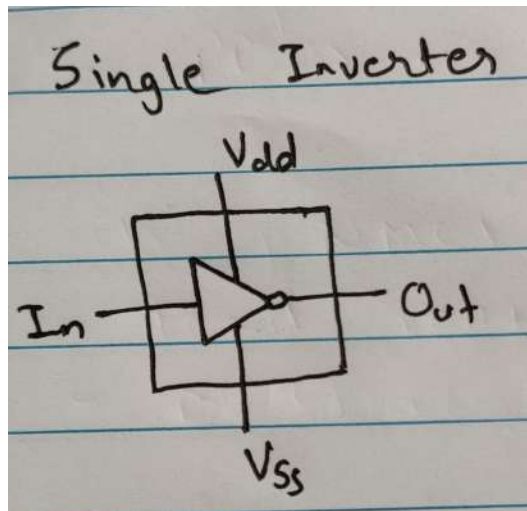
Contacts between two layers indicated by black crosses.

The thickness of the poly-silicon layer is the gate length and it defines at which node we are (20nm, 30nm, 45nm, etc.).

The thickness of the P-diffusion layer is the width of the gate of the PMOS and the thickness of the N-diffusion layer is the width of the gate of the NMOS.

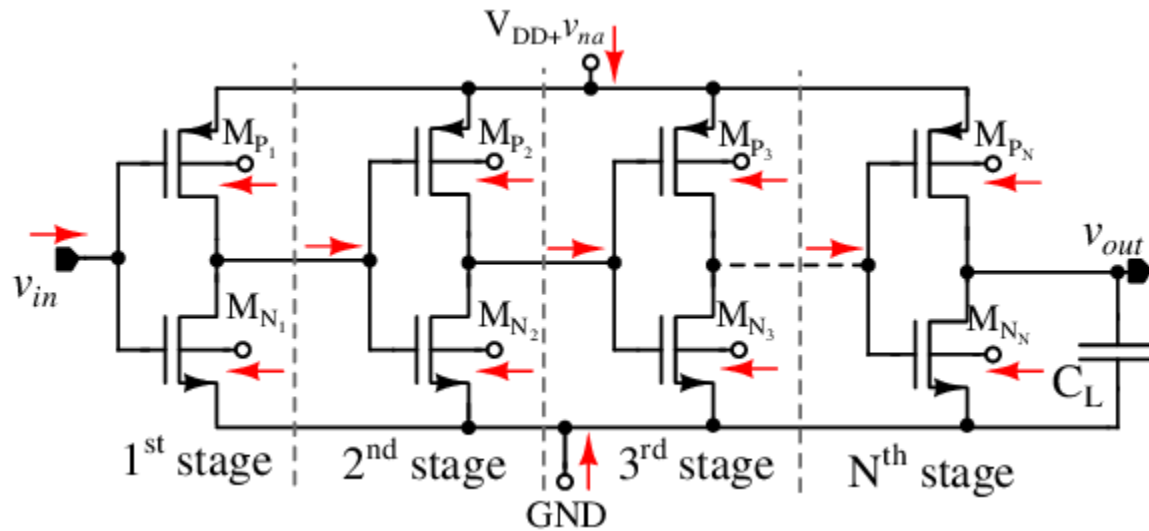
Width identifies the overlap area between the diffusion layer and the poly-silicon layer.

Fabrication is basically a lab where we have a lot of things like chemicals, water, gases, etc. running and due to these the ideal structure is distorted.



. The snap shot of the inverter chain

### Inverter Chain:



When inverters are connected back-to-back they are collectively called the "Inverter Chain".

In an inverter chain, the gates in the middle have the same structures on both sides. So, it's very likely that this particular gate structure will have a repeated distortion because they are exposed to the same kind of structures.

In an inverter chain, gates in the middle will have a structure which is different from the gates at the ends because they might be connected to different devices that will impact the gates

### 2.Oxide Thickness:

In an ideal oxidation process, the gate oxide thickness will be constant throughout the process.

In the real oxidation process, the gate oxide thickness will not be constant along the gate length.

In an inverter chain, the gate oxide thickness can vary for each transistor.

Oxide thickness directly affects the  $I_d$  equation because  $C_{ox}$  is dependent on it.

Strong PMOS:

PMOS with less resistance (possibly least resistance if the size chosen is the greatest size possible)

PMOS is wider in size (possibly widest PMOS available)

Weak NMOS:

NMOS with high resistance (possibly highest resistance if the size chosen is the least size possible)

NMOS is small in size (possibly smallest NMOS available)

Strong NMOS:

NMOS with less resistance (possibly least resistance if the size chosen is the greatest size possible)

NMOS is wider in size (possibly widest NMOS available)

Weak PMOS:

PMOS with high resistance (possibly highest resistance if the size chosen is the least size possible)

PMOS is small in size (possibly smallest PMOS available)

With the variation from Weak PMOS - Strong NMOS to Strong PMOS - Weak NMOS, the switching threshold varies from roughly 0.7V to 1.4V which is fairly acceptable because behavior of the inverter is intact

We can plot the variation if we move from Weak PMOS - Strong NMOS to Strong PMOS - Weak NMOS using SPICE simulation and the plot is given below:

From the plot given above, we can make the following conclusions:

Variation in Noise Margin high (NMh) is roughly from 2.5V to 2.1V which is a variation of 400mV which is good enough to filter out high voltage variations

Variation in Noise Margin low (NML) is roughly from 0V to 0.3V which is a variation of 300mV which is good enough to filter out low voltage variations

Overall, variation in the Noise margins is low and this leaves the operation of the gate intact.

Lab Activity:

To perform the lab activity for device variation, we need the following code:

\*Model Description

.param temp=27

\*Including sky130 library files

.lib "sky130\_fd\_pr/models/sky130.lib.spice" tt

\*Netlist Description

XM1 out in vdd vdd sky130\_fd\_pr\_\_pfet\_01v8 w=7 l=0.15

XM2 out in 0 0 sky130\_fd\_pr\_\_nfet\_01v8 w=0.42 l=0.15

Cload out 0 50fF

Vdd vdd 0 1.8V

Vin in 0 1.8V

\*simulation commands

.op

.dc Vin 0 1.8 0.01

.control

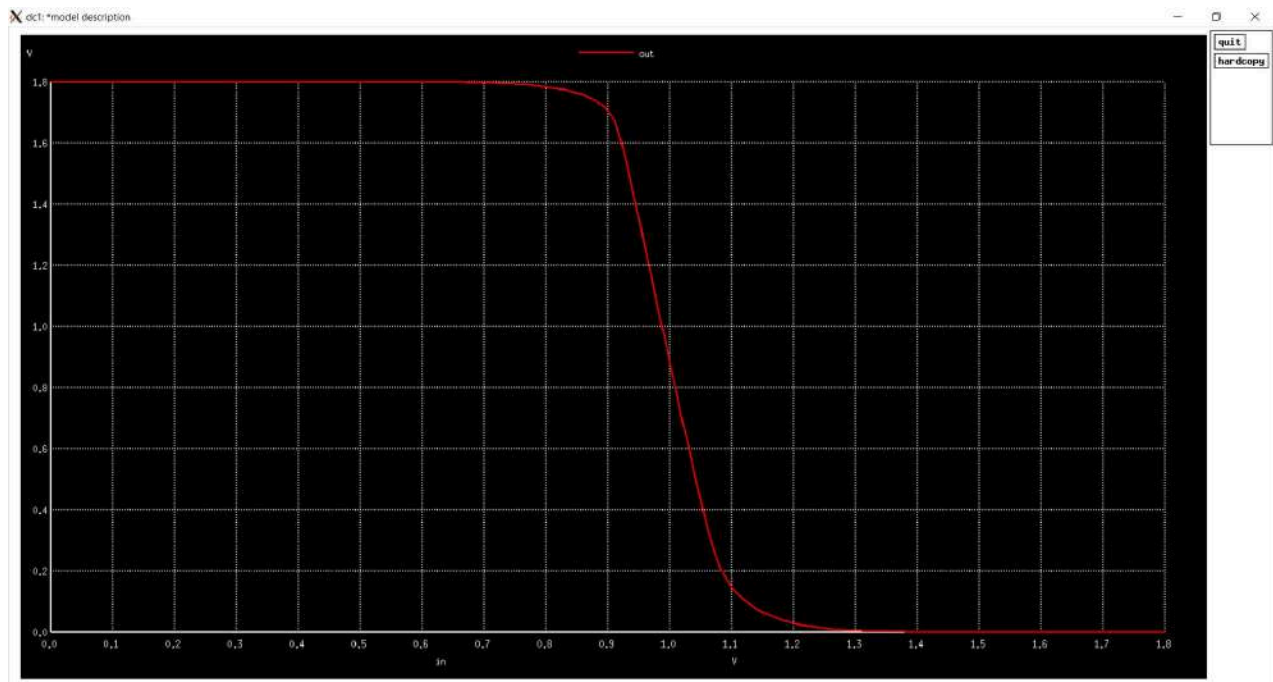
run

setplot dc1

display

.endc

.end



### The snap shot of output window to observe device variation

Since the pfet width is very huge as compared to the nfet width, the plot is shifted towards right

To find the value of the switching threshold:

Zoom in on the plot where  $V_{in} \sim V_{out}$  by right clicking and dragging the cursor to select the area

Zoom until the value of switching threshold becomes almost certain

Left click on the point where  $V_{in}$  is roughly equal to  $V_{out}$

A point  $x_0 = 0.988209$ ,  $y_0 = 0.988191$  is obtained

Since  $x_0 \sim y_0$ . Therefore, Switching Threshold Voltage =  $V_m = x_0 = y_0 = 0.988V$



## Conclusion:

During this course, I gained in-depth knowledge of **MOSFETs** and the **CMOS inverter**, exploring various techniques to modify inverter characteristics. I learned how to create a **SPICE deck** from a netlist, run simulations, and analyze results effectively. Understanding the **CMOS voltage transfer characteristics** and the factors influencing them greatly improved my grasp of static behavior evaluation, including all its sub-categories such as noise margins, switching threshold, and robustness analysis.

The **Lab Activities** were especially valuable, allowing me to experiment with parameter variations in SPICE and observe their direct impact on performance plots. This hands-on approach not only solidified my theoretical understanding but also built my confidence in applying these concepts to practical circuit design.

Overall, this workshop significantly strengthened my fundamentals in MOSFET operation, CMOS design, and SPICE simulation workflows. It also sparked a deeper interest to further master device-level design and analysis. My experience with **VLSI System Design** was exceptional, thanks to their continuous guidance, quick doubt-resolution, and practical learning approach.

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