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Suyash's Linkedin

Suyash Gadhave

OBJECTIVE

Seeking a Physical Design Engineer role in an innovative environment where I can apply my hands-on expertise in back-end flow implementation to design and optimize efficient hardware across advanced technology nodes. Passionate about developing new methodologies to enhance VLSI design efficiency and drive advancements in the semiconductor industry.

WORK EXPERIENCE

➢ PRAGMATIC SILICON — Sep 2024 - Present

Physical Design Engineer & STA

- ❖ Executed full RTL-to-GDSII flow on 7nm, 14nm, and 28nm nodes, ensuring 100% DRC/LVS signoff.
- ❖ Engineered and refined TSPC flip-flops (45nm) in Cadence Virtuoso, reducing delay by 15%.
- ❖ Performed timing closure by resolving 100+ setup/hold violations using buffer insertion, cell sizing, and path optimization.
- ❖ Conducted sign-off checks (DRV, DRC, IR drop, max transition, max capacitance), improving power integrity by 20%.
- ❖ Implemented ECO changes to fix 50+ congestion and routing issues, legalized 1.2M cells, and ensured clean routing.
- ❖ Collaborated with the clock team to optimize clock structures, reducing skew by 30% for better timing performance.
- ❖ Optimized power grid connectivity, reducing IR drop by 10% and enhancing overall design robustness.
- ❖ Executed comprehensive signoff methodologies, achieving 100% DRC/LVS clean.

➢ VLSIGURU TRAINING INSTITUTE — Feb 2024 – Sep 2024

Physical Design Trainee

- ❖ Designed and deployed multi-voltage domains, optimizing power grid (rings, straps, rails) to reduce IR drop by 15% and mitigate EM violations by 25%.
- ❖ Debugged voltage area violations, improving design integrity and reducing re-spins by 40%.
- ❖ Optimized macro placement and clock tree synthesis, reducing congestion by 25% and achieving clock skew <10ps.
- ❖ Performed physical verification (DRC, LVS, IR drop, EM analysis), ensuring a 100% tapeout-ready design.

➢ GE HEALTHCARE — Jul 2023 – Jun 2024

FPGA INTERN

- ❖ Migrated FPGA design by updating 200+ RTL modules and modifying pin configurations, ensuring 99.5% functional accuracy and seamless integration into the new FPGA architecture.
- ❖ Performed verification and validation of subsystems, ensuring 99.5% functional accuracy with the updated FPGA.
- ❖ Automated verification processes using Tcl/Python scripts, reducing test cycle time by 30% and improving debugging efficiency by 40%.
- ❖ Developed scripts for signal monitoring and validation, streamlining debugging and design verification, and reducing manual effort by 50%.
- ❖ Collaborated with the team to ensure a smooth transition from the obsolete FPGA to the new architecture, contributing to a 20% reduction in project delivery time.

SKILLS

Core Competencies : ASIC Design, Physical Design, VLSI Design, Power Distribution, Clock Tree Synthesis, Timing Closure, Signal Integrity
Programming Languages : C, C++ and Verilog
Tools & Technologies : ICC2, Design Compiler, Fusion Compiler, Xilinx ISE, Quartus Prime, Model Sim, Cadence Genus, Cadence Innovus, Cadence Virtuoso, Magic Tools, Ng Spice, PyCharm, LT Spice, Latex & AutoCAD.
Scripting : Tcl, Shell & Python

EDUCATION

✓ **Manipal Institute of Technology** – M.Tech Microelectronics | **CGPA: 7.51** | 2024
✓ **KBT College of Engineering** – B.E. Instrumentation & Control | **CGPA: 7.22** | 2021
✓ **Hande Deshmukh Hitech School & Jr. College** – XII | **63.08%** | 2016
✓ **Chaitanya Vidyalaya** – X | **82.60%** | 2014

ACADEMIC PROJECTS

1. **Design of Efficient Multiply-Accumulate Unit for Convolutional Neural Networks.**
   Constructed a neural network in Xilinx Vivado with customizable layers, integrating TensorFlow-generated weights and Verilog-based MAC units.
2. **Implementation of low power Convolutional Neural Network for Real Time application**
   Developed a low-power Convolutional Neural Network (CNN) using Xilinx ISE, optimizing MAC units and validating performance in Vivado.
3. **Implementation of Synchronous FIFO**
   Engineered and implemented a FIFO buffer with synchronized read/write pointers, ensuring efficient first-in-first-out data handling.

CONFERENCE PAPERS

- Design of Efficient Multiply-Accumulate Unit for Convolutional Neural Networks.(IOP-23)
- Implementation of low power Convolutional Neural Network for Real Time application. (ICCMEH-24)

CERTIFICATIONS & TRAININGS

- SoC Design Methodology using Intel FPGA, Workshop held at NIT, Surathkal, December 2022
- Cadence EDA tool for Chip Design (Analog RF and Digital Flow), Hands-on training on Cadence EDA tool for Chip Design. November 2022
- 1 Year Diploma of Information Technology under the program of Skill India. - May 2015
- Good extracurricular involvement in college including tech and non-tech events.