


# Suyash Mahar

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## Education

- Indian Institute of Technology, Roorkee** Roorkee, India  
*B.Tech., Electronics and Communication Engineering (GPA: 9.149/10)* July 2016 - Present
  - Coursework includes: Computer Architecture, Digital Logic Design, Data Structures & Algorithms.

## Experience

- Digital Electronics Laboratory** IIT Roorkee, India  
*Short term project* May 2016 - June 2016
  - Studied and implemented CORDIC algorithms on FPGA.
  - Used Python (Jupyter notebook) for modeling and Verilog for design and implementation.

## Awards and Achievements

- International Cyber Olympiad (SilverZone)** Dec. 2014  
*Olympiad Rank 11, State Rank 1*
- Joint Entrance Examination, Advanced (Indian Institute of Technology)** May 2016  
*All India Rank 1387, 99.3 percentile*
- Dedicated member award, National Service Scheme (IIT Roorkee) April 2017

## Skills

**Languages:** C++, (System)Verilog, C#/VB.NET, L<sup>A</sup>T<sub>E</sub>X, Java, Bash

**Applications:** MatLab, Vivado, Visual Studio 2017, Android Studio, Jupyter notebooks

**Languages:** English, Hindi

## Interests

**Academic:** Computer Architecture, Digital logic design, FPGA applications, Operating systems.

**Computers:** Currently maintains two applications on GitHub (Android and Windows).

**Campus Groups:** Active member of [Mobile Development Group](#) and Astronomy Club.