

# Suyash Mahar

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[suyashmahar.me](https://suyashmahar.me) 🌐

## Education

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- **Indian Institute of Technology, Roorkee** Roorkee, India  
*B.Tech., Electronics and Communication Engineering (CGPA: 9.149/10) July 2016 - Present*
  - Coursework includes: Computer Architecture, Digital Logic Design, Data Structures & Algorithms and Semiconductor Devices

## Experience

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- **Design of efficient FIB table for NDN routers** IIT Roorkee, India  
*Undergraduate Research Project July 2017 - present*
  - Working under [Prof. Vaskar Raychoudhury](#) and Divya Saxena on ways to accelerate FIB look ups in NDN routers using re-configurable hardware
  - Work includes search and FPGA implementation of data structure for longest prefix matching
- **FPGA implementation of CORDIC algorithms** IIT Roorkee, India  
*Short term project May 2017 - June 2017*
  - Studied and implemented CORDIC algorithms on FPGA under [Prof. Bishnu Prasad Das](#)
  - Used Python (Jupyter notebook) for modeling and Verilog for design and implementation
- **Single cycle 32-bit RISC processor**  
*Hobby project June 2017*
  - Created a simple implementation of 32-bit MIT 6.004 architecture with improvements and additions

## Awards and Achievements

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- Dedicated member award, National Service Scheme (IIT Roorkee) *April 2017*
- **Joint Entrance Examination, Advanced (Indian Institute of Technology)** *May 2016*  
*All India Rank 1387, 99.3 percentile*
- **International Cyber Olympiad (SilverZone)** *Dec. 2014*  
*Olympiad Rank 11, State Rank 1*

## Skills

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**Languages:** (System)Verilog, C++, SPICE, L<sup>A</sup>T<sub>E</sub>X, Python, C#/VB.NET, Java, Shell

**Software:** Vivado, MatLab, Visual Studio 2017, Android Studio

**Languages:** English, Hindi

## Interests

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**Academic:** Computer Architecture, Re-Configurable Computing, Embedded systems

**Computers:** Currently maintaining two applications on GitHub (Android and Windows)

**Campus Groups:** Active member of IEEE Special Interest Group and Mobile Development Group