Suyash Mahar

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Education

- **Indian Institute of Technology, Roorkee** — Roorkee, India
  B.Tech., Electronics and Communication Engineering (GPA: 9.15/10) — *Jul. 2016 - Present*
  - Relevant courses: Digital Logic Design, Data Structures & Algorithms and Semiconductor Devices

Projects

- **Indian Institute of Technology, Roorkee** — Roorkee, India
  Digital Electronics Lab — *May 2016 - Jun. 2016*
  - Implemented CORDIC algorithms on FPGA
  - Used Python (Jupyter notebook), MatLab for modeling of algorithms and Vivado design suite for design and implementation in FPGA.

Awards and Achievements

- **Joint Entrance Examination, Advanced 2016 (Indian Institute of Technology)** May 2016
  All India Rank 1387, 99.3 percentile

- **International Cyber Olympiad (SilverZone)** Dec 2014
  Olympiad Rank 11, State Rank 1

Skills

Languages: C++, Verilog, C#.NET, LaTeX, Java, VB.NET, Python

Operating Systems: Linux (Debian), Windows 8/10

Applications: MatLab, Vivado, LaTeX, Jupyter Notebooks, MS Office 2016, Visual Studio 2017, Android Studio

Miscellaneous: Strong verbal and written communication skills, excellent debugging skills

Interests

Academic: Computer architecture and microprocessors, Digital logic design

Computers: Currently maintains two applications on GitHub (Android and Windows)

Campus Groups: Active member of Mobile Development Group and Astronomy Club

GitHub Profile: https://github.com/suyashmahar