DDR3 DRAM

Suyash Mahar

suyash12mahar@outlook.com

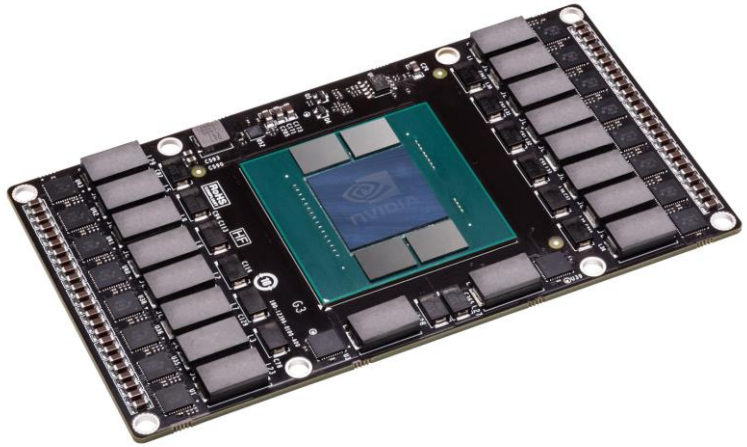
What's with the acronyms?

Double Data Rate

On both clk edges!

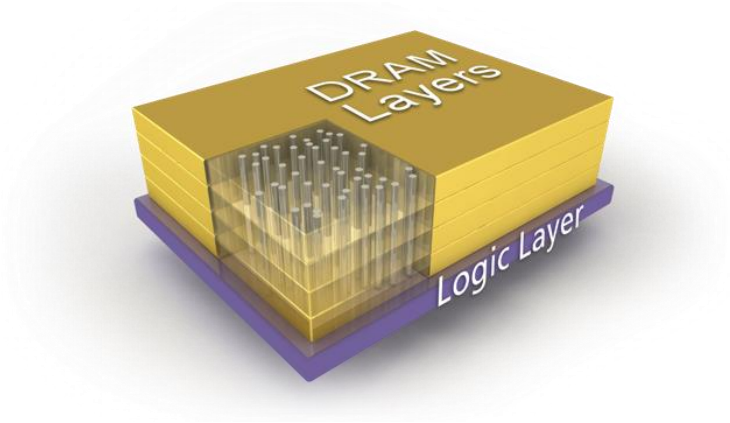
Dynamic Random Access Memory

Common types of DRAM



GDDR – Graphics memory

Photo courtesy: wccftech.com



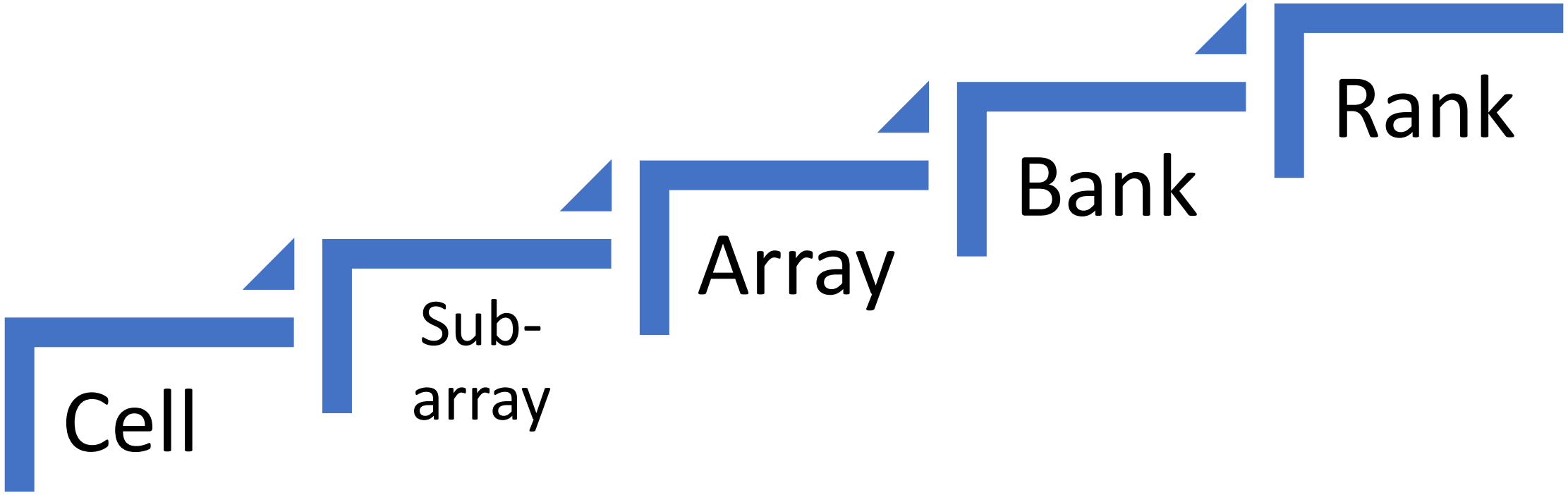
HMC – Hybrid memory cube

Photo courtesy: gigaom.com

DDR – Commodity PC/Server RAM

Photo courtesy: Crucial Technology www.crucial.com

DDR3 Hierarchy



DRAM Cell

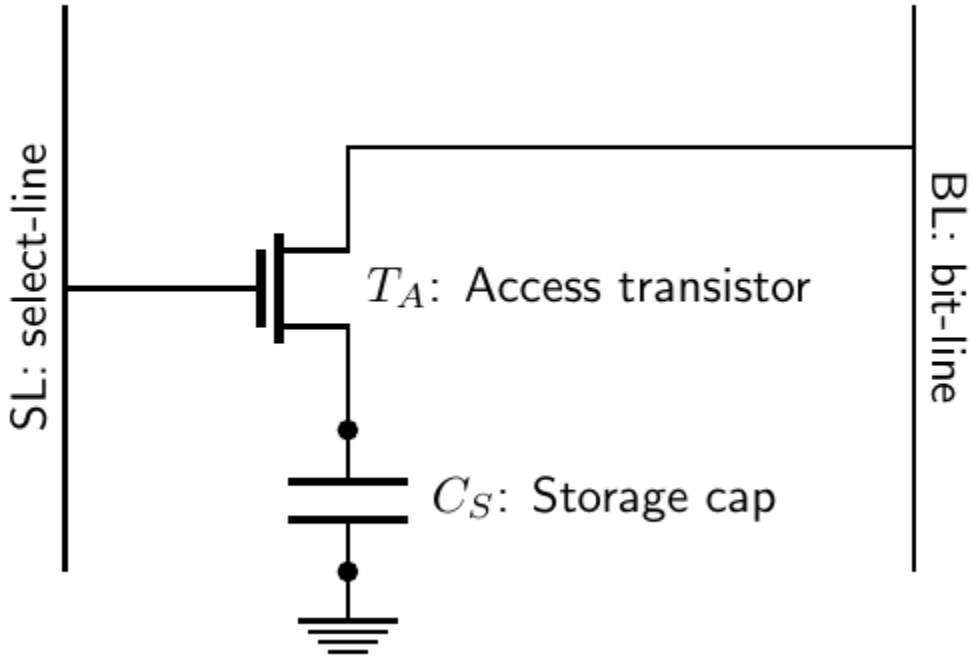


Fig. 1 Single DRAM cell.

cell
sub-arrays
row-buffers
array
bank
rank

DRAM Sub-Array

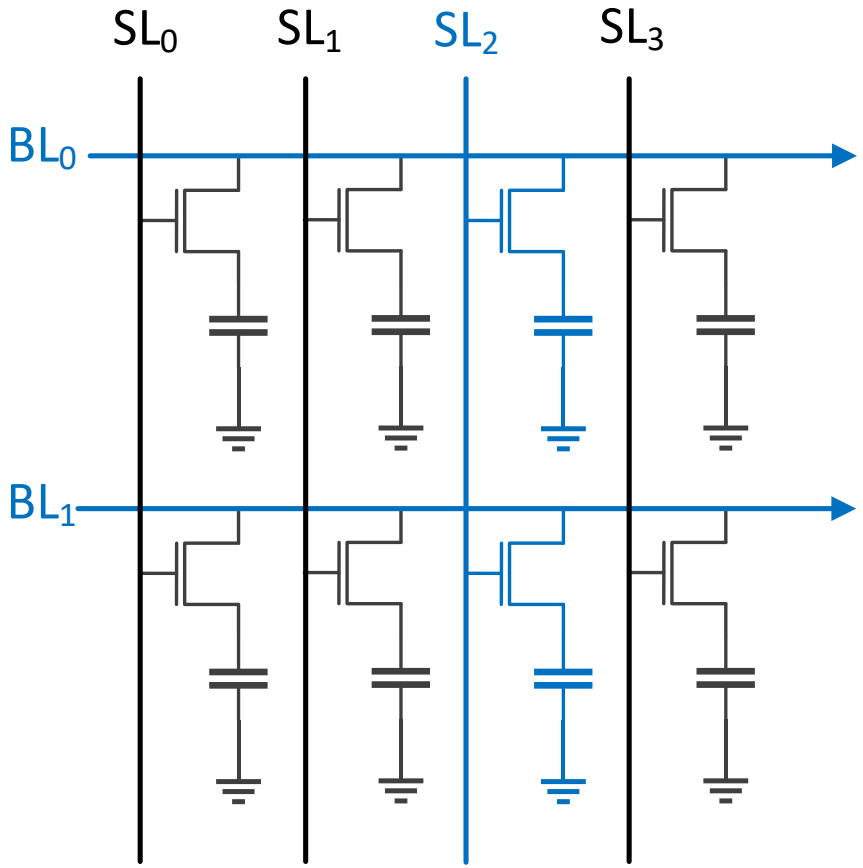


Fig. 2 Example of DRAM Cell Array of size 4x2 with SL_2 active.

cell
sub-array
row-buffers
array
bank
rank

Sub array Equivalent diagram

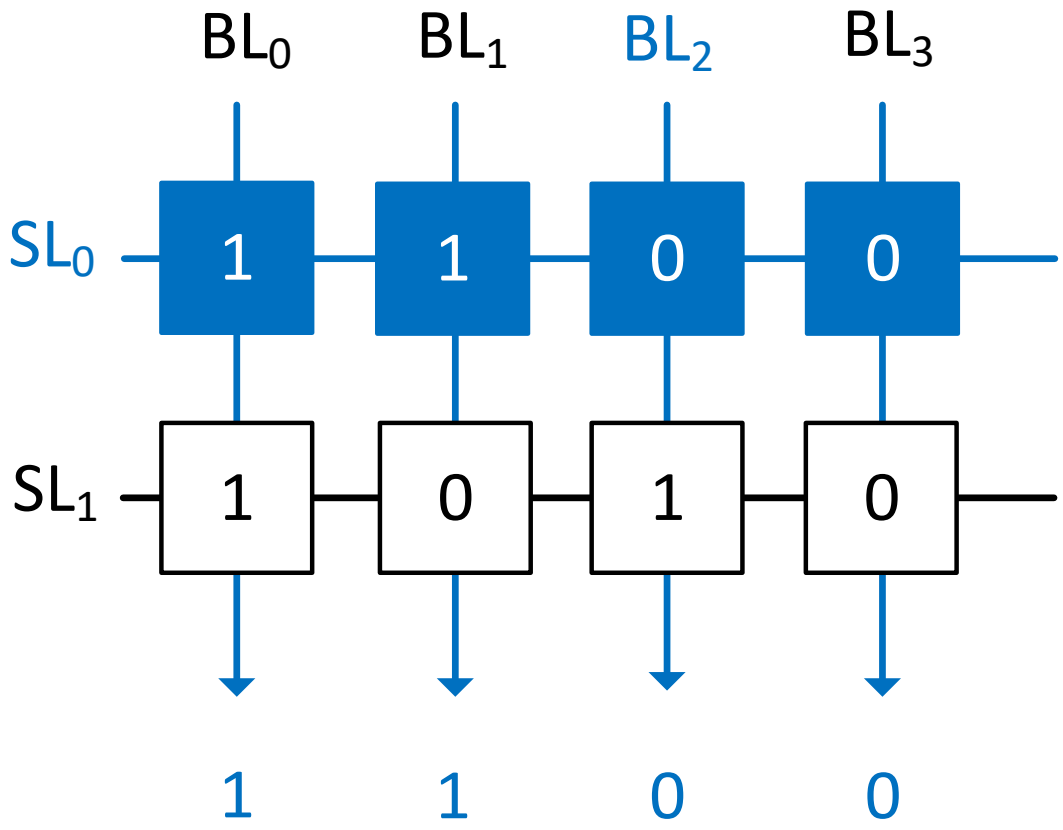


Fig. 3 Equivalent DRAM Cell Array of size 2X4 with SL_0 active.

cell
sub-array
row-buffers
array
bank
rank

Array representation

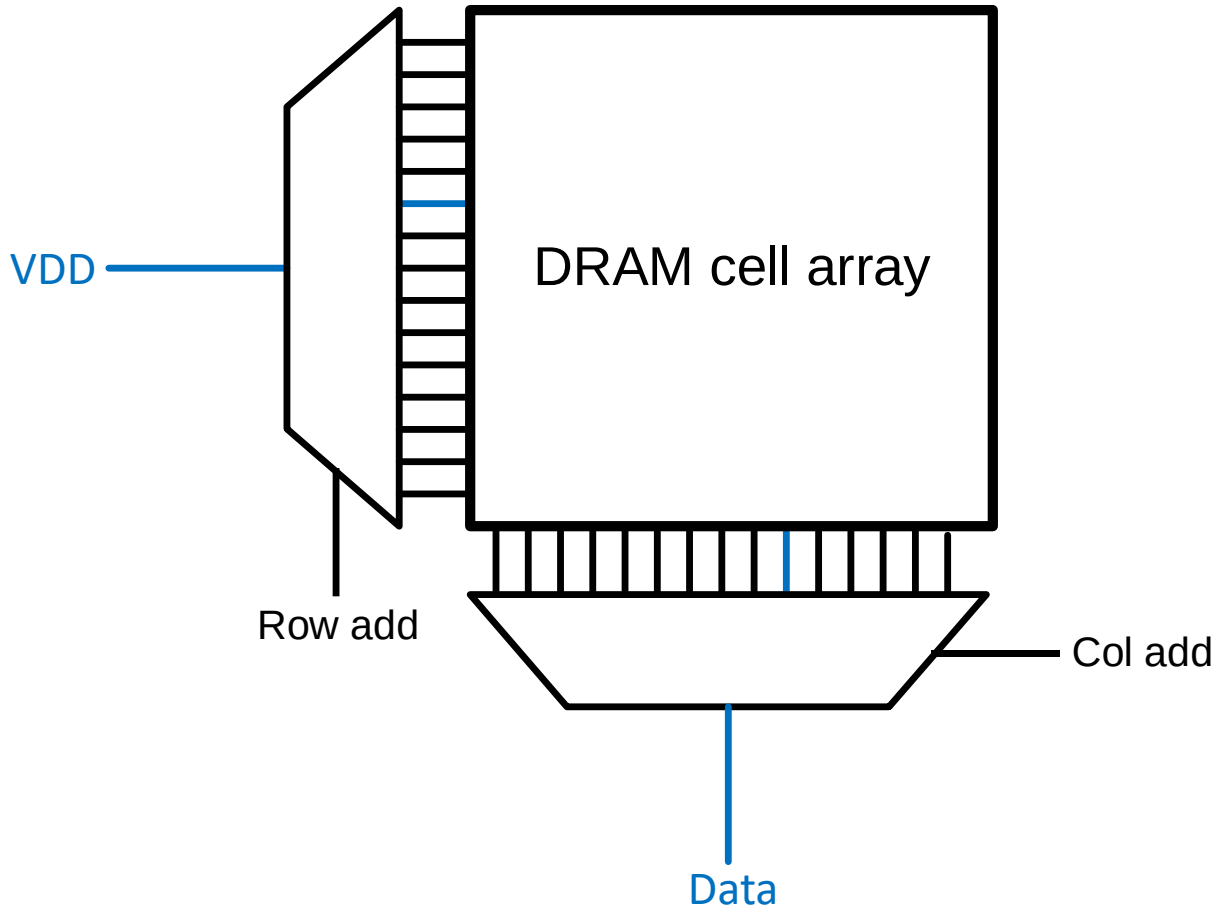


Fig. 4: DRAM sub-array with row buffers to store values read from cells.

cell
sub-arrays
row-buffers
array
bank
rank

Row Buffers

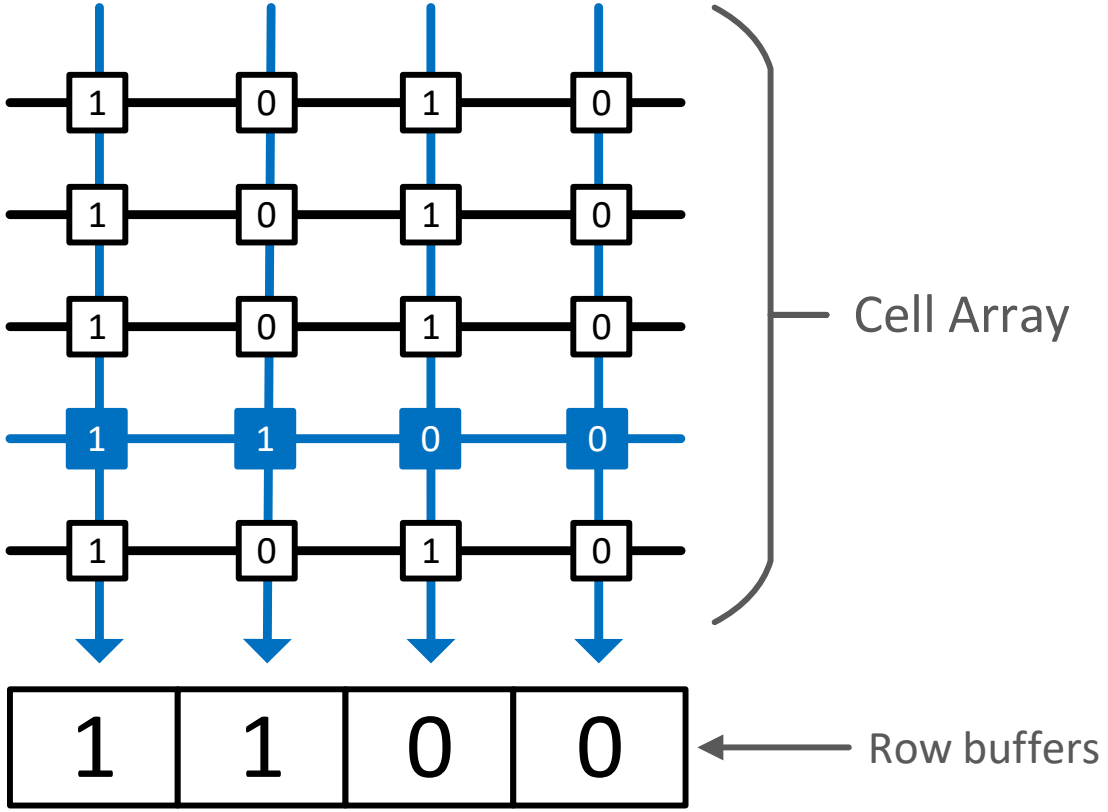


Fig. 4: DRAM sub-array with row buffers to store values read from cells.

cell
sub-arrays
row-buffers
array
bank
rank

Array

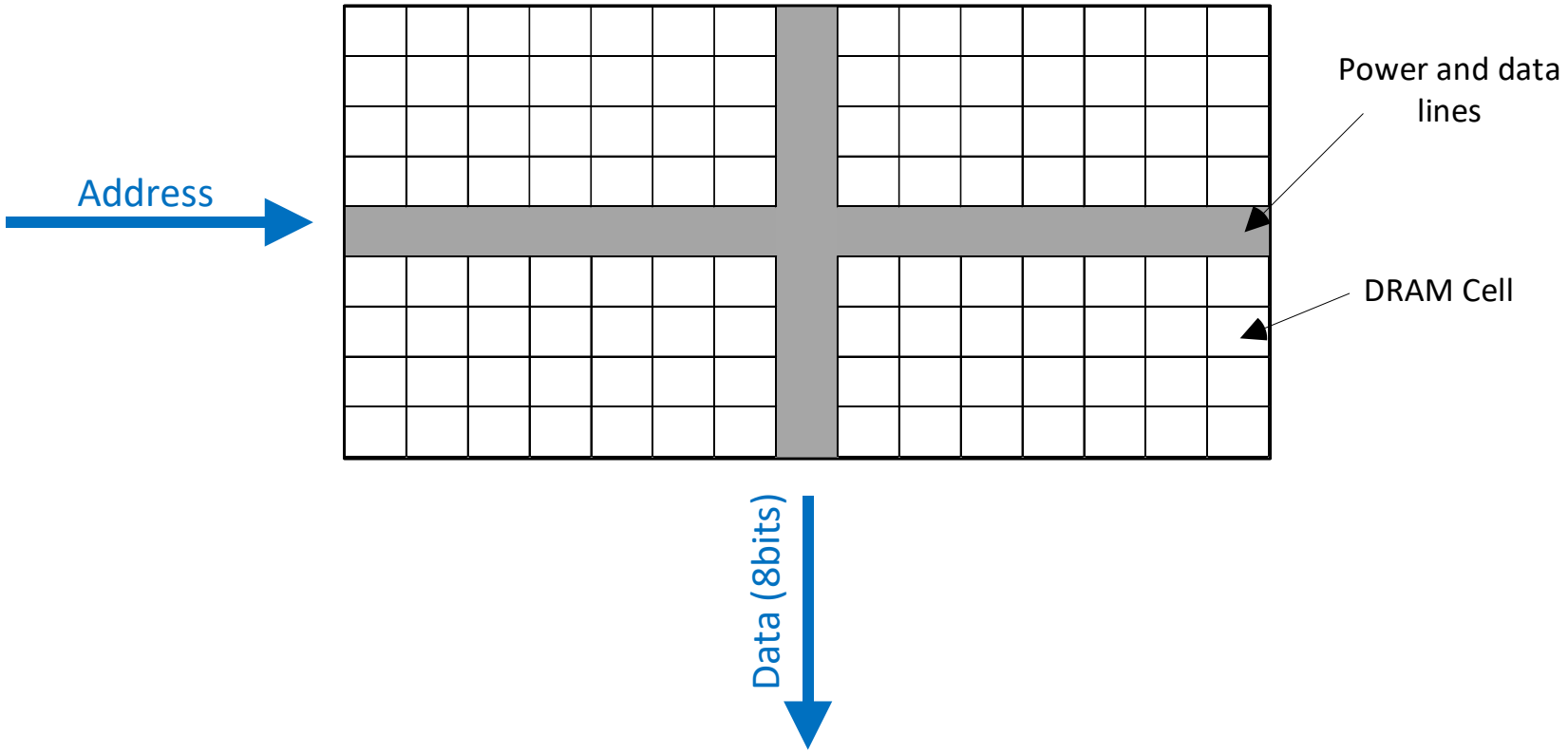
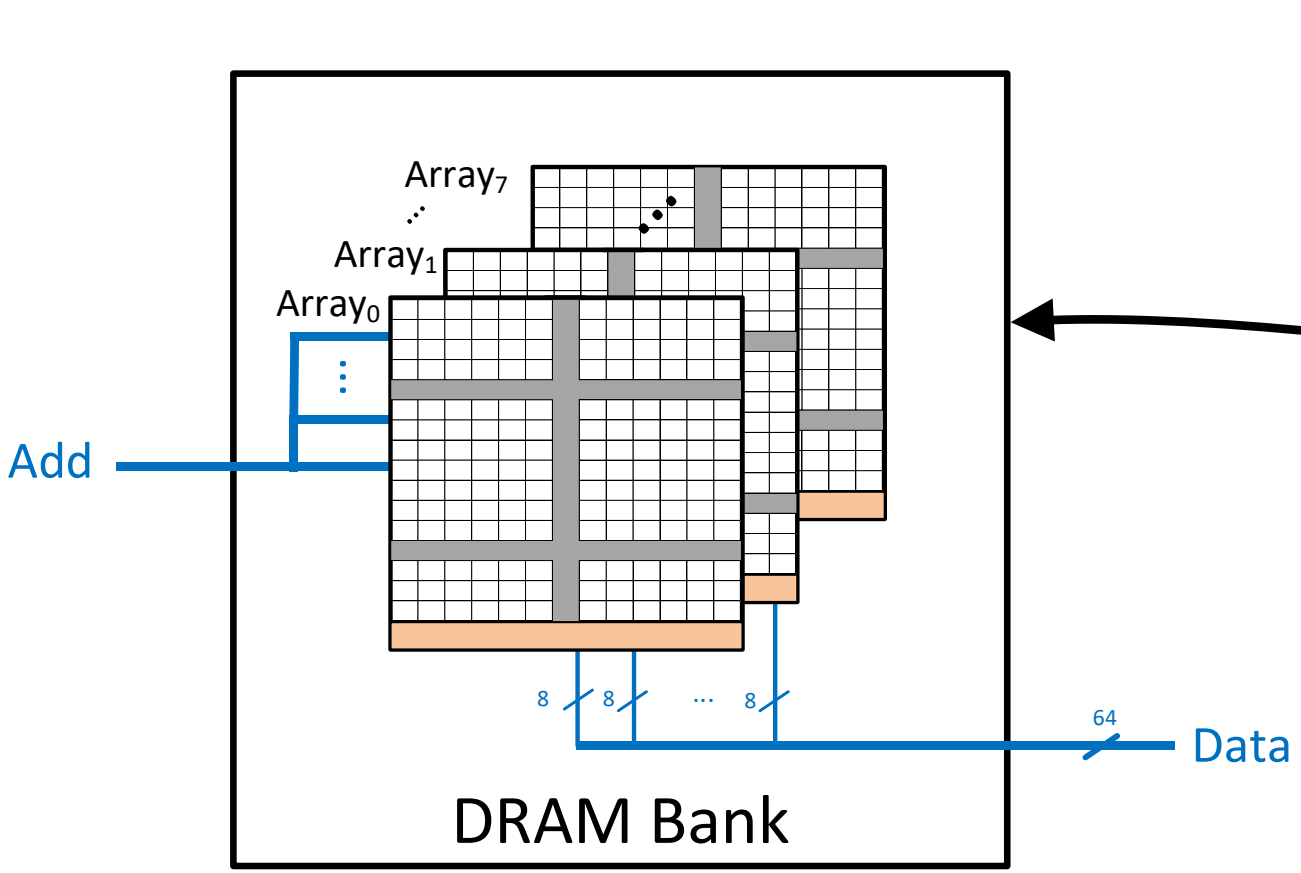
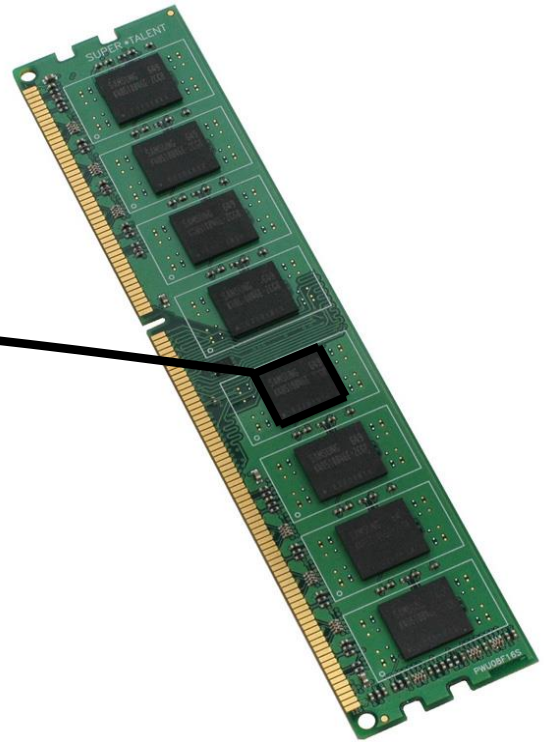


Fig. 5: Array of DRAM cells, output of this array is a single word of size 16 bit[1]

cell
sub-arrays
row-buffers
array
bank
rank

DRAM Bank





DDR3 DRAM Stick

Photo courtesy: www.extremetech.com

cell
sub-array
array
bank
rank
DIMM

Fig. 6: Organization of DRAM bank

DDR3 module

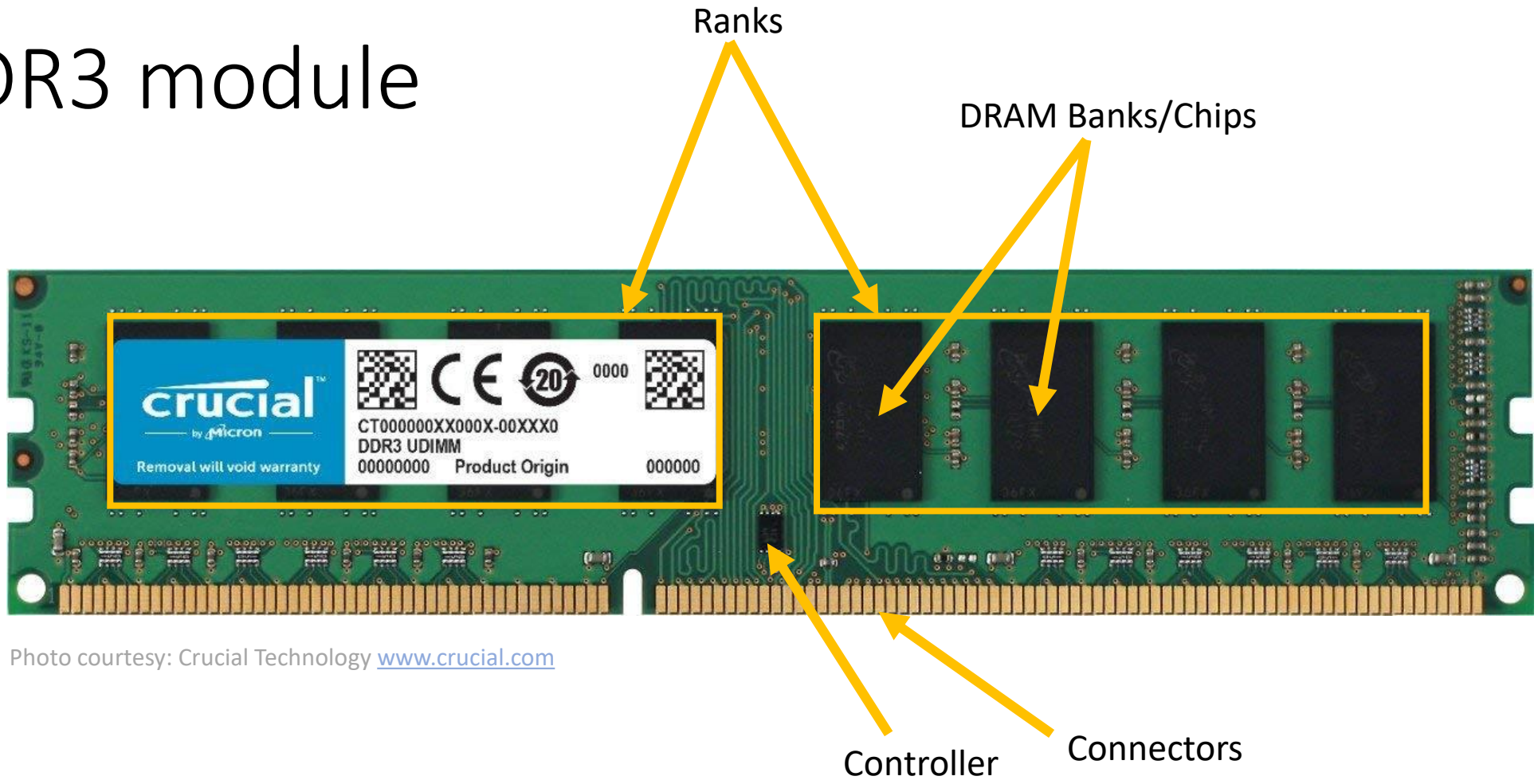


Photo courtesy: Crucial Technology www.crucial.com

Fig. 7: DIMM – Dual Inline memory module

cell
sub-array
array
bank
rank
DIMM

What's the future of DDR3?

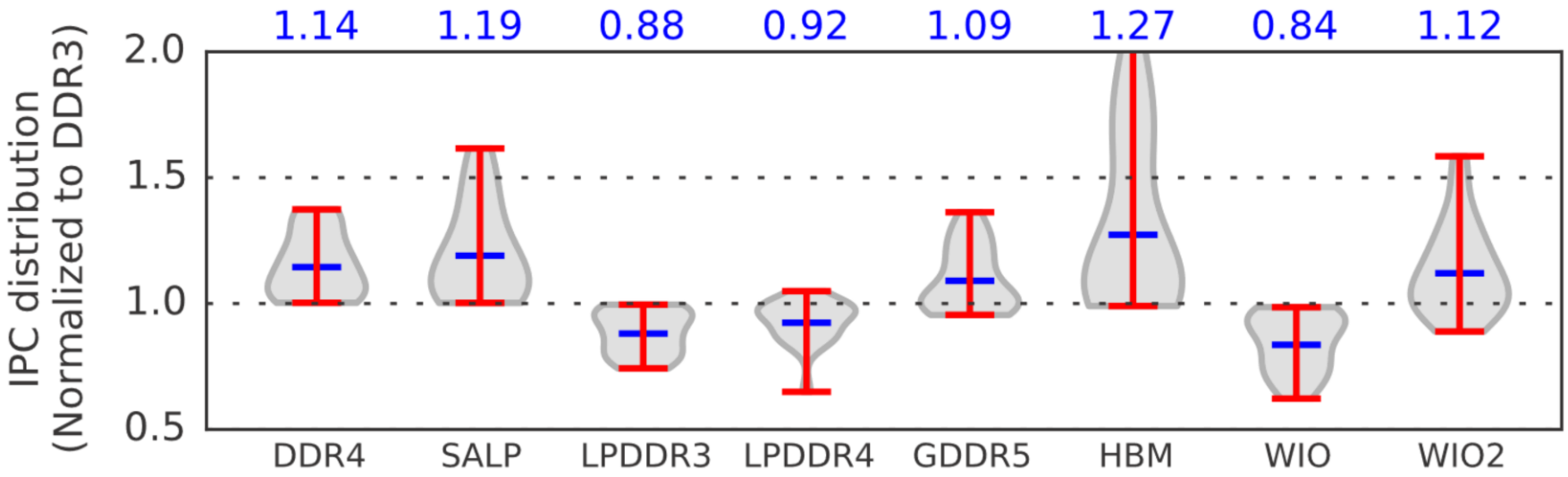


Fig. 8: Performance comparison of DRAM standards.[3]

Reference

1. T. Vogelsang, "Understanding the Energy Consumption of Dynamic Random Access Memories," *2010 43rd Annual IEEE/ACM International Symposium on Microarchitecture*, Atlanta, GA, 2010, pp. 363-374. doi: 10.1109/MICRO.2010.42
2. JEDEC, "DDR3 SDRAM standard", July 2012.
3. Y. Kim, W. Yang and O. Mutlu, "Ramulator: A Fast and Extensible DRAM Simulator," in *IEEE Computer Architecture Letters*, vol. 15, no. 1, pp. 45-49, 1 Jan.-June 2016. doi: 10.1109/LCA.2015.2414456