

# ⑥ Publishing Scientific Papers (2025-05-22; Thursday)

- Rules of publishing
- How to organize and write your paper?
- Writing the **abstract**

# ⑦ Publishing Scientific Papers (2025-05-29; Thursday)

- Writing the **introduction**
- How to select the right journal?
- How to deal with editors and reviewers?

# ⑧ Past Trends in Information Technology (2025-06-05; Thursday)

- Introduction
- Moore's law
- Physical Limits
- Power Consumption
- Manufacturing

# ⑨ Future Trends in Information Technology (2025-06-12; Thursday)

- More on Moore's Law
- Devices
- Manufacturing
- Architectures

# ⑩ Publishing Scientific Papers (2025-06-19; Thursday)

- Discussion of previous homework on publishing scientific papers
- Writing the Discussion and Conclusions
- Some rules of writing in English

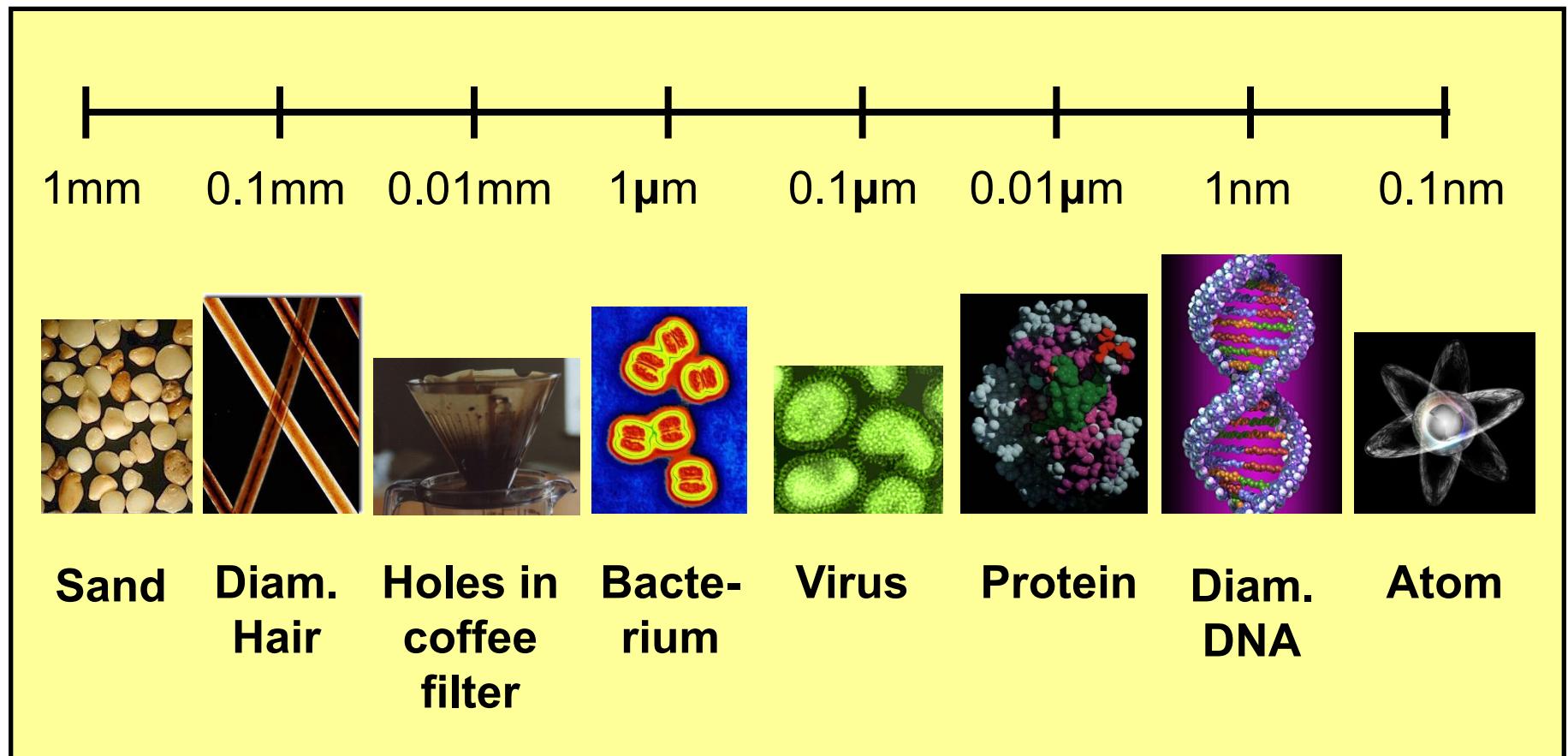
# Example: Quiz 0

How many lectures will be given in this series by Ferdinand Peper?

- a. 2
  - b. 3
  - c. 4
  - d. 5
- 

Correct answer: 0 d

# Down to Nanometers

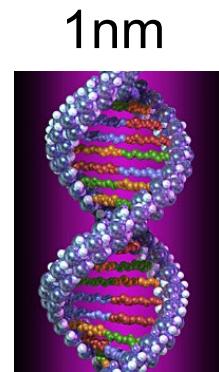


# Nanotechnology size ranges

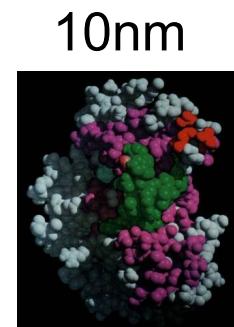
- $0.1\text{nm} \sim 10\text{nm}$



~



~



**Atom**

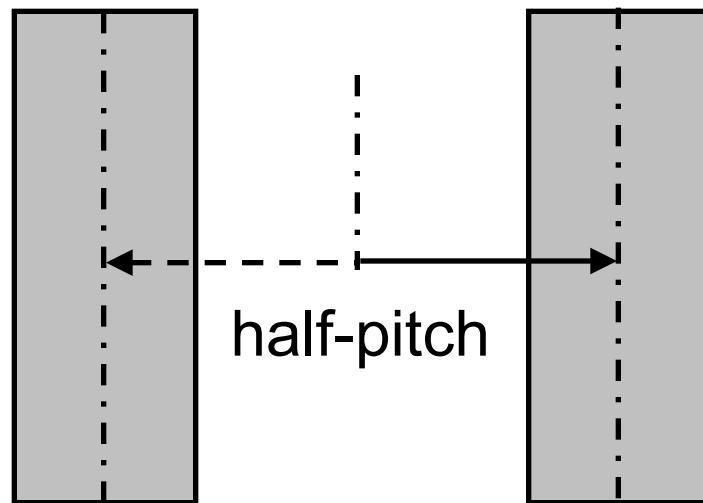
**Diam. DNA**

**Protein**

- $0.032\text{nm} = 10^{-1.5}\text{nm} \sim 10^{1.5}\text{nm} = 32\text{nm}$
- < 10nm: “requires radical new technologies”

# Half Pitch – Feature Size

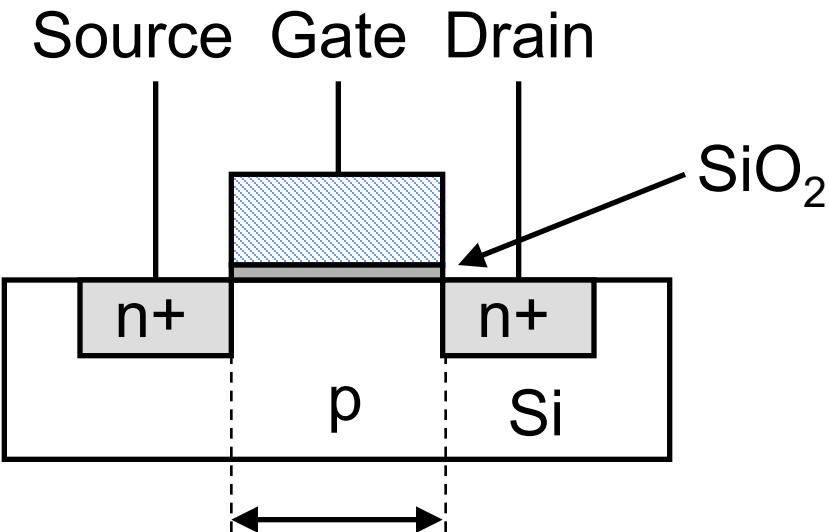
“Half the distance between centers of two adjacent wires”



“Half the spacing between cells in memory chips”

Also called *node size*

# Scaling Down CMOS



feature size	year
70nm	130nm
37nm	90nm
18nm	45nm
6nm	22nm

# Moore's Law

# of transistors on chip doubles every 18 months

History:

(1965) Doubling every 12 months

(1975) Doubling every 24 months

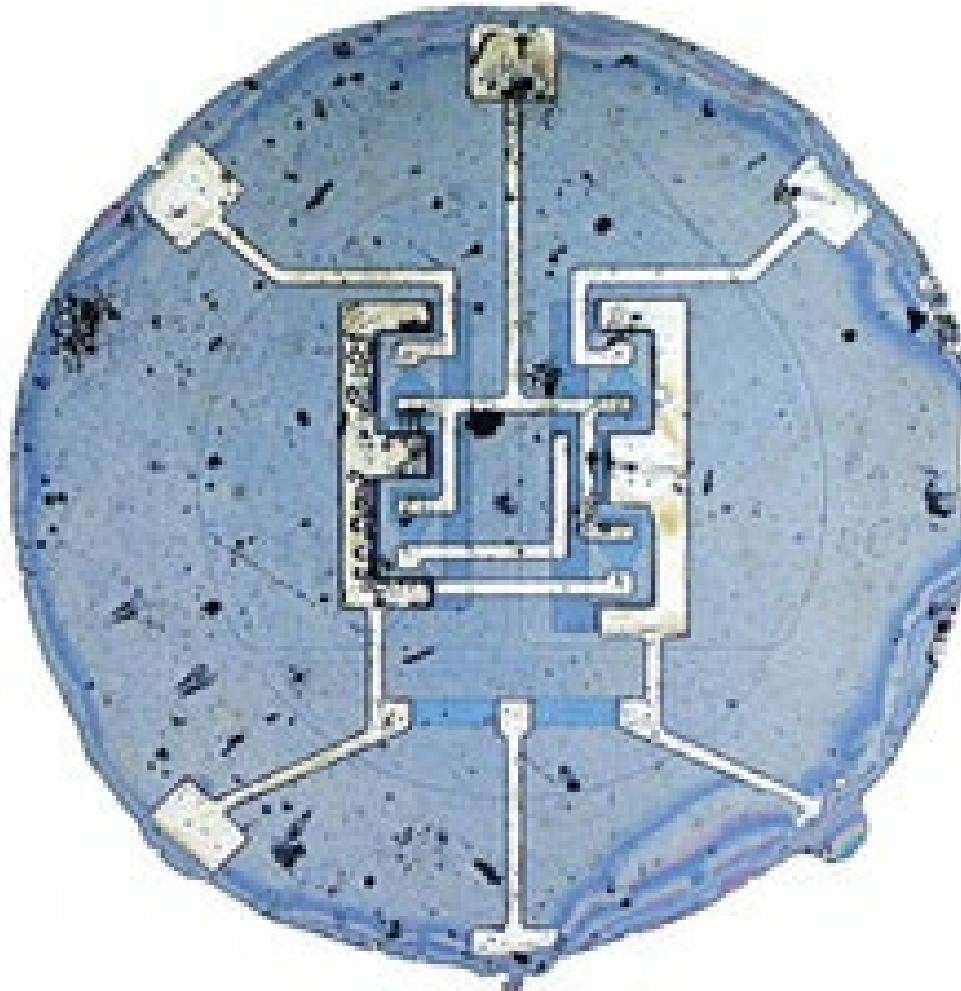
(1980's) Doubling every 18 months

2025: 60<sup>th</sup> Anniversary of Moore's Law!

Combination of increases in transistor densities and  
increases in chip sizes

Factors change: type, design overhead, architectures

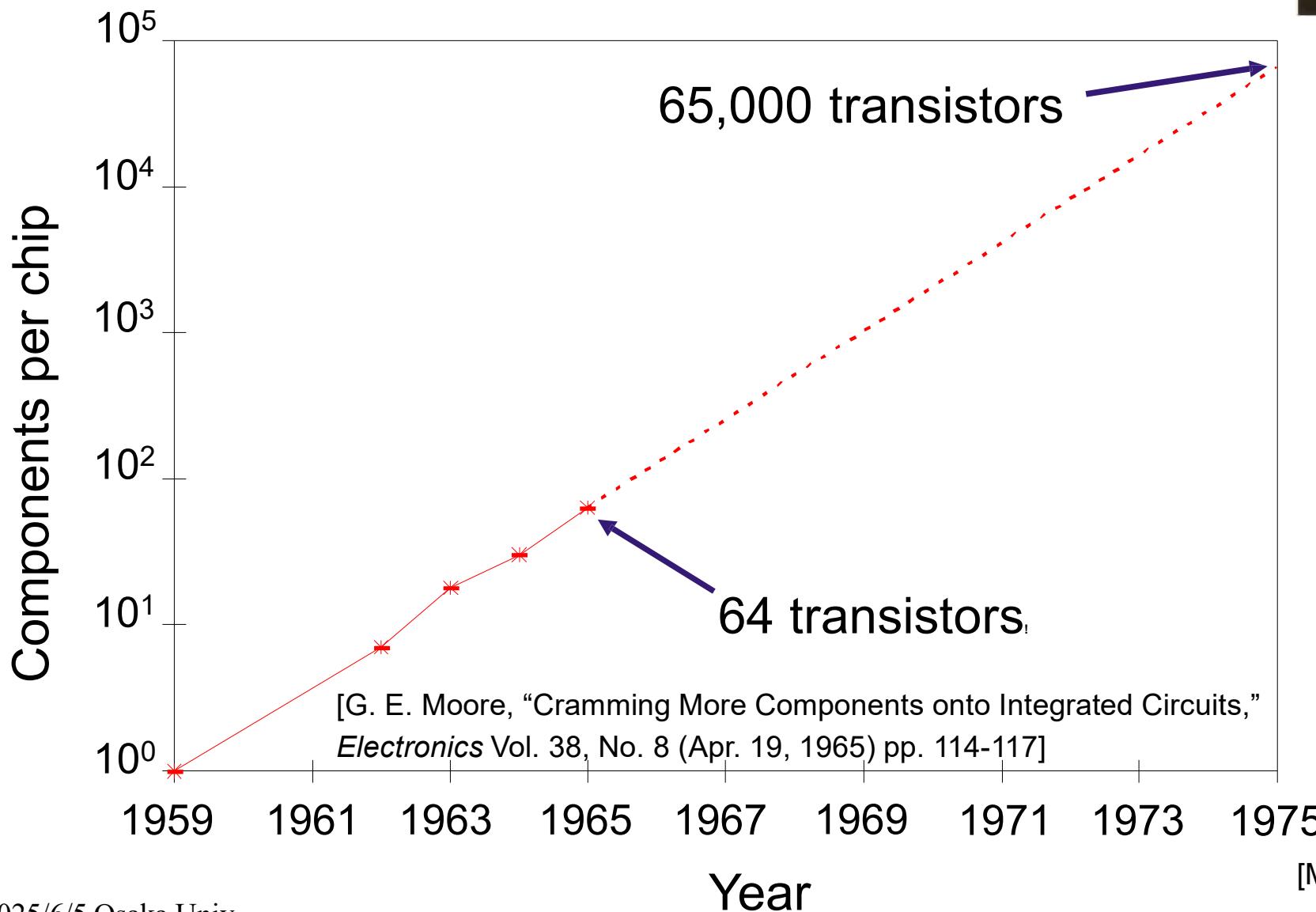
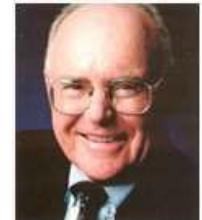
# Moore's Law



Single Planar Transistor [Fairchild, 1959]

# 1965: Moore's Law

# transistors doubling each year

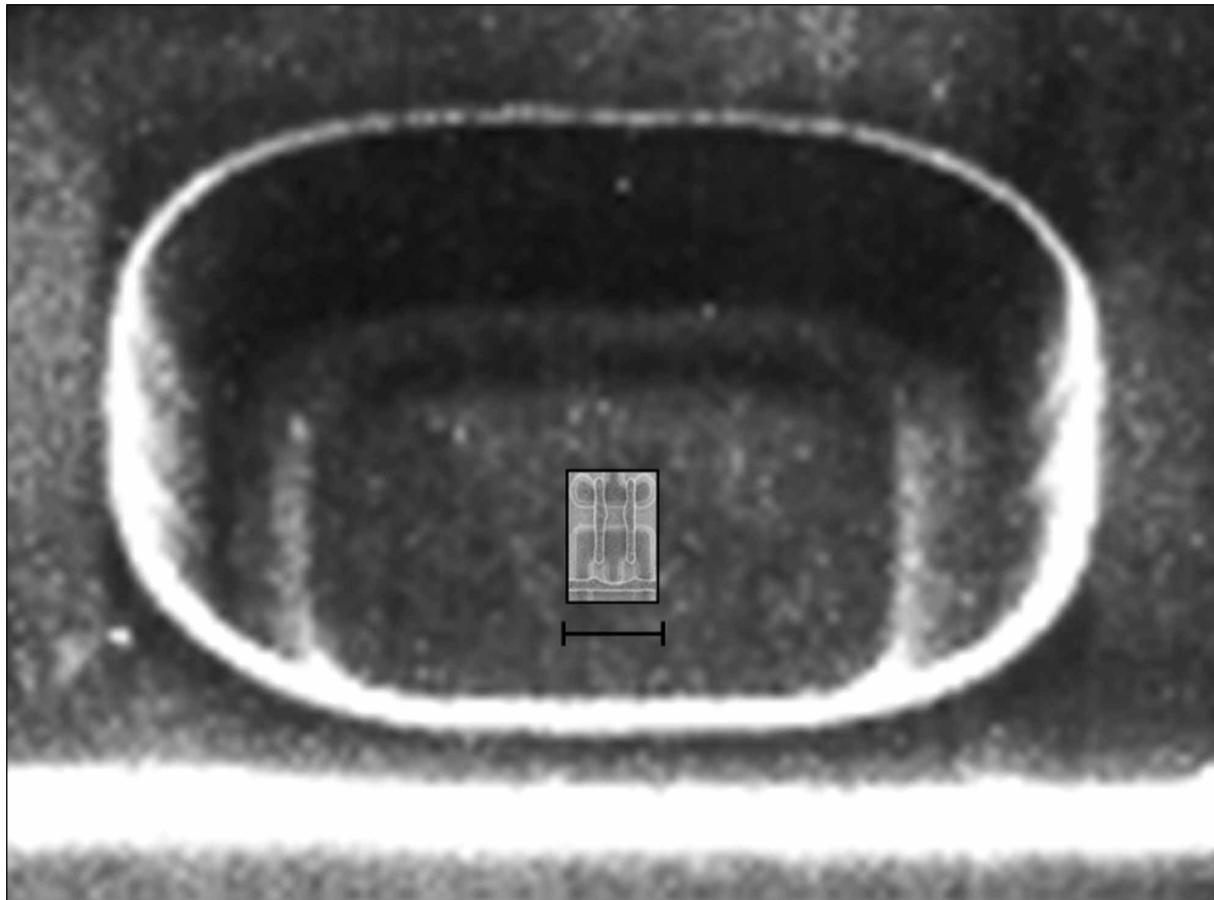


# Quiz 1

What was Moore's intention when he published his law in an electronics magazine in 1965?

- a. Moore wanted to publish his latest research on integrated circuits, and his intention was purely scientific
- b. Moore wanted to recruit excellent electronics engineers for his company
- c. Moore wanted to draw attention to integrated circuits, because there was a lot of skepticism due to unreliability of such circuits
- d. Moore developed the design principles of integrated circuits, and wanted to report that he proved that they would be applicable for at least one decade

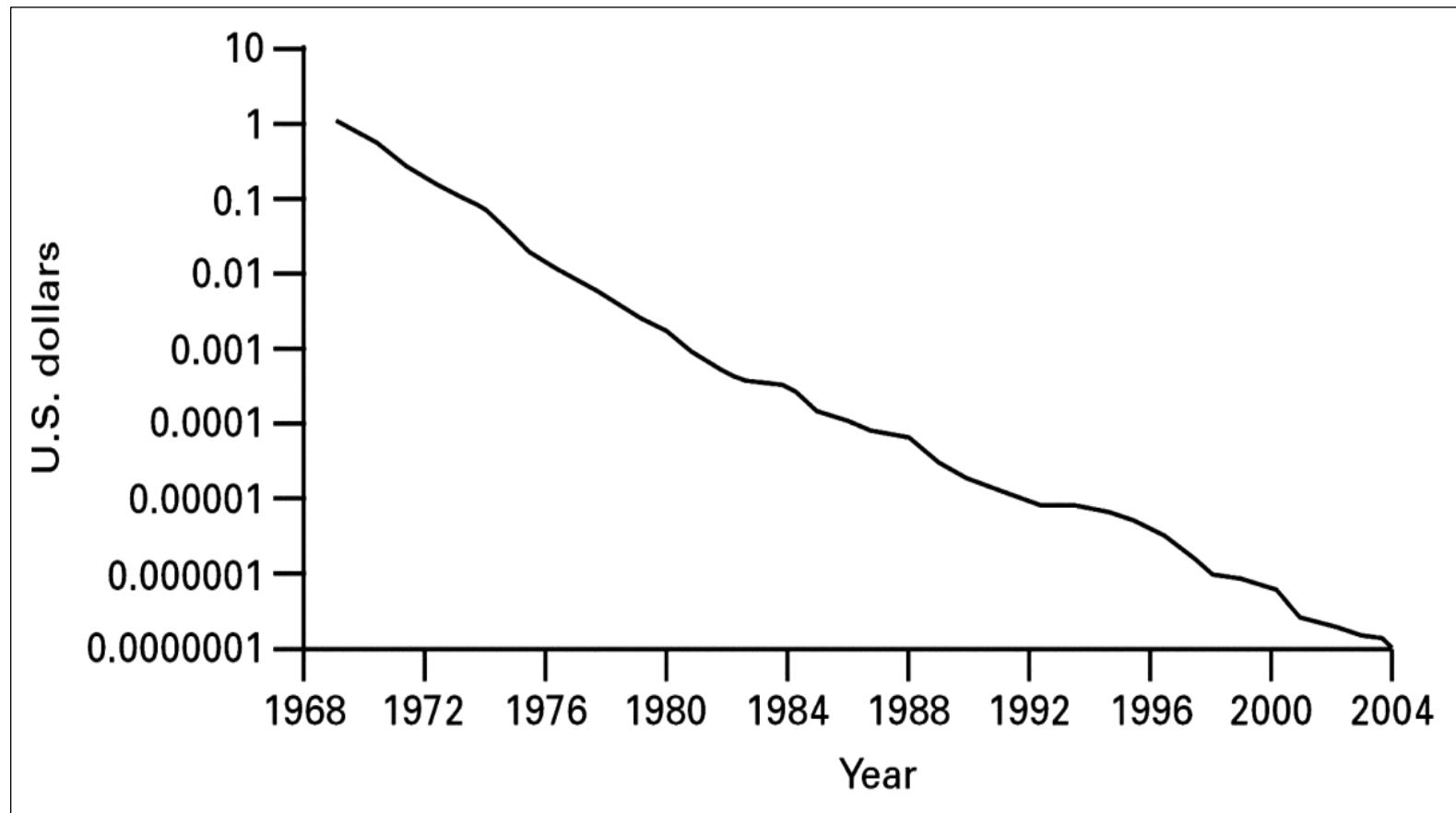
# Moore's Law



Size comparison of a single contact from 1978 with a full SRAM cell from 2002 [Intel, 2005]

# Moore's Law

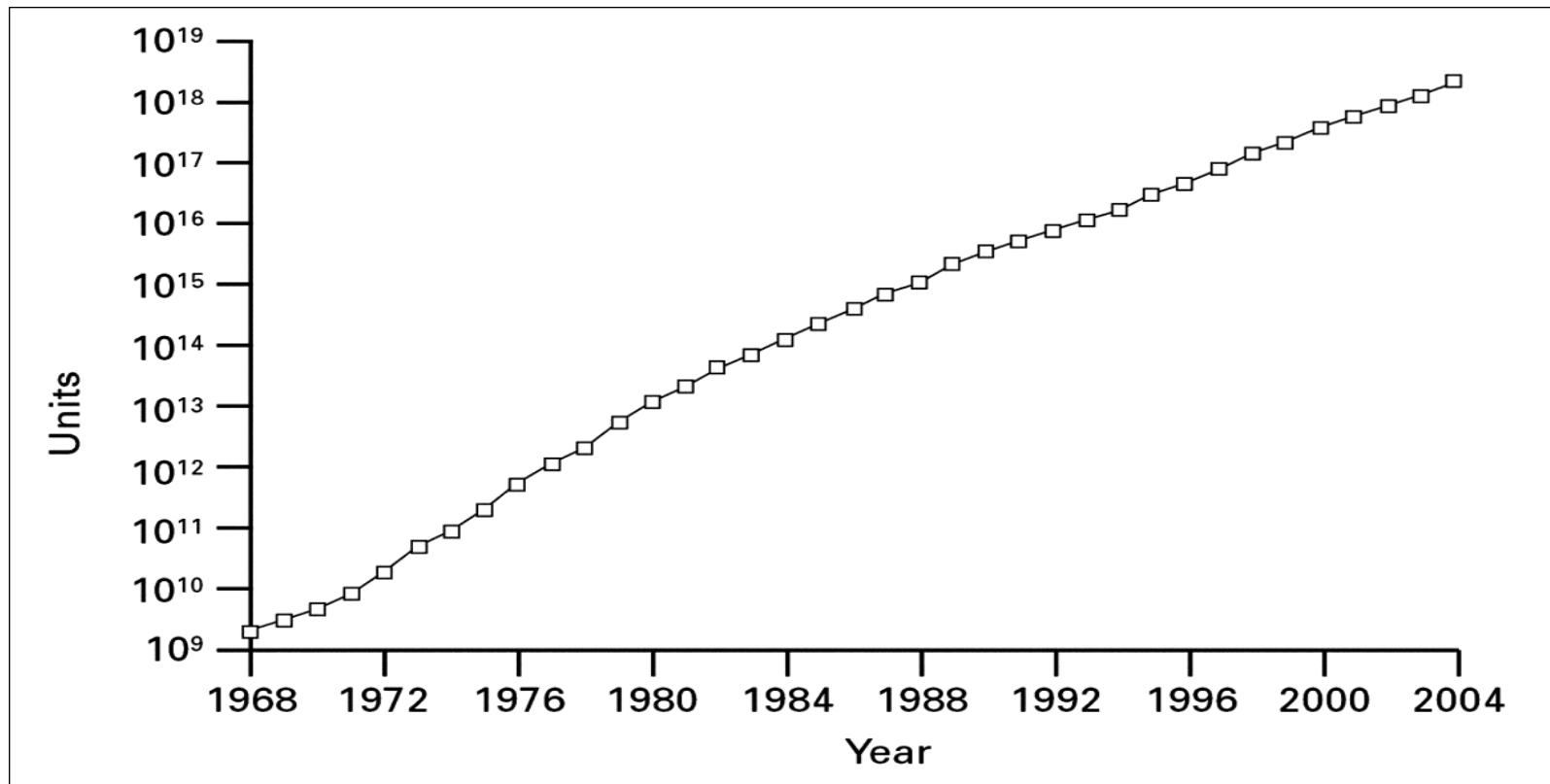
## Price per Transistor



Average price of a transistor (1968–2004) [Intel/WSTS, 2005]

# Moore's Law

## Number of Transistors Shipped



Total number of transistors shipped by the semiconductor industry (1968–2004) [Intel/WSTS, 2005]

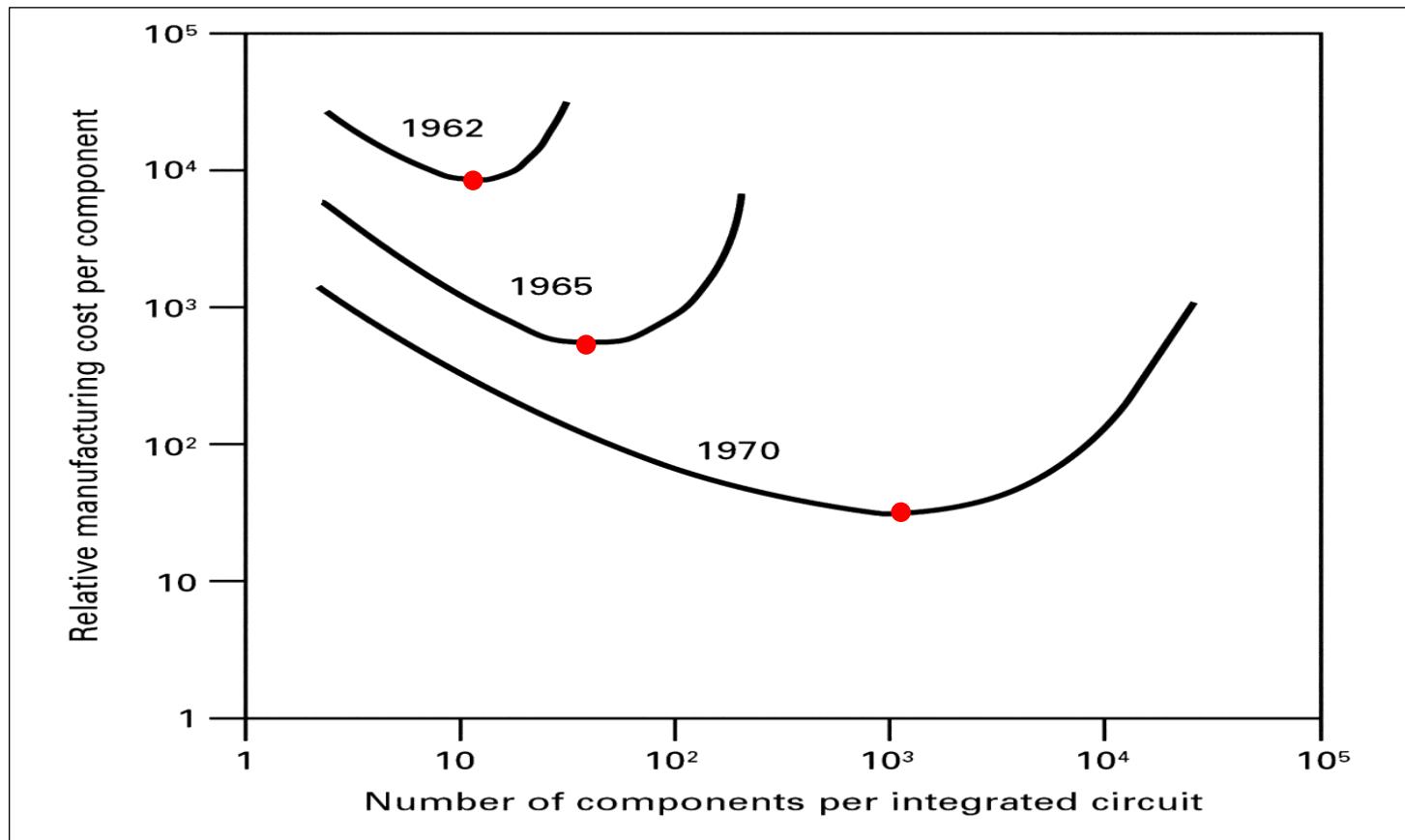
# Quiz 2

Select the correct statement about progress in the semiconductor industry:

- a. The number of shipped transistors is determined according to Moore's law
- b. According to Moore's law, in 10 years it will be cheaper to produce one transistor in an integrated circuit than to print one period (.) on paper
- c. The cost of integrated circuits is determined according to Moore's law
- d. It is now cheaper to produce one transistor in an integrated circuit than to print one period (.) on paper

# Moore's Law

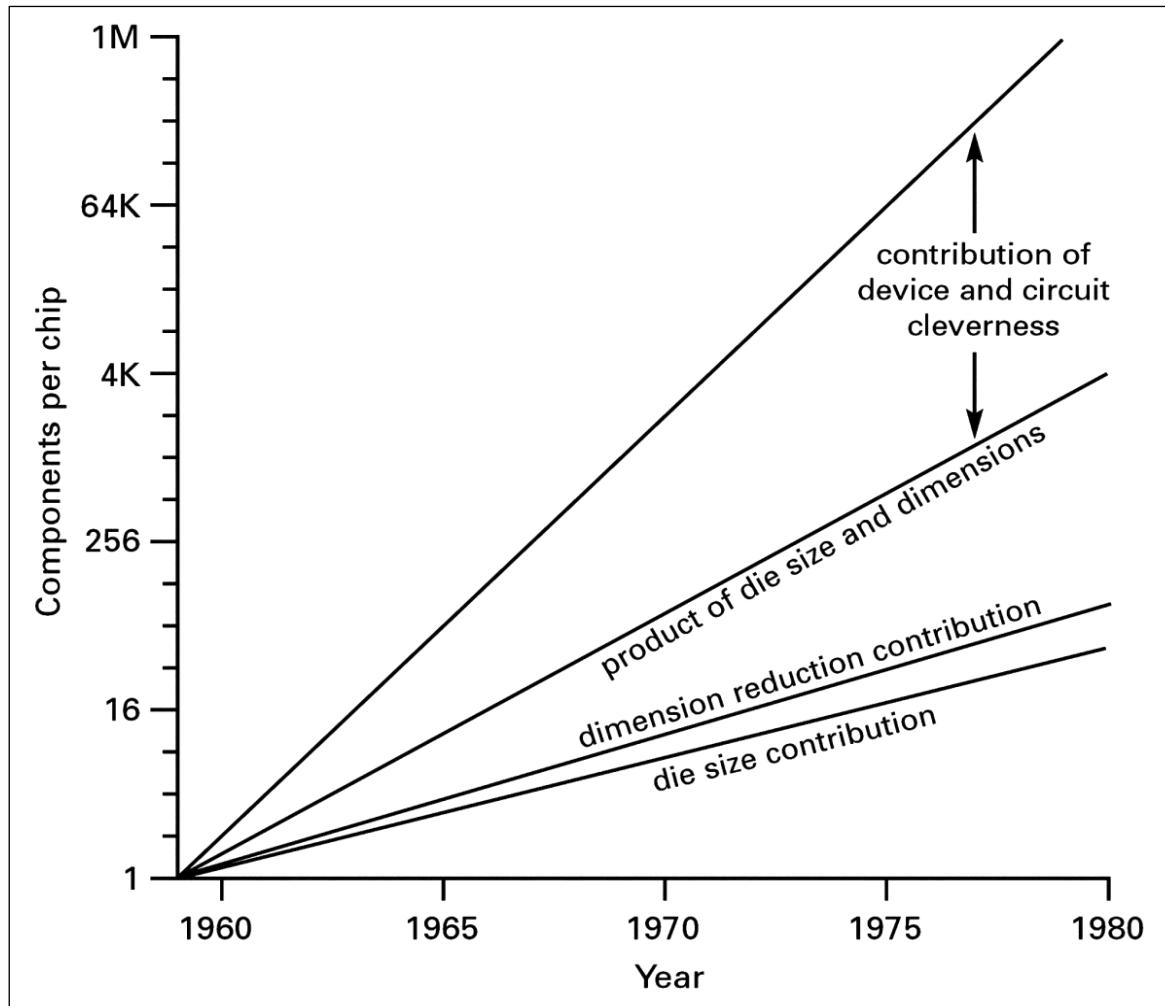
## Which Point on the Cost Curve?



Manufacturing cost per component versus number of components per integrated circuit [Moore, 1965]

# Moore's Law

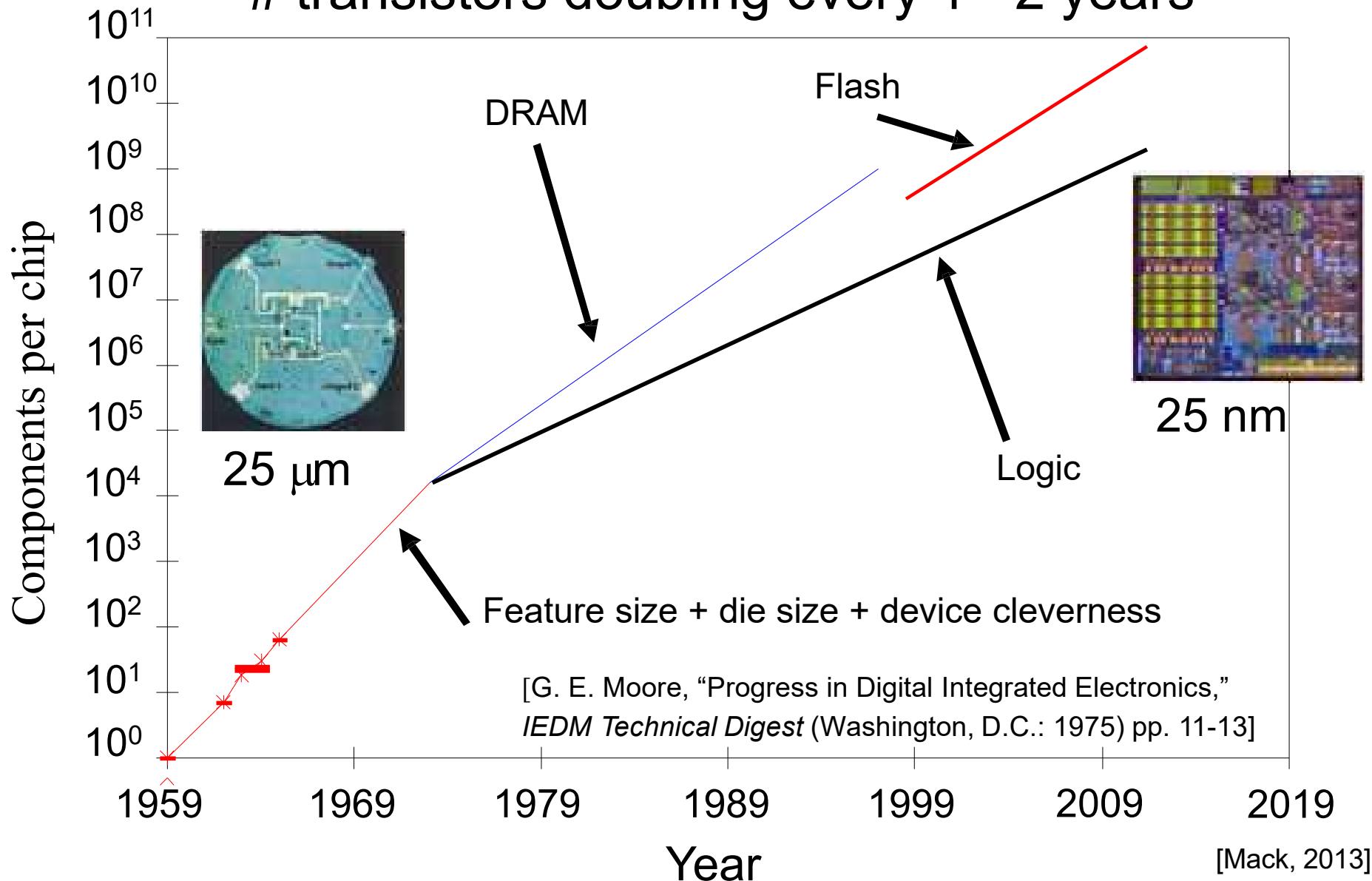
## Combination of Factors



Resolution of complexity increase into contributing factors [Intel, 2005]

# 1975: Moore's Law

# transistors doubling every 1 - 2 years

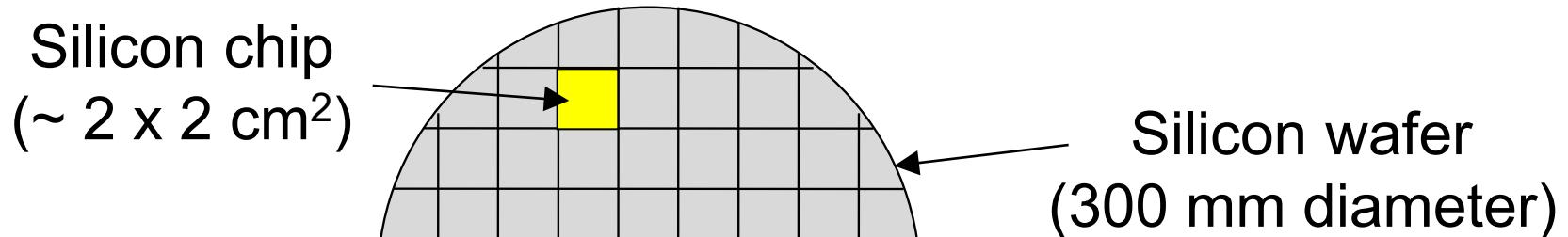


# Moore's Law and Wafer Size



A 300mm wafer with U.S. nickel (approximate size of 1959 standard  $\frac{3}{4}$ -inch wafer) for scale [Intel]

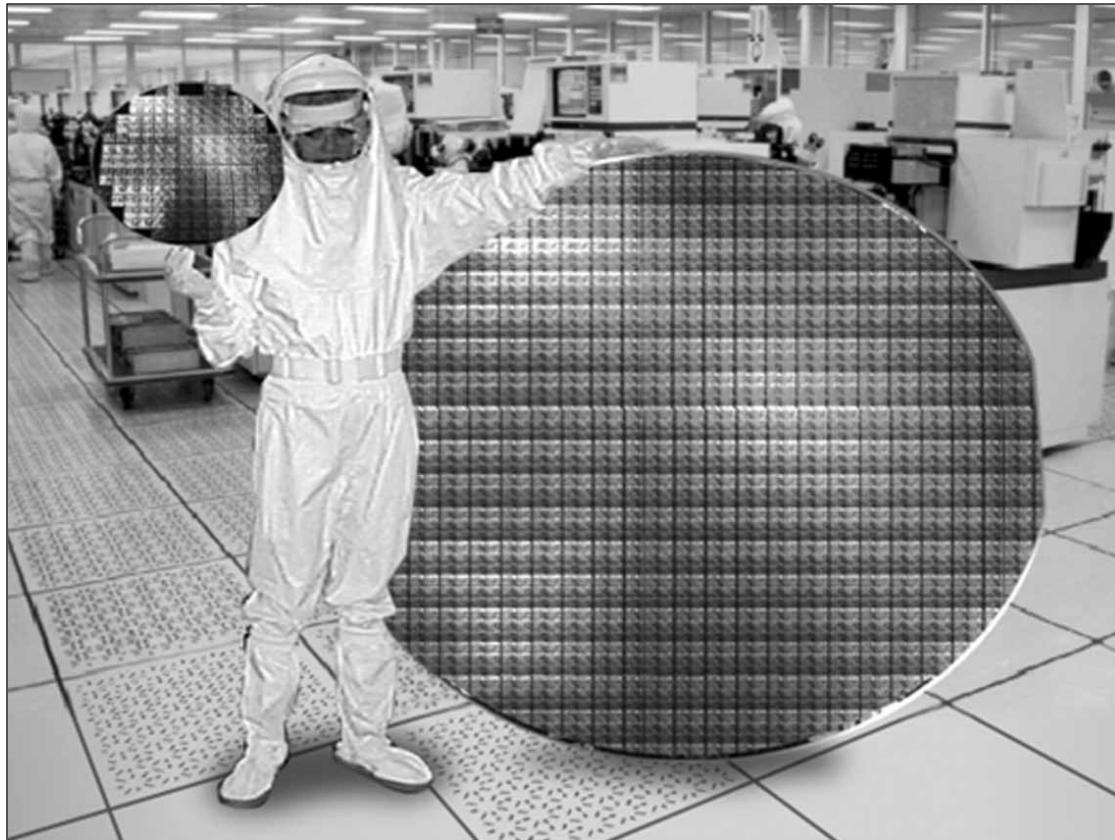
# Wafers



2010: ~ 1B transistors / chip

2016: ~10B transistors / chip

# Moore's Law and Wafer Size (Not!)

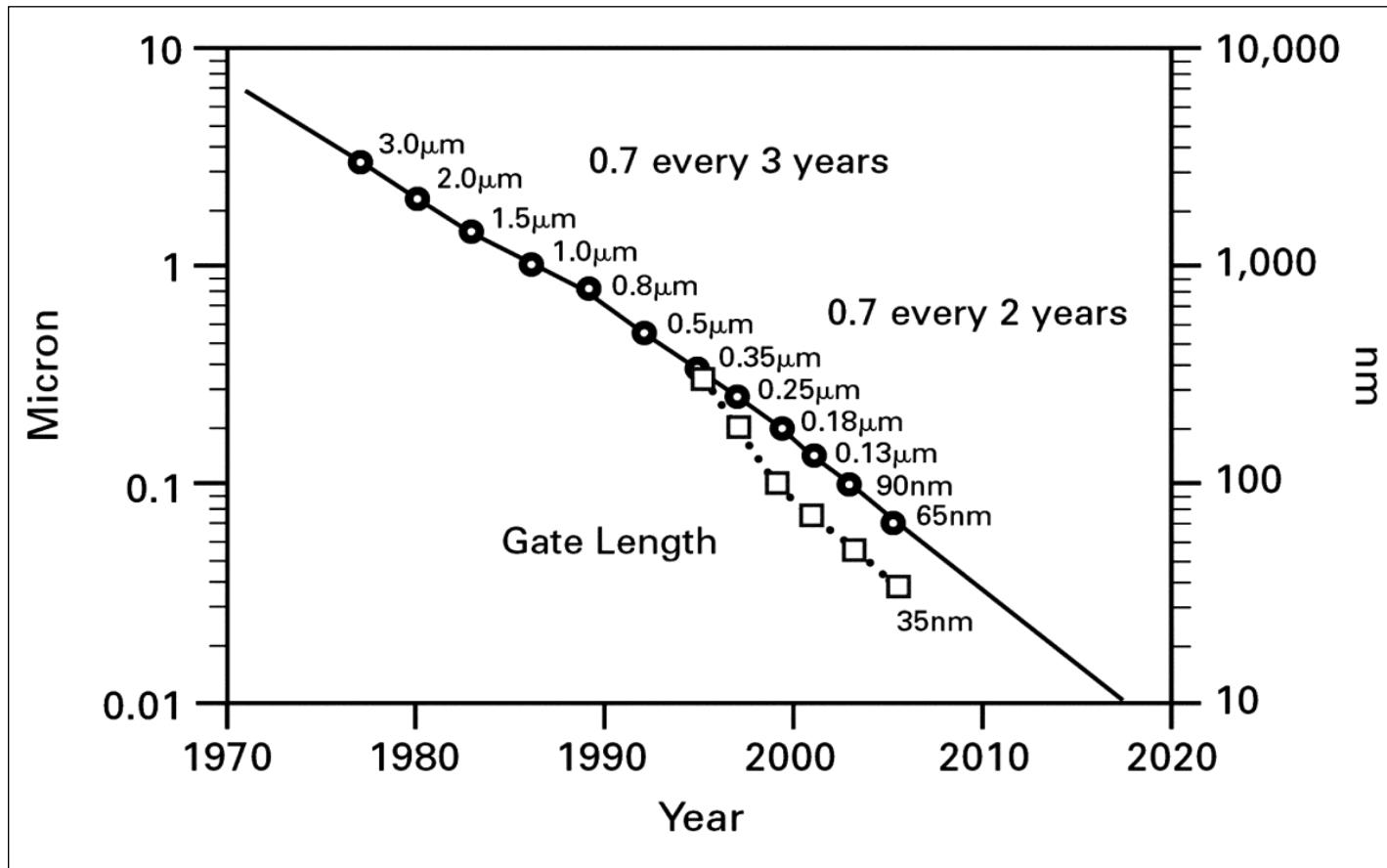


A digitally manipulated photograph showing the fictitious  
57-inch wafer [Intel]

# Moore's Law 1.0 & 2.0

- Moore's Law 1.0: scaling up
  - Doubling # transistors every 1 – 2 years
  - More powerful chip for same price
- Moore's Law 2.0: scaling down
  - Shrinking transistor lowers its cost by 30% / year
  - Same chip for lower price
- Many new applications
  - Large increase in chip volumes

# Moore's Law Accelerating? (2005)



Plot of new technology generation introductions  
(1975–2005) [Intel, 2005]

# Dennard's Design Principle

## MOSFET Scaling Rules

Device/Circuit Parameter	Scaling Factor*
Device dimension/thickness	$1/\lambda$
Doping Concentration	$\lambda$
Voltage	$1/\lambda$
Current	$1/\lambda$
Capacitance	$1/\lambda$
Delay time	$1/\lambda$
Transistor power	$1/\lambda^2$
Power density	1



\* Constant electric field scaling

[R. Dennard et al., "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," IEEE Journal of Solid-State Circuits, Vol. SC-9, pp. 256-268, Oct. 1974]

Until around 2004: No trade-offs

Everything got better when shrinking a transistor!

[Mack, 2013]

# 1974 – 2004

# Unprecedented time in technology

- Dennard Scaling: as transistor shrinks it gets
  - Faster
  - Lower power (constant power density)
  - Smaller / lighter
- Moore's Law
  - Cost / area kept approximately constant while shrinking
  - More transistors / chip & lower cost / transistor

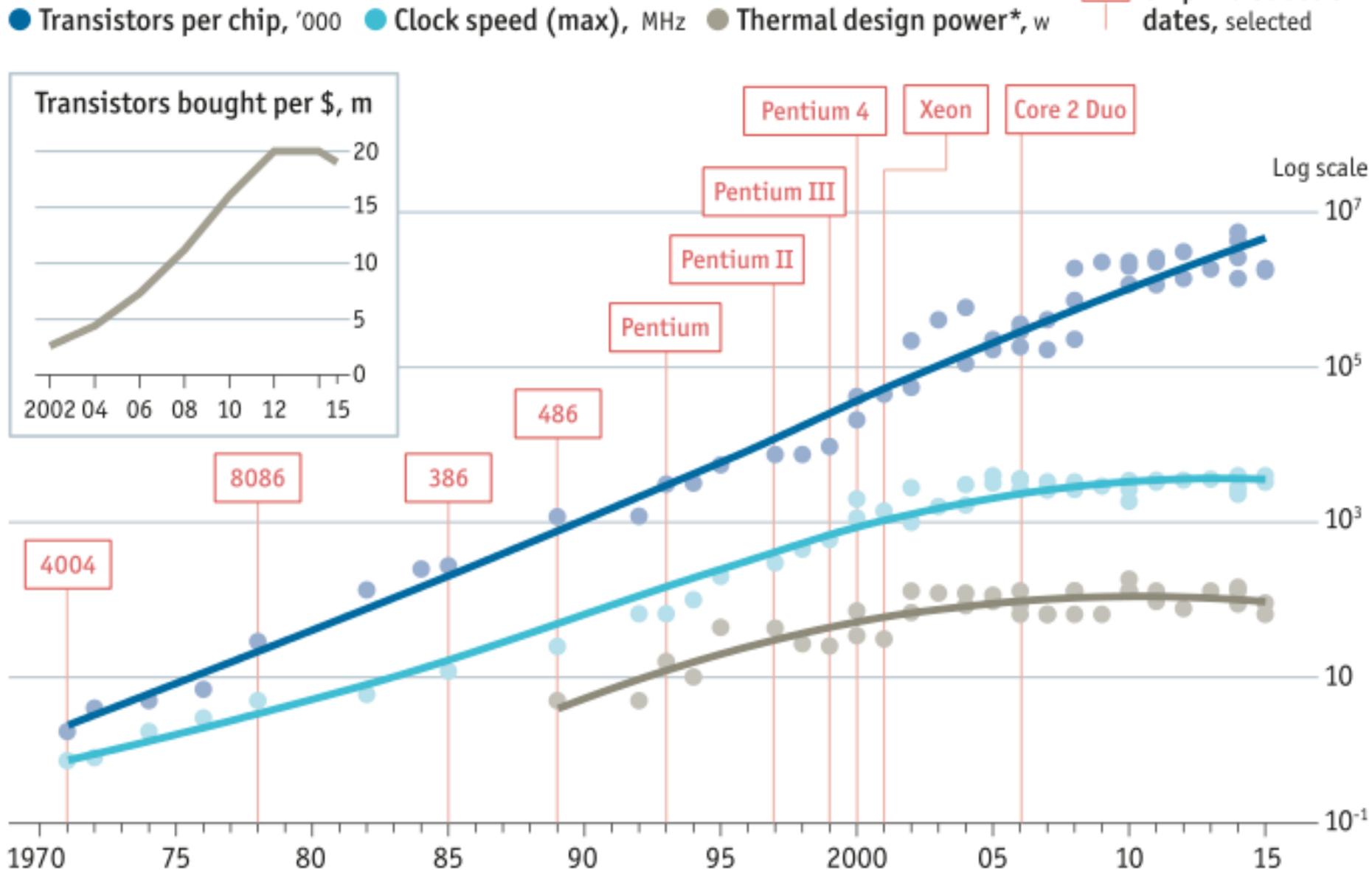
[Mack, 2013]

# Dennard Scaling: Problems

- Voltage has actually shrunk more slowly ( $\sim 1/\sqrt{\lambda}$ )
- Voltage stopped dropping around 2004
  - Thermal noise ( $kT/q = 25 \text{ mV}$  at room temperature)
  - Subthreshold leakage current
- Power considerations important to shrinking
- Clock speed won't increase much anymore

Shrinking transistors make problems worse

# # Transistors/Chip, Clock Speed, Power Consumption



\*Maximum safe power consumption

# Quiz 3

Select the most appropriate statement:

- a. Since around 2005 the clock speeds of laptop computers have not increased much anymore
- b. Dennard predicted in 1974 that clock speeds of integrated circuits would increase until around 2005
- c. Since around 2005 the speeds of laptop computers have not increased much anymore
- d. Clock speeds of integrated circuits will increase according to Moore's law in the next 10 years

# Perceived Past Limits

Period	Expected limit (size)	Cause (Source)
Late 1970's	1000nm	Short-channel effects
1980	250nm (10-30MHz)	Tunneling leakage & dopant fluctuation (Mead)
Early 1980's	500nm	Source / Drain resistance
Late 1980's	100nm	“Brick wall”: various
1999	100nm	Various (Davari at IBM)
2004	50nm	“Red brick wall”: various
2005	10nm	“Fundamental”

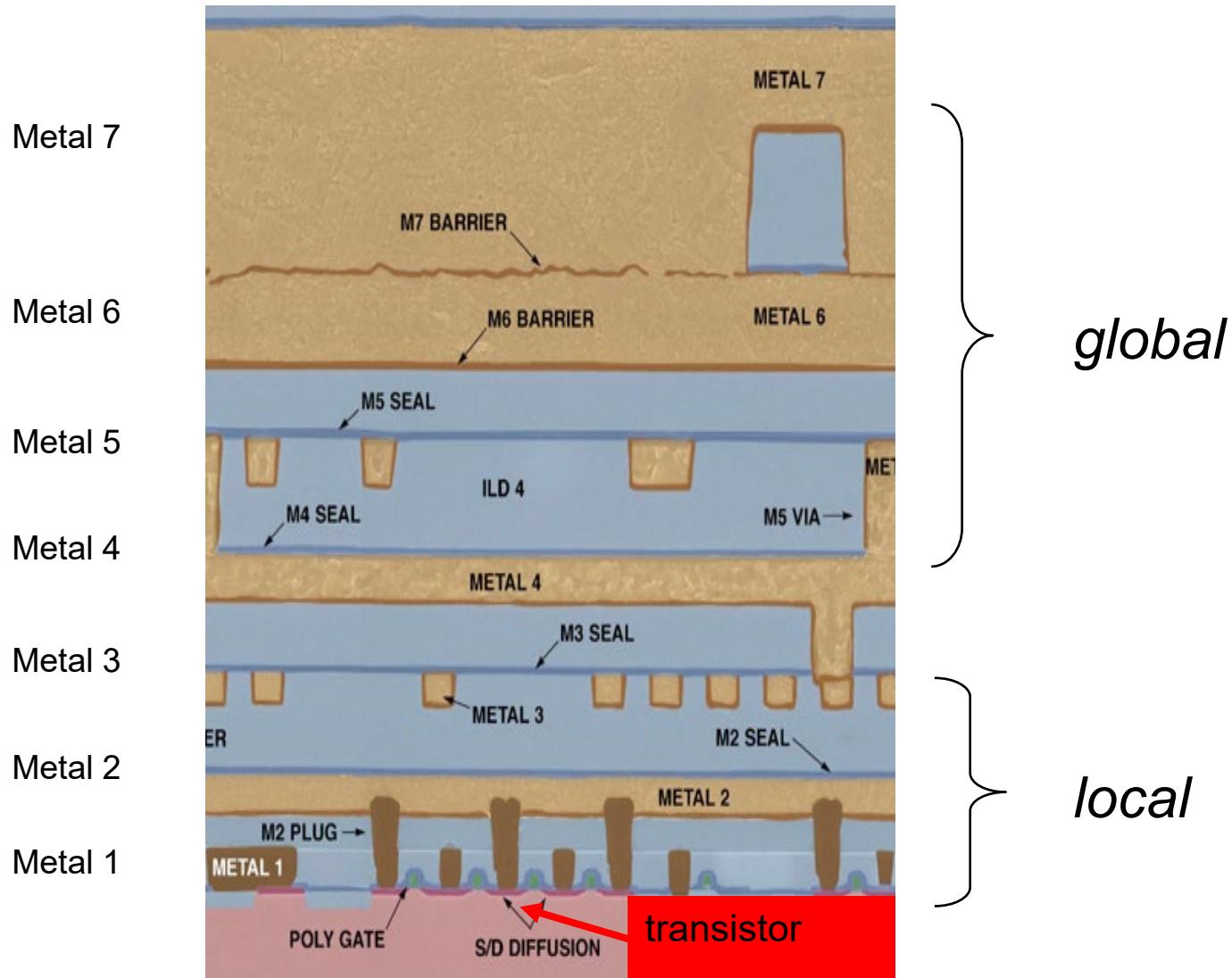
# Limits to Downscaling: Wire Delays

Determined by:

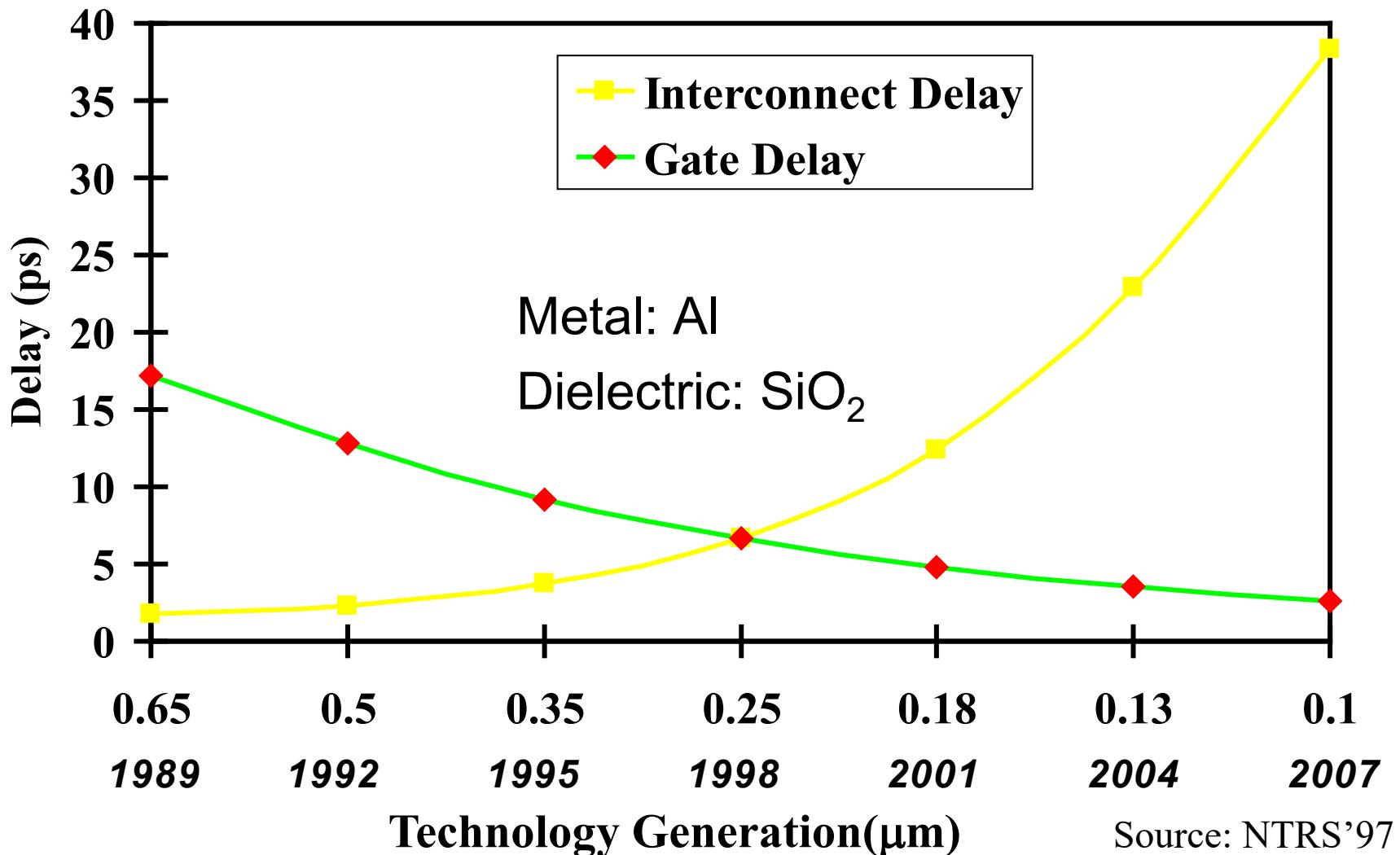
- Length of wire
- Resistance  $R$  of wire
- Capacitance  $C$  of wire

RC circuit: time constant determined by  $RC$

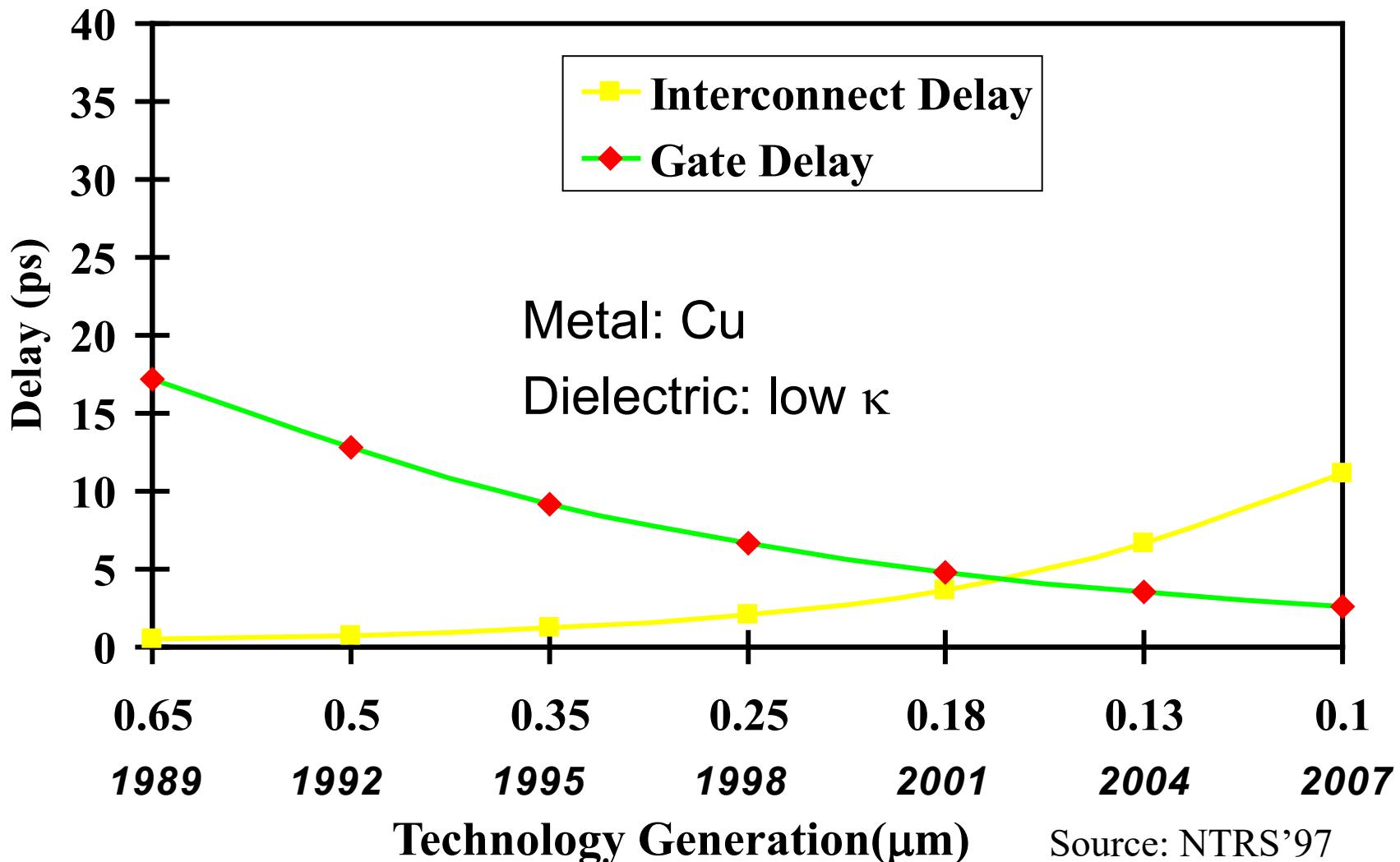
# Layers of Wires



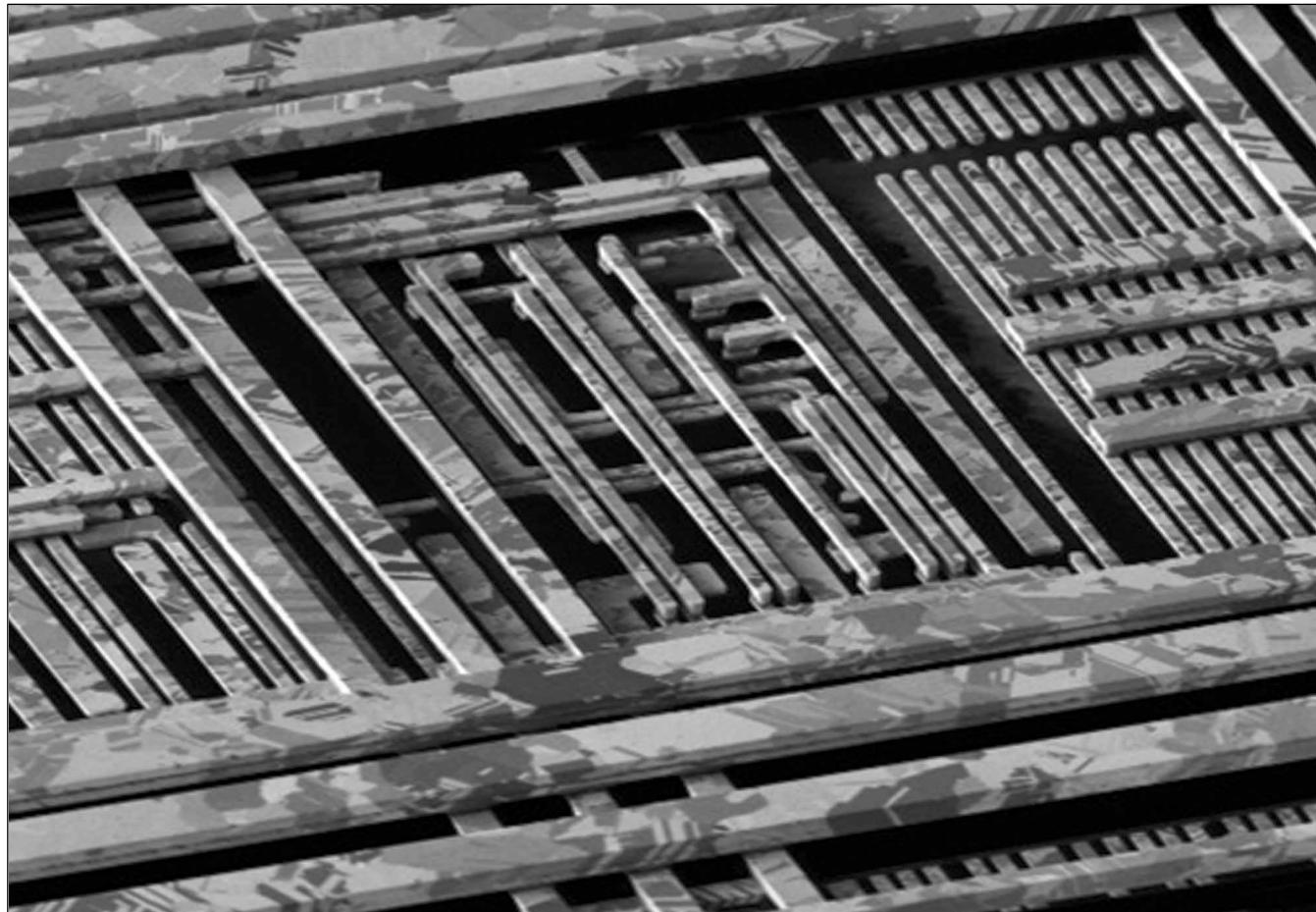
# Wire vs. Gate Delay



# Less Wire Delay with Cu Wires



# Interconnects



A region of copper interconnects for an Intel logic device from 2001 [Intel]

# Power Consumption by Computers

- 3% of electricity for computers + Internet
- Rises about 15% each year (estimated)

Computer + Monitor: 200 W → 260 kWh / year  
(8 h / day, 5 days / week → 1300 h / year)

Sleep mode: 25 Watt → 83.2 kWh / year  
(5 x 16 h / week + 48 h / weekend → 3328 h / year)

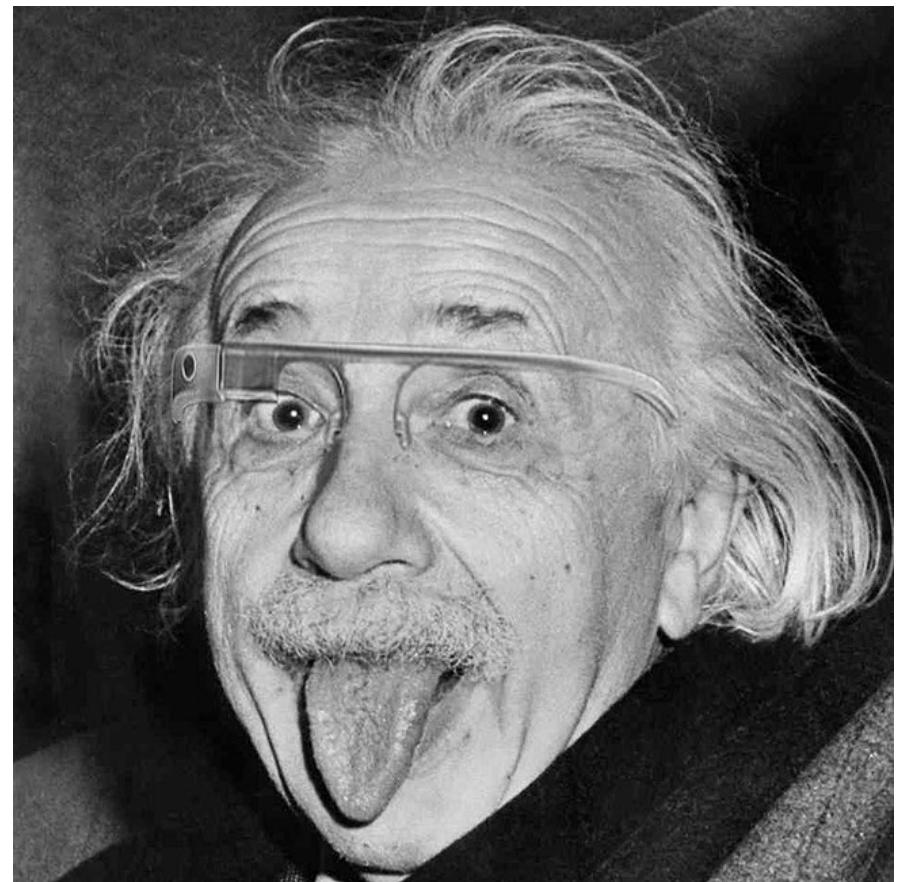
Total: 340 kWh / year

# Future Technology Characteristics (as foreseen in the past)

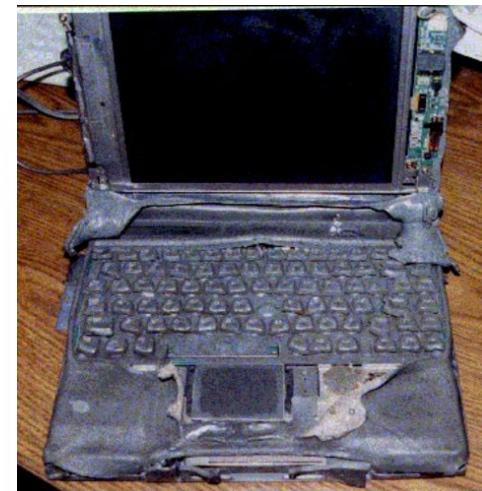
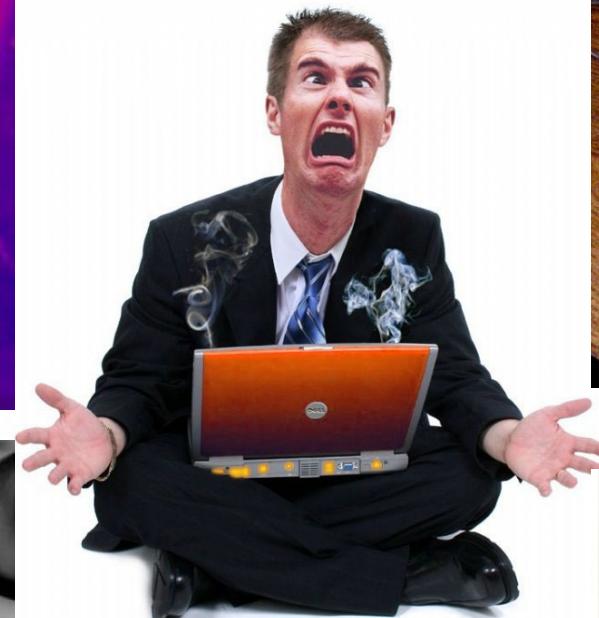
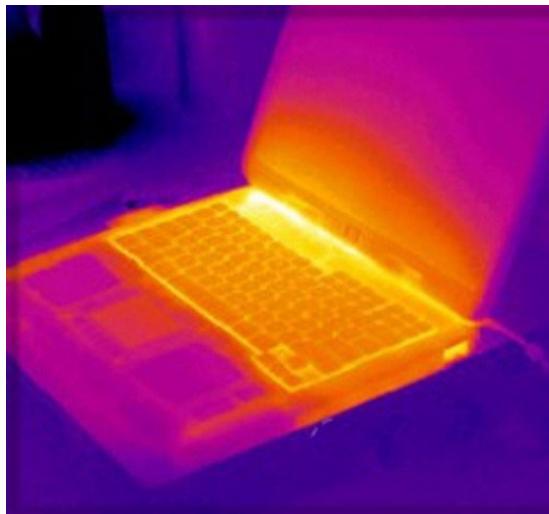
Year	2004	2007	2010	2013	2016	2018
Technology (nm)	90	65	45	32	22	18
Density (M trans./cm <sup>2</sup> )	138	276	552	1104	2209	3506
Chip size (mm <sup>2</sup> )	280	280	280	280	280	280
Power (W)	158	189	218	251	288	300
Frequency (GHz)	4.171	9.285	15.079	22.980	39.683	53.207
Max. # routing layers	10-14	11-15	12-16	12-16	14-18	14-18

\*Data for high-volume microprocessor (2003 ITRS)

# Portable devices



# Heat Dissipation



Operations / sec → Operations / Wh

How much computing  
can we do...



...with a limited  
energy source?



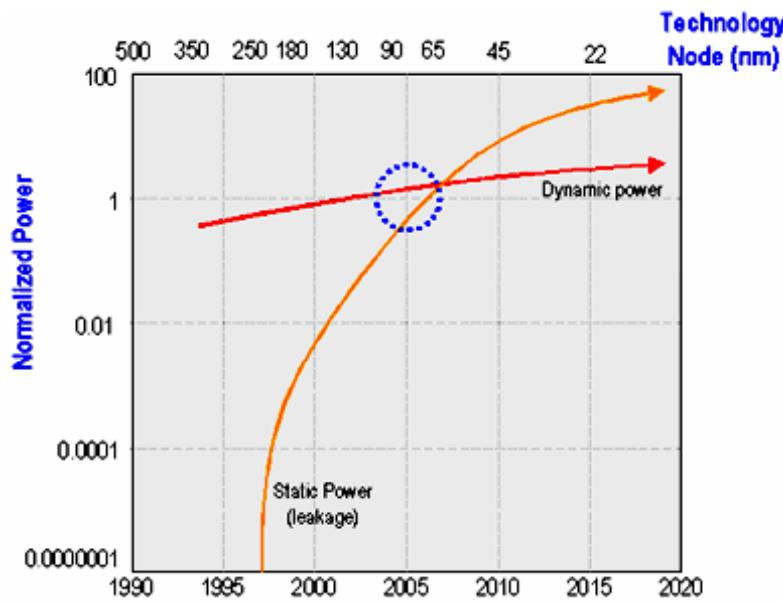
$$\begin{aligned}\text{Energy efficiency} &= \frac{\text{Operations}}{\text{Energy}} = \left[ \frac{OP}{nJ} \right] \\ &= \frac{\text{Operations/sec}}{\text{Energy/sec}} = \left[ \frac{10^6 \times OP/s}{10^{-3} \times J/s} \right] = \left[ \frac{MOPS}{mW} \right]\end{aligned}$$

# Power Dissipation

Amount of power dissipated by a chip

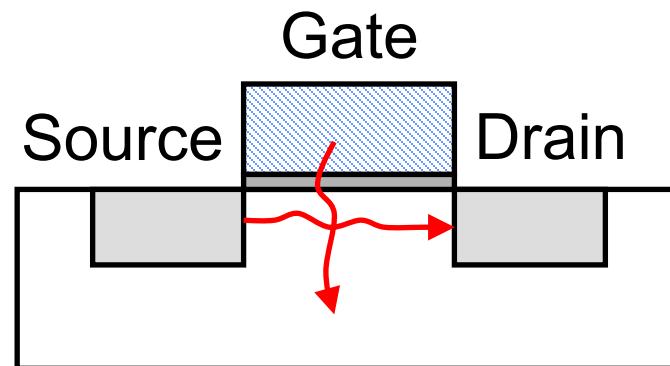
## Dynamic

Power dissipated due to switching of transistors.  
Increases with higher clock speeds and larger number of transistors



## Static

Power dissipated due to **leaking currents** in transistors. Tends to increase with higher integration densities.



# Thermal Limit

Determined by energy required to write a bit



>  $kT$  (energy of thermal fluctuation), else bit error  
↳ Boltzmann constant =  $1.38 \cdot 10^{-23} \text{ J / K}$

CMOS: energy  $\sim 10^{-13} \text{ J} \rightarrow \text{Temp} \sim 10^{10} \text{ K}$ ; Trend ↓

CMOS: optimum E at room temp =  $E \sim 4 \cdot 10^{-19} \text{ J} \sim 100 \text{ kT}$

# Power Dissipation Limit

- Power density:  $p = E f n P$ , where
- $E$  is average energy dissipation of active device in one clock cycle
- $f$  is clock frequency
- $n$  is device density
- $P$  is probability of device switching ( $P \sim 0.1$ )

$$p < 100 \text{ W / cm}^2$$

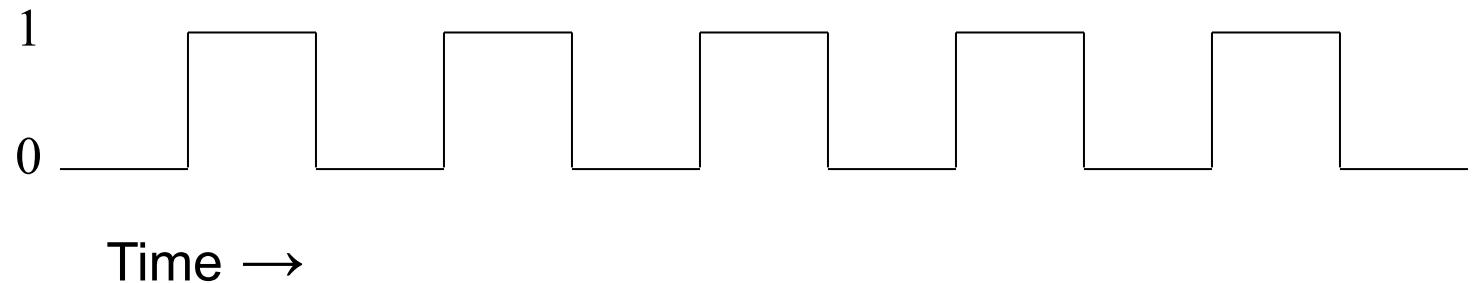
# Quiz 4

Which statement is correct?

- a. Heat dissipation by integrated circuits is a more important problem than their energy consumption
- b. Heat dissipation by integrated circuits follows Moore's law
- c. Heat dissipation by integrated circuits is independent of the clock speeds at which they operate
- d. Heat dissipation by integrated circuits tends to increase with increasing clock speeds

# Speeding up Microprocessors

- Increasing frequency
  - Clock: voltage signal that cycles at certain frequency



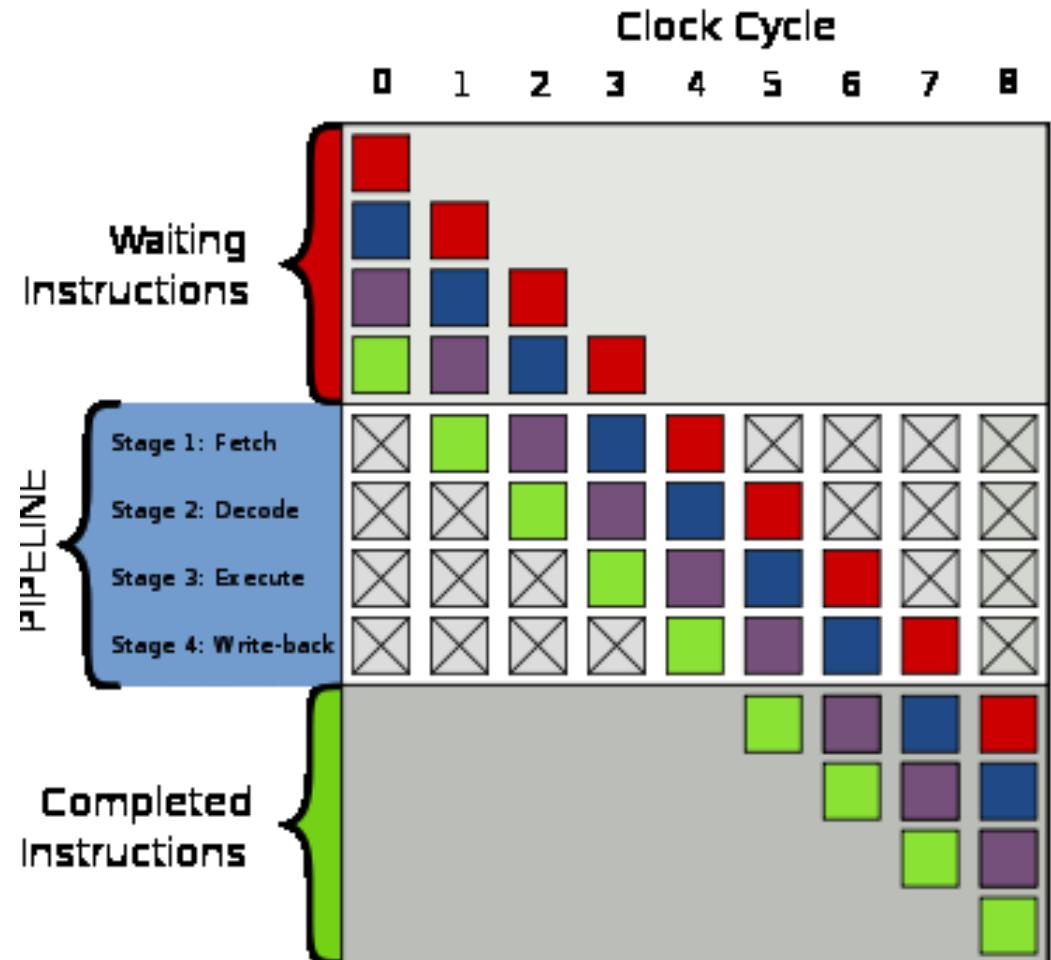
- Clock tells each stage of a circuit that **the inputs of that stage are valid and can be processed**
- Increasing # of instructions completed per cycle

# Micro-architectural Innovations

- Require additional hardware
  - strong coupling of hardware results in more than linear increase: think quadratically!  
**Pollack's Rule:** increase in performance due to micro-architectural advances is square root of complexity
- Power consumption increases linearly with hardware
- Multiple cores: speed-up equal to # of cores, and energy consumption also linear

# Single Core (1)

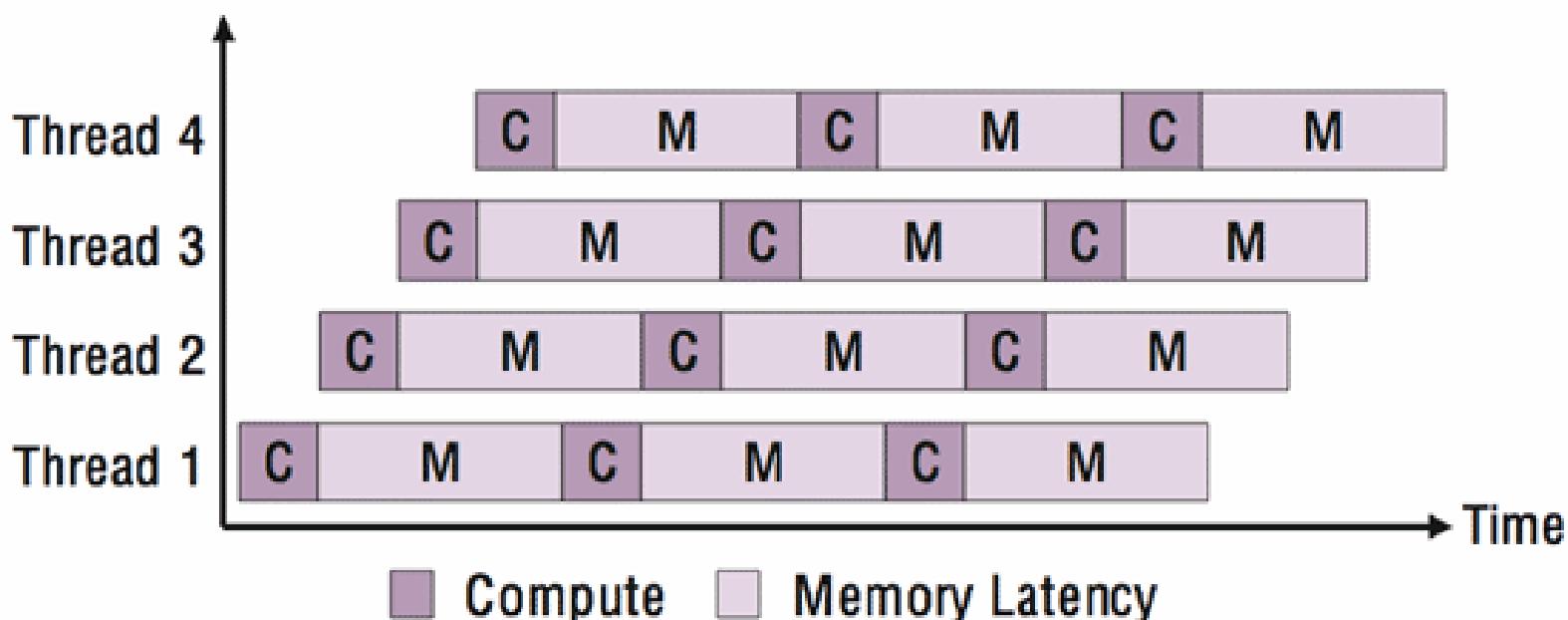
Increasing single core performance: pipelining



# Single Core (2)

## Multithreading

- Execution of two or more threads
- Time is divided and interleaved between the threads to simulate simultaneous execution



# Problems with Single Core

- Faster execution requires more circuitry and higher clock rate
- Circuitry works in parallel, so is active most of the time: increases energy consumption
- High clock rate: increases energy consumption

# Multiple Cores

- Multiple cores increase performance of system while clock rates remain at efficient level
- Two cores running at half clock rates can process instructions with similar speed as single core running at twice the clock rate, yet the dual core processor would consume less energy
- However, this assumes independence of cores

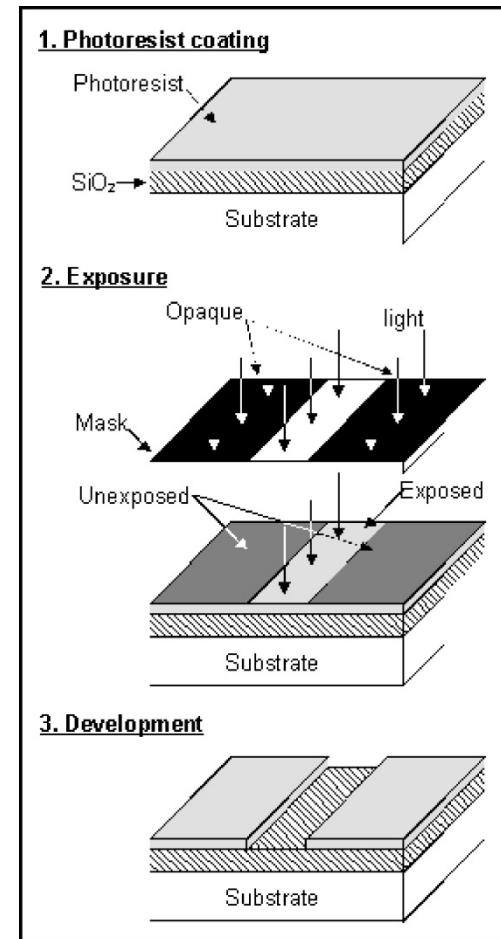
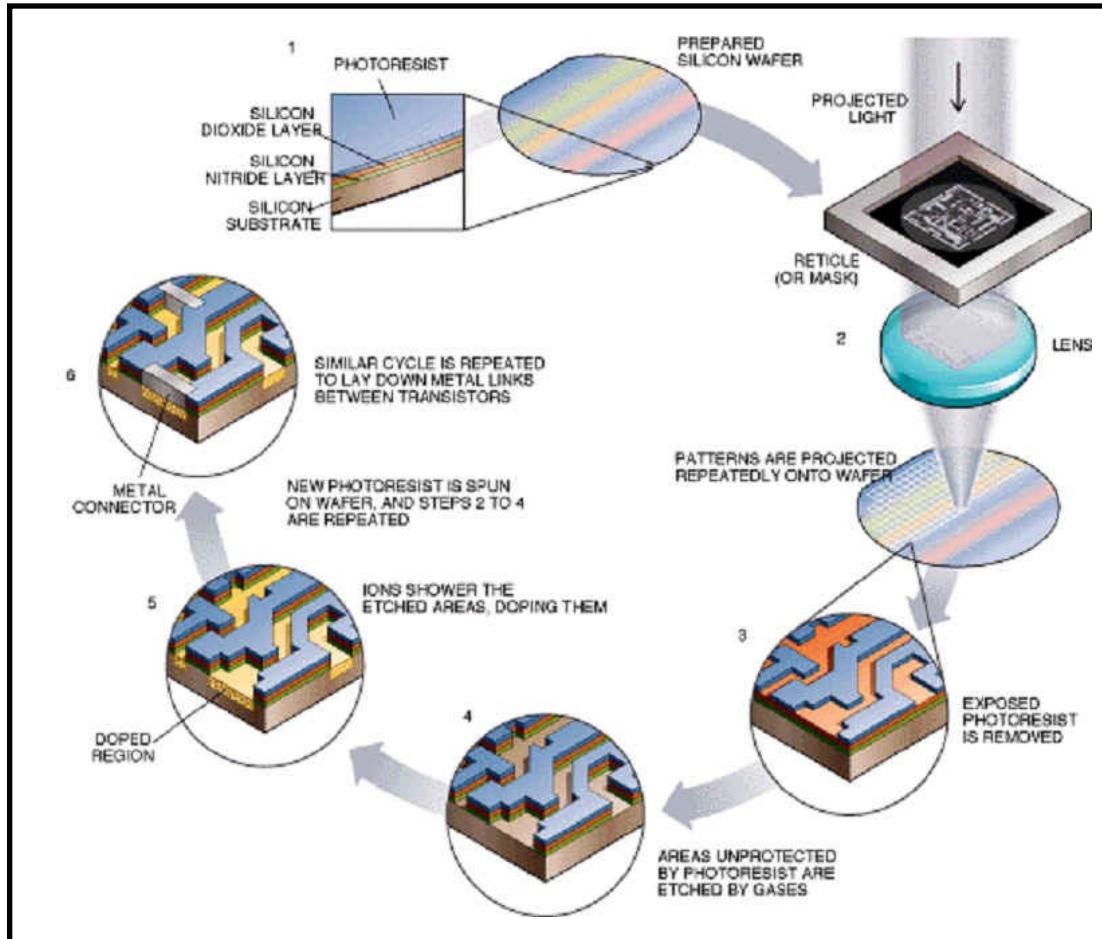
# Amdahl's Law (1)

- Fraction  $f$  of execution time perfectly parallelizable
  - No overhead for scheduling, synchronization, communication, etc.
- Fraction  $1 - f$  completely serial
- Time for 1 core =  $(1 - f) / 1 + f / 1 = 1$
- Time for  $N$  cores =  $(1 - f) / 1 + f / N$
- Speedup = 
$$\frac{1}{\frac{1-f}{1} + \frac{f}{N}}$$

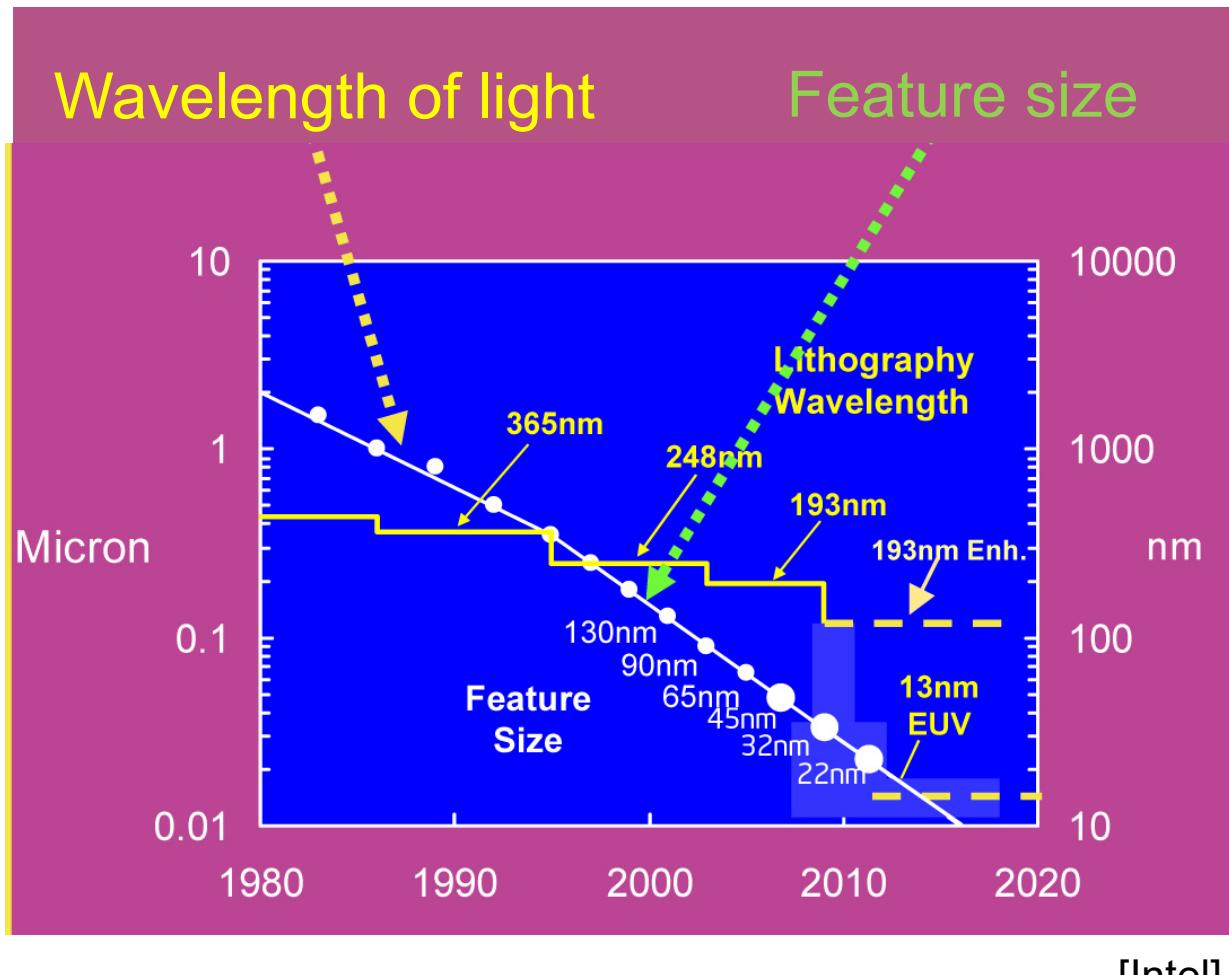
# Amdahl's Law (2)

- Fraction  $f$  parallelizable
- Fraction  $1 - f$  completely serial
- Speedup = 
$$\frac{1}{\frac{1-f}{1} + \frac{f}{N}}$$
- Example:  $f = 90\%$ , then Speedup < 10
- Example:  $f = 75\%$ , then Speedup < 4
- The serial part of a parallel program is the bottleneck!!!

# Optical Lithography

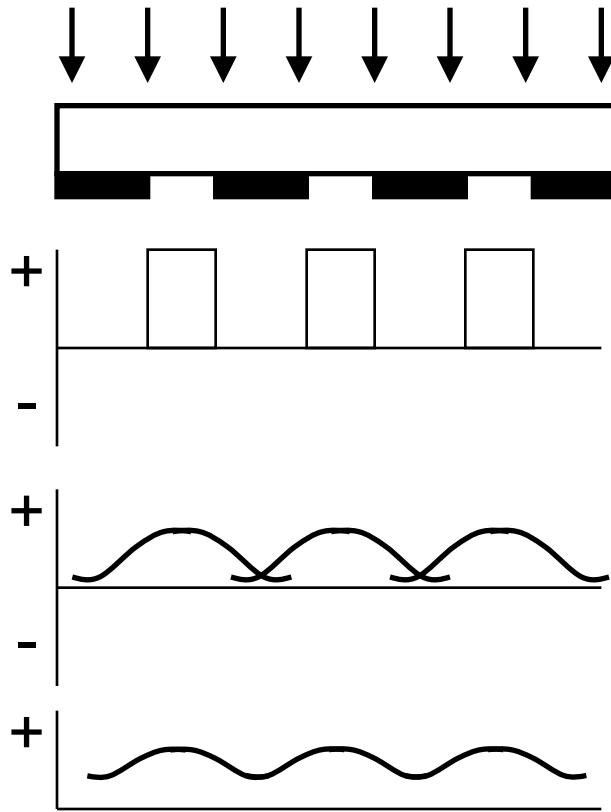


# Lithography Trends

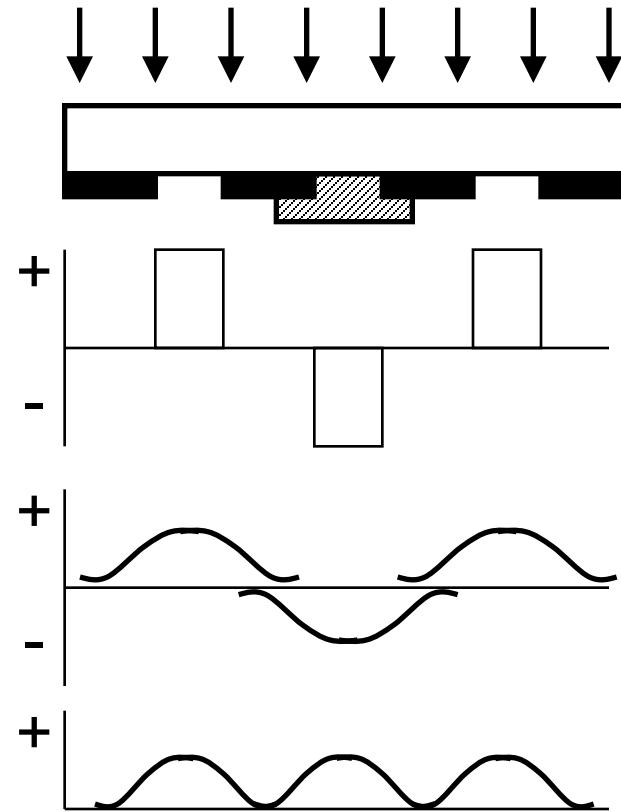


# Lithography Improvements (1a)

Use Light Phase Inversion (proposed in 1982)



Ampli-  
tude  
Inten-  
sity



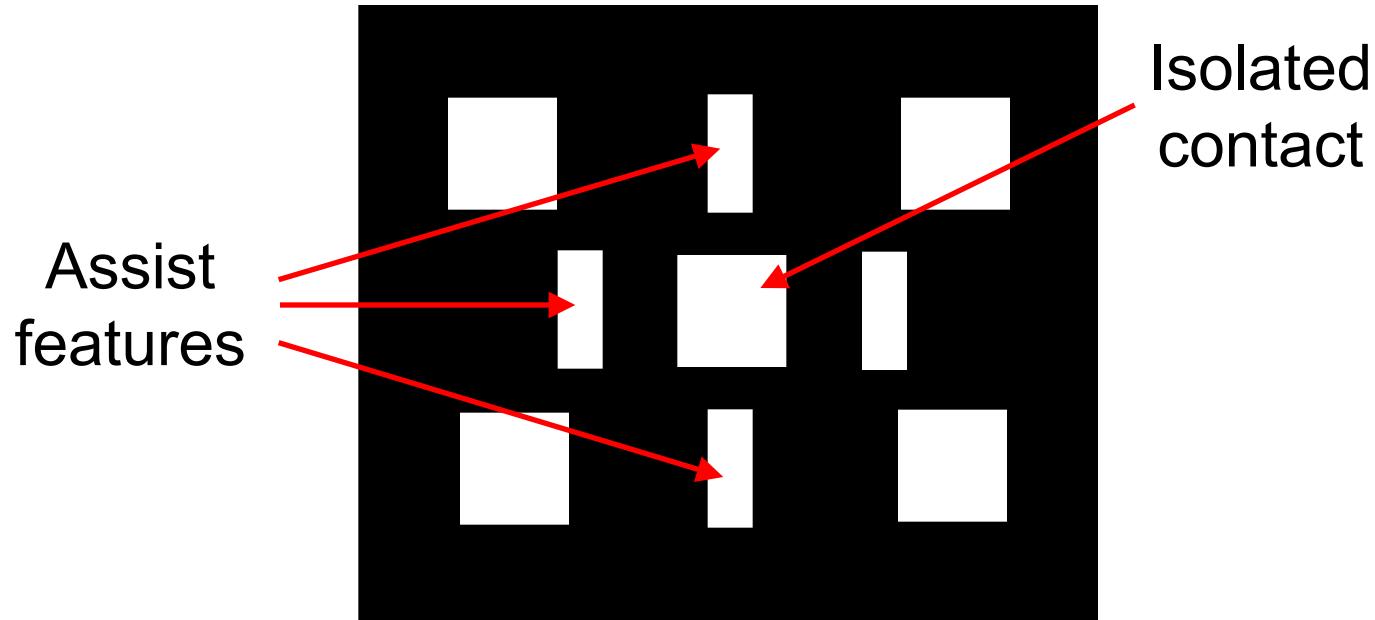
# Lithography Improvements (1b)

- Phase Shifting Masks can easily improve resolution by 50~100%
- E.g., Feature size 500nm → 160nm
- Technique also applicable to shorter wavelengths of light
- However, masks are more expensive!

# Lithography Improvements (2)

Diffraction of light by repetitive masks

Interference lithography

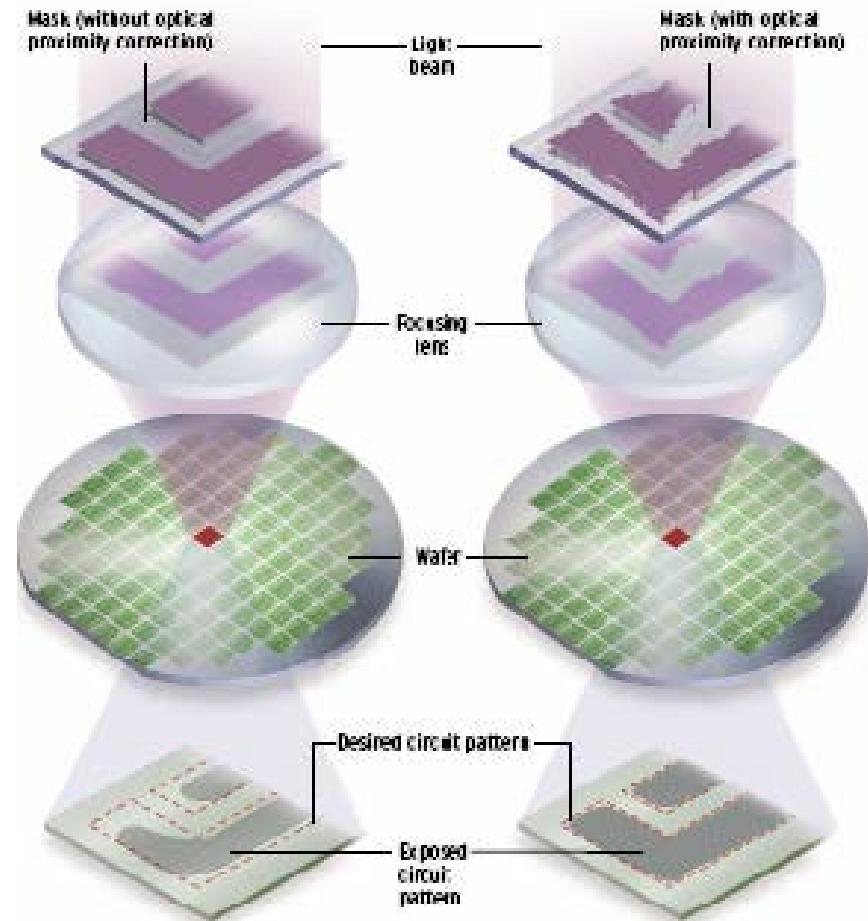


Enhances contrast significantly

# Lithography Improvements (3a)

## Computational Lithography

Use numerical simulations to improve mask design



[IEEE Spectrum]

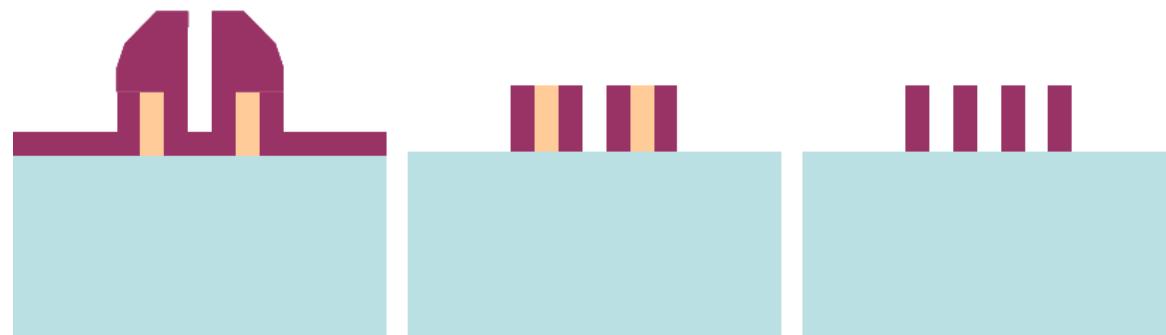
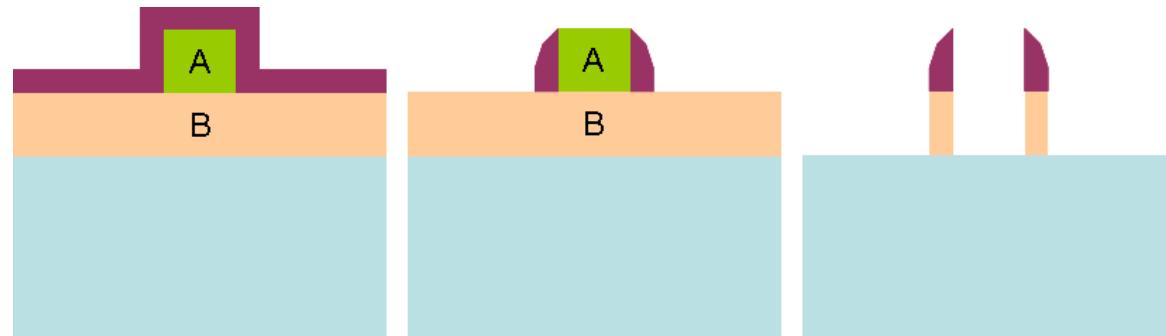
# Lithography Improvements (3b)

## **Computational Lithography Techniques:**

- Resolution Enhancement Technology (RET), exploiting interference patterns
- Optical Proximity Correction (OPC), counteracting optical distortions
- Complex modeling of lens system and photoresist

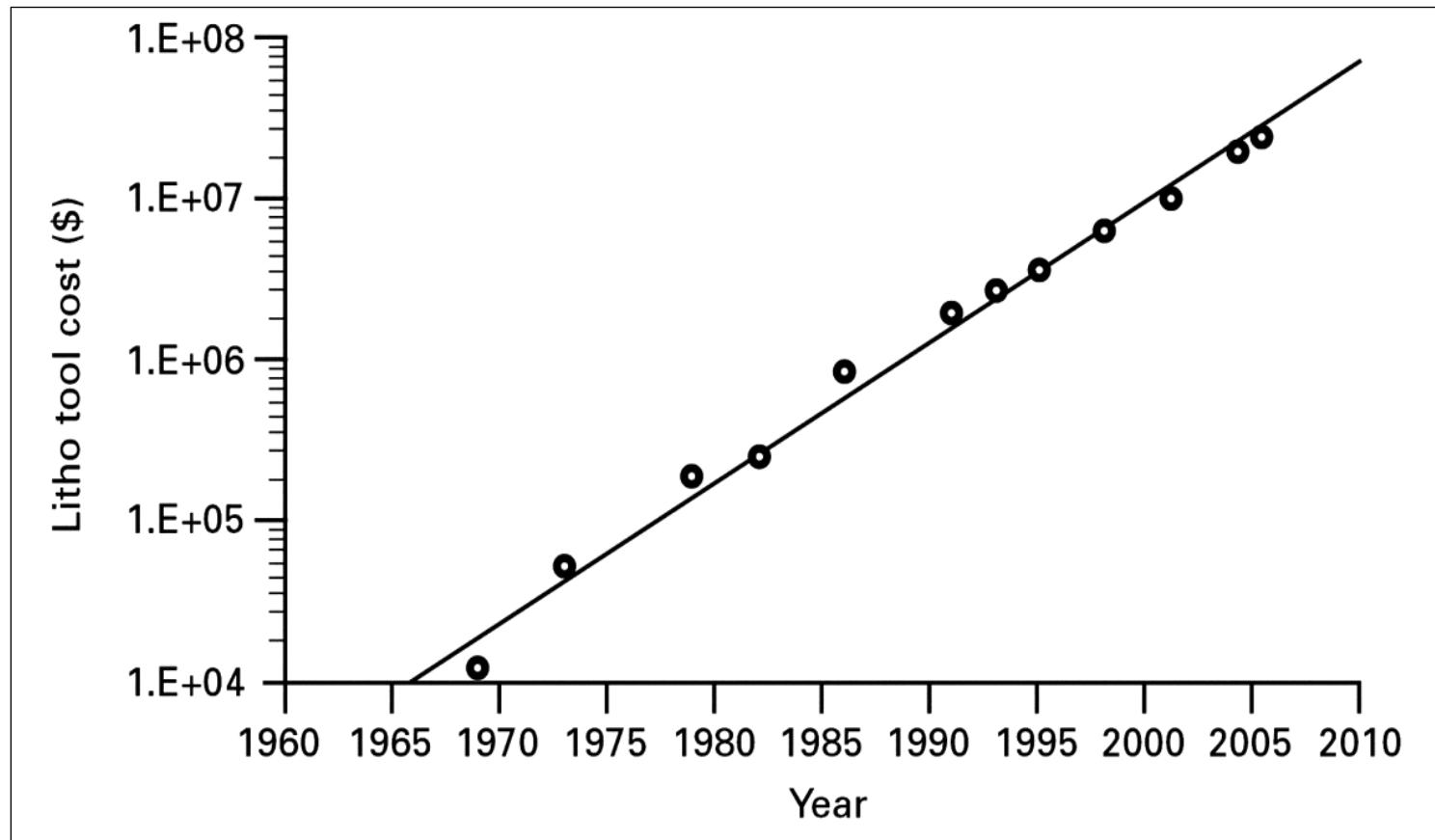
# Lithography Improvements (4)

Multipatterning (to go below 45nm)



# Moore's Law

## Cost of Equipment

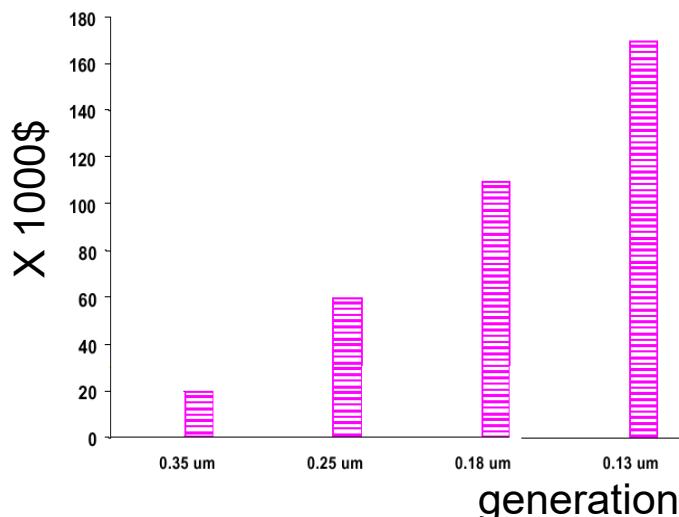


Cost of process equipment for photo lithography  
(1969–2005) [Intel, 2005]

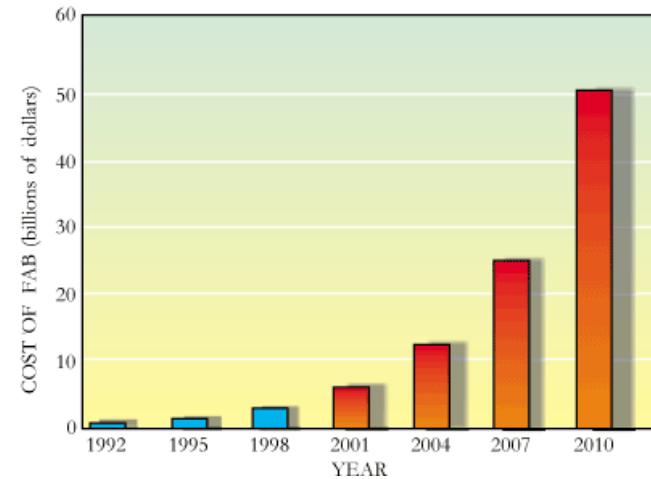
# Investment Costs

Cost of building semiconductor plants: **doubling / 3 years**

Mask cost



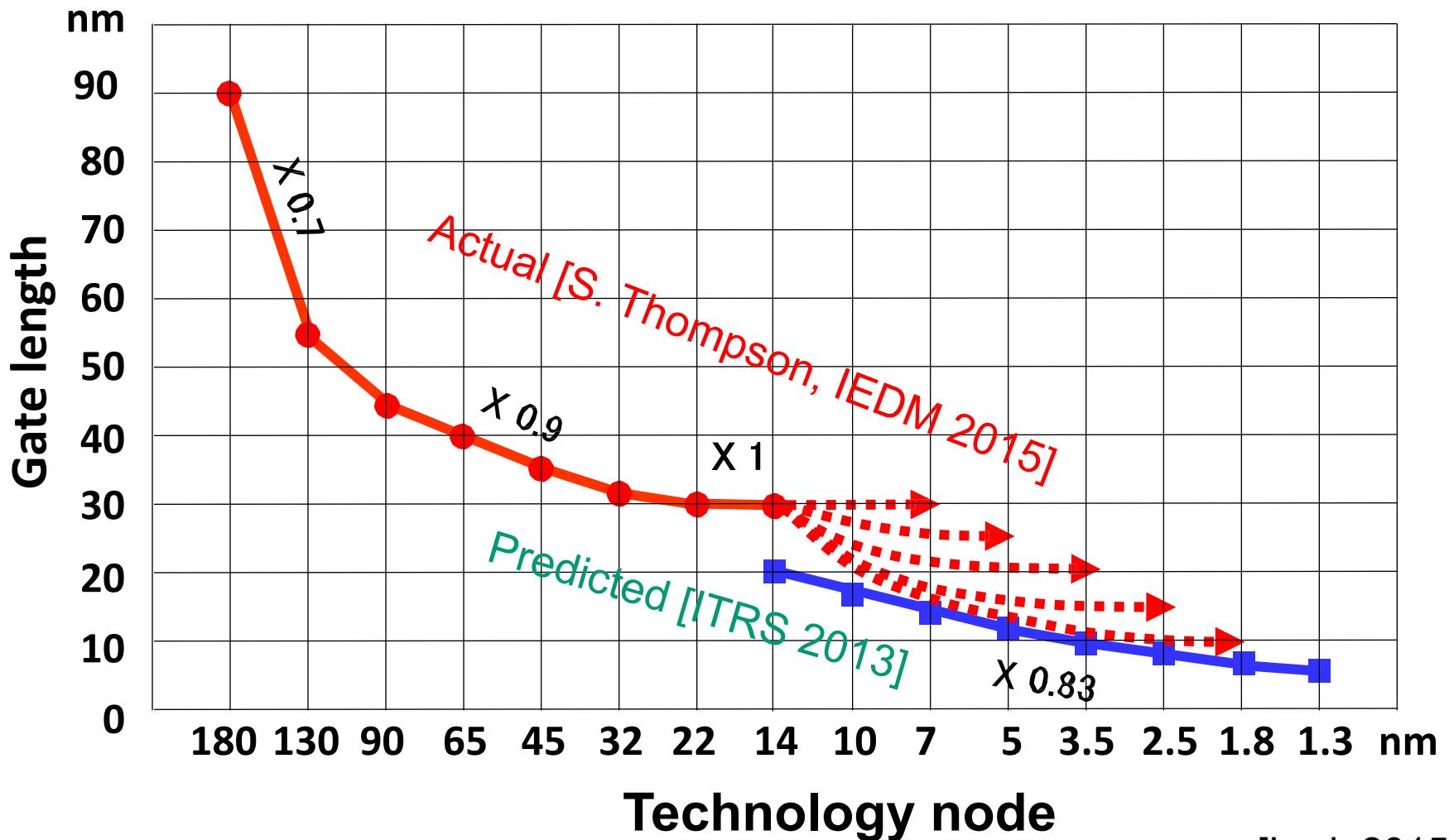
Plant cost



So, rather than *technological* limitations,  
we may face *economical* limitations

# Moore's Law: Dead at 50?

Official vs. actual technology node



[Iwai, 2015]

# Moore's Law's Law

The number of people predicting the death of Moore's law doubles every two years

# Moore's Law 3.0

- Moore's Law 1.0: Scaling Up (More for \$)
  - Only applies to Flash and supercomputers today
- Moore's Law 2.0: Scaling Down (Less \$ for same)
  - Higher costs are putting this version in danger
- Moore's Law 3.0: Scaling Out
  - New materials
  - Silicon photonics
  - Memory computing
  - Other functionalities on chips: More than Moore

[Mack, 2013]

# International Technology Roadmap for Semiconductors

- 15-year assessment of semiconductor industry's future technology requirements
- Sponsored by 5 leading chip manufacturing regions: U.S., EU, Japan, Korea, Taiwan
- Manufacturers, Universities, National labs
- Aim to advance chip manufacturing

Replaced by the International Roadmap for Devices and Systems (IRDS)

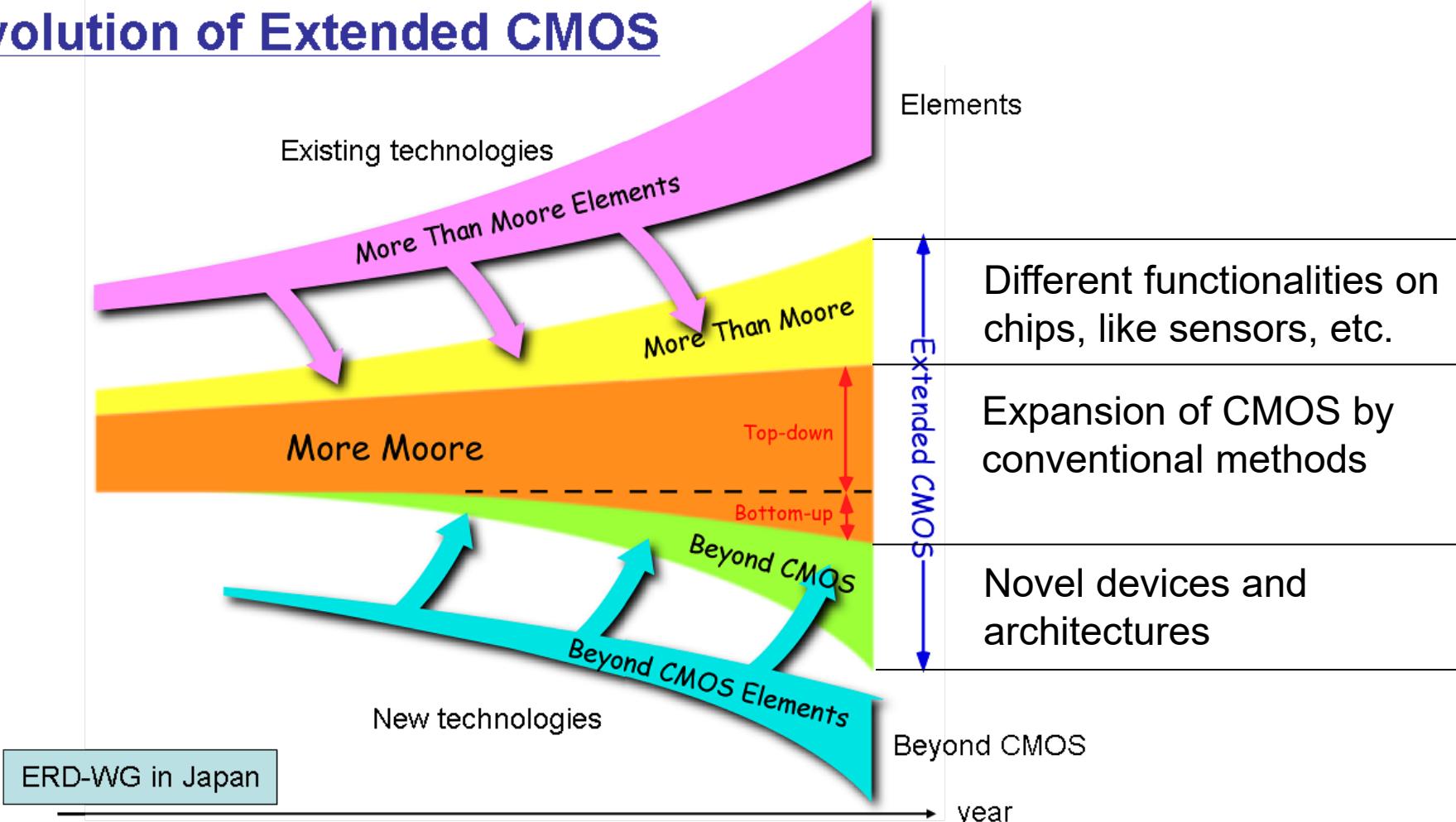
# Quiz 5

What was the International Technology Roadmap for Semiconductors (ITRS)?

- a. It was a report by semiconductor industries to satisfy their shareholders
- b. It was an effort by the US government to stimulate the semiconductor industry
- c. It was a biannual report intended to coordinate product development by semiconductor-related industries
- d. It was a plan drawn up by experts from industry, government, and the academic world according to which semiconductor industry was required to develop products

# More Moore, More Than Moore, Beyond CMOS, and Extended CMOS

## Evolution of Extended CMOS



[ITRS 2011 Report]

# End of Lecture 8

# Homework 3

1. Describe Moore's Law in your own words.
2. What is the cost point at which Moore's Law is applicable? Describe in your own words.
3. What design principle worked in the past in concert with Moore's Law to make transistors faster and at the same time consume less power? Around which year did it stop working, and why? Reply in your own words.

Email to: peper@nict.go.jp; Deadline: 10 June 2025

Subject line: "Homework 3, #YOUR NR#"

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and student number!