Improving Bank-Level Parallelism for Irregular Applications
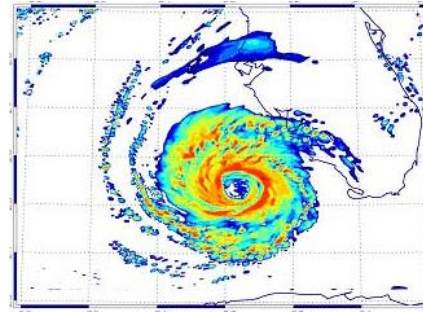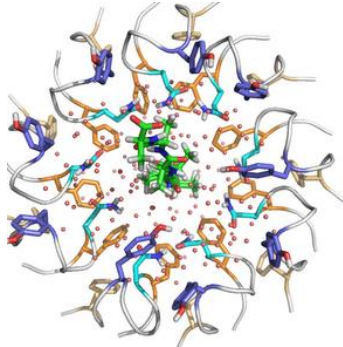
Xulong Tang, Mahmut Kandemir,

Praveen Yedlapalli, Jagadish Kotra

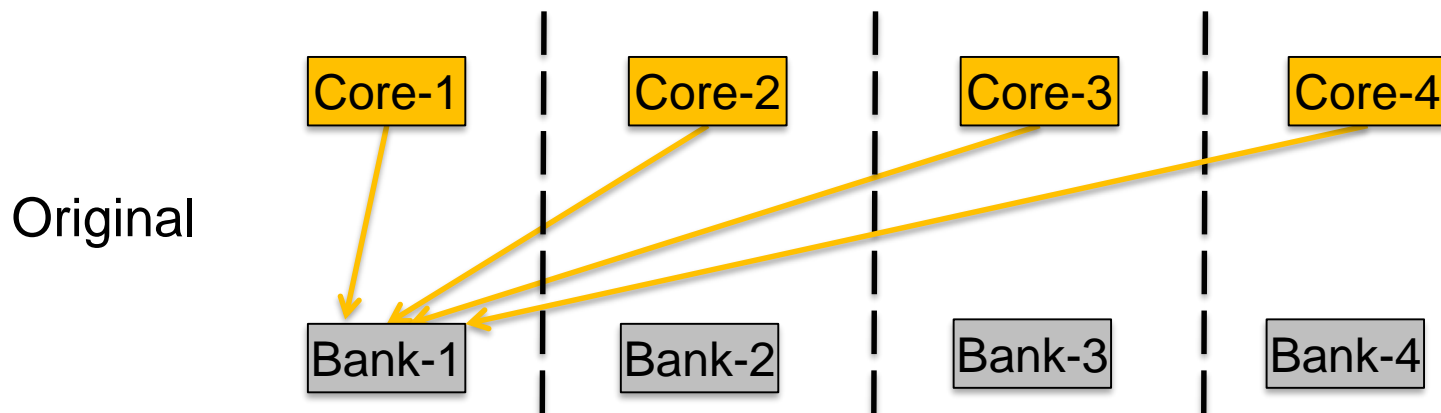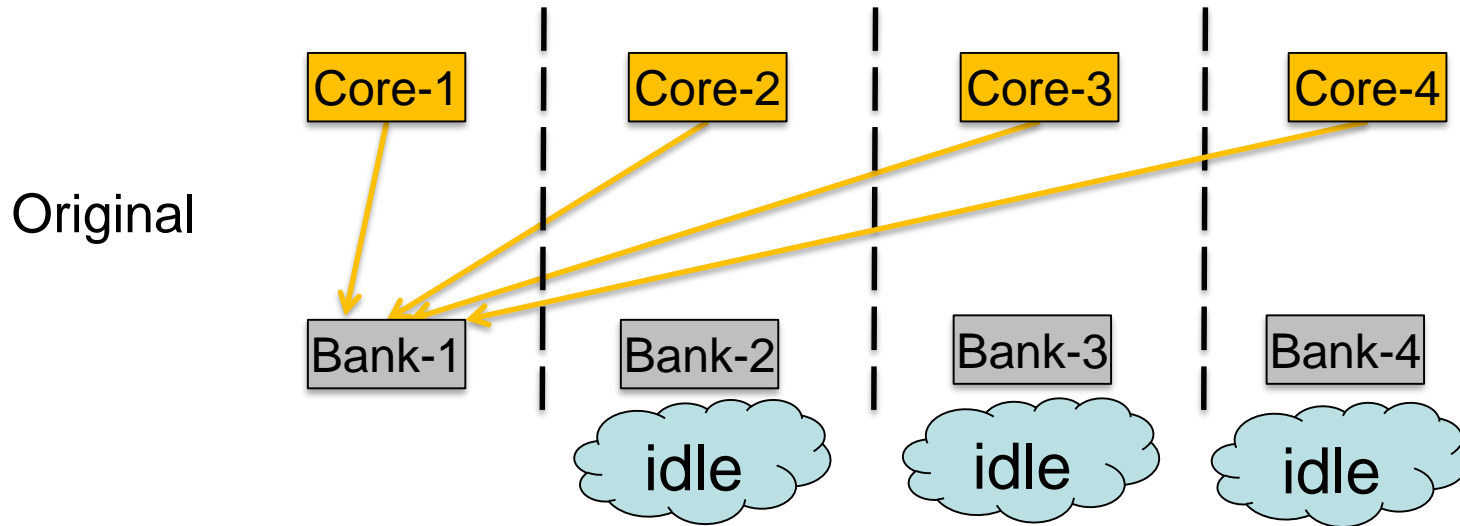**MICRO '49**

PennState

Irregular Applications on Multicores/Manycores

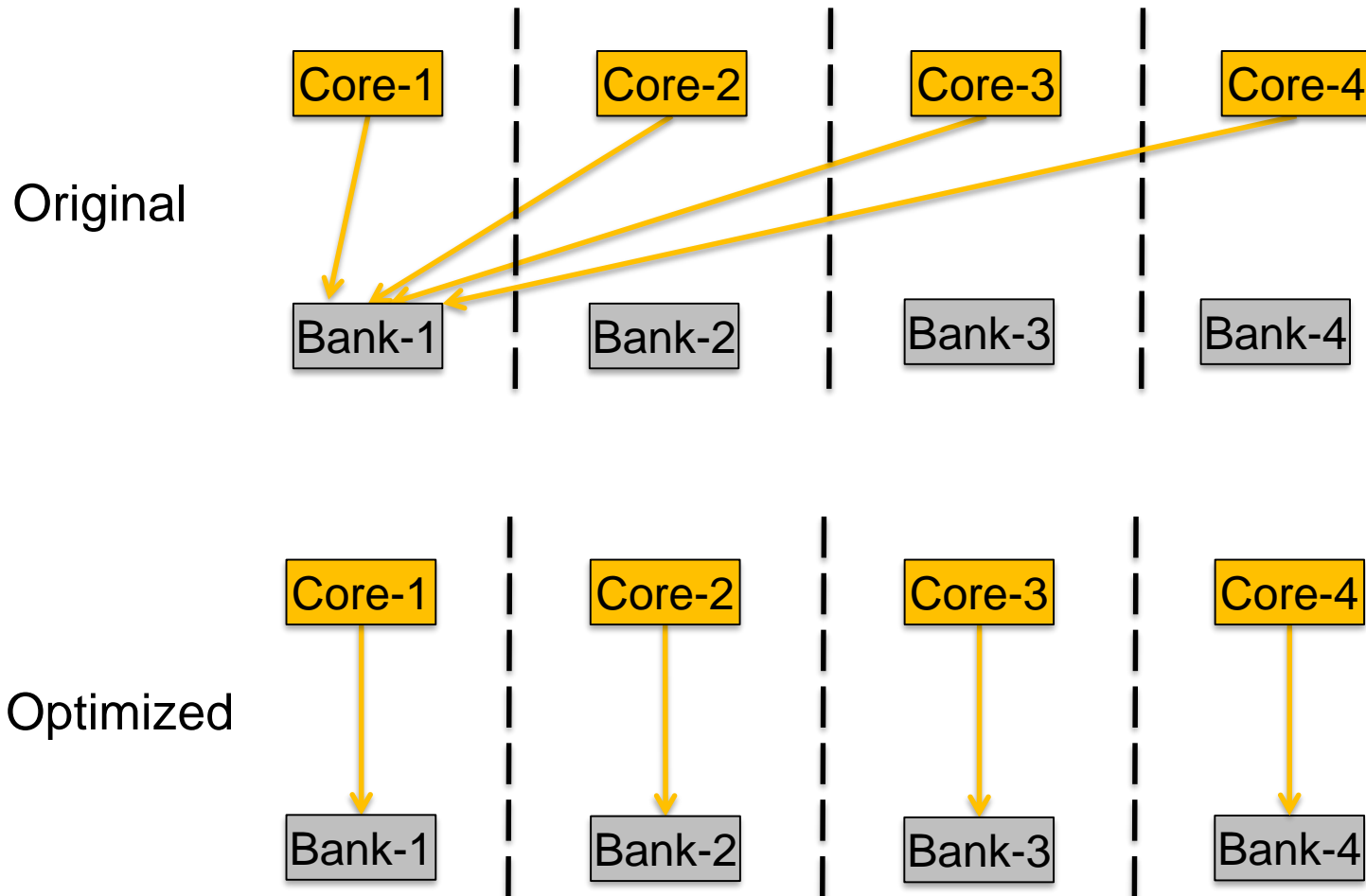# Irregular Memory Accesses

Original

Irregular Memory Accesses

Original

Core-1   Core-2   Core-3   Core-4

Bank-1   Bank-2   Bank-3   Bank-4

idle   idle   idle

Bank-Level Parallelism

Original

Core-1   Core-2   Core-3   Core-4

Bank-1   Bank-2   Bank-3   Bank-4

Optimized

Core-1   Core-2   Core-3   Core-4

Bank-1   Bank-2   Bank-3   Bank-4

Bank-Level Parallelism

Core-1   Core-2   Core-3   Core-4

Original

Our proposal: Software approach to improve BOTH bank-level parallelism and bank-reuse for irregular applications running on manycore platforms.

Core-1   Core-2   Core-3   Core-4

Optimized

Bank-1   Bank-2   Bank-3   Bank-4

Bank-Level Parallelism

Original

Core-1   Core-2   Core-3   Core-4

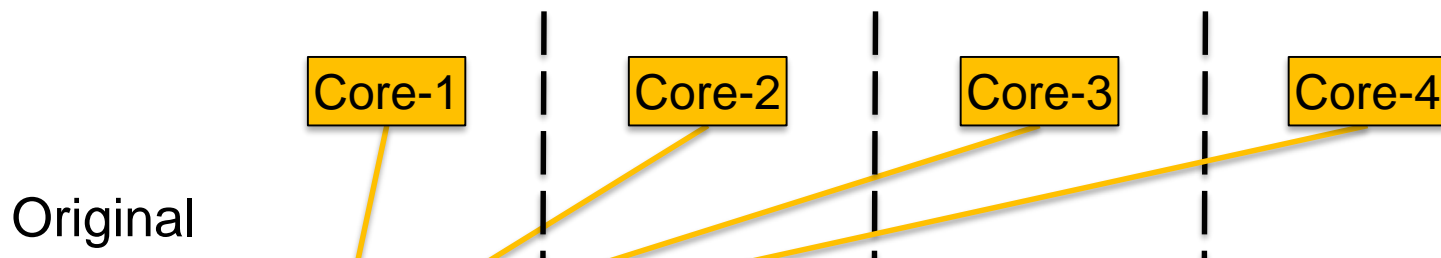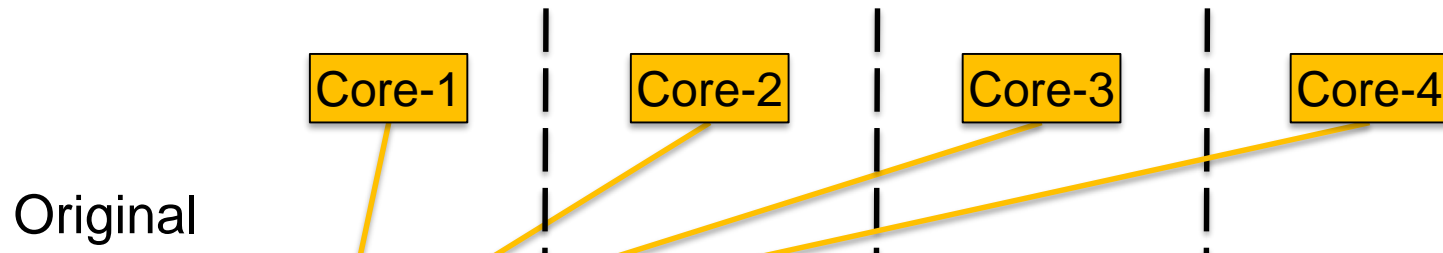**Our proposal:** Software approach to improve **BOTH** bank-level parallelism and bank-reuse for irregular applications running on manycore platforms.

Core-1   Core-2   Core-3   Core-4
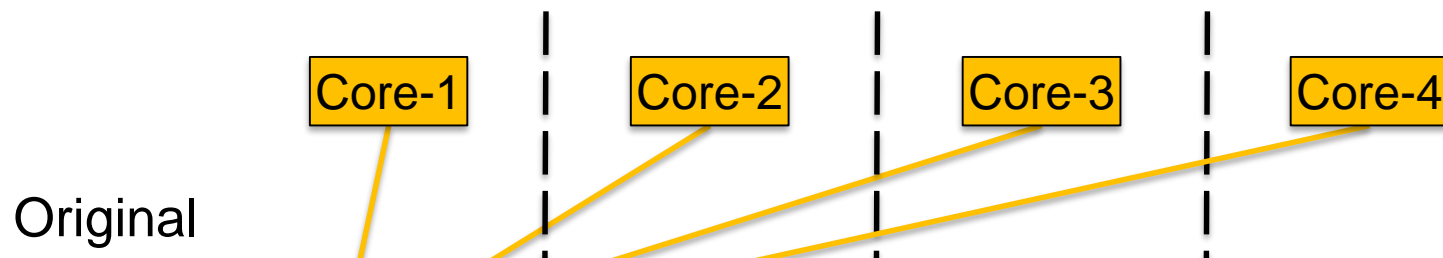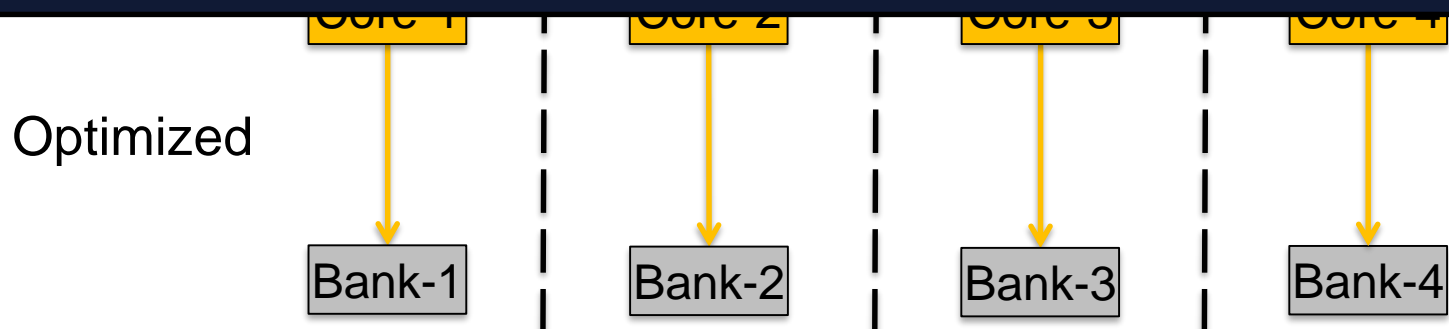
BLP improvement: **46.8%**
Execution time reduction: **18.3%**

Bank-Level Parallelism

Original

Core-1   Core-2   Core-3   Core-4

Tomorrow, 10:20am, Hall I
Session 7 (best paper candidates)

Optimized

Core-1   Core-2   Core-3   Core-4

Bank-1   Bank-2   Bank-3   Bank-4