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CS383 HW 1
I pledge my honor that I have abided by the Stevens Honor System.

1.5)

a. Processor 1: $IPS = \frac{3.0\ GHz}{1.5\ CPI} = 2.0 \times 10^9$
   Processor 2: $IPS = \frac{2.5\ GHz}{1.0\ CPI} = 2.5 \times 10^9$
   Processor 3: $IPS = \frac{4.0\ GHz}{2.2\ CPI} = 1.8 \times 10^9$
   Processor 2 has the highest performance.
b. Processor 1:
   $(3.0 \times 10^9) \times 10 = 3.0 \times 10^{10}$ cycles in 10 seconds
   $(2.0 \times 10^9) \times 10 = 2.0 \times 10^{10}$ instructions in 10 seconds
   Processor 2:
   $(2.5 \times 10^9) \times 10 = 2.5 \times 10^{10}$ cycles in 10 seconds
   $(2.5 \times 10^9) \times 10 = 2.5 \times 10^{10}$ instructions in 10 seconds
   Processor 3:
   $(4.0 \times 10^9) \times 10 = 4.0 \times 10^{10}$ cycles in 10 seconds
   $(2.2 \times 10^9) \times 10 = 2.2 \times 10^{10}$ instructions in 10 seconds
c. $CPU\ time = \frac{Instruction\ count \times CPI}{Clock\ Rate}$
   $(.7)CPU\ time = \frac{Instruction\ count \times (1.2)CPI}{(x)Clock\ Rate} \rightarrow$ x = 1.71 $\rightarrow$
   Clock rate increases by 71%
   Processor 1: $3.0 \times 1.71 = 5.1$ GHz
   Processor 2: $2.5 \times 1.71 = 4.3$ GHz
   Processor 3: $4.0 \times 1.71 = 6.8$ GHz

1.6)

a. P1:
   $CPU\ Clock\ Cycle = (0.1 \times 10^6) + (2 \times 2 \times 10^5) + (3 \times 5 \times 10^5) + (3 \times 2 \times 10^5) = 2.6 \times 10^6$
   $CPI = \frac{2.6 \times 10^6}{10^6} = 2.6$
   P2:
   $CPU\ Clock\ Cycle = (0.2 \times 10^6) + (2 \times 2 \times 10^5) + (2 \times 5 \times 10^5) + (2 \times 2 \times 10^5) = 2.0 \times 10^6$
   $CPI = \frac{2 \times 10^6}{10^6} = 2.6$
b. P1:
   $CPU\ Clock\ Cycle = (0.1 \times 10^6) + (2 \times 2 \times 10^5) + (3 \times 5 \times 10^5) + (3 \times 2 \times 10^5) = 2.6 \times 10^6$
   P2:
   $CPU\ Clock\ Cycle = (0.2 \times 10^6) + (2 \times 2 \times 10^5) + (2 \times 5 \times 10^5) + (2 \times 2 \times 10^5) = 2.0 \times 10^6$

1.7)

a. $CPU\ Time\ =\ Instruction\ Count\ \times CPI\ \times Clock\ Cycle\ Time$

$\rightarrow CPI\ =\ \frac{CPU\ Time}{Instruction\ Count \times Clock\ Cycle\ Time}$

Compiler A: $\frac{1.1s}{(1.0 \times 10^{9}) \times (1 \times 10^{-9}\ s)} = 1.1$

Compiler B: $\frac{1.5s}{(1.2 \times 10^{9}) \times (1 \times 10^{-9}\ s)} = 1.25$

b. $(x) \times (1.1) \times (1.0 \times 10^{9}) \times (1 \times 10^{-9}\ s)\ = (1.25) \times (1.2 \times 10^{9})\ \times\ (1 \times 10^{-9}\ s)$

$\rightarrow x =\ 1.36$

The clock of processor running compiler A's code is 27% slower than the clock of processor running compiler B's code.

c. Compiler C: $(6.0 \times 10^{8})\ \times (1.1)\ \times (1 \times 10^{-9}\ s) = 0.66\ \text{s}$

$\frac{1.1}{0.66} = 1.67 \rightarrow$ Compiler C is 67% faster than Compiler A.

$\frac{1.5}{0.66} = 2.27 \rightarrow$ Compiler C is 127% faster than Compiler A.

1.8.1) $\frac{power}{voltage^2 \times frequency}$

Pentium 4 Prescott processor: $\frac{90W}{(1.25)^2 \times (3.6\ GHz)} = 16\ \ \rightarrow 16 \times 2 = 32\ nF$

Core i5 Ivy Bridge processor: $\frac{40W}{(0.9)^2 \times (3.4\ GHz)} = 14.52 \rightarrow 14.52 \times 2 = 29.04\ nF$

1.8.2)

Percentage of static power:

Pentium 4 Prescott processor: $\frac{10}{10+90} = 10\%$

Core i5 Ivy Bridge processor: $\frac{30}{30+40} = 47.86\%$

Ratio of static to dynamic power:

Pentium 4 Prescott processor: $\frac{10W}{90W} = 0.11$

Core i5 Ivy Bridge processor: $\frac{30W}{40W} = 0.75$

1.8.3) $P_{total} = P_{static} + P_{dynamic}$

$P = V \times I$

$0.9P_1 = P_2$

$0.9P_1 = IV_2$

$\frac{0.9P}{I} = V_2$

The voltage must be reduced by 90%.

1.10.1)

$\frac{15}{2} = 7.5$

$(3.14) \times (10)^2 = 314$

$\frac{176.625}{84} = 2.10$

$\frac{314}{100} = 3.14$

$\frac{1}{1+(.02\times(\frac{2.1}{2}))^2} = 0.959$

$\frac{1}{1+(.031\times(\frac{3.14}{2}))^2} = 0.909$

1.10.2

Cost per die 1: $\frac{12}{(84)(0.959216)} = 0.15$

Cost per die 2: $\frac{15}{(100)(0.909289)} = 0.16$

1.10.3

$\frac{176.625}{84.1\times1.1} = 1.91$

$\frac{314}{100\times1.1} = 2.85$

$\frac{1}{1+((.02)(1.15)\times(\frac{1.91}{2}))^2} = 0.958$

$\frac{1}{1+((.051)(1.15)\times(\frac{2.85}{2}))^2} = 0.906$