Viraj Bontha

+91 6281122607 | bonthaviraj@gmail.com | linkedin.com/in/viraj-bontha | Hyderabad, Telangana

Education

BITS Pilani — Goa Campus
B.E. (Hons.) Electrical and Electronics Engineering — Current GPA: 8.13 — *2022-2026*

FIITJEE JUNIOR COLLEGE — Hyderabad
Telangana Board of Intermediate Education (TSBIE) (CLASS XII) — 97.6 percent — *2022*

DAV PUBLIC SCHOOL — Hyderabad
CBSE (CLASS X) — 96 percent — *2020*

Experience

Research Intern — May 2024 - Jul 2024
CSIR - Central Electronics Engineering Research Institute (CEERI) — *Pilani, Rajasthan*
- Developed an optimised decimation filter for a network chip with implementation in MATLAB.

Circuital and Electronics Intern — Oct 2023 - Jan 2024
Khageshvara Aviation Technology Pvt. Ltd — *Remote*
- Collaborated on electronic system enhancements, optimising designs to align with company objectives and improve performance.

Projects

5-Stage Pipelined MIPS Processor — Feb 2025 - Mar 2025
- Designed a **5-stage pipelined MIPS processor** supporting **multiple instructions**.
- Implemented **32-bit data and address buses** with **4 pipeline registers**.
- Developed a **hazard detection unit** and **forwarding unit** for efficient pipeline execution.
- Verified functionality using a **testbench** with a **predefined instruction sequence.**
- Analysed synthesis feasibility and optimised for **sequential logic efficiency.**

SoC Verification using SystemVerilog — Dec 2024 - Present
- Developed and verified testbenches for **memory verification** (**FIFO**) and **bus protocols** (**APB, AHB, AXI**).
- Verified **interface communication protocols (SPI, UART) and sequential logic blocks (Flip-Flops)**.
- Currently enhancing expertise in functional coverage techniques.

Digital Filter Design - Design and Implementation of Decimation Filters — May 2024 - Jul 2024
- Developed an **optimised decimation filter for a network chip.**
- Researched, selected, and implemented efficient **CIC, FIR Compensation, and Half-Band FIR Filters in MATLAB.**
- Achieved **69 percent hardware savings and 28 percent power reductio**n compared to traditional architectures.

POSITIONS OF RESPONSIBILITY

International Programmes Collaboration Division Student Coordinator: Supported student and faculty exchange programs, coordinated joint academic activities, and assisted in planning international academic events.
Department of Backstage and Infrastructure Management: Managed backstage operations and infrastructure for various events in my college.

COMPETITIONS AND ACHIEVEMENTS

2nd Prize – IEEE Student Chapter Paper Presentation Contest: Presented research on Pseudo Random Number Generator verification. Verified the PRNG design using SystemVerilog for ASIC applications.
DigiCraft - Digital Circuit Design Competition: Excelled in Digicraft, showcasing skills in digital design and problem-solving.
CBSE National Science Exhibition: Developed an automated irrigation system, earning national recognition.

Student Image

Candidate Code – **CC 0104R**

Subjects/ Electives	Digital Design, Computer Architecture, Analog and Digital VLSI Design, Static Timing Analysis, Microelectronic Circuits, Microprocessors and Interfacing, Electronic Devices, Control Systems, Signals & Systems, Digital Signal Processing, Computer Programming.
Technical Proficiency	Verilog, SystemVerilog, Cadence Virtuoso, MATLAB, C Programming, Python.

SUMMER INTERNSHIP/ WORK EXPERIENCE

Research Intern *May 2024 - Jul 2024*
CSIR - Central Electronics Engineering Research Institute (CEERI), Pilani, Rajasthan
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Circuital and Electronics Intern *Oct 2023 - Jan 2024*
Khageshvara Aviation Technology Pvt. Ltd.
Collaborated on electronic system enhancements, optimising designs to align with company objectives and improve performance.

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International Programmes Collaboration Division Student Coordinator *Apr 2024 - Present*

- Supported student and faculty exchange programs, coordinated joint academic activities, and assisted in planning international academic events, enhancing my college's global partnerships and presence.

Department of Backstage and Infrastructure Management Dec 2022 - Apr 2024

- Managed backstage operations and infrastructure for various events in my college. Played a key role in operating Audio-Visual systems, coordinating logistics, and ensuring smooth event execution during various fests.

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CBSE National Science Exhibition *Jan 2020*

- Developed an **automated irrigation system**, earning **national recognition**.