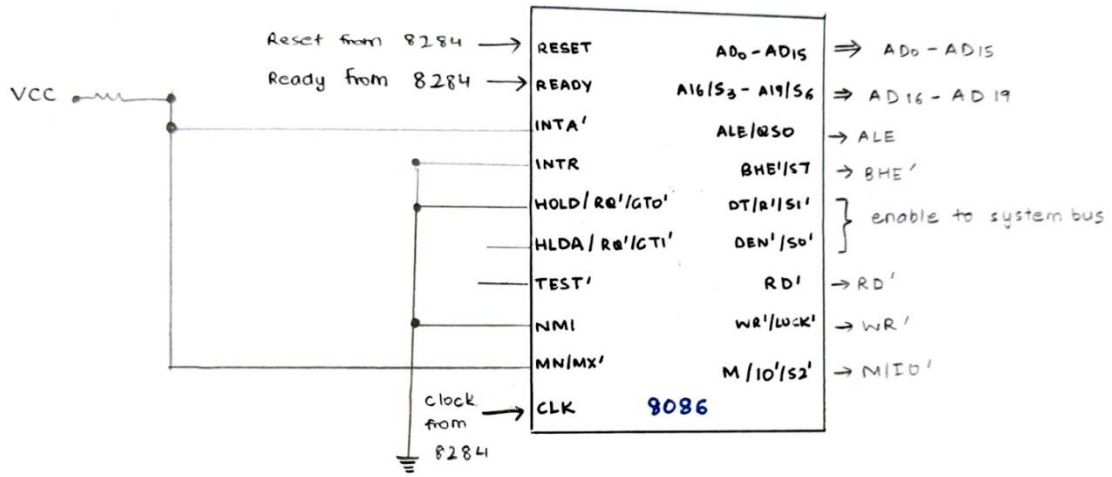
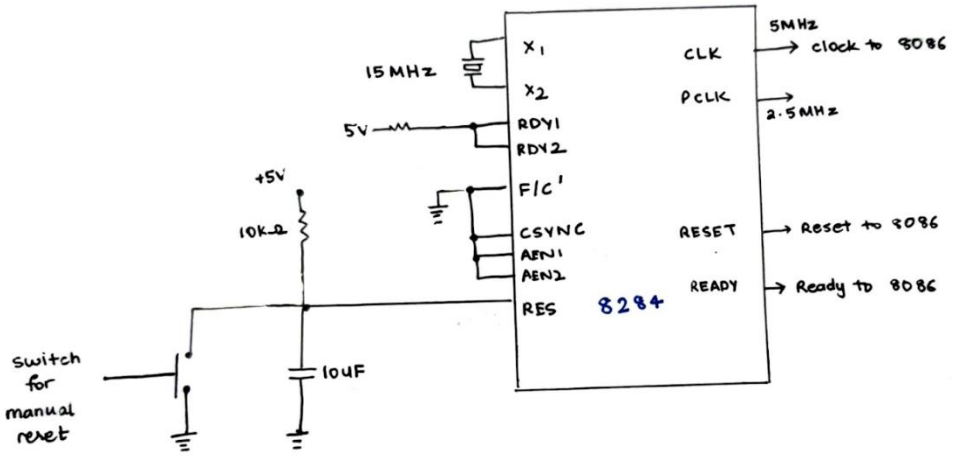
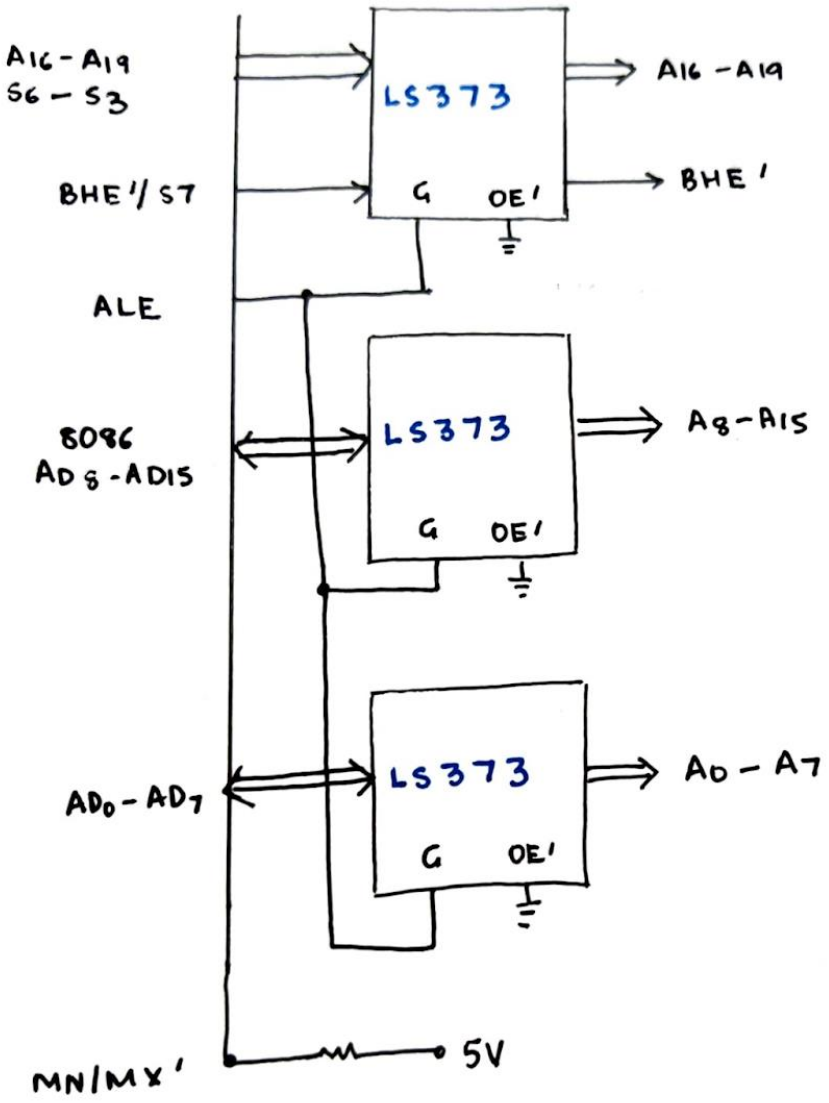
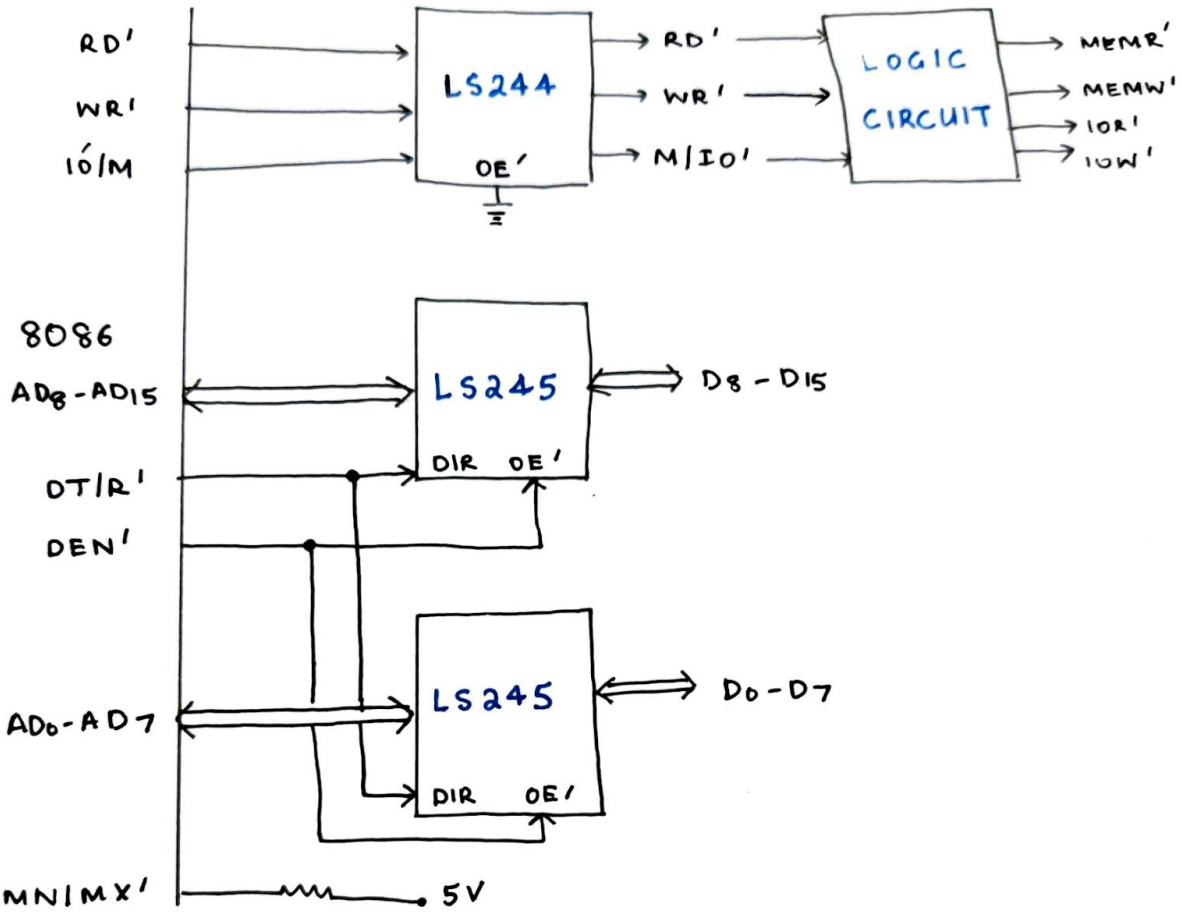
Design


Reset from 8284
Ready from 8284
VCC
RESET
READY
INTA'
INTR
HOLD/RQ'/GT0'
HLDA/RQ'/GT1'
TEST'
NMI
MN/MX'
CLK
8086
clock from 8284
AD0 - AD15
A16/S3 - A19/S6
ALE/QS0
BHE'/S7
DT/R'/S1'
DEN'/S0'
RD'
WR'/LOCK'
M/IO'/S2'
⇒ AD0 - AD15
⇒ AD16 - AD19
→ ALE
→ BHE'
enable to system bus
→ RD'
→ WR'
→ M/IO'

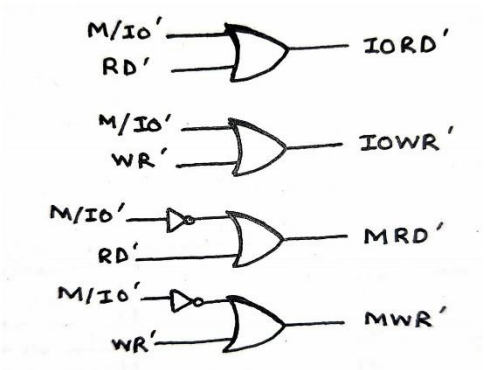

15 MHz
X1
X2
5V
RDY1
RDY2
+5V
10KΩ
F/C'
CSYNC
AEN1
AEN2
RES
8284
CLK
PCLK
RESET
READY
5MHz
clock to 8086
2.5MHz
Reset to 8086
Ready to 8086
switch for manual reset
10uF



System Bus of 8086 (Address)



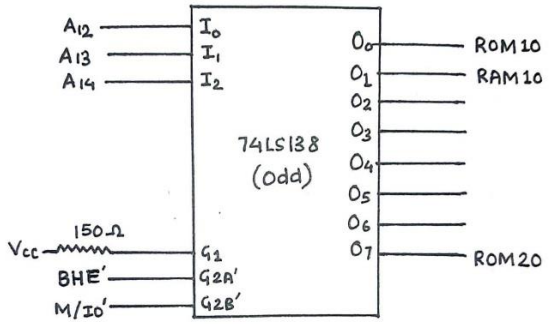
System Bus of 8086 (Data + Control)

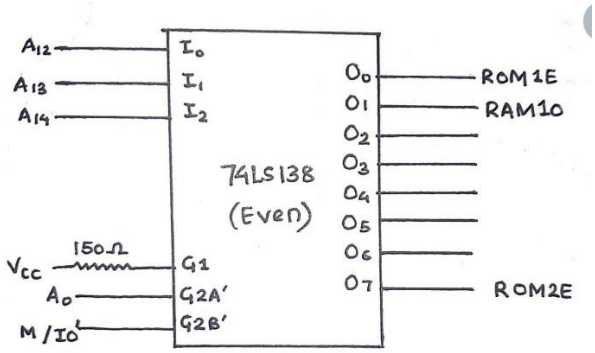


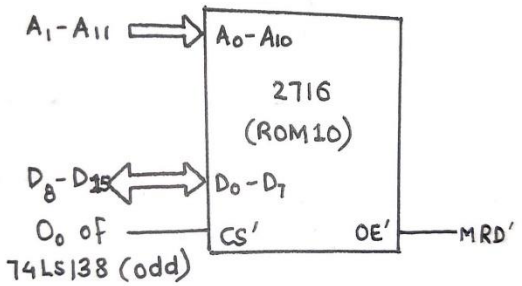
M/IO'	RD'	WR'	Bus Cycle
1	0	1	MRD'
1	1	0	MWR'
0	0	1	IORD'
0	1	0	IOWR'

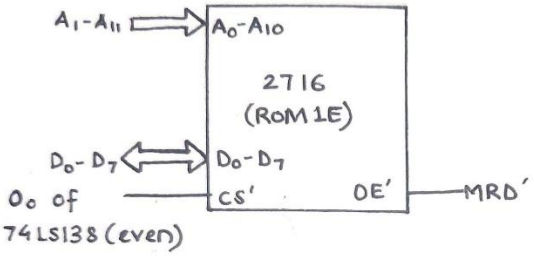
Here, MRD' and MWR' correspond to the memory read (MEMR') and memory write (MEMW') bus cycles, IORD' and IOWR' correspond to I/O read (IOR') and I/O write (IOW') bus cycles respectively

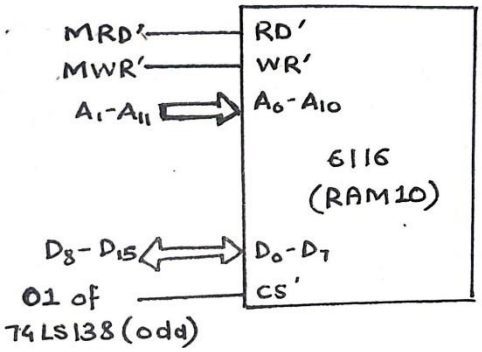
Memory Interfacing Diagrams

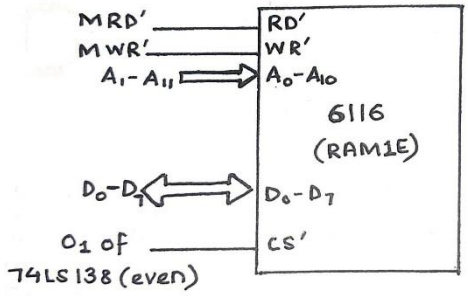


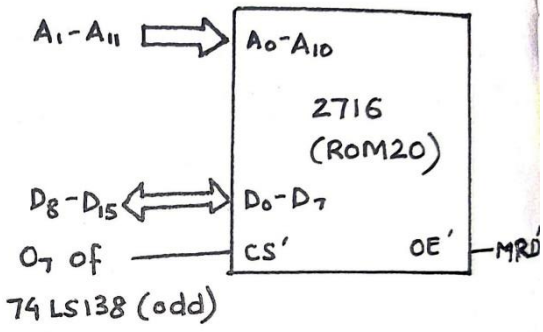


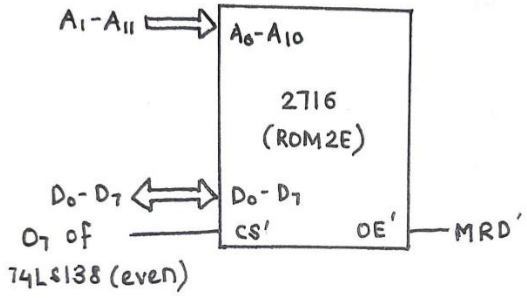




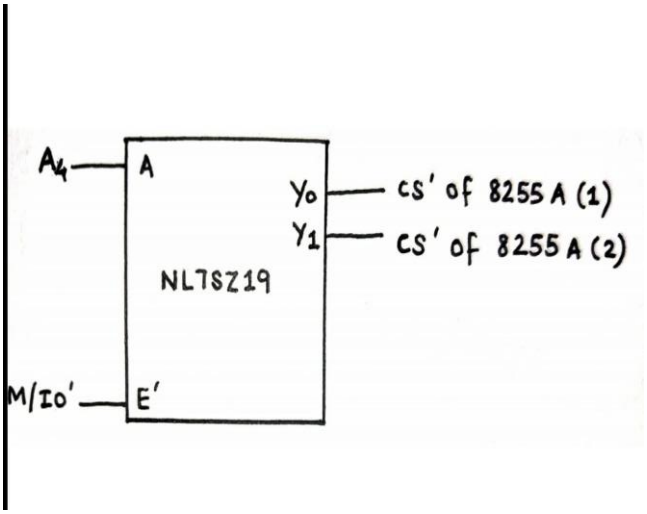


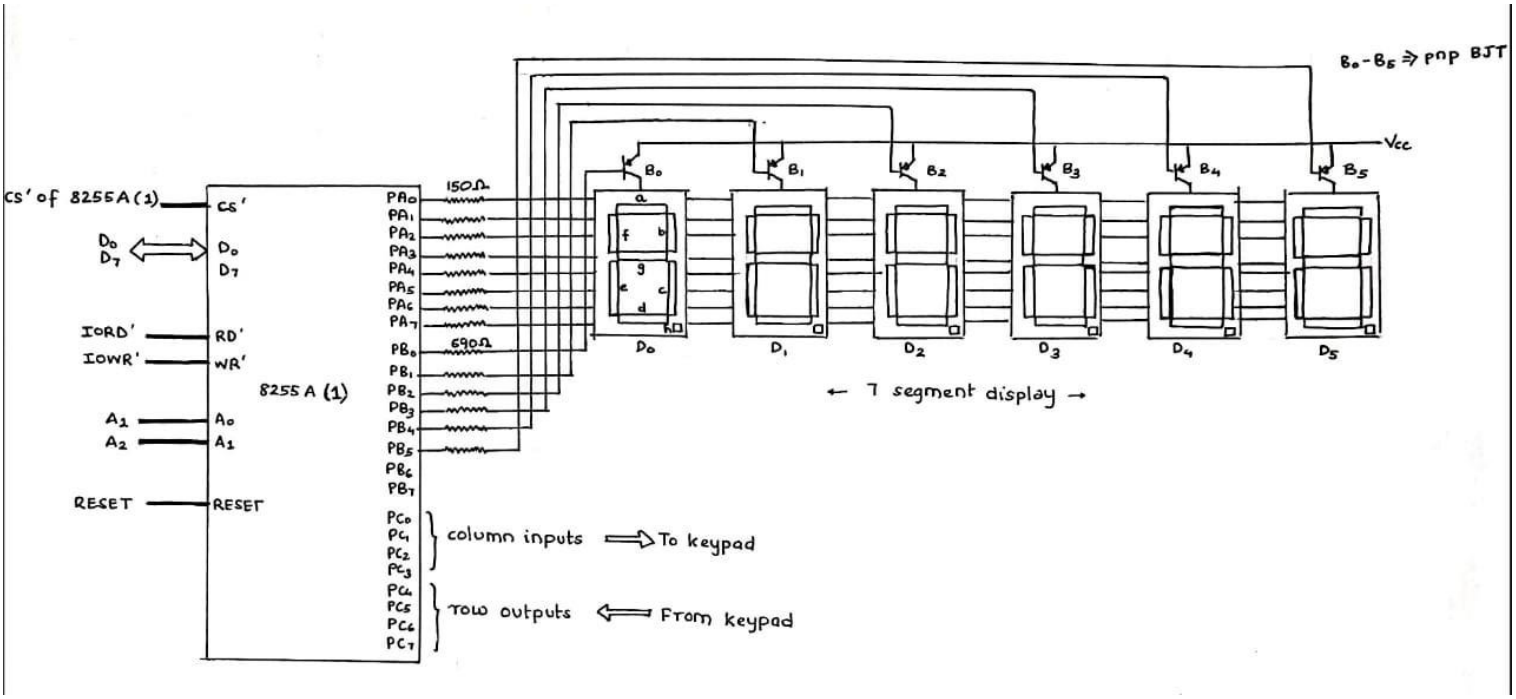


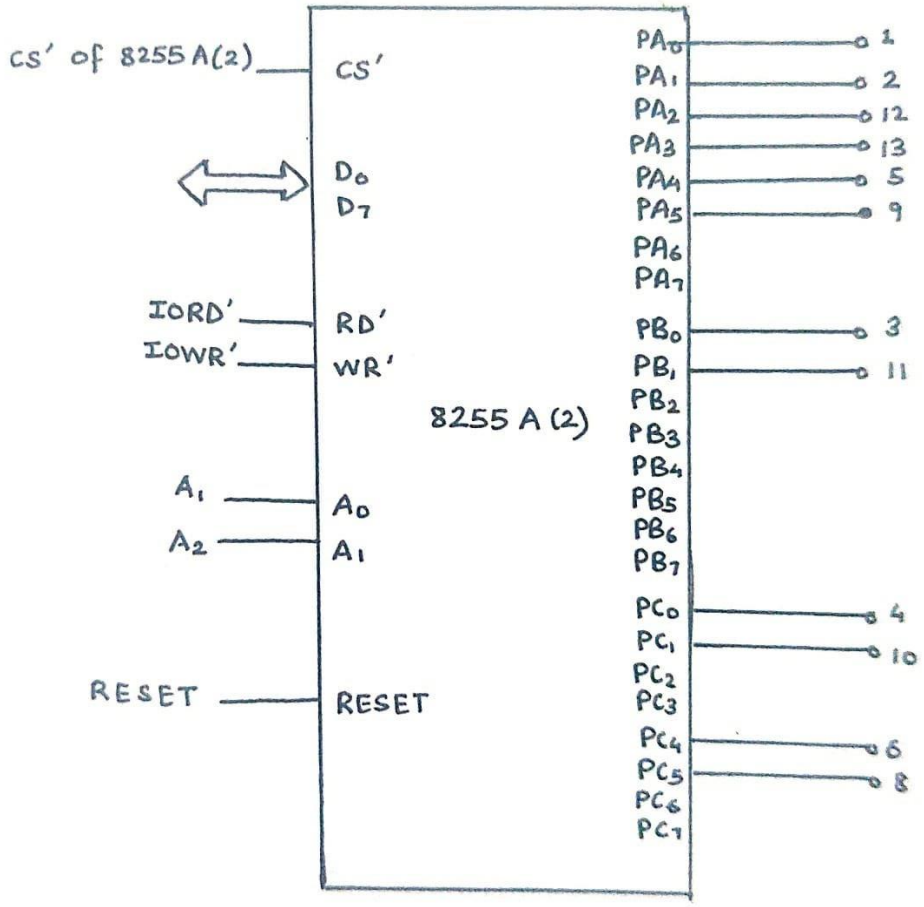


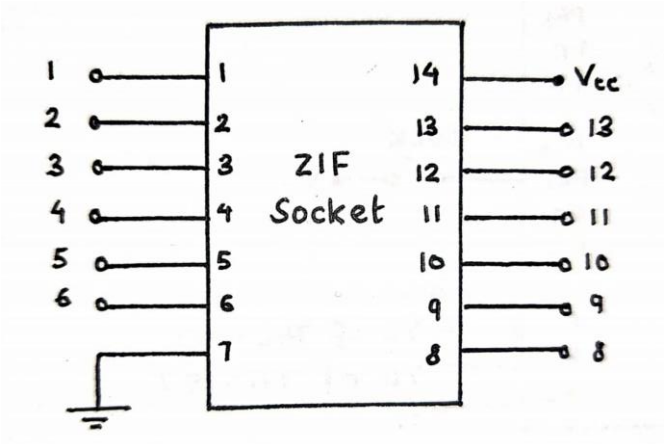


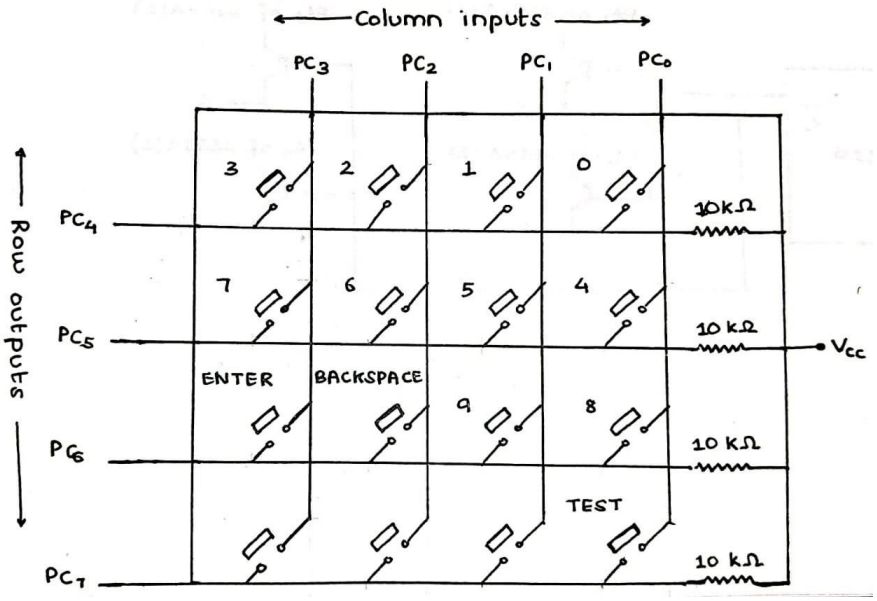
I/O Interfacing Diagrams






CS' of 8255 A(2)
CS'
D0
D7
IORD'
RD'
IOWR'
WR'
8255 A (2)
A1
A0
A2
A1
RESET
RESET
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
1
2
12
13
5
9
3
11
4
10
6
8

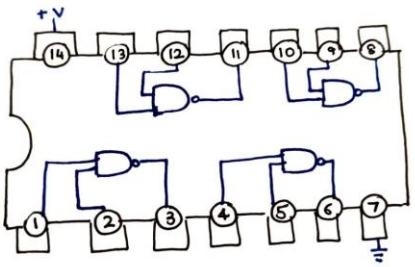

1
2
3
4
5
6
1
2
3
4
5
6
7
ZIF
Socket
14
13
12
11
10
9
8
Vcc
13
12
11
10
9
8



IC's Used

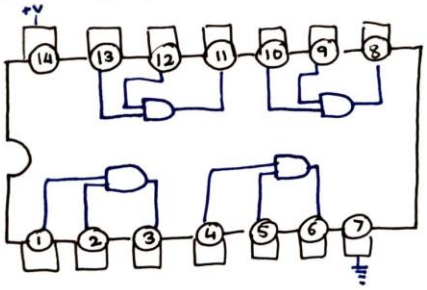
IC-7400

2 input NAND Gate IC



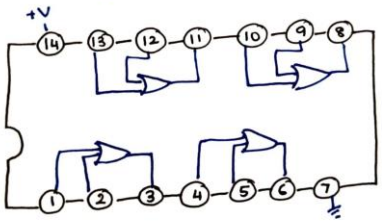
IC-7408

2 input AND gates



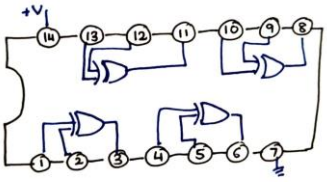
IC 7432

2 input OR gates



IC 7486

2 input XOR gates



2 INPUT X NOR gates