RISC-V based computers in the data center

Bachelor Defence

Simon Vinding Brodersen, 20-06-2024

KØBENHAVNS UNIVERSITET

Context

- Data centers play an ever increasing role in the IT sector.
- SSDs replaced previous hard drives with similar interfaces.
- Move from interfaces to open-channel SSD.
- Heavy reliance on the CPU and the general purpose OS.

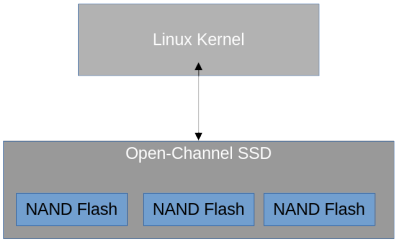

Figure: Open-channel SSD

Problem and Approach

- What computation should be handled by a storage device?
- Is it feasible to implement such a computation on a bare metal RISC-V processor.
- Implemented following the RISC-V instruction set architecture.
- implemented on the QEMU virtual machine.

Figure: QEMU virtual machine. Created using Microsoft Designer

Background

Accelerator-based Computer Architecture

- Off-loading the CPU.
- Optimized for distinct objectives, instead of General Purpose.
- Prominent example is the Graphical Processing Unit(GPU).

RISC-V

- Reduced Instruction set Computing(RISC), version 5 (V).
- Open source, minimize intellectual property, reduce barrier of entry.
- Provides RV32I, RV64I and RV128I.

Figure: RISC-V logo
By ™/®RISC-V Foundation - Vectorised by Vulphere from https://riscv.org/wp-content/uploads/2017/05/Tue1100-RISC-V-Foundation-Update.pdf, Public Domain, https://commons.wikimedia.org/w/index.php?curid=69489388

Background

QEMU

- Able to emulate both a 32-bit and 64-bit RISC-V processor.
- Made it possible to develop a binary file targeting RISC-V working on another ISA.

LLVM

- A collection of reusable compiler and toolchain technologies.
- LLVM allows for the use of an LSP.
- Includes a cross-compiler capable of targeting RISC-V, but without newlib.

Figure: LLVM-logo https://www.llvm.org/Logo.html

Design