AN1890

Simple SRAM Buffering for Large LED Arrays

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INTRODUCTION

The Configurable Logic Cell (CLC) in the PIC16F1509 microcontroller allows multiple peripherals to be connected together in unique and flexible ways, enabling the creation of custom peripherals that would otherwise be very difficult or would require external logic.

While this application note was written specifically for PIC16F1509, nearly any device with at least two CLC modules will work as well. At the time of this writing, this includes the following PIC® microcontrollers:

- PIC16F1508
- PIC16F1509
- PIC16F1615
- PIC16F1619
- PIC16F1704
- PIC16F1705
- PIC16F1708
- PIC16F1709
- PIC16F1713
- PIC16F1716
- PIC16F1717
- PIC16F1718
- PIC16F1719

Application notes are available which demonstrate extended resolution PWMs, Manchester decoding, glitch suppression and other combinations, without requiring external hardware or "bit-banging", which refers to toggling an I/O pin in software with (hopefully) the correct timing.

One such application note is AN1606, "*Using the Configurable Logic Cell (CLC) to Interface a PIC16F1509 and WS2811 LED Driver*" (DS00001606), which describes a method of using the Configurable Logic Cell (CLC) to create a custom interface to a series of WS2811/WS2812 LEDs. These LEDs are well-known in LED video display systems and in strip lights with individually addressable LEDs. Each LED allows for 256 levels of brightness on each of the RGB colors, which requires 24 bits, or three bytes of information for each LED in the string. Individual LEDs are connected serially in a daisy chain format, allowing a single I/O pin to address several, dozens or even hundreds of LEDs.

Because of the strict timing requirements of the serial protocol used by WS2811/WS2812, there is very little time between bytes to compute color information for subsequent LEDs in the string. Once the transmission of data to the LED strings has begun, any gaps in the data will cause the data to be latched into whatever LEDs the data is passing through at that time, resulting in incorrectly displayed information. The usual alternative is to buffer the contents of the LED array in RAM and shift it out in one continuous stream.

For smaller microcontrollers driving larger arrays of LEDs, this buffering of data can rapidly consume all available RAM. This application note describes a method of using the CLC to connect an external serial SRAM as a display buffer, which allows large LED arrays to be driven by smaller microcontrollers.

CUSTOM PERIPHERAL

AN1606 describes the creation of a custom peripheral which uses the CLC to combine the MSSP and a PWM to create the necessary serial protocol for WS2811-WS2812. Please refer to AN1606, for a complete description of this method. AN1606 describes the use of the Low-Speed mode of the WS2811, while what is described in this application note will use the High-Speed mode of WS2811, which is also compatible with WS2812.

A SIMPLE SRAM BUFFER

The CLC configuration described in AN1606 allows WS2811/WS2812 to be driven by simply writing bytes to the SPI port in software. Since the CLC and its combination of peripherals take care of all the protocol timing, the only thing that the software needs to do is keep writing the SPI port until the entire LED array has been updated. The 23LC512 Serial SRAM is connected to the same SPI port and can be used as a display buffer. Since WS2811/WS2812 is a "write only" device, it is possible to read the SRAM and write the LED display simultaneously on the SPI port.

The SPI port on PIC16F1509 implements two Shift registers which exist at the same address, one for transmitting and one for receiving. Writes to the SSP1BUF register will transmit the byte just written and will shift in a byte from the external peripheral at the same time, which then becomes available by reading the SSP1BUF register. By having both the SRAM and the LEDs connected to the SPI port, the software simply needs to read the SSP1BUF register and write the data to the same register to re-transmit it to the LED array. It does this repeatedly until the entire LED array has been updated. The only thing to remember is that a dummy byte has to be written before the display is enabled to allow the first byte from the SRAM buffer to arrive in the SSP1BUF register.

Dealing with potential conflicts between the LEDs and the SRAM being connected to the same SPI port is simply a matter of enabling and disabling the appropriate peripherals. When the SRAM is being written, the output to the LEDs is disabled by reconfiguring the CLC to disable its output. When sending buffered data to the LEDs from the SRAM, the LED output is disabled while the appropriate command byte and address are transmitted to the SRAM. After a dummy byte is transmitted to begin the whole process, the LED output is enabled and software just executes a tight loop, copying the SSP1BUF register to itself whenever an SPI transaction completes. If the software needs to write non-buffered data to the array, such as when writing all zeros (clearing the array), it will not activate the Chip Select to the SRAM.

Depending on how often the LED array needs to be updated, the number of LEDs driven can be arbitrarily large, as the LED array size is limited only by the update rate and the size of the external SRAM. The display buffer can be changed when the display is not being updated, which allows time to do more complex computations, table look-ups and whatever else is needed to build the displayed image.

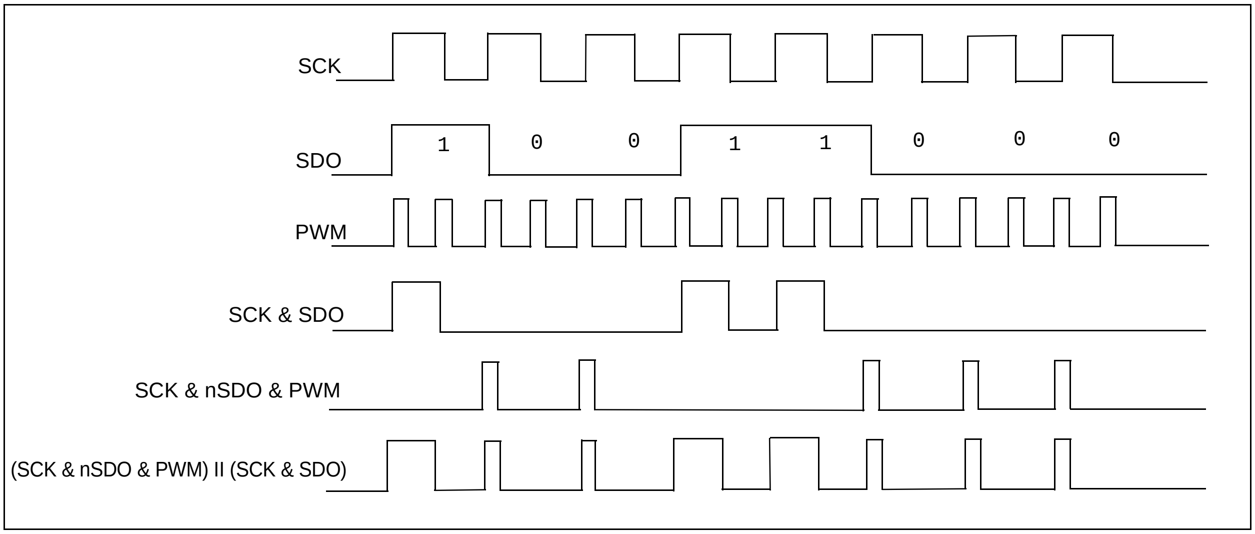
Having a buffered image in SRAM also allows displayed patterns or images to move by simply using a different starting address in SRAM when updating the LED array. Each iteration of the display update uses a slightly different address offset which will cause the entire displayed image to move.

WS2812 PROTOCOL

The WS2812 serial protocol is PWM-based, with one PWM period being one bit time, and the duty cycle during that period indicating a logic one or a logic zero. The WS2812 PWM period is 1.25 µs (±600 ns). A logic zero is represented by a high time of 350 ns and a low time of 800 ns, while a logic one is represented by a high time of 700 ns and a low time of 600 ns. All these times are ±150 ns. In addition to these two logic states, a third state is defined: a low time greater than 50 µs represents a Reset, and the WS2812 will latch the current data to its LED drivers when this state is detected. Testing has demonstrated that actual Reset times hover around 6 µs, so there is very little time for processing between transmitted bytes.

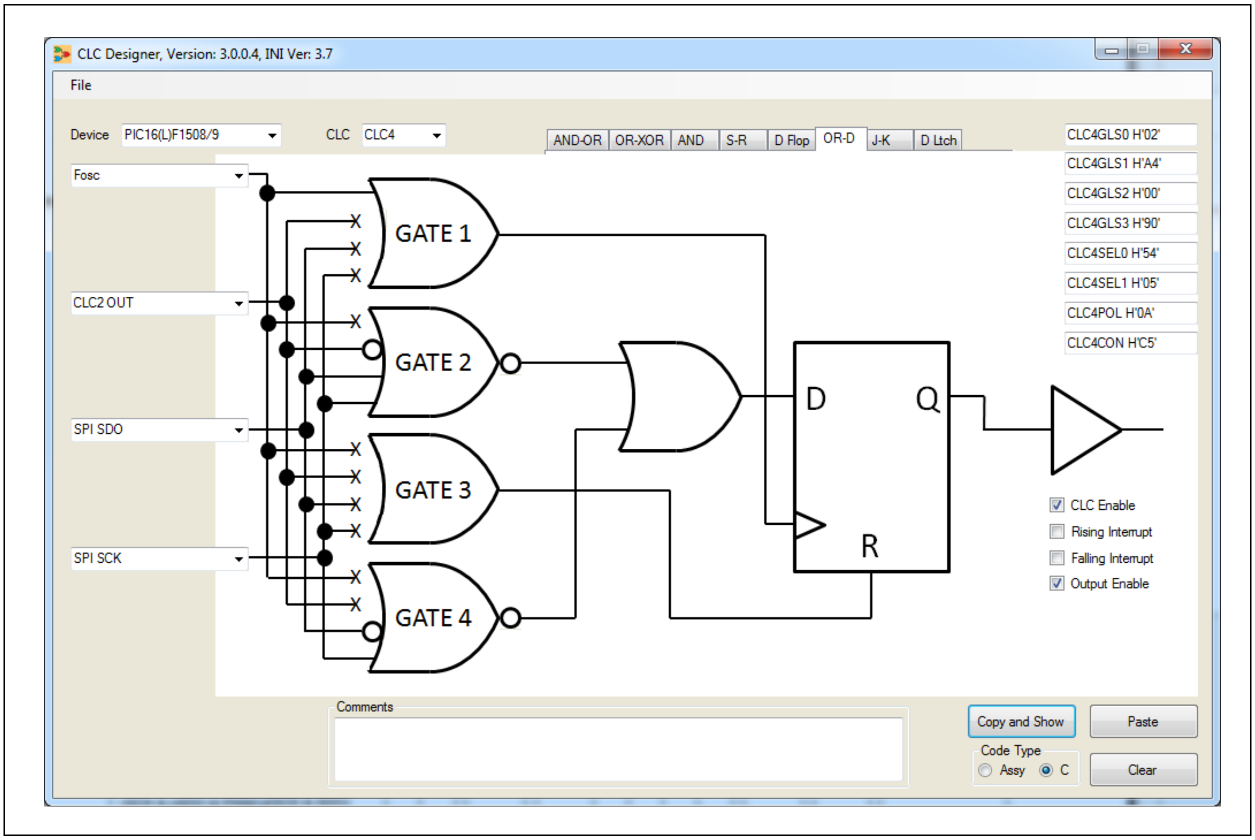
AN1606 describes the SPI signals SCK and SDO ANDed together to generate the logic '1' portion of the LED data, and using a PWM to generate the logic '0' portion of the LED data, and ORing these two together for the desired waveform (see Figure 1).

FIGURE 1: FINAL WAVEFORMS



The CLC Designer tool (www.microchip.com/clc) can be used to convert this to the code for the PIC16F1509 microcontroller. For this application, CLC4 was used because of its access to the SPI signals. CLC4 can be set up as shown in Figure 2 below.

FIGURE 2: CLC4 SETUP USING CLC DESIGNER



The OR-D configuration was chosen to allow the signals to be resynchronized to the FOSC clock. Although it would probably work without it, this results in more predictable timing at the output. This configuration is displayed as OR-OR, so a little bit of logic conversion is needed to make the original logic equation fit (see Equation 1).

EQUATION 1: ORIGINAL LOGIC FROM AN1606

$$(SCK \ \& \ nSDO \ \& \ PWM) || (SCK \ \& \ SDO)$$

By applying DeMorgan's Theorem, the original equation can be converted to fit the above configuration as seen in Equation 2.

EQUATION 2: APPLICATION OF DEMORGAN'S THEOREM

$$n(nSCK \ || \ SDO \ || \ nPWM) \ || \ n(nSCK \ || \ nSDO)$$

This handily fits into gates two and four of CLC4.

Note that CLC2OUT is used for PWM1, since PWM1 is not available at this logic cell. PWM1 is simply routed through another logic cell (CLC2).

When connecting the 23LC512 Serial SRAM, the SRAM needs to be driven by an inverted SPI clock. This is taken into account by one more modification of the Equation 2, which re-inverts the SPI clock, since it needs to be non-inverted in this logic cell. The final equation will look as shown in Equation 3.

EQUATION 3: FINAL LOGIC FOR CLC4

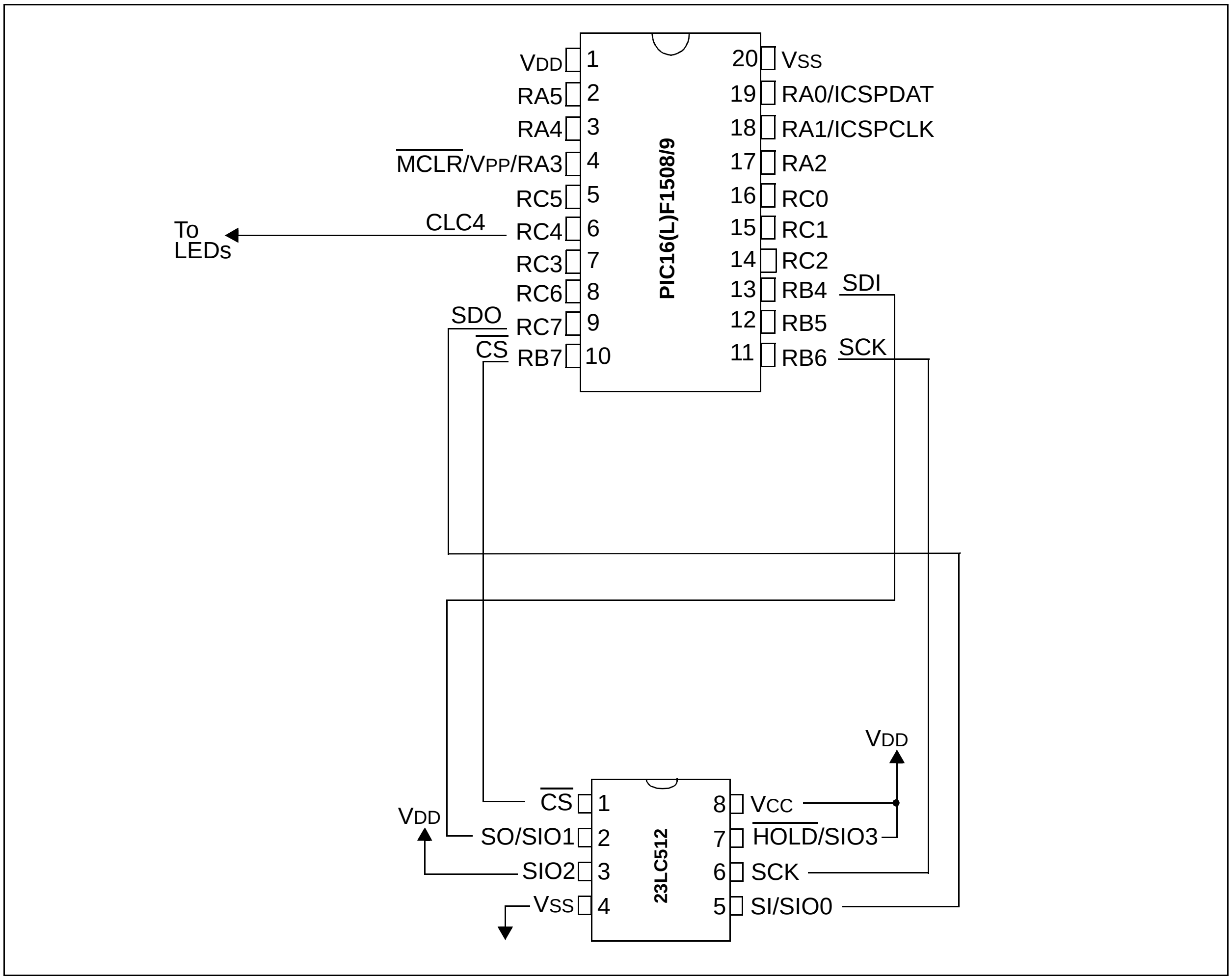
$$n(SCK \ || \ SDO \ || \ nPWM) \ || \ n(SCK \ || \ nSDO)$$

This equation is illustrated in the CLC Designer in Figure 2.

IMPLEMENTATION

The connections for a PIC16F1509 are shown in Figure 3 below.

FIGURE 3: SRAM AND LED CONNECTIONS TO THE PIC16F1509



The accompanying source code sets the microcontroller to run at 16 MHz, and all the timing is based on this clock rate.

Timer2 is used as a clock source for the SPI port and also as a timebase for PWM1. If a bit time of 1.25 µs and a 16 MHz internal oscillator are used, then Timer2 should be set up as shown in Example 1 below.

EXAMPLE 1: TIMER2 SETUP

```
T2CON = 0x04
PR2   = (bit time/2) * (Fosc/4) + 1
```

Plugging in a bit time of 1.25 µs yields a PR2 value of 2.25. Truncating this to two and using it results in an actual bit time of 1.5 µs, which is well within the ±600 ns specification for WS2811/WS2812. Therefore, the obtained value is the one displayed in Example 2.

EXAMPLE 2: PR2 REGISTER VALUE

```
PR2 = 2
```

The PWM duty cycle must be configured for the logic zero-pulse width. This width is specified at 350 ns, so the closest match in terms of 16 MHz clock periods will be chosen. Six clock periods figure out to 375 ns (which is within the specified ±150 ns), so the logic zero-pulse width needs to be six FOSC cycles wide. The Period register for PWM1 is actually composed of two registers: the High 8-bit register and the Low 2-bit register. The two bits are at the Most Significant end of the PWM1DCL register, so these two registers become as per Example 3.

EXAMPLE 3: PWM1 SETUP

```
PWM1DCH = 1
PWM1DCL = 0x80
```

Configuring the SPI port to use Timer2 Period/2 as the clock and outputting an inverted clock will yield the result indicated in Example 4.

EXAMPLE 4: SPI CONTROL REGISTER SETUP

```
SSP1CON1 = 0x33
```

All these are set up in an initialization function in the source code. The source code writes a pattern to the serial SRAM, then sends this pattern to the LEDs periodically, offsetting the SRAM address by three bytes each time, thus causing the pattern to move across a string of LEDs. This demo code was written to drive a string of 60 WS2812 LEDs, but it can be easily modified to drive nearly any number of LEDs, limited only by update rate and available SRAM. The AN1890 source code can be downloaded from the Microchip web site at www.microchip.com/applicationnotes.

CONCLUSION

The CLC enables features that would normally be difficult to do. With just a few lines of code and an external serial SRAM, a small microcontroller like the PIC16F1509 can easily drive an arbitrarily large array of WS2811/WS2812 LEDs with complex patterns. The source code is written entirely in C and is not timing critical, other than keeping the SPI port serviced. This method can be easily modified to fit other microcontrollers containing the CLC peripheral, and the serial SRAM could also be replaced with a serial EEPROM for nonvolatile LED images.

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ISBN: 978-1-63277-124-7

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