Elmore Model for Energy Estimation in RC Trees

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Abstract

This paper presents analysis methods for energy estimation in RC trees driven by time-varying voltage sources, e.g., buffers, time-varying power supplies, and resonant clock generators. An Elmore energy model that is the computational analog of the conventional Elmore delay model for RC trees is described. Simulation results indicate that the error in energy estimation is less than 2.5% in the worst-case in comparison to HSPICE simulations, with over a 1000X speed-up.

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General Terms: Algorithms
Keywords: Energy estimation, RC trees, interconnect.

1. Introduction

Basic extrapolations from the International Technology Roadmap for Semiconductors (ITRS) [9] indicate that continued scaling will make interconnect the primary show-stopper to increased performance, power, and reliability in integrated circuits [7, 8]. These concerns will be further exacerbated by rising substrate temperature as power densities in the sub-100 nm regime approach 100 W/cm^2 and non-uniform thermal gradients along the substrate impact interconnect performance and reliability significantly. Specifically, there is literature on modeling and analysis to evaluate the impact of thermal gradients on interconnect (1) delay, which increases by approximately 5% for each 20^{o}C increase in temperature [3], (2) clock skew, both in normal and test modes of operation [6], and (3) electromigration effects [1, 5]. As the number of interconnect levels increase, line widths shrink, and low-k materials with poor conductivity are used to reduce noise and delay, self-heating (Joule-heating) energy dissipation along the interconnect also impacts its performance and reliability [5].

Conventional techniques for interconnect energy estimation have mostly improved on the well known $1/2CV_{\rm DD}^2$ model that estimates total energy dissipated by the source and the interconnect [11, 16, 17]. A significant shortcoming of these models is that they estimate energy consumption on individual interconnects without providing effective spatial information about this energy consumption. In this paper, it is shown that the conventional $1/2CV_{\rm DD}^2$ model for energy analysis is inaccurate, and that it does not account for source delay in estimating the distribution of energy between the source and the interconnect. The experiments and supporting analysis show that as sources switch faster, the interconnect consumes more energy and this can impact interconnect self-heating.

This paper presents analysis methods for energy estimation in RC trees driven by time-varying voltage sources, e.g., buffers, time-varying power supplies, and resonant clock generators. An Elmore energy model that is the computational analog of the conventional Elmore delay model for RC trees is described. Energy estimation is performed using a recursive graph traversal method that is analogous to delay computation by the Elmore method. The proposed models are computationally more efficient than the model-order reduction techniques proposed in [15] and more general and accurate than the technique for RC ladders proposed in [2]. Simulation results from 1,000 runs on RC trees with 10,000 elements indicate that the error in total energy estimation is less than 2.5% in the worst-case in comparison to the results obtained from HSPICE simulations, with over a 1000X speed-up. Closed-form bounds for energy estimation in interconnects are also derived. The error in interconnect energy estimation using the weighted average of the upper and lower bounds is 2.0% on the average, and 3.5% in the worst-case across 10,000 simulation runs. Note that the effect of inductance on energy dissipation is not considered in this paper.

The models derived in this paper also provide a generalized approach for the analysis of adiabatic charging [4, 14]. Adiabatic charging suggests that it is possible to reduce energy dissipation to an arbitrary degree by increasing the switching time of the power supply. In such designs, the saved energy from the capacitive load is recovered by the time-varying power supply. By modeling the clocked power supply in adiabatic logic as a voltage source with time constant τ and the load circuit by RC trees, closed-form expressions for exploring the tradeoff between energy and delay in adiabatic design are derived in this paper.

The rest of this paper is organized as follows. Section 2 describes relevant work and motivates the dependence between delay and energy. Section 3 presents the general energy model for energy estimation in resistors in RC trees. Section 4 presents an application of this model to interconnect energy estimation. Section 5 presents simulation results and comparisons to prior work. Section 6 is a conclusion.

2. Motivation

We begin by making the observation that the power dissipated as self-heating by the interconnect depends on the relative delay between the driver and the interconnect. Consider an inverter driv-

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ing a 2 mm long interconnect modeled by 10 equal RC segments in three process technologies: 130nm, 100nm, and 65nm. The load is modeled by two inverters that scale in size with the driver. Note that the interconnect also scales with the technology node. By varying the size (and hence, the delay) of the driving inverter, the relative power consumption between the driver and the interconnect is measured and plotted in Fig. 1.

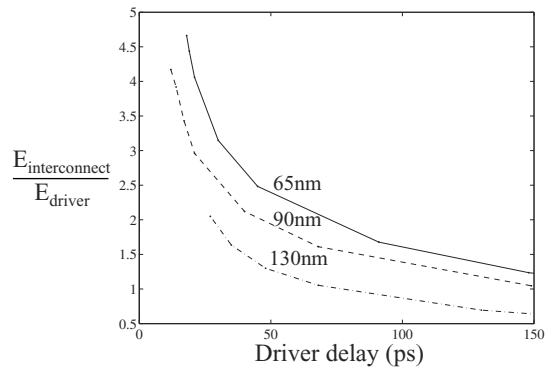

Figure 1: This figure presents the ratio of energy consumed in the interconnect to the energy consumed in the driver for three process technologies. It is clear that as drivers get faster, and as process technology shrinks, interconnect becomes the dominant consumer of energy. The theoretical explanation that relates driver delay to interconnect energy is provided in Sec. 2.1

The power distribution between the driver and the interconnect is highly dependent on the driver delay as shown in Fig. 1. From the plot, it is clear that a larger fraction of the total energy is delivered to the interconnect (and dissipated as heat) as the driver switches faster. Interconnect resistance per unit length is predicted to increase from $100\,\Omega/\text{mm}$ currently to more than $1000\,\Omega/\text{mm}$ at the 45 nm technology node [10], further skewing this proportion. Hence, traditional power models have to be augmented with source and interconnect delay terms to estimate energy and self-heating effects accurately.

2.1 Delay-dependent energy model

Consider a voltage source $v(t)$ driving a linear circuit. The total energy E_{total} delivered by $v(t)$ to the circuit is $\int_0^\infty v(t)i(t)\text{d}t$. Without loss of generality, let $v(t)$ be given by the sum of exponential terms $V_{\text{DD}}\left(1+\sum_{i=1}^{q} r_i e^{-p_i t}\right)$. $v(t)$ in the Laplace domain is given by $V(s) = V_{\text{DD}}\left(1/s + \sum_{i=1}^{q} r_i/(s+p_i)\right)$. For a circuit with zero initial states, the total energy E_{total} delivered by the source when a $0 \rightarrow 1$ transition occurs is

$$\begin{aligned} E_{\text{total}} &= \int_0^\infty v(t)i(t)\text{d}t \\ &= V_{\text{DD}} \int_0^\infty i(t)\text{d}t + V_{\text{DD}} \sum\nolimits_{i=1}^{q} \int_0^\infty r_i i(t) e^{-p_i t}\text{d}t \\ &= V_{\text{DD}} \cdot CV_{\text{DD}} + V_{\text{DD}} \sum\nolimits_{i=1}^{q} r_i\ I(s)|_{s=p_i} \end{aligned}$$

where $\int_0^\infty i(t)\text{d}t = CV_{\text{DD}}$ is the total charge stored in all the capacitances, $I(s)$ is the Laplace transform of the current $i(t)$, and $I(s)|_{s=p_i}$ is the driving point current generated by $V(s)|_{s=p_i}$. Since capacitances are lossless elements and do not dissipate energy, $1/2CV_{\text{DD}}^2$ is the energy stored in the capacitances on a transition from $0 \rightarrow V_{\text{DD}}$. Consider a simple RC circuit driven by the voltage source $v(t)$. The self-heating energy E_{cct} dissipated in the circuit on a $0 \rightarrow V_{\text{DD}}$ transition is then given by

$$E_{\text{cct}} = E_{\text{total}} - 1/2CV_{\text{DD}}^2 = 1/2CV_{\text{DD}}^2 + \sum_{i=1}^{q} r_i\ I(s)|_{s=p_i} V_{\text{DD}}$$

Thus, the classical expression for E_{cct} given by $1/2CV_{\text{DD}}^2$ corresponds to the self-heating that occurs when an ideal step input (which has no exponential terms) initiates a $0 \rightarrow V_{\text{DD}}$ transition.

Consider the case when a non-ideal source with a finite rise delay τ given by $v(t) = (1-e^{-t/\tau})V_{\text{DD}}$ is used to charge the same RC circuit. E_{cct} is given by

$$\begin{aligned} E_{\text{cct}} &= CV_{\text{DD}}^2 - V_{\text{DD}}\ I(s)|_{s=1/\tau} - 1/2CV_{\text{DD}}^2 \\ &= \left(C - 1/2C\frac{1}{1+RC/\tau} - 1/2C\right) V_{\text{DD}}^2 \\ &= \frac{RC}{\tau+RC} \cdot 1/2CV_{\text{DD}}^2 \\ &\equiv \gamma \cdot 1/2CV_{\text{DD}}^2 \end{aligned} \tag{1}$$

The scale factor $\gamma = \frac{RC}{\tau+RC}$ accounts for the effect of a non-ideal source with finite rise delay on interconnect energy consumption.

If the RC circuit represents a single-stage lumped model for interconnect, γ is the ratio of the Elmore delay of the interconnect to the total delay that includes the delay of the source and the Elmore delay of the interconnect. Thus, less energy is dissipated in the interconnect as the source switches slower, motivated for three process technologies in Fig. 1.

It is also possible to interpret γ through the principle of adiabatic charging [4, 14]. If the power supply were an exponential source with time constant τ, the ratio $\frac{RC}{\tau+RC}$ suggests that it is possible to reduce energy dissipation to an arbitrary degree by increasing the switching time τ of the power supply – this is at the core of all design based on adiabatic charging. In contrast to a buffer as the source driving the interconnect with a constant power supply, the saved energy $(1-\gamma)1/2CV_{\text{DD}}^2$ is recovered by the time-varying power supply.

In the following sections, we generalize and extend the $\gamma \cdot \frac{1}{2}CV_{\text{DD}}^2$ form to RC trees.

3. Energy estimation in resistive elements

Consider a RC tree excited by an exponential input source. The segments are numbered 1 through n, with segment 1 being closest to the source. The approach to energy estimation in RC trees is an extension of the method described in Sec. 2.1 in three steps:

1. A second-order (2-pole) model for the current $\tilde{I}_i(t)$ through each resistor R_i in the RC tree (Sec. 3.1),
2. Estimation of the energy dissipated as self-heat in each resistor R_i using the appropriate form of the classical $\tilde{I}_i^2(t)R_i$ model (Sec. 3.2), and
3. A summation over all the resistors to obtain the total energy dissipated in the RC tree (Sec. 4).

3.1 Second-order current model $\tilde{I}_i(t)$

The Laplace transform of the current $I_i(t)$ through the i^{th} resistor R_i in the tree is given by

$$I_i(s) = \sum\nolimits_{k \in D(i)} sC_k V_k, \tag{2}$$

where $D(i)$ denotes all nodes downstream of node i, C_k is the capacitance at node k, and V_k is the voltage at node k. For a simple interconnect with n segments and no branching, $D(i)$ would just be the nodes i through n. For an exponential input, $V_k(s)$ can be

expanded into the following series that is consistent with the final value theorem:

$$V_k(s) = V_{\rm DD}\left(s^{-1} - m_0^k + m_1^k s + m_2^k s^2 \cdots\right). \quad (3)$$

Note that if an exponential input is applied, the voltage response $V_k(t)$ at the $k^{\rm th}$ node will converge to $V_{\rm DD}$ since $V_k(n \rightarrow \infty)$ equals $\lim_{s\rightarrow 0} sV_k(s) = V_{\rm DD}$. Substituting the series expansion for $V_k(s)$ into Eqn. (2) yields:

$$I_i(s) = \sum\nolimits_{k\in D(i)} C_k V_{\rm DD}(1 - m_0^k s + m_1^k s^2 + m_2^k s^3 \cdots).$$

If the first two moments are retained, and the rest discarded, we obtain the following truncated approximation $\tilde{I}_i(s)$ for $I_i(s)$:

$$\tilde{I}_i(s) = \sum\nolimits_{k\in D(i)} C_k V_{\rm DD}(1 - m_0^k s + m_1^k s^2).$$

The summation is completed and the terms are rearranged to obtain

$$\tilde{I}_i(s) = \hat{C}_i V_{\rm DD}(1 - b_1^i s + b_2^i s^2) \quad (4)$$

where $\hat{C}_i = \sum_{k\in D(i)} C_k$ denotes the total capacitance downstream of node i,

$$b_1^i = \frac{\sum_{k\in D(i)} C_k m_0^k}{\sum_{k\in D(i)} C_k}, \text{ and } b_2^i = \frac{\sum_{k\in D(i)} C_k m_1^k}{\sum_{k\in D(i)} C_k}.$$

Whereas the above form is convenient for moment matching, it is unsuitable when a time domain expression is desired through the inverse Laplace transform. The following equivalent form for Eqn. (4) is convenient to obtain a time domain expression for $\tilde{I}_i(t)$:

$$\left(\tilde{I}_i(s) \approx \frac{\hat{C}_i V_{\rm DD}}{1 + b_1^i s + ((b_1^i)^2 - b_2^i)s^2}\right) \equiv \frac{\hat{C}_i V_{\rm DD}}{1 + \frac{p_1+p_2}{p_1 p_2}s + \frac{1}{p_1 p_2}s^2}$$

where $\frac{p_1+p_2}{p_1 p_2} = b_1^i$. A similar closed-form expression for b_2^i can be derived, but it is omitted here since it is not necessary for energy estimation. This form for $\tilde{I}_i(s)$ is highly advantageous since for simple roots, the time domain expression for the current $\tilde{I}_i(t)$ through the $i^{\rm th}$ resistive element in the RC tree is given by the following double-exponential function:

$$\tilde{I}_i(t) = \hat{C}_i V_{\rm DD} \frac{p_1 p_2}{p_2 - p_1}(\mathrm{e}^{-p_1 t} - e^{-p_2 t}). \quad (5)$$

This double-exponential, 2-pole approximation for the current is justified by the fact that the current in RC trees is a smooth function without discontinuities. The corresponding double-exponential function $\tilde{I}_i(t)$ for $I_i(t)$ matches the waveform well in RC trees and has been verified by HSPICE simulations.

3.2 Resistor energy

In the previous section, a double-exponential model for the current through the $i^{\rm th}$ resistor was obtained. The instantaneous power in the resistor is given by the classical I^2R model, and hence energy is obtained by an integration of this expression over the time interval $[0, \infty)$. The energy delivered to and dissipated as self-heat within resistor R_i is given by

$$\begin{aligned} E^i_{\rm tree} &= \int_0^\infty I_i^2(t) R_i \mathrm{d}t \approx \int_0^\infty \tilde{I}_i^2(t) R_i \mathrm{d}t \\ &= \hat{C}_i^2 V_{\rm DD}^2 \frac{p_1 p_2}{2(p_1+p_2)} R_i = \frac{R_i \hat{C}_i}{b_1^i} \cdot \frac{\hat{C}_i}{2} V_{\rm DD}^2 \\ &\equiv \gamma_i \cdot 1/2 \hat{C}_i V_{\rm DD}^2. \end{aligned}$$

Note that the expression $E^i_{\rm tree}$ for energy is independent of the coefficient b_2^i. The scaling coefficient γ_i is analogous to the scaling coefficient γ presented in Eqn. (1) for the lumped RC case, and can be expressed as

$$\gamma_i = \frac{R_i \hat{C}_i}{b_1^i} = \frac{R_i \hat{C}_i}{\frac{1}{\hat{C}_i}\sum_{k\in D(i)} C_k m_0^k}. \quad (6)$$

Note that γ_i only depends on the m_0^k shown in Eqn. (3). The closed-form expression for γ_i in Eqn. (6) can be further simplified by obtaining a simple expression for m_0^k as follows.

Note that m_0^k is the first moment of the voltage of node k with an exponential voltage input. The transfer function for the voltage at node k can be expressed using a Taylor series around $s = 0$ in the form $g_k(s) = 1 - a_1^k s + a_2^k s^2 + \cdots$, where the first moment $a_1^k = \sum_{j\subset U(k)} R_j \hat{C}_j$. Here, $U(k)$ denotes all nodes upstream of node k. Note that a_1^k is equivalent to the Elmore delay as measured at the $k^{\rm th}$ node in the tree and is denoted by $\Delta^k_{\rm Elmore}$, i.e.,

$$a_1^k = \sum\nolimits_{j\subset U(k)} R_j \hat{C}_j \equiv \Delta^k_{\rm Elmore}. \quad (7)$$

When an exponential input of the form $v(s) = \frac{V_{\rm DD}}{s(1+s\tau)}$ is used, $V_k(s)$ is given by

$$V_k(s) = v(s) g_k(s) = \frac{V_{\rm DD}}{s(1+s\tau)}(1 - a_1^k s + a_2^k s^2) \quad (8)$$

The first two moments in Eqn. (3) can be derived by matching corresponding terms in Eqn. (8) to obtain:

$$m_0^k = a_1^k + \tau \text{ and } m_1^k = a_2^k + m_0^k \tau. \quad (9)$$

Only m_0^k is required to simplify the expression for the scaling coefficient γ_i in Eqn. (6):

$$\begin{aligned} \gamma_i &= \frac{R_i \hat{C}_i}{\frac{1}{\hat{C}_i}\sum_{k\in D(i)} C_k \left(\Delta^k_{\rm Elmore} + \tau\right)} \\ &= \frac{R_i \hat{C}_i}{\tau + \frac{1}{\hat{C}_i}\sum_{k\in D(i)} C_k \Delta^k_{\rm Elmore}} \end{aligned} \quad (10)$$

Note that the term $\frac{1}{\hat{C}_i}\sum_{k\in D(i)} C_k \Delta^k_{\rm Elmore}$ is just the weighted average Elmore delay of all downstream nodes of node i, where the weight is the node capacitance C_k. Hence, we define

$$\hat{\Delta}^i_{\rm Elmore} = 1/\hat{C}_i \sum\nolimits_{k\in D(i)} C_k \Delta^k_{\rm Elmore} \quad (11)$$

The scaling coefficient γ_i for RC trees is similar in structure to γ for the lumped RC case in Eqn. (1). Note also that for n equals 1, γ_1 reduces to the expression $\frac{RC}{\tau+RC}$ that corresponds to γ for the lumped RC case. The closed-form solution to the energy dissipated at resistance R_i is then given by

$$E^i_{\rm tree} = \gamma_i \cdot 1/2 \hat{C}_i V_{\rm DD}^2 = \left(\frac{R_i \hat{C}_i}{\tau + \hat{\Delta}^i_{\rm Elmore}}\right) 1/2 \hat{C}_i V_{\rm DD}^2 \quad (12)$$

This expression provides the energy distribution profile when interconnects are modeled by distributed RC trees. In the next section, we derive bounds for $\hat{\Delta}^i_{\rm Elmore}$ to obtain a closed-form expression for the total energy consumption in RC trees and interconnect.

4. Energy estimation in RC trees

Based upon the analysis in the previous section, the total energy consumed over all the resistors in the RC tree is given by

$$E_{\rm tree} = \sum_{i=1}^{n} \left(\frac{R_i \hat{C}_i}{\tau + \hat{\Delta}^i_{\rm Elmore}}\right) \frac{1}{2} \hat{C}_i V_{\rm DD}^2 \quad (13)$$

The computational cost of Eqn. (13) includes three traversals of the RC tree: one post-order traversal to compute $\hat{C}_i$ for each node, one pre-order traversal to compute Δ^k_{Elmore}, and one post-order traversal to compute E^i_{tree}. Note that these traversals need to be performed just once (analogous to the Elmore model for delay) across multiple runs. Thus, energy estimation using this closed-form expression has $O(n)$ runtime complexity, where n is the number of resistors in the RC tree. We analyze two cases based on this model. First, we consider the case when an interconnect line is assumed to drive no capacitive load. In Sec. 4.2, we extend this to the case when there is a capacitive load.

4.1 Interconnect without capacitive load

Consider an interconnect line composed of n RC segments whose resistance and capacitance per segment are R_{I}/n and C_{I}/n respectively. Let E^i_{int} be the energy dissipated by the i^{th} resistor and E_{int} the total energy dissipated by the interconnect line. Summing over the terms in Eqn. (11), the closed-form expression for $\hat{\Delta}^i_{\text{Elmore}}$ is given by

$$\hat{\Delta}^i_{\text{Elmore}} = R_{\text{I}}C_{\text{I}}\frac{(2n+1)(n+i)-i(i-1)}{6n^2}.$$

In order to obtain bounds for $\hat{\Delta}^i_{\text{Elmore}}$, its first derivative w.r.t. index i is given by

$$\frac{\partial\,\hat{\Delta}^i_{\text{Elmore}}}{\partial\, i} = \frac{n-i+1}{3n^2} > 0 \quad \text{for} \quad 1 \le i \le n.$$

Since $\hat{\Delta}^i_{\text{Elmore}}$ is a strictly increasing function of i, $\hat{\Delta}^1_{\text{Elmore}} \le \hat{\Delta}^i_{\text{Elmore}} \le \hat{\Delta}^n_{\text{Elmore}}$. For large n, $\lim_{n\to\infty} \hat{\Delta}^i_{\text{Elmore}}$ at nodes 1 and n yield the following bounds for $\hat{\Delta}^i_{\text{Elmore}}$:

$$\left\{\hat{\Delta}^1_{\text{Elmore}} = R_{\text{I}}C_{\text{I}}/3\right\} \le \hat{\Delta}^i_{\text{Elmore}} \le \left\{\hat{\Delta}^n_{\text{Elmore}} = R_{\text{I}}C_{\text{I}}/2\right\}$$

Substituting the bounds for $\hat{\Delta}^i_{\text{Elmore}}$ into Eqn. (10) gives the following bounds for γ_i:

$$\frac{R_i\hat{C}_i}{\tau + R_{\text{I}}C_{\text{I}}/2} \le \gamma_i \le \frac{R_i\hat{C}_i}{\tau + R_{\text{I}}C_{\text{I}}/3}.$$

Substituting the bounds for γ_i in Eqn. (12), summing the E^i_{int} terms over all the RC segments, and evaluating $\lim_{n\to\infty}\sum_{i=1}^{n} E^i_{\text{int}}$ results in the following bound for E_{int}:

$$\left(\frac{R_{\text{I}}C_{\text{I}}/3}{\tau + R_{\text{I}}C_{\text{I}}/2}\right)\frac{1}{2}C_{\text{I}}V^2_{\text{DD}} \le E_{\text{int}} \le \left(\frac{R_{\text{I}}C_{\text{I}}/3}{\tau + R_{\text{I}}C_{\text{I}}/3}\right)\frac{1}{2}C_{\text{I}}V^2_{\text{DD}} \tag{14}$$

4.2 Interconnect driving a load C_{L}

The analysis from the previous section can be extended to the case when the interconnect drives a capacitive load C_{L} as follows. The closed-form expression for $\hat{\Delta}^i_{\text{Elmore}}$ is given by:

$$\begin{aligned}\hat{\Delta}^i_{\text{Elmore}} &= \tfrac{1}{\hat{C}_i}\textstyle\sum_{k\in D(i)} C_k\Delta^k_{\text{Elmore}} \\ &= \tfrac{1}{\hat{C}_i}\textstyle\sum_{k\in D(i)} C_k\left(\sum_{j\in U(k)} R_j \sum_{l\in D(j)} C_l\right)\end{aligned}$$

where $C_k, C_l = C_{\text{I}}/n$ for $1 \le i,l \le (n-1)$ and $C_k, C_l = C_{\text{I}}/n + C_{\text{L}}$ for $i,l = n$. The derivation of the closed-form expression for $\hat{\Delta}^i_{\text{Elmore}}$ is omitted here for brevity. It can be shown that the closed-form expression for $\hat{\Delta}^i_{\text{Elmore}}$ is a monotonically increasing function of i. The following bounds can be derived for $\hat{\Delta}^i_{\text{Elmore}}$:

$$\begin{array}{ccccc}\hat{\Delta}^1_{\text{Elmore}} & \le & \hat{\Delta}^i_{\text{Elmore}} & \le & \hat{\Delta}^n_{\text{Elmore}}, \text{ i.e.,} \\ \frac{R_{\text{I}}\left(C^2_{\text{I}}/3 + C_{\text{I}}C_{\text{L}} + C^2_{\text{L}}\right)}{C_{\text{I}}+C_{\text{L}}} & \le & \hat{\Delta}^i_{\text{Elmore}} & \le & R_{\text{I}}\left(C_{\text{I}}/2 + C_{\text{L}}\right)\end{array}$$

In a manner similar to the previous section, the following bounds can be derived for E_{int}:

$$\begin{aligned}1/2\frac{C^2_{\text{I}}/3 + C_{\text{I}}C_{\text{L}} + C^2_{\text{L}}}{\tau + \hat{\Delta}^n_{\text{Elmore}}}R_{\text{I}}V^2_{\text{DD}} \le E_{\text{int}} \le \\ 1/2\frac{C^2_{\text{I}}/3 + C_{\text{I}}C_{\text{L}} + C^2_{\text{L}}}{\tau + \hat{\Delta}^1_{\text{Elmore}}}R_{\text{I}}V^2_{\text{DD}}\end{aligned} \tag{15}$$

In Sec. 5, we present validation results that use a weighted sum of the lower and upper bounds on E_{int} to estimate the energy consumption in the interconnect with high accuracy.

4.3 Source versus interconnect energy

In order to relate the bounds for E_{int} in Eqn. (15) to the graphs presented in Fig. 1, consider $\lim_{\tau\to 0} E_{\text{int}}$. In Fig. 1, this corresponds to moving from the right to the left along the x-axis, since τ equals zero in the limiting case at the origin. $\lim_{\tau\to 0} E_{\text{int}}$ is given by the following general expression:

$$\begin{aligned}1/2\left(2/3(C_{\text{I}}+C_{\text{L}}) + \frac{1/3C^2_{\text{L}}}{C_{\text{I}}/2 + C_{\text{L}}}\right)V^2_{\text{DD}} \le \\ \lim_{\tau\to 0} E_{\text{int}} \le 1/2(C_{\text{I}}+C_{\text{L}})V^2_{\text{DD}}\end{aligned} \tag{16}$$

(i) For example, if the stage at the end of the interconnect is small, it has negligible input capacitance, i.e., $C_{\text{L}} \ll C_{\text{I}}$. The bounds for $\lim_{\tau\to 0} E_{\text{int}}$ simplify to the following:

$$0.67\left(1/2C_{\text{I}}V^2_{\text{DD}}\right) \le \lim_{\tau\to 0} E_{\text{int}} \le 1/2C_{\text{I}}V^2_{\text{DD}}.$$

Note that for $C_{\text{L}} \ll C_{\text{I}}$, the above bounds can be independently derived from Eqn. (14).
(ii) Similarly, if $C_{\text{I}} \approx C_{\text{L}}$, the bounds for $\lim_{\tau\to 0} E_{\text{int}}$ in Eqn. (15) simplify to the following:

$$0.78\left(1/2(C_{\text{I}}+C_{\text{L}})V^2_{\text{DD}}\right) \le \lim_{\tau\to 0} E_{\text{int}} \le 1/2(C_{\text{I}}+C_{\text{L}})V^2_{\text{DD}}.$$

Both bounds show that as sources are sized to drive signals faster, i.e., as $\tau\to 0$, the energy delivered and dissipated as self-heating in the interconnect approaches the classical $1/2(C_{\text{I}} + C_{\text{L}})V^2_{\text{DD}}$ term. This is in agreement with the simulation results presented in Fig. 1. Thus, buffer sizing to decrease propagation delay has the side-effect of increasing self-heating in the interconnect significantly.

5. Results

The simulation and experimental results presented here are organized into three sub-sections. The first sub-section describes the experiments that were conducted to validate the models presented in this paper. In the second sub-section, we compare the proposed method to previously proposed techniques. In the third sub-section, we discuss possible applications for the models and analysis techniques presented in this paper. The simulation framework for all the experiments was implemented in C++ and the experiments were run on a Linux workstation with an AMD Athlon XP 2600+ CPU and 2.0 GB RAM.

5.1 Model validation

Two sets of experiments were conducted as part of our validation efforts. The first set of experiments were used to verify the general expressions for energy consumption in RC trees given by Eqn. 13. We ran 1000 simulations on randomly generated RC trees with 10,000 resistors and 10,000 capacitors. Energy dissipation in each resistor was calculated using Eqn. (12). The energy consumed by the RC tree is then obtained by summation and is given by

Eqn. (13). The error in total energy estimation is less than 2.5% in the worst-case in comparison to the results obtained from HSPICE simulations. Note that although our algorithm has $O(n)$ runtime complexity with average runtime of 10ms per run, a HSPICE run on the same platform takes about 10s. This limited the total number of experimental runs to 1000.

The second set of experiments were used to verify the general expressions on the bounds for energy consumption in interconnect lines described in Sec. 4 and given by Eqn. (15). We ran 10,000 simulations on interconnect lines using randomly generated parameters such that resistance $R_{\rm I} \in [0, 2{\rm K}\Omega]$, capacitance $C_{\rm I} \in [0, 2{\rm pF}]$, load capacitance $C_{\rm L} \in [0, 1{\rm pF}]$, and source $\tau \in [0.1R_{\rm I}(C_{\rm I}+C_{\rm L}), 10R_{\rm I}(C_{\rm I}+C_{\rm L})]$. The interconnect was represented by a 50-stage distributed RC model in all the cases. Since the solution given by Eqn. (15) uses bounds, we used a weighted average of the lower and upper bounds in order to estimate total energy $E_{\rm int}$. The weighted average is obtained by assigning weights of 1/3 and 2/3 to the lower and upper bounds respectively. These heuristic weights are chosen since the upper bound is tighter than the lower bound. The error in energy estimation using the weighted average of the two bounds is 2.0% on the average, and 3.5% in the worst-case across the 10,000 simulation runs.

In Fig. 2, we present the self-heating profile for an interconnect line with 50 RC stages where $R_{\rm I}$ equals 200Ω, $C_{\rm I}$ equals 200 fF, and $C_{\rm L}$ equals 20 fF. τ was set to $0.2R_{\rm I}(C_{\rm I}+C_{\rm L})$. In Fig. 2(a), the energy consumed in each stage as a percentage of the total energy consumed by the interconnect line is presented. It is clear that the stages closer to the source (lower index) consume a significant fraction of the energy and are hence subject to more self-heating. In Fig. 2(b), the cumulative self-heating up to the $i^{\rm th}$ stage is presented. It is clear from the figure that about 50% of the self-heating occurs in the first ten stages of the interconnect closest to the source.

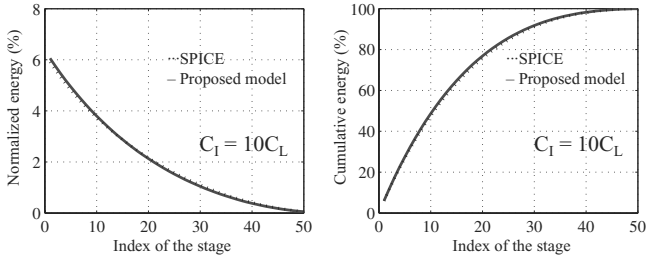

Figure 2: Plots of normalized and cumulative energy distribution for a 50-stage interconnect line

5.2 Comparison to prior work

In this sub-section, the proposed method is compared to previous methods [2, 15] to estimate the energy dissipated in RC networks. The RC tree shown in Fig. 3 is from the AWE paper [13] and it was used as the reference circuit in [15]. The time constant of the exponential voltage driver τ was chosen over the range $\{0.2R_{\rm I}C_{\rm I}, 5R_{\rm I}C_{\rm I}\}$ where $R_{\rm I}$ and $C_{\rm I}$ are the total resistance and capacitance of the tree (column 1, Table 1).

Table 1 reports the error in total energy dissipation (in %) with HSPICE as the reference for the different approaches. Since the method described in [2] only handles ladder networks, we generated a ladder network by removing resistors R_9 and R_{10} and capacitors C_9 and C_{10}. The rise time used in [2] was approximated by $\tau{\rm log}(0.9/0.1)$, where τ is the time constant of the exponential input voltage source. The error in total energy estimation for the

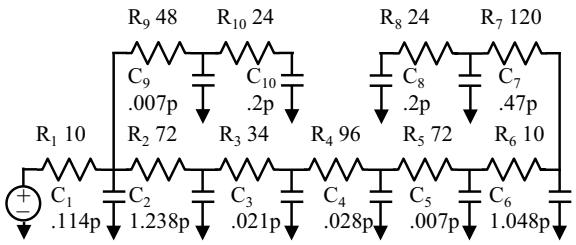

Figure 3: RC tree from [13] used for comparison to [2, 15]

ladder using the method from [2] and the proposed method are reported in columns 2 and 3, respectively. It is clear that the proposed method is significantly more accurate than [2]. Both [2] and the proposed method have closed-form solutions with linear runtime in the number of nodes. Besides lower accuracy, the other limitations of [2] are that it cannot handle RC trees and that it cannot be used to calculate the energy dissipated in each resistor in the network.

Table 1: The proposed method is compared to [2] and [15]. Errors in total energy estimation are reported in % with HSPICE as the reference.

τ	Ladder		Tree	
	[2]	Proposed	2-pole MOR [15]	Proposed
$0.2R_{\rm I}C_{\rm I}$	8.18	1.42	1.84	1.10
$0.5R_{\rm I}C_{\rm I}$	2.02	0.29	0.56	0.19
$R_{\rm I}C_{\rm I}$	2.21	0.06	0.21	0.03
$2R_{\rm I}C_{\rm I}$	5.15	0.01	0.13	0.01
$5R_{\rm I}C_{\rm I}$	7.28	0.01	0.19	0.01

Columns 4 and 5 present the results obtained using the model-order reduction (MOR) method proposed in [15] and the proposed method. A 2-pole MOR form of [15] for the current through each resistor was used since it is a fair comparison to the proposed technique that uses a 2-pole approximation $\tilde{I}_i(t)$ (Eqn. (5)). The MOR steps were the following: first use MOR to approximate the transfer function to two poles, then compute the current response with the input voltage source in the Laplace domain, and finally compute energy dissipation using poles and residues. It is clear from the results that the proposed method is as accurate as the 2-pole MOR method [15]. Note that this substantiates the 2-pole approximation for $I_i(t)$ used in this paper. However, the MOR method is computationally expensive since (i) each MOR run is super-linear in the number of nodes in the RC tree and (ii) MOR has to be performed for each resistor in the RC tree. Further, its application for back-of-the-envelope calculations is limited since past analysis cannot be leveraged, and MOR has to be repeated when there is a change in any network element (resistor or capacitor). Nevertheless, the MOR method can achieve higher accuracy if the reduced system uses more than two poles for the current through each resistor.

5.3 Remarks

Although this paper primarily focuses on the application of the developed models to interconnect energy analysis, the models and closed-form solutions for RC trees have broad applications. Our results show that the delay of the source – buffer, time-varying power supply, or resonant clock generator – determines the energy dissipated by the load circuit. This insight exposes potential solutions that can reduce the power consumption of a capacitive load to

less than $1/2CV_{\rm DD}^2$, something that has been the focus of research in adiabatic circuit design [4, 12, 14, 18, 19]. Adiabatic design is based on a slow charge and discharge of a capacitive load using a time-varying clocked power supply, usually realized by resonant LC-based oscillators. However, state-of-the-art models for energy estimation in adiabatic gates [2] are not as accurate and generic as the model proposed in this paper, as described in detail in Sec. 5.2. Hence, the proposed model can be used to analyze the the power-performance tradeoffs of generic adiabatic circuits, all of which are reducible to RC trees.

Full-chip thermal estimation tools combine substrate temperature profiles with inter-layer and intra-layer heat transfer equations to obtain global thermal profiles for the integrated circuit. The proposed interconnect self-heating models can be used to augment such thermal simulation with interconnect self-heating data. This can help predict performance degradation due to changes in RC delay in the interconnect, and identify reliability concerns due to electromigration.

6. Conclusions

The relationship between source delay and energy dissipation in RC trees was investigated in this paper. An Elmore energy model that is the computational analog of the conventional Elmore delay model for energy estimation in RC trees was described. The analysis techniques can be used to estimate interconnect self-heating effects to very high accuracy in a computationally efficient manner. Other applications include the analysis of tradeoffs between source delay and energy dissipation in adiabatic circuit design.

7. References

[1] S. Alam, *et al.,* "Circuit-level reliability analysis of Cu interconnects," *Proc. Intl. Symposium Quality Electronic Design*, pp. 238–243, 2004.

[2] M. Alioto, G. Palumbo, and M. Poli, "Evaluation of energy consumption in RC ladder circuits driven by a ramp input," *IEEE Trans. VLSI Systems*, Vol. 12, No. 10, pp. 1094–1107, Oct. 2004.

[3] A. H. Ajami, *et al.,* "Analysis of non-uniform temperature-dependent interconnect performance in high performance ICs," *Proc. Design Automation Conference*, pp. 567–572, 2001.

[4] W. C. Athas, *et al.,* "Low-power digital systems based on adiabatic-switching principles," *IEEE Trans. VLSI Systems,* Vol. 2, No. 4, pp. 398–407, Dec. 1994.

[5] K. Banerjee and A. Mehrotra, "Global (interconnect) warming," *IEEE Circuits and Devices Magazine*, Vol. 17, No. 5, pp. 16–32, Sep. 2001.

[6] S. A. Bota, *et al.,* "Within die thermal gradient impact on clock-skew: A new type of delay-fault mechanism, " *Proc. Intl. Test Conference,* pp. 1276–1284, 2004.

[7] J. A. Davis and J. D. Meindl (editors), *Interconnect technology and design for gigascale integration,* Kluwer Academic Publishers, 2003.

[8] M. Horowitz, R. Ho, and K. Mai, "The future of wires," *Proc. IEEE,* Vol. 89, No. 4, pp.490–504, Apr. 2001.

[9] International Technology Roadmap for Semiconductors, 2003.

[10] P. Kapur, G. Chandra, and K. C. Saraswat,"Power estimation in global interconnects and its reduction using a novel repeater optimization methodology," *Proc. Design Automation Conference,* pp. 461–466, 2002.

[11] K. Kim, *et al.,* "Noise-aware interconnect power optimization in domino logic synthesis," *IEEE Trans. VLSI Systems*, Vol. 11, No. 1, pp. 79–89, Feb. 2003.

[12] S. Kim and M. C. Papaefthymiou, "True single-phase adiabatic circuitry," *IEEE Trans. VLSI Systems*, Vol. 9, No. 1, pp. 52–63, Feb. 2001.

[13] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. Computer-aided Design*, Vol. 9, No. 4, pp. 352–366, Apr. 1990.

[14] C. L. Seitz, *et al.,* "Hot clock nMOS," *Proc. Chapel Hill Conference on VLSI,* pp. 1–17, 1985. Also available as Caltech TR 5177:TR:85.

[15] Y. Shin and T. Sakurai, "Power distribution analysis of VLSI interconnects using model order reduction," *IEEE Trans. Computer-aided Design*, Vol. 21, No. 6, pp. 739–745, Jun. 2002.

[16] C. N. Taylor, S. Dey, and Y. Zhao, "Modeling and minimization of interconnect energy dissipation in nanometer technologies," *Proc. Design Automation Conference,* pp. 754–757, 2001.

[17] T. Uchino and J. Cong, "An interconnect energy model considering coupling effects," *IEEE Trans. Computer-aided Design*, Vol. 21, No. 7, pp. 763–776, Jul. 2002.

[18] B. Wang and P. Mazumder, "On optimality of adiabatic switching in MOS energy-recovery circuit," *Proc. Intl. Symposium Low Power Electronics and Design*, pp. 236–239, 2004.

[19] Y. Ye and K. Roy, "Energy recovery circuits using reversible and partially reversible logic," *IEEE Trans. Circuits and Systems I*, Vol. 43, No. 9, pp. 769–778, Sep. 1996.