# A 10.6mW/0.8pJ Power-Scalable 1GS/s 4b ADC in 0.18$\mu$m CMOS with 5.8GHz ERBW

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## ABSTRACT

We present a 4-bit power scalable flash analog-to-digital converter in digital 0.18-$\mu$m CMOS, targeting low power ultra-wide band receivers. To minimize static power consumption, we exploit dynamic comparators with built-in digitally tunable thresholds. The converter has been realized and tested outperforming recent comparable designs even in more advanced technologies. The main performance figures include 5.8GHz effective resolution bandwidth and 0.8pJ/conversion-step at 1-GS/s and Nyquist conditions.

**Categories and Subject Descriptors:** B.7.1 [Integrated Circuits]: Types and Design Styles

**General Terms:** Design, Measurement, Performance.

**Keywords:** Ultra-low power high-speed converter design, flash converters, Ultra-Wide Band.

## 1. INTRODUCTION

The emerging applications in the wireless sensor arena, such as multi-band OFDM and pulsed Ultra-Wide Band (UWB) systems for wireless personal area networks, are posing very stringent requirements on transceivers. Minimum energy consumption is a must but good receiver performance is nonetheless needed for a large signal bandwidth [1, 2]. As a consequence, very demanding requirements on speed, bandwidth and power specifications of the Analog-to-Digital Converter (ADC) exist in the receiver front-end and make the design extremely challenging. Most of the reported ADCs for similar applications employ interleaving [1, 3], with each channel typically based on flash converters. Beside the high sampling rates, flash ADCs guarantee the smallest number of clock cycles per conversion and minimum latency. Moreover, in low resolution applications power consumption can still be contained.

In this paper we describe the concept, design, and measurement results of a 4-bit flash ADC optimized for ultra-low power and wide analog bandwidth at sufficiently high conversion rate for UWB applications. At 1 GS/s rate, the ADC consumes 10.6 mW and achieves a 5.8 GHz Effective Resolution Bandwidth (ERBW). Therefore, the proposed architecture is well suited for interleaved systems and can support different receiver topologies operating both at Nyquist and sub-sampling rates. The figure of merit of 0.8pJ/conversion-step at maximum sampling frequency and Nyquist conditions proves the efficiency of the proposed design when compared to recently published designs implemented with similar or even more advanced technologies.


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## 2. CONVERTER ARCHITECTURE

When implementing ADCs with reduced number of bits, flash converters provide a viable solution for low-power implementations. A drawback of traditional flash architectures is the large static power consumption in the preamplifier chain (to implement comparators) as well as in the reference resistive ladder because of the small resistance values required to overcome the signal feed-through problem [4]. In our system, shown in Figure 1, a latch-type *dynamic* comparator has been used both to sample (without using a specific track-and-hold circuit) and amplify the input signal, with no DC power consumption. Moreover, thresholds are *embedded* in the comparator chain through proper imbalance in the sizes of the input transistors thus avoiding power consuming circuits to generate reference voltages. In order to provide low ADC differential input capacitance, the comparator area has been minimized. Therefore, the converter accuracy would be irreparably impaired if offset compensation and fine threshold tuning were not performed. For this purpose, we rely on a dynamic offset correction technique which allows foreground ADC calibration through a set of digital words (one for each comparator) stored in the calibration registers.

Each comparator is then followed by an SR-latch to generate a thermometer code for the ADC back-end and increase the global regeneration gain. This contributes to reducing the error probability due to comparator metastability in presence of very small signals, especially after preamplifiers have been removed. A first order bubble correction stage follows the latch chain and converts the thermometer code to a 1-out-of-$2^n$ code. Finally, a 4-bit Gray code is produced, using a dynamic logic based ROM-table, and buffered at the output. Although Gray coding is rather tolerant to single bit errors, the first-order bubble correction block avoids the risk that, for very fast input signal, small timing differences between the response of the comparators cause the contemporary selection of two consecutive ROM locations. Design robustness and dynamic performance are consequently improved incurring in negligible power and area penalties.

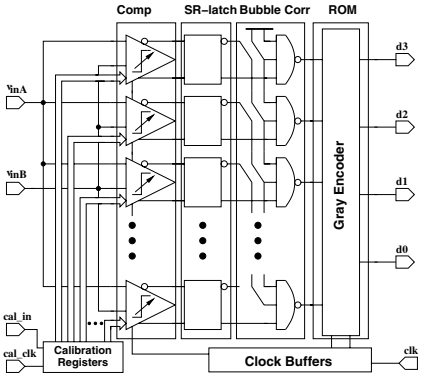


**Figure 1:** Flash ADC architecture.

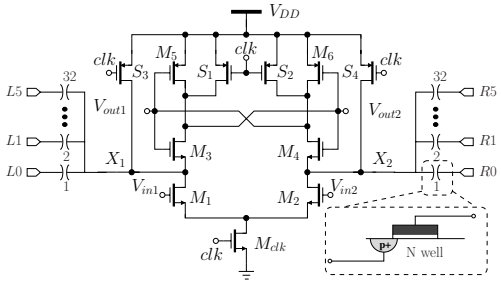


**Figure 2:** Dynamic comparator with calibration devices.

## 3. DESIGN AND IMPLEMENTATION

Pulsed UWB applications can work with resolution as low as 4 bits but at high conversion rates, as shown in [1]. Therefore, this design has been tailored to meet 3.5 minimum Effective Number of Bits (ENOB) at 1 GS/s. Additional specifications include: (i) 200mV peak-to-peak input differential voltage; (ii) less than 2 clock cycle latency. The dynamic architecture selected for the design allows drastic power savings during ADC inactivity, which is a desirable feature in energy constrained systems. In addition, latency requirements guarantee that the converter can be switched off almost immediately after the last input sample has been acquired and converted.

### 3.1 The Comparator Chain

The core of the ADC is the comparator chain. The architecture used in this design is a fast dynamic regenerative structure based on the architecture in [5]. The schematic diagram is represented in Figure 2. The *clk* signal sets the operating phase of the comparator. When *clk* is low, switches $S_1$, $S_2$, $S_3$, $S_4$ reset the comparator pushing the output node and nodes $X_1$ and $X_2$ up to $V_{DD}$. After the comparator is cleared of the previous output, *clk* goes high and the input differential voltage is sensed. A decision is then taken by the regenerative back-to-back inverter pair $M_{3,5} - M_{4,6}$. The evaluation phase can be divided in two sub-phases. At first, $M_1$ and $M_2$ operate in saturation regime, nodes $X_1$ and $X_2$ and, later, the output nodes are discharged almost linearly while the cross-coupled inverters are off. In this phase, any voltage difference between $V_{in1}$ and $V_{in2}$ generates an imbalance between the drain currents $I_1$ and $I_2$ so that the discharge rate of the outputs is not the same. As a consequence, a voltage difference appears between the output nodes. The second phase begins when the output voltages drop approximately to $V_{DD}+V_{Tp}$ ($V_{Tp}$ is the threshold voltage of the PMOS transistors). At this point, the inverters start to conduct and a strong positive feedback amplifies the output voltage difference set by the previous (slewing) phase. No current flows in the circuit after the transition is complete so that the comparator does not dissipate any static power.

Due to the time-varying nature of the circuit, it is not easy to derive an accurate analytical model for sizing. In fact, in the slewing phase, the discharge time is determined by the discharge current $I_0$ set by the $M_{clk}$ switch and the capacitances at nodes $X_1$, $X_2$, $V_{out1}$ and $V_{out2}$. In the regenerative phase, the time constant is primarily determined by the approximate expression:

$$\tau_R = \frac{(g_{ds1} + g_{m3})C_{out}}{g_{ds1}(g_{m3} + g_{m5}) + g_{m3}g_{m5}}, \qquad (1)$$

which reduces to $C_{out}/(g_{m3} + g_{m5})$ when $g_{ds1} \gg g_{m3}, g_{m5}$. The computation of the small signal parameters is problematic since no "traditional" bias point is reached. An empirical estimation of the total decision time is reported in [6], but accuracy is not enough for an optimized design. Therefore, we resorted to simulations to extract design parameters and determine device sizings while meeting the stringent requirement that a decision is taken in half of the clock period even when very small signals (much less than 100$\mu$V) are applied. Transistor channel lengths have been all set to the minimum feature size to maximize speed and the widths have been also selected as small as possible to minimize the input differential capacitance while relying on digital calibration for mismatch compensation.

### 3.2 Reference Thresholds

According to the traditional mismatch theory applied to differential pairs [7], undesired offset is caused by mismatch in transistor current factors and in threshold voltages due to process variability. In fact, any impairment in the $M_1 - M_2$ pair results in an input offset voltage $V_{io}$ that needs to be compensated to establish symmetric operation. We exploit this result to implement the ADC reference thresholds by creating an intentional imbalance in the widths of each comparator input pair devices. If a difference $\Delta W$ is deterministically imposed on the pair differentially so that $W_1 = (W + \Delta W/2)$ and $W_2 = (W - \Delta W/2)$, then the trip point of the comparator shifts by an amount that is linearly proportional to $\Delta W$. Using a square law model (valid for $M_{1,2}$ in saturation during the slewing phase) and Taylor expansion for small $\Delta W/2W$, the total input referred offset needed to compensate for the drain current imbalance can be approximated as:

$$V_{io} \approx -\frac{(V_{GS} - V_{Tn})}{2}\frac{\Delta W}{W} - \frac{(V_{GS} - V_{Tn})}{32}\frac{\Delta W^3}{W^3} \qquad (2)$$

where $V_{GS} = (v_{GS1} + v_{GS2})/2$ and $V_{Tn}$ is the threshold voltage of the NMOS input transistors. Using (2) we denote with $\Delta W_0$ the imbalance corresponding to the first threshold level (1 LSB) and then generate all levels using:

$$\Delta V_{th_i} = i\frac{(V_{GS} - V_{Tn})}{2}\frac{\Delta W_0}{W} \qquad (3)$$

where $i$ varies in $\{-7, \ldots, +7\}$. Trip points can indeed be assumed proportional to $\Delta W$ if the error (approximated by

the third order term) on thresholds is negligible. In particular, requiring that INL≤LSB/2 we obtain the following condition for the ADC resolution $n$:

$$\frac{\Delta W_0^2}{W^2} \leq \frac{8}{(2^{n-1}-1)^3}. \quad (4)$$

INL has been computed at the boundaries of the input signal where the cubic term in (2) is maximum. In our case ($\Delta W_0/W = 4.8\%$) linearity deviations become influent only for $n > 6$ thus making it feasible to reach 4 bit accuracy through (3).

In the proposed architecture, intentional mismatch lowers the overall CMRR. Moreover, the comparator trip points become more sensitive on process variability, power supply and other environmental factors. We addressed these problems implementing a calibration scheme that allows achieving almost ideal performance.

### 3.3 Threshold Calibration Circuit

The reference thresholds imposed by intentional imbalance in the comparators have to be guaranteed in the presence of offset due to device mismatch, that is also penalized because of the absence of static pre-amplification. Threshold calibration is performed using a dynamic technique, as in [8], through binary-scaled arrays of variable capacitors added at the drain nodes of the input pair $X_1$ and $X_2$. A difference $\Delta C = (C_1 - C_2)$ at the drain nodes need to be compensated by a corresponding difference $\Delta I = (I_1 - I_2)$ in the discharging currents during the slewing phase of the comparator operation. This difference translates into a shift in the comparator trip point given by:

$$V_{OD} = \frac{I}{g_{m1}}\frac{\Delta C}{C} = \frac{V_{GS} - V_{Tn}}{2}\frac{\Delta C}{C} \quad (5)$$

where $C = (C_1 + C_2)/2$, $I = (I_1 + I_2)/2 = I_0/2$ and $g_{m1}$ is the averaged transconductance of the input pair in the slewing phase. A switchable array of capacitors is implemented using devices similar to half of PMOS transistors with only a gate controlling the value of the capacitance and a source connected to the comparator node, as shown in Figure 2. If the gate voltage is low, the gate-channel capacitance is added at the comparator node and the device is enabled. In contrast, if a high gate voltage is applied only parasitic capacitances are present and the device is basically disabled. To minimize overlap and junction capacitances, PMOS source areas are shared between adjacent devices in the layout.

The insertion of additional capacitance slows the slewing phase of the comparator. On the other hand, as evident from (5), the larger is the total capacitive load, the smaller the minimum calibration step becomes (intended as the dynamic offset due to a minimum imbalance $\Delta C_{min}$). The accuracy of the calibration scheme must therefore be traded with comparator speed at design time. The input referred offset has been determined using an automated extraction procedure [9], which allows avoiding expensive statistical simulations. In fact, exploiting standard mismatch models we can express the total offset variance $\sigma_{OR}^2$ as:

$$\sigma_{OR}^2 = \sum_{i=1}^{N}\left[\left(\frac{\partial v_{OR}}{\partial V_{Ti}}\right)^2 \sigma_{V_{Ti}}^2 + \left(\frac{\partial v_{OR}}{\partial \beta_i}\right)^2 \sigma_{\beta_i}^2\right] \quad (6)$$

where $N$ is the total number of transistors and the standard deviations ($\sigma_{V_{Ti}}$,$\sigma_{\beta_i}$) are expressed in terms of transistor sizes and technology constants. The partial derivatives in (6) are determined through finite differences according to the following approximation:

$$\frac{\partial v_{OR}}{\partial X_i} \approx \frac{\Delta v_{OR}}{\Delta X_i} = \frac{v_{OR,X_i}}{\sigma_{X_i}}. \quad (7)$$

Based on (7) a number of electrical simulations have been performed by applying for every statistical variable its $\sigma$ value, and leaving all other variables at their mean value, and the offset in this conditions has been extracted through a bi-section method based root finder. Finally, the evaluation of (6) produces a $\sigma_{OR}$ approximately 12mV. As a consequence, the capacitor array has been sized to provide a minimum correction voltage less than LSB/2 and a maximum correction voltage larger than the $3\sigma_{OR}$ worst case. Six binary scaled devices per side have been used requiring a 12 bit digital calibration word for each comparator.

Calibration is performed off-line during a period of inactivity of the ADC. The calibration range available with the capacitor array can be further widened varying the input pair overdrive by setting the input common mode voltage. It is thus possible to allow flexible tuning of the converter thresholds for different dynamic ranges and different LSB values.

### 3.4 ADC Back-End

The ADC back-end consists in a 3-input AND gate chain, connected as in Figure 1, to detect the transitions from zero to one in the thermometer code, and a custom designed Gray encoded ROM. The ROM is driven by two non-overlapping clock phases generated by a clock buffering circuit. Most of the bubble correction schemes proposed in the literature require additional circuitry, which increases power consumption and delay. Based on the approach reported in [4] we decrease the amount of cascaded logic stages as much as possible to get 1 clock cycle latency, so that the sample taken at the rising edge of one clock cycle is available at the rising edge of the next clock cycle.

The verification of the system was performed bottom-up. First single comparator performance and calibration circuit capabilities were verified using extracted netlists including the compensation devices and the SR-latch. Then, the overall ADC front-end and, finally, the global system were simulated. A transient analysis at 1GS/s with an input voltage ramp (with approximately two samples per code) took 4 hours on a Pentium IV. The final extracted netlist included more than 7600 BSIM3v3 devices and lumped parasitic capacitors.

## 4. TESTING AND MEASUREMENT RESULTS

The ADC was fabricated in a 0.18-$\mu$m pure digital 1P6M CMOS process with standard-threshold MOS devices. The chip photograph is shown in Figure 3, where the main blocks, completely shielded by metal layers, have been highlighted. A large portion of the chip is decoupling capacitance (64pF), which is needed to ensure that the ground and power bounces do not degrade the performance. Several samples have been measured both in a probe set-up and on a PCB, at room temperature. Given the limited number of pins available in a probe setup, the original 4 bit output has been multiplexed on two pins so that the LSBs and the MSBs are selected at different clock phases. Therefore, sampling speed in the acquisition system has been doubled since sampling

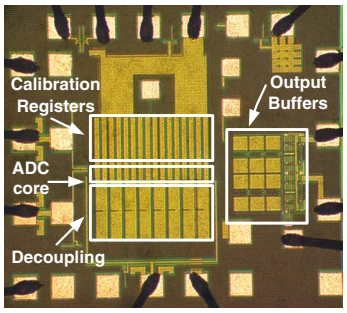


**Figure 3:** Chip microphotograph (The ADC core without calibration registers is 420×50 $\mu m^2$).

was needed at both phases, and the clock signal was also necessary for output synchronization and de-multiplexing. In order to bring off chip the multiplexed output signal two low swing (200mV) output drivers have been added, consisting in a PMOS differential pair with single-ended output and on-chip 50Ω load.

The measurement setup is shown in Figure 4. Matlab code implements the calibration algorithm and the other testing automated procedures. For spectral testing the RF input signal has been applied differentially to the chip using baluns and a 7GS/s acquisition system was used (HP ParBERT) to read and synchronize the ADC output.

## 4.1 ADC Calibration and Static Performance

The purpose of calibration is to find the digital pattern which minimizes the difference between the actual ADC threshold vector and the desired one. More formally, we define:

- $\boldsymbol{T}=(T_1,\ldots,T_{15}) \in \mathbb{R}^{15}$, vector of ideal thresholds;
- $\boldsymbol{C}=(R_1,L_1,\ldots,R_{15},L_{15})$, vector of the right side and left side calibration data of all comparators ($R_i, L_i \in \mathcal{D}=\{0,\ldots,63\}$);
- $\boldsymbol{t}(\boldsymbol{C})=(t_1(R_1,L_1),\ldots,t_{15}(R_{15},L_{15})) \in \mathbb{R}^{15}$, vector of real thresholds.

Calibrating means then finding $\boldsymbol{C}^{opt}$ that solves the following problem:

$$\boldsymbol{C}^{opt} = \arg \min_{C \in \mathcal{D}^{30}} \|\boldsymbol{t}(\boldsymbol{C}) - \boldsymbol{T}\|. \quad (8)$$

This is an optimization problem on a multi-dimensional discrete domain, which cannot be efficiently solved unless some simplifications are made to limit the search space.

In order to reduce the dimensionality of the problem and set up an automatic calibration procedure, we solved the previous optimization problem generating 15 independent optimization problems each calibrating a single comparator. Also, since capacitances from both side are not strictly necessary for calibration (even if their combined use could provide more flexibility), we further decreased the optimization problem complexity using capacitors from each side in mutual exclusion. With the above simplification the *calibration data* $c$ of each comparator is defined to vary in $\mathcal{C}=\{-63,\ldots,0,\ldots,63\}$. If $c>0$ a capacitance $\Delta C = |c| \cdot \Delta C_{min}$ is activated in the side which increases the input offset, if $c<0$ capacitance is activated in the side which decreases the offset, $c=0$ means that no device is activated.

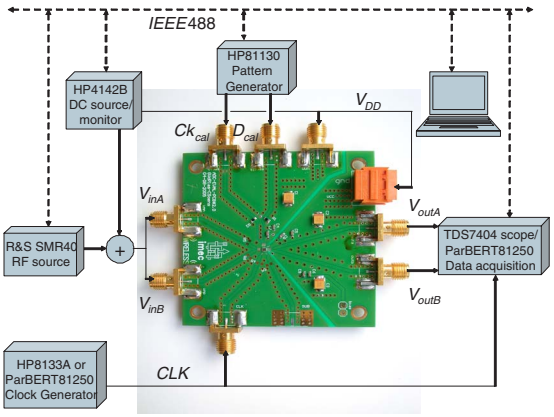


**Figure 4:** Measurement setup with a PCB photograph.

The single comparator optimization problem therefore reduces to:

$$c_k^{opt} = \arg \min_{c_k \in \mathcal{C}} |t(c_k) - T_k| \quad (9)$$

where $T_k$ is the desired (ideal) $k^{th}$ threshold and $t$ is the actual (real) one, as a function of $c_k$. Since the comparator characteristic is monotonic, we can solve the previous problems observing the ADC output. In fact, if we present the ADC with the input $T_k$, the *mean output code* $y_{c_k}(T_k)$, averaged with respect to random thermal noise, should be as close as possible to $k-\frac{1}{2}$ when the ADC is correctly calibrated. Based on these considerations we obtain:

$$c_k^{opt} = \arg \min_{c_k \in \mathcal{C}} |y_{c_k}(t) - y_{c_k}(T_k)| = \arg \min_{c_k \in \mathcal{C}} \left| y_{c_k}(T_k) - (k-\frac{1}{2}) \right|. \quad (10)$$

In order to isolate one comparator at a time we remove interference from the other comparators by shifting the other thresholds sufficiently far from the one under calibration. Based on this formulation the calibration of each comparator is performed based on a bisection algorithm, as outlined in Figure 5. Fine prototyping of the calibration algorithm has been possible relying on a statistical behavioral model of the ADC including offset and noise effects, as reported in [10]. Calibration data are transferred through a serial link and stored using a shift register designed on the chip. The input voltages are applied with an external voltage generator.

The system was clocked at a lower rate (40 MS/s) to simplify the calibration setup. It was not necessary to recalibrate the ADC between different testing sessions: under the same biasing conditions calibration provided the same results. The automated procedure allowed getting 0.18 LSB maximum DNL and 0.08 LSB maximum INL (Figure 6) for a 100mV input range; 0.25 LSB maximum DNL and 0.17 LSB maximum INL for a 200mV input range. The exact input voltages at all code boundaries have been found for INL and DNL calculations, using a bisection-based method. This was not expensive given the limited number of thresholds (15) and using the same setup available as for calibration.

## 4.2 ADC Dynamic Performance

In Figure 7 the signal-to-noise plus distortion ratio (SNDR) is plotted against the clock frequency for a fixed input signal in order to explore the maximum operating frequency. The ADC starts with 3.9 ENOB at low frequency and achieves more than 3.7 ENOB up to 1 GS/s. This can be considered

```
function cal = calibrate(T_k, k)
maxshift = 63; % set maximum calibration data
comp_set_input(T_k); % impose the wanted threshold voltage
a = 0; comp_set_pattern(a); % load initial calibration data
y_a = comp_get_out; % read the mean output code
d_a = y_a − (k − 0.5);
b = sign(d_a) * maxshift; % find the right side to trap the root
comp_set_pattern(b); y_b = comp_get_out; d_b = y_b−(k−0.5);
while (abs(a−b) > 1) % bisection loop
    c = floor((a + b) / 2); comp_set_pattern(c);
    y_c = comp_get_out; d_c = y_c − (k − 0.5);
    if (d_c * d_a) > 0
        a = c; d_a = d_c;
    else b = c; d_b = d_c; end
end
if abs(d_a) > abs(d_b)
    cal = b; % take minimum difference solution
else cal = a; end
```

**Figure 5:** Matlab-like pseudo-code for single comparator threshold calibration.

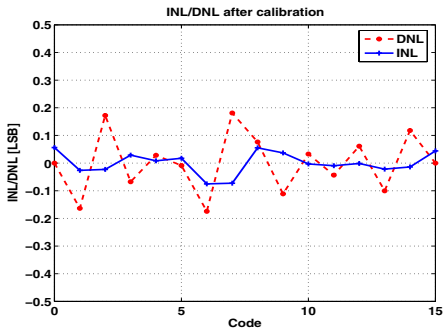


**Figure 6:** DNL (dashed) and INL (continuous) plot for the converter after calibration (100mV input range).

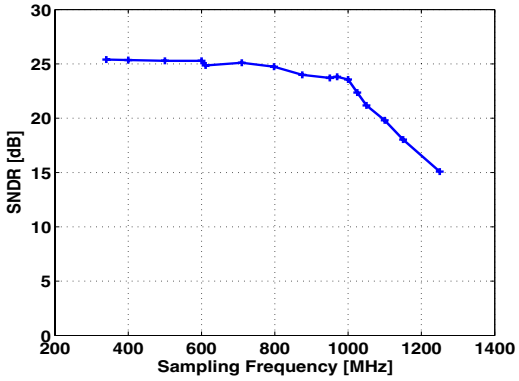


**Figure 7:** Measured SNDR versus sampling frequency ($f_{in}$=30MHz, $v_{in}$=200mVptp).

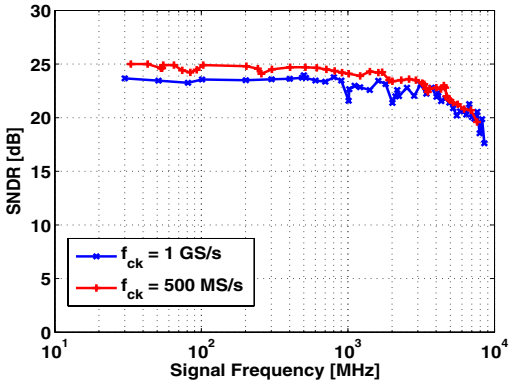


**Figure 8:** Measured SNDR versus signal frequency at 1GS/s and 500MS/s.

as the maximum operating frequency, after which performance quickly degrades, mainly because of limitations in the digital circuitry. Figure 8 shows the ADC dynamic performance respectively at 1 GHz and 500 MHz sample rates for a 200-mV peak-to-peak input voltage. At 1 GS/s the ADC achieves 3.7 ENOB from low frequency up to the Nyquist frequency. SNDR drops by 3-dB at an ERBW of 5.8 GHz. At 500 MS/s the low frequency ENOB is 3.9 and the ERBW is 4.7 GHz. The output spectrum for a full-swing 485 MHz sine wave input signal is shown in Figure 9 at 1GS/s. The SFDR is 35 dB and power consumption is 10.6 mW.

Because of the dynamic architecture, the ADC power consumption scales almost linearly for a wide range of the clock frequency as shown in Figure 10, and this is a very desirable feature for energy-constrained applications. Table 1 summarizes the ADC performance.

### 4.3 State-of-the-Art Comparison

In order to compare our design with similar state-of-the-art high speed, low resolution ADCs the quantization energy figure of merit (FoM), physically related to the energy required for one thermometer voltage step, is calculated as:

$$E_Q = \frac{\text{Power}}{2^{\text{ENOB}} \cdot 2f_{in}} \qquad (11)$$

where power is computed at the maximum sampling frequency $f_{sample}$, $f_{in}$ is the minimum between the Nyquist frequency ($f_{sample}/2$) and the ERBW and ENOB is measured at maximum sample frequency and input frequency equal to $f_{in}$. In Table 2 comparison is done with recently published designs and the dependence of the FoM on the technology is made evident.

Our design achieves the highest ERBW ever reported, 0.8 pJ/conversion-step at 1 GS/s and 0.73 pJ/conversion-step at 500 MS/s, both with a 1.8 V power supply. These are the lowest FoM values ever reported up to the 130 nm technology node, being superior only to 90-nm designs. Moreover, an ADC implementing a similar front-end architecture in 90-nm [11], even if without the bubble error correction logic (Figure 1), achieves the best FoM. Since power scales with frequency, better ENOB values and hence FoM values can be obtained scaling down the conversion rate. Operating at 1.7 V supply and 200 MS/s sample rate the ADC still achieves 3.9 ENOB with only 2 mW power consumption corresponding to a FoM as low as 0.67 pJ. Both the excellent dynamic performance and energy efficiency demonstrate the capability of the design and the adopted architecture even if implemented in a mature process technology.

## 5. CONCLUSIONS

Through careful architecture selection, design and innovative mixed signal solutions, this work has highlighted the feasibility, in 0.18-$\mu$m CMOS, of an high-speed, large ana-

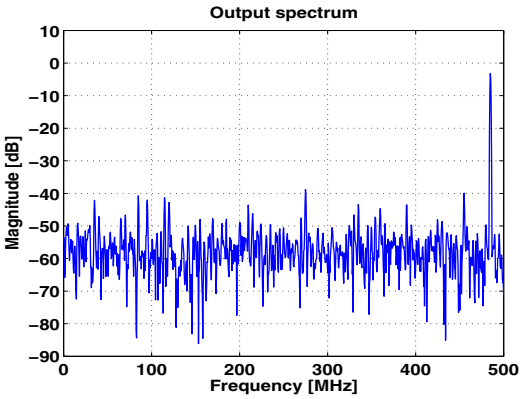


**Figure 9:** Measured power spectrum (2048-point DFT) at $f_{in}$=485MHz and $f_{ck}$=1GS/s.

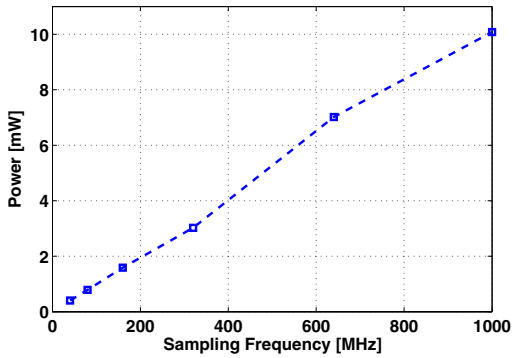


**Figure 10:** Average ADC power consumption as a function of the sampling frequency.

log bandwidth and power scalable ADC with sufficient accuracy for ultra-wide band signal detection in ultra-low power wireless receivers. Both design and testing processes have been thoroughly described. We selected a flash architecture based on dynamic comparators with built-in thresholds to limit DC power dissipation. The accuracy lost in the analog portion of the system in order to save power and increase speed is successfully recovered with digital calibration, which enhances the converter performance. With a 5.8 GHz ERBW and 0.8 pJ/conversion-step at 1 GS/s and Nyquist conditions, the converter outperforms recent comparable designs even in a smaller feature size technology. The presented ADC has been embedded in a low power impulse radio UWB receiver chip for low data rate sensor network applications [2].

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| Technology | 0.18-$\mu$m CMOS 1P6M | |
|---|---|---|
| Input Range (IR) | 200mVptp | |
| DNL | < 0.18LSB (@100mV IR)<br>< 0.25LSB (@200mV IR) | |
| INL | < 0.08LSB (@100mV IR)<br>< 0.17LSB (@200mV IR) | |
| Sampling Frequency | 500MS/s | 1GS/s |
| DC ENOB | 3.9 | 3.7 |
| SNDR Nyquist | 24.8dB | 23.9dB |
| ERBW | 4.7GHz | 5.8GHz |
| Power | 5.2mW | 10.6mW |
| Input Capacitance | 150fF | |
| Latency | 1 clock cycle | |
| Supply Voltage | 1.8V | |
| Area | 420×50$\mu$m$^2$ | |

**Table 1:** Performance summary.

| Ref. | P (mW) | Res. (bit) | $f_{clk}$ (GS/s) | ERBW (MHz) | Process ($\mu$m) | FoM (pJ) |
|---|---|---|---|---|---|---|
| [4] | 600 | 6 [5.4] | 1.3 | 600 | 0.25 | 11 |
| [3] | 1000 | 4 [3.3] | 12 | 2500 | 0.25 | 8.2 |
| [12] | 310 | 6 [4.7] | 2 | 750 | 0.18 | 3.5 |
| [13] | 340 | 6 [5.7] | 1.6 | 550 | 0.18 | 4 |
| [14] | 70 | 5 [4.0] | 0.6 | [—] | 0.18 | 7.3 |
| *This* | *10.6* | *4 [3.7]* | *1* | *5800* | *0.18* | *0.81* |
| *design* | *5.2* | *4 [3.8]* | *0.5* | *4700* | *0.18* | *0.73* |
| [15] | 182 | 4 [—] | 4 | [—] | 0.13 | 2.8 |
| [16] | 160 | 6 [5.5] | 1.2 | 700 | 0.13 | 2.2 |
| [17] | 10 | 6 [4.9] | 0.6 | 300 | 0.09 | 0.54 |
| [11] | 2.5 | 4 [3.7] | 1.25 | 3300 | 0.09 | 0.16 |

**Table 2:** Comparison with state-of-the-art high speed low resolution ADCs—The ENOB at Nyquist is given in brackets.


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