A CMOS SoC for 56/18/16 CD/DVD-dual/RAM Applications

Jyh-Shin Pan, Hao-Cheng Chen, Bing-Yu Hsieh, Hong-Ching Chen, Roger Lee,
Ching-Ho Chu, Yuan-Chin Liu, Chuan Liu, Lily Huang, Chang-Long Wu, Meng-Hsueh Lin,
Chun-Yiu Lin, Shang-Nien Tsai, Jenn-Ning Yang, Chang-Po Ma, Yung Cheng,
Shu-Hung Chou, Hsiu-Chen Peng, Peng-Chuan Huang, Benjamin Chiu, Alex Ho

MediaTek Inc.

No.1-2, Innovation Road 1, Science-Based Industrial Park, Hsin-Chu City, Taiwan 300, R.O.C.

Contact Info: BY_Hsieh@mtk.com.tw

ABSTRACT

A SoC, integrating RF/AFE and 1.5 Gb/s SATA PHY, is presented. It supports 471 Mb/s bit-rate at 18xS DVD. A partial parity mode reduces SDRAM bandwidth. A power control mode minimizes system clock rate. The SoC has 10M transistors, occupies 5.4 x 5.1 mm^2 in 0.18 mm CMOS process, and consumes 772 mW during 16xS DVD read.

Categories and Subject Descriptors

B.4.2 [**Input/Output Devices**]: Channels and controllers

General Terms: Performance, Design, Verification.

Keywords

DVD-RAM, Optical Storage, WSR, SATA, CMOS

1. INTRODUCTION

In the era that DVD recording speed increases to 16xS or more, the design challenge is to find low cost solution with higher performance and lower power consumption. The most promising solution to this challenge is SoC. This paper presents a fully-integrated multi-format SoC (FMSOC), which has recording/decoding capabilities of DVD-ROM/±R/±RW/RAM, DVD±R dual layer, and CD-ROM/R/RW. The SoC accomplishes CD/DVD-dual/RAM operation speed up to 56xS/18xS/16xS respectively. Maximum channel bit-rate achieves 471Mb/s at 18xS DVD-dual operation.

This paper also shares some experience for low power design used in FMSOC to satisfy the requirement of portable application.

2. ARCHITECTURE AND CHIP OVERVIEW

The block diagram of FMSOC is illustrated in Figure 1. The block Analog Front-End synthesizes RF and servo signals according to

reflected signals from optical pickup unit (OPU). A cost effective frequency tuning method for RF equalizer filter, based on configurable digital-aided calibration architecture with a Gm replica cell, is proposed. A 1.5Gb/s SATA PHY controller with wide capture range is also integrated. Unlike other solutions, in which write strategy generator is on OPU, WSG in FMSOC is built on-chip with 4 LVDS channels to accomplish 1xS to 18xS DVD recording. A PRML read channel is incorporated for high-speed application. A partial parity encoding method [1] improves both the efficiency of SDRAM access and the speed of PO parity generation. Advanced power control mechanism, together with the benefit of RF integration and high-efficient DRAM access, saves 45% power at 16xS DVD playback [1].
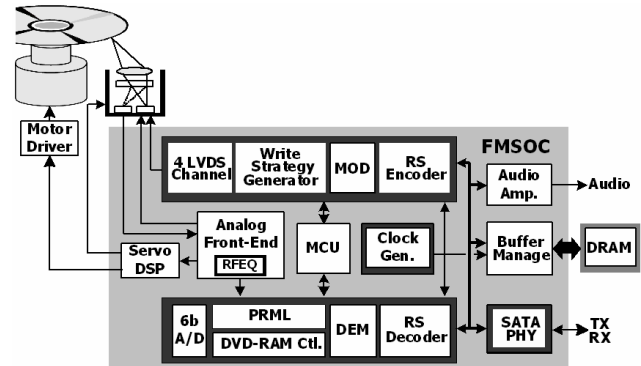

Figure 1. Block diagram of FMSOC in optical storage system

3. SOLUTION FOR LOW POWER ISSUE

Some solutions from architecture design to system operation are used in FMSOC.

A. Improvement of DRAM Access Efficiency

Using the partial parity encoding method, the efficiency of SDRAM access is improved. The advantage is that it can provide required memory bandwidth with relative low system clock, which reduces the power of system clock tree and the capacitance charge/discharge of external SDRAM pins.

B. Clock Suppression and Gating

FMSOC has multiple read/write functions, and the clock separation is the key issue for low power in FMSOC. There are two steps for clock separation. The first step is to separate clock by function in RTL level. The second step is to modify the netlist

for further clock gating control according to the power estimation result of clock tree in early P&R stage. In addition, the constraint of clock tree skew is also adjusted according to the estimated result.

C. Minimum Frequency Detection Loop

This item is to optimize power during system operation. The reason is that data throughput varies with both rotation speed and radius position of OPU in optical storage system. According to the throughput-rate, a minimum frequency detection loop [1] in FMSOC dynamically adjusts the operation system clock frequency to make it as small as possible.

D. Dual V_{th} Process

The leakage power is dominant in the sleep mode of FMSOC. For this case, the dual V_{th} flow is adopted in FMSOC to save the leakage power in sleep mode since the design effort is low and it is compatible to the original design flow without area and time delay overhead.

E. Voltage Partition

According to the functionality of analog/mix-mode/logic, the circuits are partitioned into separate physical regions. High-speed operation regions use higher supply voltage, while less timing critical regions use lower supply voltage. It requires level shifter and state retention flip-flops to ensure a proper interface between different voltage domains.

F. Multiple Clock Design

Multiple clock skill is utilized in FMSOC where different clock rate is provided to different modules according to throughput requirement. It can avoid unnecessary power dissipation by setting proper clocking rate to fulfill performance requirement instead of over-design. In contrast to single clock design, the penalty is additional FIFO in the interface across different frequency domain.
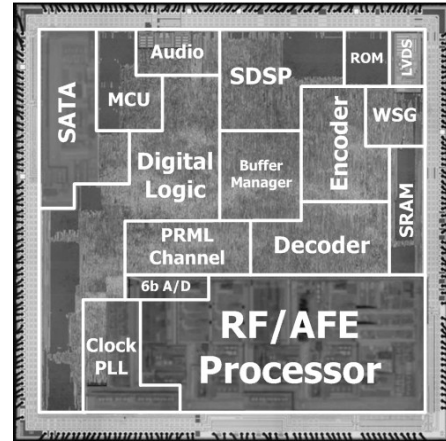

Figure 2. Die micrograph of FMSOC

4. CONCLUSION

The chip is implemented in 0.18μm 1P6M CMOS process. The physical implementation is carried out by Astro design automation tools. The 5.4x5.1 mm^2 die has an equivalent transistor count of about 10M. The chip micrograph is shown in Figure 2. At 16xS DVD playback, maximum power consumption is 772mW. It saves 45% power dissipation at 16xS DVD playback compared with previous results [1].

5. REFERENCE

[1] J.-S. Pan, T.-H. Hsu, H.-C. Chen, J.-W. Chen, B.-Y. Hsieh et. al.; "Fully Integrated CMOS SoC for 56/18/16 CD/DVD-dual/RAM Applications with On-Chip 4-LVDS Channel WSG and 1.5Gb/s SATA PHY"; ISSCC'06, Feb. 2006