Resistive-Open Defect Injection in SRAM Core-Cell: Analysis and Comparison between 0.13µm and 90nm Technologies[1]

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ABSTRACT

Resistive-open defects appear more and more frequently in VDSM technologies. In this paper we present a study concerning resistive-open defects in the core-cell of SRAM memories. The first target of this work is a comparison of the effect produced by resistive-open defects in the 0.13 µm and 90 nm core-cell. We show that the 90 nm core-cell is more robust than the 0.13 µm core-cell in presence of resistive-open defects. On the other hand we show that dynamic faults are most likely to occur in the 90 nm than in 0.13 µm core-cell. Finally we propose a unique March test solution that ensures the complete coverage of all the extracted fault models for both technologies.

Categories and Subject Descriptors

Area: T2.1 Testing; fault modeling and simulation; TPG; test validation and DFT

General Terms

VDSM Technologies, Test, Defect Analysis.

Keywords

SRAM Memories, Core-cell, Dynamic Faults, March Test.

1. INTRODUCTION

The silicon area dedicated to memory elements is constantly growing in recent designs. This fact is confirmed by the SIA Roadmap which forecasts a memory density approaching 94% of System on Chip (SoC) silicon area in the next ten years [1]. Therefore, memories are becoming the main responsible of the overall SoC yield. Consequently, efficient test solutions and repair schemes for memories are needed.

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RAM testing is traditionally based on functional fault models such as stuck-at, transition and coupling fault models [2]. In VDSM technologies these fault models are not enough sufficient to guaranty a good test efficiency. In fact, the improvements in manufacturing process density and memory architecture have brought new fault models as dynamic faults [7, 8] that require more than one operation in sequence to be sensitized. For this reason, dynamic faults are not directly detectable with standard March tests.

Most of dynamic faults are delay faults and specific test sequences with at-speed tests are necessary to detect them. Many links have been established between delay faults and resistive-open defects [4, 5]. The occurrence of resistive-open defects has considerably increased in recent technologies, where many interconnection layers and an ever-growing number of connections between each layer are present. In particular, it is reported in [6] that open/resistive vias are the most common root cause of test escapes in deep-submicron technologies.

Based on this fact, we started a study on the injection of resistive-open defects in memory core-cells of the Infineon synchronous embedded-SRAM. The characterization of the 0.13 µm core-cell in presence of resistive-open defects has been studied recently and results are reported in [10, 11]. In these papers, we have shown that resistive-open defects can lead to static behaviors, as for TF (Transition fault), RDF (Read Destructive Fault [3]), DRDR (Deceptive Read Destructive Fault [3]) and IRF (Incorrect Read Fault), or a dynamic behavior, as for dRDF (dynamic Read Destructive Fault [7, 9]).

Here, we propose a comparative study between the 0.13 µm and the 90 nm SRAM core-cell on the basis of new simulations performed with similar defect insertion. With this study, we show that the 90 nm core-cell is more robust than the 0.13 µm core-cell in presence of resistive-open defects. On the other hand, although its higher robustness, we show that dynamic faults are most likely to occur in the 90 nm than in 0.13 µm core-cell. In other words, the 90 nm core-cell is more sensitive to dynamic faults. Finally,

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we propose a unique March test solution that ensures the complete coverage of all the extracted fault models for both technologies.

The rest of the paper is organized as follows. In Section 2, we describe the simulation flow and we give the first comparative results between the two technologies. In Section 3 we present the differences between the 0.13 µm and 90 nm technologies in terms of fault models. A March solution allowing complete fault coverage is given in Section 4. Concluding remarks are in Section 5.

2. SIMULATIONS

Several resistive-open defects have been analyzed in the 0.13µm and 90 nm core-cells. Figure 1 depicts the scheme of a standard 6-transitors cell where we have inserted six different resistive-open defects. They have been placed on the interconnections, where the probability of occurrence is higher. The defects are not injected into all possible locations because of the symmetry of the core-cell, the chosen six locations allow an exhaustive analysis of the resistive-open defects in the core-cell.

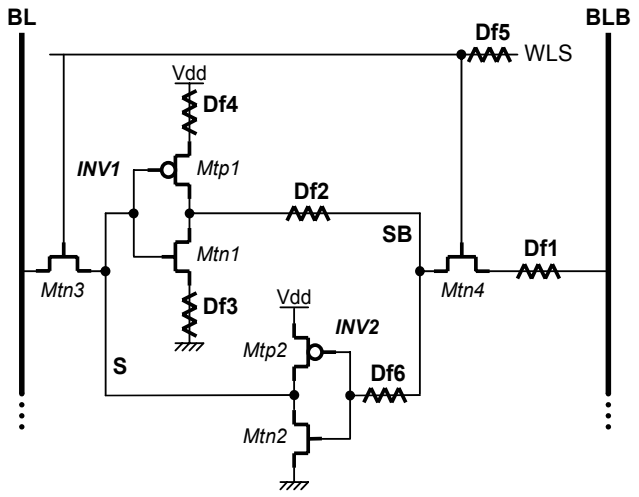


Figure 1: Resistive-open defects injected into the memory core-cell

All the electrical simulations have been performed with the Infineon internal SPICE-like simulator. A reference 8Kx32 memory block has been considered, organized as an array of 512 word lines x 512 bit lines. In order to reduce the simulation time, the simulations have been performed on a simplified version of the memory circuit that includes a reduced set of the core-cells and all the critical paths as pre-charge devices, sense amplifiers, write drivers, output buffer and the column and row address decoders. The resistance values have been chosen in a range between few ohm up to several Mohm in order to produce a complete view on the studied phenomena.

In order to allow a correct comparison between the two technologies, we have considered similar simulation conditions for both technologies, with the typical working parameters: same temperature 27°C and process typ (typical), a supply voltage of 1.5V for the 0.13 µm and 1.2V for the 90 nm, simulations performed in the 'active mode' (normal functional mode).

In Table 1, we present the main simulations results in terms of resistance values and related fault models. The first column gives the defect names (Dfi). The second one indicates the simulated technology. The third and fourth columns give respectively the related fault models and the minimum resistance value that induce a faulty behavior.

Table 1: Summary of simulations for both technologies, with related fault models and corresponding minimum detected resistance (typical working parameters)

	Technology	Fault model	Minimum resistance
Df1	**0.13 µm tech**	TF	25 kΩ
	90 nm tech	TF	200 kΩ
Df2	**0.13 µm tech**	RDF	20 kΩ
	90 nm tech	RDF	1 MΩ
Df3	**0.13 µm tech**	RDF	7 kΩ
	90 nm tech	RDF	500 kΩ
Df4	**0.13 µm tech**	dRDF	16 MΩ
	90 nm tech	dRDF	50 MΩ
Df5	**0.13 µm tech**	TF	200 kΩ
	90 nm tech	TF	10 MΩ
Df6	**0.13 µm tech**	TF	2 MΩ
	90 nm tech	TF	3 MΩ

The definitions of the reported fault models are the following ones:

- **Transition Fault (TF):** A cell is said to have a TF if it fails to undergo a transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) when it is written.
- **Read Destructive Fault (RDF) [3]:** A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output.
- **Dynamic Read Destructive Fault (dRDF) [7, 9]:** A cell is said to have an dRDF if a write operation immediately followed by a read operation performed on the cell changes the logic state of this cell and returns an incorrect value on the output.
- **Deceptive Read Destructive Fault (DRDF) [3]:** A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell.
- **Incorrect Read Fault (IRF):** A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, and the correct value is still stored in the cell.

Before producing any comment about the core-cell reliability in connection with the simulation results it is useful to do some considerations. Independently from what the simulations have brought, it is important to point out that the 0.13 µm memories are produced since several years and much is known about them. The 90 nm technology is young and many important aspects are not already known. This study and further similar studies are therefore needed to reach the same level of yield (in terms of stability and reliability) than that of the 0.13 µm technology.

Let us now discuss the results shown in Table 1. Firstly, for both technologies, the same fault models have been extracted. On the other hand, the analysis of the results has brought a crucial difference between the two technologies concerning the robustness of the 90 nm core-cell in presence of resistive-open defects. This is related to the capability of the cell to continue to work correctly even after the defect injection, till a certain threshold value of resistance. In order to illustrate this difference, the results, already shown in Table 1, are graphically reported in Figure 2. It is useful to note that the value of the resistances have been placed in a logarithmic scale.

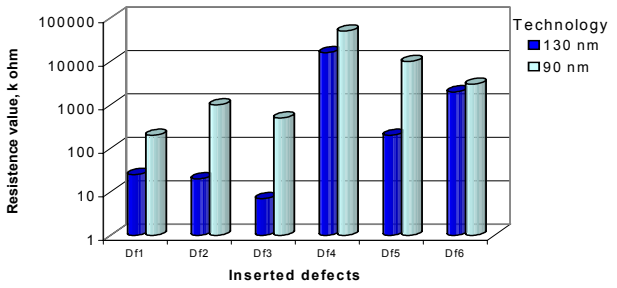


Figure 2: Graph of the minimal resistive values that produce faulty behavior

It is easy to observe that the 90 nm technology is always more resistant to the defect injection. In other words, the 90 nm core-cell has a correct activity for resistive values that induce a faulty behavior in the 0.13 µm core-cell. Df4 and Df6 apart, the other defects require a resistance value that normally is an order of magnitude higher in the case of the 90 nm core-cell. This means that, in this way, the 90 nm core-cell is much more robust than the 0.13 µm core-cell in presence of resistive-open.

This important difference between the two technologies requires further comments. We have to remark that we use different values of supply voltage, 1.5 V for the 0.13 µm and 1.2 V for the 90 nm technology. As we have shown in [10], in this kind of resistive-open defect injection, the faulty behavior appear more frequently at high voltage. High supply voltage makes the memory surprisingly less stable than a lower supply voltage. In fact, in this condition, the commutations become quicker as the voltage difference gets higher. Consequently, the cell is more sensitive to any perturbation.

3. FURTHER SIMULATIONS AND DYNAMIC FAULTS

In this section, we expose the results of simulations performed by considering all different operation conditions in terms of temperature, supply voltage, and process corner. These results are summarized in Table 2 and concern only the extracted fault models. In most of the cases, each defect involves the same fault models in both technologies. We have a different behavior only for Df2, at the output of INV1, and Df3 in the pull down of INV1. Df2 and Df3 produce read destructive faults in both technologies. However, in the 0.13 µm core-cell the fault is static while in the 90 nm core-cell the fault is dynamic in certain conditions.

Table 2: Fault model extraction: simulation results with any parameters

	Technology	Extracted fault models
Df1	**0.13 µm tech**	TF
	90 nm tech	TF
Df2	**0.13 µm tech**	DRDF - RDF
	90 nm tech	DRDF - RDF - dRDF
Df3	**0.13 µm tech**	DRDF - RDF
	90 nm tech	DRDF - RDF – dRDF
Df4	**0.13 µm tech**	dRDF
	90 nm tech	dRDF
Df5	**0.13 µm tech**	IRF - TF
	90 nm tech	IRF - TF
Df6	**0.13 µm tech**	TF
	90 nm tech	TF

This dynamic behavior has been obtained with the specific following conditions:

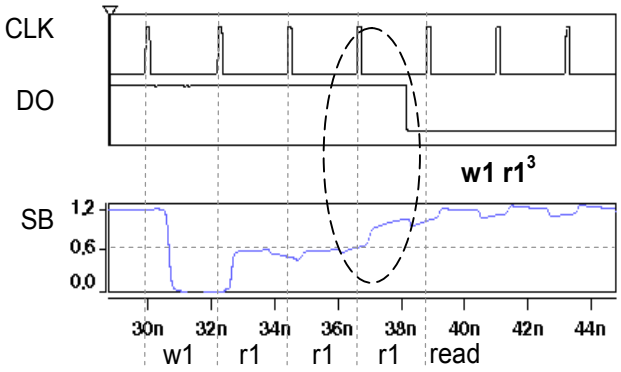
Defect Df2: - active mode (normal functional mode):
Process: typical
Supply voltage: 0.8V
Temperature: – 40°C
- slow mode (low-power):
whatever the process corner, temperature and supply voltage.

Defect Df3: - active mode (normal functional mode):
Process: typical
Supply voltage: any value
Temperature: – 40°C.
- slow mode (low-power):
Process: typical
Supply voltage: any value
Temperature: – 40°C.

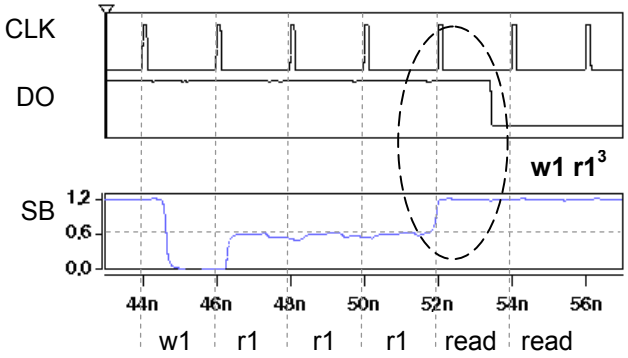
The dynamic nature of the faults, brought by Df2 and Df3, is visible in the two examples of the waveforms in Figure 3. Several read operations (w1r13 for Df2 and Df3) are necessary to produce the faulty swap of the cell (see encircled transitions in Figure 3). This can be explained by the fact that those defects are inserted in the loop of the two inverters, consequently they disturb the self refreshment of the stored value.

Concerning Df2 and Df3, in the case of the 90 nm core-cell, when there is a dRDF, the refreshment of the loop has a degradation that is proportional to the value of the resistive-open defect inserted. When a certain resistance value is reached the fault loses its dynamic nature and becomes a simple RDF. A simple read operation is sufficient to produce a faulty swap of the cell. In the case of the 0.13 µm core-cell, the transition range of resistance value in which there is a dynamic behavior is reduced to a point that we call 'cut point'. This cut point is at R=20 kΩ for Df2 and R=7 kΩ for Df3. Before this cut point, the value of the

injected resistance is not sufficient to induce a faulty behavior. After the cut point all the resistance values are able to cause a (static) read destructive fault. For larger resistive defects it is impossible to perform write operation (w1) correctly on the cell and there is a transition fault.



(a): Df2 - 950 kΩ, mode slow, typ, 1.2V, 27°C- dRDF



(b): Df3 – 1 MΩ, mode slow, typ, 1.2V, 27°C- dRDF

Figure 3: Dynamic faulty behavior induced by Df2 and Df3 in the 90 nm core-cells

Note that Df6, which is also placed inside the refreshment loop, has a very low effect on the behavior of the cell because it is placed at the gates of the two transistors of INV2. No bias current enters in the CMOS transistor gate. Thus the resistive defect has to be very large to generate a large delay.

From this analysis, we can conclude that the test of dynamic faults is much more important for the 90 nm core-cell than for the 0.13 µm core-cell. In fact, three defects among the six may cause a dynamic fault in the 90 nm core-cell while only one defect can cause a dynamic fault in the 0.13 µm core-cell. In Section 4 we show how the test procedure that we have proposed in [11] to test all the fault models of the 0.13 µm core-cell is still effective for the 90 nm core-cell, even with the mentioned differences concerning the fault models.

4. TEST PROCEDURE

In the previous section it has been shown that a dRDF can be the consequence of resistive-open defects in the core-cell of SRAMs. In particular it has been empathized that in presence of the resistive-open defects Df2, Df3 and Df4 (Df2 and Df3 only for the 90 nm technology), the action of single or multiple read immediately after a write operation may cause the inversion of the value stored in the cell. Consequently in order to sensitize this fault it is necessary that the test algorithm has sequences with multiple read operations like w0r0n and w1r1n. In [11] we have demonstrated that a cell can undergo a stress equivalent to a read operation (Read Equivalent Stress, RES) when a read/write operation is performed on other cells of the same word line.

It is useful to remember that when a cell is selected for a read or write operation the pre-charge circuit is normally turned off in its bit line. For the bit lines that are not involved in the operation, the pre-charge circuit is commonly left on. With the pre-charge active and the word line being high on the unselected columns, the cells fight against the pre-charge circuit. A consequent deduction is that the stress produced by a read operation on a cell is equivalent to the stress caused by a read or write operation performed on whatever cell on the same word line. During a read action the perturbation of the cell is produced by the charge stored previously on its two bit lines, while in the other case the cell is stressed by the same bit line charge, but with the pre-charge circuit still on. In order to simplify what exposed above we produce the example referred to the scheme in Figure 4.

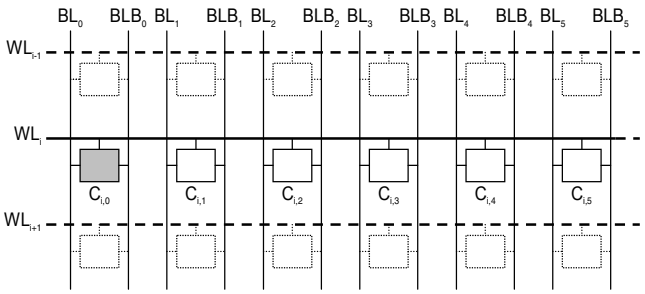


Figure 4: A portion of an SRAM block

This scheme depicts a section of an SRAM block, and in particular in the middle there are the first six cells of the word line WLi. We assume that on WLi the first cell on the left Ci,0 is affected by a resistive-open defect in the pull-up transistor of one of the two inverters (as Df4 in Figure 1). This defect may cause a dRDF. This fault is detectable when, immediately after a write data on cell Ci,0, one or multiple read operations are performed on the same cell. An equivalent faulty behavior can also occur when the write data in cell Ci,0 is followed by read or write operations on the other cells of the same world line. This is possible because, if for example cell Ci,1 is selected, the pass transistors (Mnt3 and Mnt4 in Figure 1) of all the cells on the same word line, in particular the faulty cell Ci,0, are saturated. So, Ci,0 fights against the pre-charge circuit that is in on state as for all the non-selected columns. Consequently, the faulty cell Ci,0 undergoes a stress (RES) similar to a read operation.

In [11] we have produced formal confirmations to the previous statements with electrical simulations that have been performed on Infineon 0.13 µm embedded-SRAM family with the Infineon internal SPICE-like simulator. It has been considered a reference 8kx32 memory, organized as an array of 512 word lines x 512 bit lines. The cell array of this memory is split in 128 blocks. When a word line is selected all the 512 cells on this word line are

connected to respective bit lines. Similar simulations have been performed on the Infineon 90 nm embedded-SRAM and confirm the efficiency of RESs to sensitize dRDFs.

In order to use the RESs for the production of an efficient March test for the detection of the dRDF caused by Df2, Df3 and Df4 the algorithm has to have the following requirements:

It is necessary that the read/write operations are performed with a particular addressing order with the purpose to execute the March elements on the memory array by acting on word line after word line. This is necessary because the RESs are produced only by operating on the cells of the same word line. For example, considering the mentioned Infineon embedded-SRAM architecture, the read and write operations of the March elements have to be operated firstly on all the 512 cells of the first word line, then on the 512 cells of the second word line, and so on.

The elements of the March test have to include w0 operations to sensitize the dynamic faults induced by Df4, w1 operations for those induced by Df2 and Df3. Moreover the elements with w1 allows the detection of dRDF produced by resistive-open defects placed symmetrically in reference with Df4, while the elements with w0 allows the detection of dRDF produced by resistive-open defects placed symmetrically in reference with Df2 and Df3 (see Figure 1).

The presence of r0 and r1 operations is necessary for observation.

All the elements, in particular the sensitization ones, need to be performed in ⇑ and ⇓ sequence.

The last statement is necessary to obtain the best distribution of RESs on all the memory cells. For details see [11].

Considering the previous requirements, let us show how it is possible to produce an efficient test for all the fault models that we have identified in the core cell, in particular for the dynamic ones produced by Df4, and Df2 and Df3 only in the case of 90 nm technology. In [11] we have proposed to use the March C- that normally covers 0% of dRDF [9], with an opportune modification that make it able to cover all the faults generated by the resistive-open defects injection in the 0.13 µm core-cell. March C- is represented in Figure 5 and the modification is the following one: the read/write operations of the algorithm have to be performed with a particular addressing order with the purpose to execute the March elements on the memory array by acting on word line after word line.

$$\{\ \Updownarrow(w0)\ \ \Uparrow(r0,w1)\ \ \Uparrow(r1,w0)\ \ \Downarrow(r0,w1)\ \ \Downarrow(r1,w0)\ \ \Updownarrow(r0)\ \}$$
$$M_0 \qquad M_1 \qquad M_2 \qquad M_3 \qquad M_4 \qquad M_5$$

Figure 5: March C- structure

This is necessary because the RESs are produced only by operating on the cells of the same word line. For example, let us consider again the already mentioned Infineon embedded-SRAM architecture. The read and write operations of the March elements have to be operated firstly on all the 512 cells of the first word line, then on the 512 cells of the second word line, and so on.

This modified March C- is able to cover all the dRDF of 90 nm technology. In facts, some elements of March C- include w0 and w1 operations, necessary for sensitization of all the dRDF, and r0 and r1 necessary for their observation. Moreover, the elements, in particular the sensitization ones, are performed in ⇑ and ⇓ sequence. This condition allows that the cells endure a good average distribution of RESs for all the cells along the entire word lines.

The modification makes March C- able to detect dRDFs, though in the mean time, due to the first of the six degrees of freedom [12, 13] of March tests, it does not change the capability of March C- to detect the former target faults. Among these faults there are the static faults TFs and IRFs that are induced by Df1, Df5 and Df6. Moreover the use of the effect of RESs allows the modified March C- to cover also the DRDF, deceptive read destructive fault, caused by Df2 and Df3, in certain resistive ranges.

The proposed March test solution presents many advantages as its linear complexity and the reutilization of an already existing March test. The main benefit is the high efficiency to detect dRDF and its capability to cover exhaustively all the core-cell faults related to the resistive-open defect injection.

5. CONCLUSIONS

The present study has focused on a comparison between the faults produced by the resistive-open defect injection in SRAM core-cell with the 0.13 µm and 90 nm technologies. In particular, we have shown two main differences concerning the extracted fault models and the robustness of the cell.

Firstly, the 90 nm core-cell is always more resistant to this kind of defect injection. In facts, in the case of the 90 nm core-cell, resistance values with an order of magnitude higher than for the 0.13 µm core-cell are necessary to produce a faulty behavior. The good rejection to the presence of resistive-open defects, shown by the 90 nm core-cell, is especially evident for Df2, Df3 and Df5.

The second important difference between the two technologies concerns the extracted fault models. In particular defects Df2 and Df3 involve static read destructive faults in the 0.13 µm technology while for the 90 nm technology these faults can be dynamic.

In the final part of the paper we have presented a test procedure that covers all the fault models in both technologies. This solution is based on the use of the concept of RES (Read Equivalent Stress) that allows to produce efficient algorithms for dynamic read destructive faults in spite of a very low complexity.

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