CAD Tools for Variation Tolerance

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ABSTRACT

Process variability greatly affects power and timing of nanometer scale CMOS circuits, leading to parametric yield loss due to both timing and power constraint violations. This parametric yield loss will continue to worsen in future technologies as a result of increasing process variations [1] and the increased importance of leakage power. Hence, statistical techniques are required to maximize parametric yield under given power and frequency constraints. Recently, much progress has been reported in the area of statistical modeling of leakage power [6] and circuit timing [2-5]. These techniques are useful in analyzing the impact of process variations on performance and power in nanometer CMOS designs. In this extended abstract, we outline the need for statistical optimization methods.

Categories and Subject Descriptors: Performance analysis and Design Aids
General Terms: Reliability, Performance
Keywords: Yield, Variability, Design Flows

1 Variation tolerant design optimization

Parametric yield is one of the most pressing issues for advanced IC design in nanometer CMOS technologies. While there has been extensive work in statistical delay and power modeling, there has been relatively little work on how to use these statistical methods to perform yield optimization. Most of the work in circuit optimization has been limited to deterministic optimization using corner-case model files.

A key issue with deterministic design optimizations is that they are blind to the impact of the optimization decisions on the yield of the design. Hence, they invariably result in the formation of a so-called timing wall, since the optimization has no incentive to reduce the delay of non-critical paths. While non-critical paths cannot affect circuit delay in deterministic analysis, near-critical paths can affect the circuit delay under process variations. As the number of near-critical paths increases, the likelihood that one of these near-critical paths becomes performance limiting under process variations also increases. Hence, the timing wall created by deterministic optimization will make the design more susceptible to process variations and will increase its statistical circuit delay for high confidence points. A new optimization methodology based on a truly statistical objective function is therefore needed need for cost-effective VLSI design in the nanometer technology regime.

A second consideration for variation-aware optimization is that both circuit timing and leakage power must be taken into consideration. Leakage power has grown to contribute a significant fraction of the total power budget and is also highly susceptible to process variations. In [7], it was shown that a 20X variation in chip-level leakage current can occur over 1000 samples of a microprocessor design in 0.18µm technology. Furthermore, it was demonstrated that a strong inverse correlation exists between power and performance/speed. Approaches that perform individual optimization for only timing or power neglect this correlation. Hence, they may simply be trading off gains in one yield category for yield loss in another. For instance, timing yield gains due to assignment of devices to low-vt or larger width would come at a loss in yield due to increased power. There is a clear need to develop approaches that are statistical in nature and that maximize yield, considering both timing and performance constraints while considering their correlation.

Finally, statistical design optimization needs to be applied across a range of design phases. Most research has focussed on statistical analysis for post-layout designs where detailed spatial information is available. This facilitates the analysis since spatial correlations between gate delays can be modeled in detail. However, late in the design cycle, the optimization horizon is severely limited, constraining the yield improvement that is attainable. Hence, variation-aware design exploration and optimization should not be limited only to this phase of the design, and new methods and their application early in the design cycle, such as during technology mapping or even before synthesis, are needed. Therefore, similar to the statistical wireload models used for traditional front-end synthesis flows, novel modelling techniques are also required for representing variability at higher level of abstraction. However, since less specific design information is available, accurate statistical analysis is, calling for the development of new statistically-aware analysis and optimization methods.

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