Interconnects are Moving from MHz->GHz Should you be Afraid? Or… "My Giga Hertz, Does Yours?"

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PANEL ABSTRACT

Chip interfaces, including standards like PCI Express, are increasingly relying on high-speed serial technology. This move from MHz to GHz brings with it a myriad of chip design challenges that many designers have never faced before. This diverse panel of experts in chip and IP mixed-signal design will describe not only why you SHOULD be afraid (very afraid), but also what's being done to make this transition practical, including new design techniques and standards.

SUMMARY

In the coming years, nearly every SoC will have an interface that relies on high-speed interconnect technology. Today, designers are "comfortable" with connections that run at 100's of megabits/sec, but making the transition to standards like PCI Express and SATA will instantly bring them into the gigabits/sec range, introducing a whole new universe of design challenges. Designers will need to understand the challenges they'll face as well as what to look for in the solutions they acquire to add this kind of technology to their SoCs.

Making practical the adoption of this kind of high-speed technology requires both a holistic understanding of the problem and a similar approach to the solution. This requires incorporating theory; semiconductor technology; design techniques, tools, IP, methodology; packaging and physical interconnect knowledge and technology.

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This is a truly diverse panel of accomplished experts have all proven their ability to make this high-speed technology practical to adopt by mainstream SoC designers.

1. GIGABIT INTERFACES: BACKGROUND

Why is this panel appropriate to the DAC audience?

- Everybody's doing it (or soon will) - the movement today is from parallel to high-speed serial interfaces, with PCI Express and SATA as leading examples of standards which will see broad use, quickly
- Those who see this coming know to be afraid; those who don't see it coming, should be afraid
- It's tough! 600MHz may seem tough, but when you cross 1GHz and slide right up to 2.5GHz, you're in for a whole new set of chip, packaging, and system-level challenges
- It's a surprise - 600MHz to 2.5GHz is a big step, and the challenges will catch a lot of designers by surprise
- Ok, get the signal issues straight and what about yield?
- When things to wrong, they go REALLY wrong - how do you debug a 2.5 (or 5 or 10) GHz circuit that fails in your system? How do you even measure what's wrong?
- The solution is a combination of good design techniques & engineering, tools, along with new IP & methodologies

2. PANEL VIEWPOINTS

As the challenges of integrating gigabit interfaces are manifold, and the solutions require holistic approaches, the viewpoints and experience included in this panel of experts (who have all experienced the pain of implementing these interfaces) spans device physics to system chassis: system-level design and integration, backplane materials and manufacturing considerations, board design, IC packaging, signal integrity and power (on-chip and in-system), silicon intellectual property, SoC design and integration.