BEOL Variability and Impact on RC Extraction

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Abstract
Historically, Back End of Line (BEOL) or interconnect resistance and capacitance have been viewed as parasitic components. They have now become key parameters with significant impact on circuit performance and signal integrity. This paper examines the types of BEOL variations and their impact on RC extraction. The importance of modeling systematic effects in RC extraction is discussed. The need for minimizing the computational error in RC extraction before incorporating random process variations is emphasized.

Categories & Subject Descriptors:
B.7.2 [Hardware]: IC; B.8.2 [Hardware]: Performance and Reliability; J.6 [Computer Applications]: CAD

General Terms: Design, Performance, Verification

Keywords: Process variation, Interconnect, Extraction

1. Introduction

Contribution to circuit performance can be divided into transistor and interconnect components. The interconnect components can be further divided into intra-cell (within library cells) and inter-cell (between cells) components. Fig. 1 shows the contributors to intra-cell and inter-cell parameters.

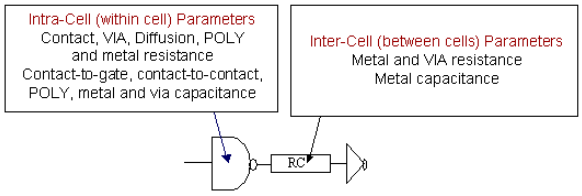

Fig. 1 Contributors to intra-cell and inter-cell parameters

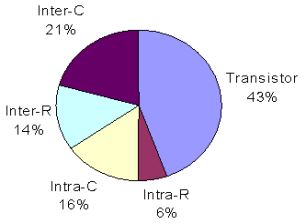

Fig. 2 An illustration of delay components

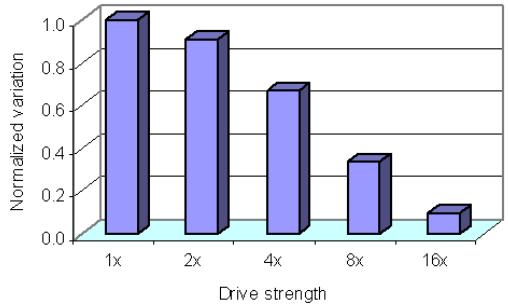

Fig.3 Normalized delay variation

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Fig. 2 shows an illustration of the delay components in a 65nm critical path. It can be clearly seen that the intra-cell components have become significant fraction of overall circuit delay. Hence the variations on both the inter-cell and intra-cell components need to be analyzed. Fig.3 shows the normalized variation in delay for a 3-sigma variation of inter-cell RC parameters. It can be seen that for a given interconnect load, smaller drive strengths are more susceptible to interconnect variations than larger drive strengths (transistor dominated).

2. Interconnect Variations

In this section, systematic and random interconnect variations are discussed. Critical systematic variations include Non-Linear Resistance (NLR) effect, Selective Process Bias (SPB) effect, thickness variations due to etch and CMP (Chemical Mechanical Polishing). Metal sheet resistance (Rsheet) is not a constant parameter. As shown in Fig.4, sheet resistance varies as a non-linear function of line width. Two phenomena cause significant systematic changes in sheet resistance as a function of line width for copper technologies. The first one is due to scattering of electrons off of the edges of the conductor and along the grain boundaries. The second includes systematic changes in copper cross-sectional area as a function of line width that are induced by the damascene process flow. An example of such an effect is CMP (Chemical Mechanical Polishing) induced copper dishing that would increase resistance.

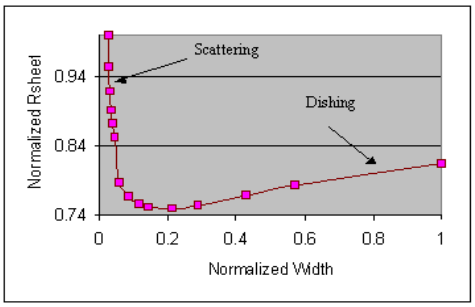

Fig.4 Non-linear relation between Rsheet and line width

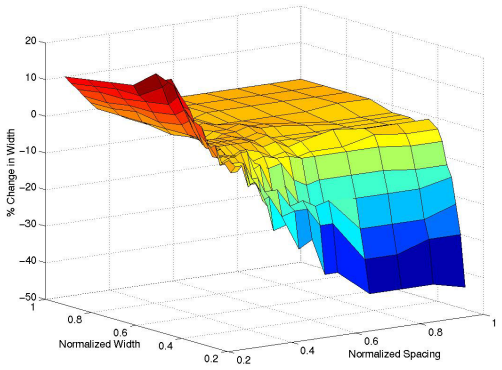

Fig.5 Change in Effective line width due to SPB

In DSM copper technologies, as route dimensions are becoming increasingly smaller, "what you draw is not what you get". This effect is referred to as Selective Process Bias (SPB) in this paper (different terms used in the industry to describe this effect). As shown in Fig.5, effective line width (and hence effective spacing) varies as a function of drawn width and spacing. It should be noted that isolated lines could have significant change in width. Change in width can be negative and positive as well, depending on the spacing of a given line to adjacent line(s).

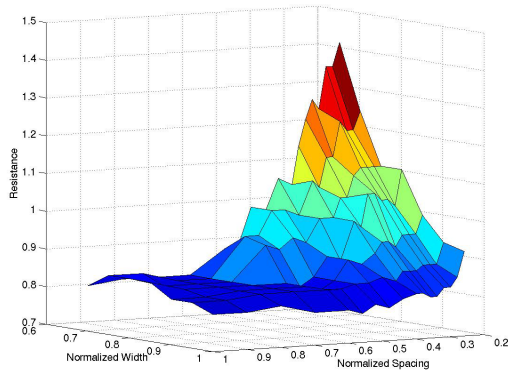

Fig.6 Change in effective resistance due to SPB

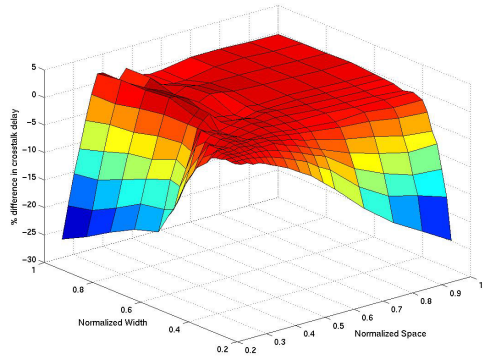

Fig.7 Impact of SPB on crosstalk delay

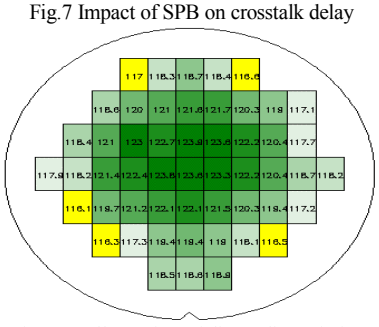

Fig.8 An Illustration of die-to-die variations

Fig. 6 shows the combined effect of SPB and non-linear resistance for narrow line widths. Fig. 7 shows the combined impact of SPB and NLR on crosstalk delay. Metal thickness can vary as a function of line width, local and global densities. This systematic effect due to CMP and etch can be modeled to determine the impact on resistance and capacitance. Other sources of variations include die-to-die variations, wafer-to-wafer variations, lot-to-lot variations and fab-to-fab variations. Fig.8 shows an illustration of die-to-die variations.

3. RC Extraction

Silicon validation of parasitics helps in closing the loop between process realities and interconnect extraction [1]. Fig. 9 illustrates an example where only one of four commercial extraction tool (tool A) bounded silicon results for min and max process corners. Fig. 10 illustrates one of the classic limitations of commercial capacitance extraction tools in accurately extracting coupling capacitances, especially for shorter nets. As we continue technology scaling, we are moving from femtoFarad era to attofarad era and accuracy of smaller capacitances make a difference. It is critical to ensure the basic computational accuracy of RC extraction tools before including process variation effects.

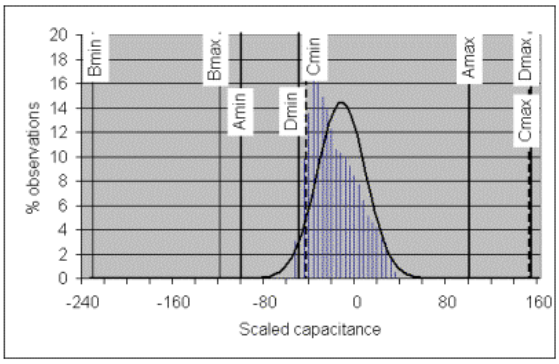

Fig.9 Silicon results for diagonal capacitance structure

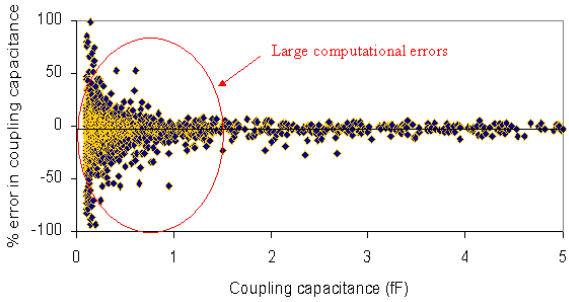

Fig.10 Computational error in extraction of coupling capacitance

Most of the interconnect variations can be approximated as normal distributions, with the exception of via and contact resistance. Via and contact variations can be approximated as lognormal distributions. It is critical to account for correlations among different interconnect levels in statistical RC extraction and analysis.

4. Summary

The importance of intra-cell parameters in addition to inter-cell parameters is illustrated. It is important to establish the basic computational accuracy in RC extraction tools before including systematic and random process variation effects.

5. Acknowledgements

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6. Reference

[1] Nagaraj NS et. al., "Benchmarks for Interconnect Parasitic Resistance and Capacitance" in proc. of ISQED 2003.