Statistical Analysis of SRAM Cell Stability

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Abstract — The impact of process variation on SRAM yield has become a serious concern in scaled technologies. In this paper, we propose a methodology to analyze the stability of an SRAM cell in the presence of random fluctuations in the device parameters. We provide a theoretical framework for characterizing the DC noise margin of a memory cell and develop models for estimating the cell failure probabilities during read and write operations. The proposed models are verified against extensive Monte-Carlo simulations and are shown to match well over the entire range of the distributions well beyond the 3-sigma extremes.

Categories and Subject Descriptors: B.3.3 [**Memory Structures**]: *Performance Analysis and Design Aids*

General Terms: Performance, Design, Reliability

Keywords: SRAM, reliability, stability, noise margin, modeling

I. INTRODUCTION

Manufacturing variations can be classified as *systematic* or *random*. Systematic variations are predictable in nature and depend on deterministic factors such as layout structure and surrounding topological environment [1]-[3]. On the other hand, random variations are unpredictable and are caused by random uncertainties in the fabrication process such as microscopic fluctuations in the number and location of dopant atoms in the channel region [4],[5]. Random variations are harder to characterize and can have a detrimental effect on the yield of critical modules in a design.

Random variations can cause a significant mismatch in neighboring devices and hence are largely responsible for the poor yield of the *static random access memory* (*SRAM*) arrays in scaled technologies [6],[7]. SRAM yield is very important from an economic viewpoint due to the critical and the ubiquitous nature of memory in modern processors and SoCs. Density is a very important metric for memories and hence SRAM cells use the smallest manufacturable device sizes in a given technology. However, the threshold voltage variation due to *random dopant fluctuation* is inversely proportional to gate area [8]-[10]. Due to this dependence, the small sized transistors in a memory cell see a highly pronounced random dopant effect. Moreover, SRAM cells are traditionally designed to ensure that the contents of the cell do not get altered during *read* access while the cell should be able to quickly change its state during the *write* operation. These conflicting read and write requirements are satisfied by balancing the relative strengths of the devices in the design. Such careful design of an SRAM cell provides stable read and write operation, but it also makes the cell vulnerable to the failures caused by random variations in the device strengths.

Due to increased sensitivity of SRAM designs to process variation, failure analysis of a memory cell has become an extremely important exercise. The electrical yield of a cell is typically analyzed through Monte-Carlo simulations which treat the threshold voltage of each device in the cell as an independent random variable. However, the large number of simulations required to obtain full stability coverage makes Monte Carlo simulations computationally prohibitive. Reference [11] illustrates this problem with an example of a 4 MB cache. The authors show that a typical 4 MB cache with *error correcting code (ECC)* cells contains approximately 38 million cells. To ensure that there is at most one failure in this cache, the circuit must operate correctly up to 5.44 sigmas. This sort of fault coverage can only be verified by millions of simulations. Furthermore, Monte-Carlo simulations provide little insight to the designer about optimizing cell yield in subsequent iterations. A modeling based approach, on the other hand, can not only be used to estimate cell failure probability in an efficient manner, but it can also guide cell optimization for yield enhancement.

Analytical modeling of SRAM cell stability is not an entirely new concept. Earlier work in this field focused on characterizing SRAM robustness by modeling *Static Noise Margin (SNM)* of the cross-coupled inverters in a memory cell [12],[13]. More recently, there have been efforts in characterizing cell stability during read and write operations [14],[15]. Most of these works rely on device equations to solve for parameters such as SNM, *read disturbance* and *inverter trip-point*. In this work, we propose a simple and accurate method for modeling read, write and access time failure probabilities of an SRAM cell. First, we provide a theoretical framework for computing DC noise margins and demonstrate that the noise margin is better characterized by computing the loop gain of the cross-coupled inverters in the memory cell. We apply the loop-gain concept to the read stability problem and develop a read stability metric called *read noise margin (RNM)*. We show that RNM has a Gaussian distribution and can be easily modeled as a linear function of the random parameter variations in different transistors in the cell. Similar to Reference [14], we also make an observation that the write failures occur due to timing violations. However, Reference [14] tries the model the non-Gaussian distribution of the *write delay* with a *Non-Central F* distribution. We show that the inverse of write and access delays also follow Gaussian distributions and can be characterized by sensitivity-based linear models. We use these models to analyze different failure mechanisms. In the proposed formulation, the various failure probabilities are directly expressed as functions of the parameter fluctuations in different devices, which allows us to analyze sensitivities of different failure mechanisms to underlying sources of variation and enables efficient computation of joint failure probability of a memory cell. This work focuses on the analysis of conventional 6-T SRAM cell as shown in Figure 1.

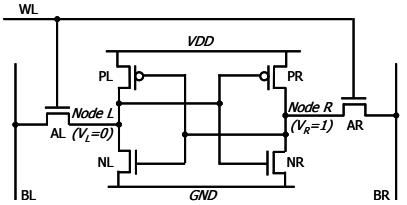

Figure 1: Schematic of a conventional 6-T SRAM cell

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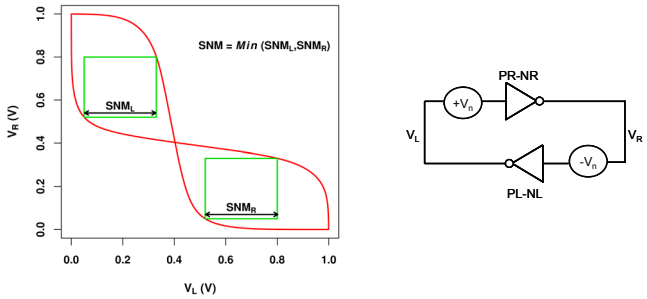


Figure 2: Graphical method of characterizing static noise margin (SNM) of an SRAM cell.

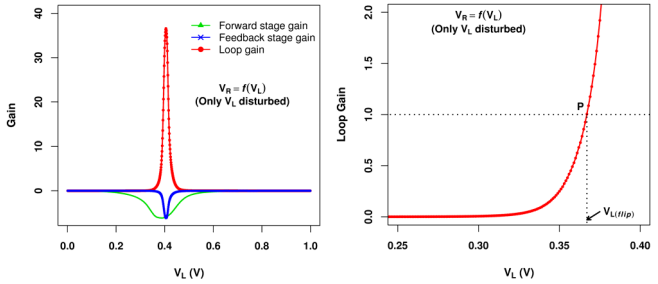


Figure 3: Gain of the positive feedback system formed by the cross-coupled inverters as a function of voltage at node *L*. The figure on the right shows a zoomed in version of the left plot.

II. DC NOISE MARGIN

The noise margin of an SRAM cell is defined as the minimum amount of DC noise required to flip the state of the cell. Traditionally, it is modeled by measuring the side of the longest square that can be inscribed between mirrored DC characteristics of the cross-coupled inverters in a memory cell. However, as shown in Figure 2, this noise metric, called static noise margin (SNM), assumes that the two storage nodes in the cell are subjected to equal and opposite DC noise offsets [12], [13]. Reference [16] shows that the SRAM noise margin can also be characterized by modeling the cross-coupled inverters as a positive feedback loop system. The authors show that the cell is on the verge of instability if its loop gain is unity. In this section, we generalize the loop gain concept and propose a new criterion for quantifying cell stability in the presence of DC noise offsets.

We begin by considering the case of an SRAM cell which stores a value (V_L = 0 and V_R = 1). Let us assume that a DC noise disturbance at node *L* causes its potential V_L to rise above zero. Our objective is to find the minimum DC noise disturbance at node *L* that causes the cell to lose its state. Let us assume that the DC transfer characteristics of the *PR-NR* and the *PL-NL* inverters (as labeled in Figure 1) can be modeled by functions *f* and *g* respectively. For a symmetric cell, the two functions should be identical, but they will differ due to random mismatches in the device characteristics.

$$V_R = f(V_L) \qquad (Inverter\ PR-NR)$$
$$V_L = g(V_R) \qquad (Inverter\ PL-NL) \tag{1}$$

Due to the non-linear nature of the transfer-characteristics *f* and *g*, the gains of the two inverter stages depend on their input voltages. Hence a disturbance at node *L* causes a change in the gain of the *PR-NR* stage. A noise offset at node *L* also changes the potential at node *R* and hence impacts the gain of the feedback stage. The loop gain of the system as a function of node *L* potential can be expressed as:

$$LoopGain(V_L) = \frac{\partial f}{\partial V_L} \cdot \frac{\partial g}{\partial V_R}\bigg|_{V_R = f(V_L)} \tag{2}$$

Figure 3 shows the gains of individual stages and the loop gain as a function of V_L. Figure 3 also shows the value of V_L that causes the loop gain to become unity. This value, labeled as $V_{L(flip)}$ in the figure, represents the minimum DC potential required to flip the contents of a cell. In other words, $V_{L(flip)}$ is the maximum potential that can be tolerated by node *L* without altering its state from zero to one.

Figure 4 shows the significance of $V_{L(flip)}$ in analyzing the noise margin of an SRAM cell. The figure shows the butterfly curves of the cross-coupled inverters as modeled by Equation 1. The figure also shows the shifted DC transfer characteristics $V_L = g(V_R) + Noise_L$ of

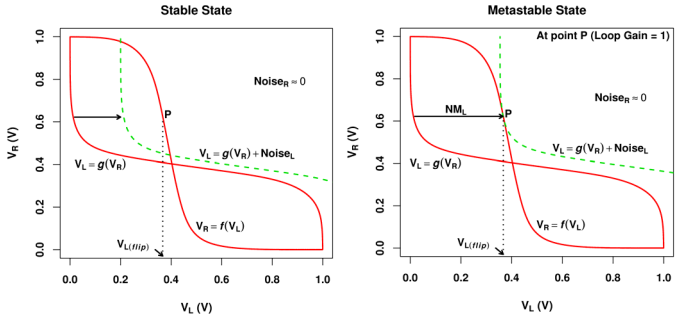


Figure 4: Stable and metastable states of an SRAM cell in the presence of a positive DC noise offset ($Noise_L$) on node *L*.

the feedback inverter due to a positive DC noise offset at the node *L* ($Noise_L$). For a small noise offset, the cell maintains its state because it has a stable operating point in the vicinity of the initial state (V_L = 0 and V_R = 1). However, as the noise is increased, the shifted curve moves far enough such that it intersects the forward inverter characteristics at only one point (as labeled *P* in Figure 4). If the noise is increased beyond this point, then the cell will lose its state because the two DC characteristics will not have a stable intersection point required to maintain the initial state. The state of the cell, when the two curves barely touch each other and the cell is on the verge of instability, is defined as *metastable* state. Interestingly, the potential at node *L* in the metastable state is $V_{L(flip)}$. Based on this observation, we define the noise margin of the cell as:

$$NM_L = V_{L(flip)} - g\left(f(V_{L(flip)})\right) \tag{3}$$

Next, we consider the case when the cell still stores a value (V_L = 0 and V_R = 1) but a negative DC noise disturbance is applied at node *R*. The negative disturbance causes node *R*'s potential to fall below one. Similar to Equation 2, the loop gain of the system as a function of node *R* potential (V_R) can be expressed as:

$$LoopGain(V_R) = \frac{\partial f}{\partial V_L}\bigg|_{V_L = g(V_R)} \cdot \frac{\partial g}{\partial V_R} \tag{4}$$

Now we can compute the potential V_R that causes the loop gain to become unity ($V_{R(flip)}$) by solving the above equation. Figure 5 shows the loop gain as a function of V_R. Figure 5 also shows the significance of $V_{R(flip)}$ on the butterfly curves. As shown in the figure, a negative offset at node *R* shifts the DC transfer characteristics of the forward inverter vertically by $Noise_R$. Similar to Equation 3, the noise margin of the cell from this side can be calculated as:

$$NM_R = f\left(g(V_{R(flip)})\right) - V_{R(flip)} \tag{5}$$

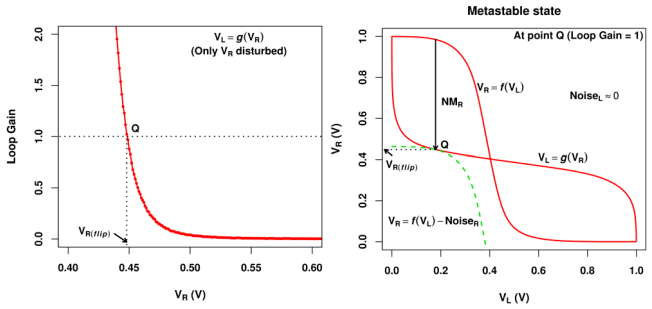


Figure 5: Loop-gain of the cross-coupled inverters as a function of the voltage at node *R*. The figure on the right shows the butterfly curves in the metastable state due to negative DC noise offset ($Noise_R$) on node *R*.

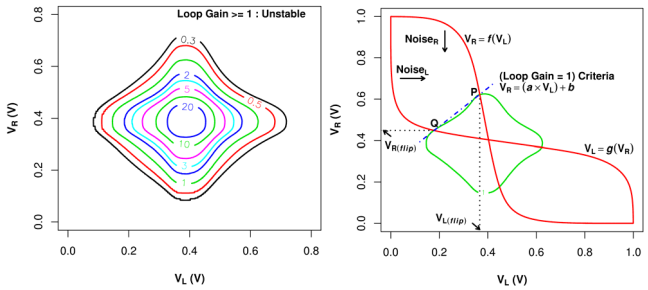


Figure 6: Loop-gain contours as a function of V_L and V_R. The unity loop-gain contour can be used to derive SRAM stability criteria in the presence of dual-sided disturbance.

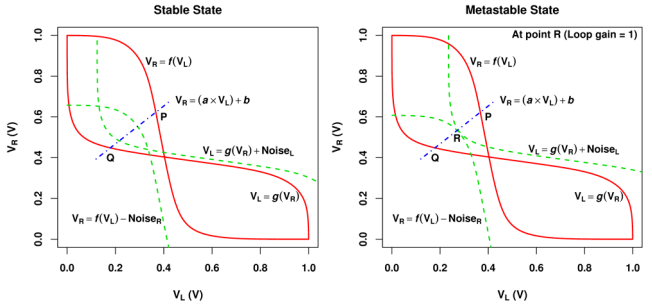


Figure 7: Stable and metastable states of an SRAM cell when a positive DC noise offset ($Noise_L$) is applied on node *L* and negative noise ($Noise_R$) is applied on node *R*.

NM_L models the maximum positive noise a cell can tolerate at its zero node without losing its contents while NM_R represents the maximum tolerable negative noise offset at the node storing one. Given NM_L and NM_R, the noise margin of a cell can be expressed as:

$$NM = Min(NM_L, NM_R) \tag{6}$$

The above noise margin metric is different from SNM because it characterizes a cell's stability under the assumption that only side of the cell is disturbed by external noise. SNM, on the other hand, is a measure of noise margin when simultaneous positive and negative DC noise offsets are present at the two nodes of the cell. SRAM failures due to *read noise* and also due to *alpha particle* strikes usually occur due to one-sided disturbances. Therefore, the noise margin model of Equation 6 is more useful in checking cell stability in the presence of DC noise offsets. However, for the sake of completeness, we extend the above loop-gain concept to model cell stability in the presence of noise disturbs at both ends of a cell.

Once again we consider the case of an SRAM cell storing a value ($V_L = 0$ and $V_R = 1$). However, this time we assume that both nodes in the cell are subjected to external disturbances. When V_L and V_R can take any possible values, the loop gain of the system as a function of node *L* and node *R* potentials can be expressed as:

$$LoopGain(V_L, V_R) = \frac{\partial f}{\partial V_L} \cdot \frac{\partial g}{\partial V_R} \tag{7}$$

Figure 6 shows the loop-gain contours as obtained by solving the above equation. Figure 6 also shows the (loop-gain = 1) contour plotted over the butterfly curves. The points *P* and *Q*, as labeled in the figure are same as the point *P* ($V_{L(flip)}$) and the point *Q* ($V_{R(flip)}$) shown in the Figures 4 and 5, respectively. For an initial state of $V_L = 0$ and $V_R = 1$, the relevant side of the unity loop-gain contour can be approximated with a straight line.

$$V_R = (a \times V_L) + b \tag{8}$$

Here, coefficients *a* and *b* can be easily calculated using $V_{L(flip)}$ and $V_{R(flip)}$ values

$$a = \frac{f(V_{L(flip)}) - V_{R(flip)}}{V_{L(flip)} - g(V_{R(flip)})} \qquad b = \frac{V_{L(flip)} V_{R(flip)} - f(V_{L(flip)}) g(V_{R(flip)})}{V_{L(flip)} - g(V_{R(flip)})} \tag{9}$$

Now, if we assume that a positive noise ($Noise_L$) is applied at the node *L* (storing zero) and a negative DC offset ($Noise_R$) occurs at node *R* (storing one), then the SRAM stability criterion in the presence of double-sided noise can be formulated by checking the linearized unity loop-gain constraint from Equation 8. We first solve for the node *L* potential ($V_{L(gain)}$) by computing the intersection point of $V_L = g(V_R) + Noise_L$ curve with the unity loop-gain constraint $V_R = (a \times V_L) + b$. The stability criteria can then be expressed as:

Cell is unstable if:

$$(a \times V_{L(gain)}) + b > f(V_{L(gain)}) - Noise_R \tag{10}$$

Figure 7 demonstrates the stable and the metastable state of a cell in the presence of double-sided noise. The figure shows that noise offsets at nodes *L* and *R* result in a horizontal and vertical shift in the transfer characteristics of the two inverters. In the metastable state, the combination of $Noise_L$ and $Noise_R$ shifts the butterfly curves such that they intersect at only one point. In this state, the cell is on the verge of instability as a small amount of additional noise will change the contents of the cell.

III. READ STABILITY FAILURES

An SRAM cell is most prone to failure during read operation. A read operation in SRAM typically involves precharging the bitlines followed by reading the contents of the cell through the access transistors. When the access transistors are turned on, one of the precharged bitlines discharges through the access device and the inverter pull-down transistor. For example in Figure 1, during a read access, the bitline *BL* will discharge through the access device *AL* and the pull-down device *NL* to read a zero at node *L*. This method of reading cell contents exposes the internal storage node *L* to the disturbance caused by the resistive voltage division between the access and the pull down devices. Typically, this disturbance is minimized by making the pull-down device much stronger than the access transistor. However, random variations in the threshold voltages and therefore the strengths of various devices in an SRAM cell can cause the read operation to flip the contents of the cell. These failures are defined as *read stability failures*.

In the previous section, we discussed the stability of a cell in the presence of a positive disturbance at the node storing zero. Conceptually, read stability failures can be analyzed in a similar manner. The DC noise analysis is valid because the read access time is usually larger than the time required to flip the state of the cross-coupled inverters. When the wordline (WL) is turned on, a noise voltage is immediately developed at the internal node of the cell. The WL stays high for duration long enough for the bitline to discharge by a specific value. During this period, if the DC noise voltage at the internal node is large enough to flip the contents of the cell, the cell loses its state resulting in the read stability failure.

The read stability of a cell can be analyzed by computing the loop gain of the system in read mode. The forward and the feedback characteristics are computed by including access devices along with the inverters as shown in Figure 8. Let us assume that the transfer characteristics of the *PR-NR-AR* and the *PL-NL-AL* stages can be modeled by functions f^R and g^R respectively. Similar to Equation 2, the loop gain of the system as a function of node *L* potential (V_L) can be expressed as:

$$LoopGain(V_L) = \frac{\partial f^R}{\partial V_L} \cdot \frac{\partial g^R}{\partial V_R}\bigg|_{V_R = f^R(V_L)} \tag{11}$$

The value of V_L that causes the loop-gain to become unity, $V^R_{L(flip)}$ can be computed by solving the above loop-gain equation. The read noise margin (RNM) can then be expressed as:

$$RNM = V^{Rd}_{L(flip)} - g^{Rd}\left(f^{Rd}\left(V^{Rd}_{L(flip)}\right)\right) \tag{12}$$

The concept of read noise margin (RNM) is demonstrated in the right half of Figure 8. RNM is a useful metric in analyzing read stability failures. A positive value of RNM represents a stable read operation while a zero or negative value of RNM signifies that the read operation will cause the cell to lose its state resulting in the read stability failure.

We characterize the impact of random variations on RNM through SPICE-based Monte-Carlo simulations in an industrial 65 nm technology. The simulations model the threshold voltage of each device in the cell as an independent random variable. The threshold tolerances for different devices in the cell are chosen from the technology specifications and include the dependence of sigma-V_T on device width. Figure 9 shows the histogram and the quantile-quantile (Q-Q) plot of RNM. The observed Gaussian nature of RNM indicates that it can be well modeled as a simple linear model.

$$RNM = RNM_{nom} + k_R^{AL}\Delta V_T^{AL} + k_R^{NL}\Delta V_T^{NL} + k_R^{PL}\Delta V_T^{PL} + k_R^{AR}\Delta V_T^{AR} + k_R^{PR}\Delta V_T^{PR} + k_R^{NR}\Delta V_T^{NR} \tag{13}$$

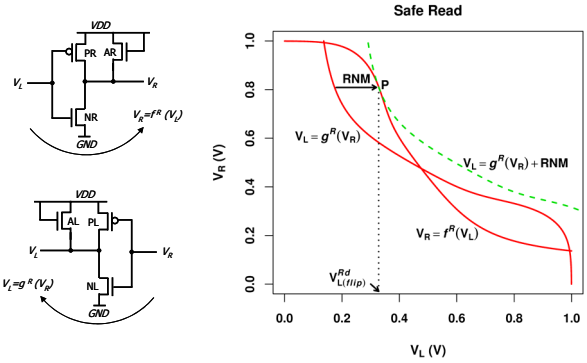


Figure 8: The forward and the feedback DC transfer characteristics of a memory cell in the read state. The read stability is characterized by measuring RNM.

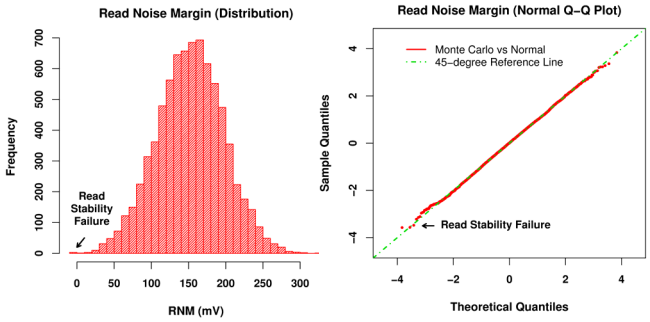


Figure 9: The distribution of read noise margin as obtained from Monte-Carlo simulations. The normal Q-Q plot shows the Gaussian nature of the distribution.

Here, variation in the threshold voltage of each device in a 6-T cell is modeled as an independent ΔV_T. The above model can be easily characterized by evaluating the nominal value of RNM (RNM_{nom}) and its sensitivities to different threshold variations. With each V_T being an independent random variable, the mean (μ_{RNM}=RNM_{nom}) and the standard deviation (σ_{RNM}) of the RNM distribution can also be easily calculated from Equation 13. The read stability failure probability (P_R) can then be expressed as:

$$P_R = Prob(RNM < 0) = \Phi\left(\frac{-RNM_{nom}}{\sigma_{RNM}}\right) \tag{14}$$

Here Φ is the standard normal cumulative density function.

IV. WRITE FAILURES

Write failures are caused when a SRAM cell fails to write a desired state in a cell during the write operation. The write operation in an SRAM cell is performed by setting the bitlines to the desired values and enabling the access transistors to drive the internal nodes of the cell. For example in Figure 1, a zero is written at the node *R* by driving bitline *BR* low and setting the wordline high. The resistive voltage division between the pull-up device *PR* and the access transistor *AR* pulls the internal node *R* to zero causing the cell to change its state. Typically, a stronger write capability is achieved by making the pull-up device weaker than the access transistor.

For a successful write, node *R* must be pulled low within the duration when the wordline is high. The write failure probability (P_W) can therefore be expressed as

$$P_W = Prob(T_W < T^W_{WL}) \tag{15}$$

Here T_W is the time required to pull the node (storing one) low and T^W_{WL} represents the wordline duration for the write operation. The condition in Equation 15 is same as the write failure criterion proposed in [14]. Figure 10 shows the histogram of T_W as obtained from 100,000 Monte-Carlo simulations. It can be seen from the figure that the T_W distribution has a tail and cannot be approximated with a normal distribution. Write failures usually occur in the tail region and hence modeling that region well is critical for an accurate analysis of the write failure probability. Reference [14] suggests modeling the tail with a *non-central F* distribution. To first order, the delay can be expressed using the alpha-power law model [17].

$$\left(D \cong \frac{CV_{DD}}{I}\right) \propto \frac{CV_{DD}}{(V_{DD} - V_T)^{\alpha}} \tag{16}$$

The long tail observed in the T_W distribution can be explained by the inverse dependence of delay on the $(V_{DD} - V_T)^{\alpha}$ term. If we apply a transformation T on delay D defined as $T : D \rightarrow D^{-(1/\alpha)}$, then the transformed value of delay becomes a linear function of $(V_{DD}$-$V_T)$.

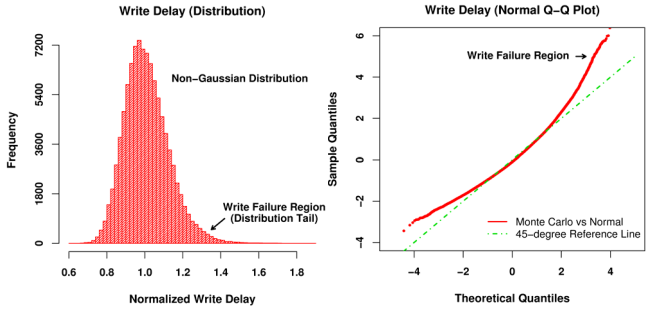


Figure 10: The distribution of write delay as obtained from Monte-Carlo simulations. The normal Q-Q plot shows the non-Gaussian nature of the distribution.

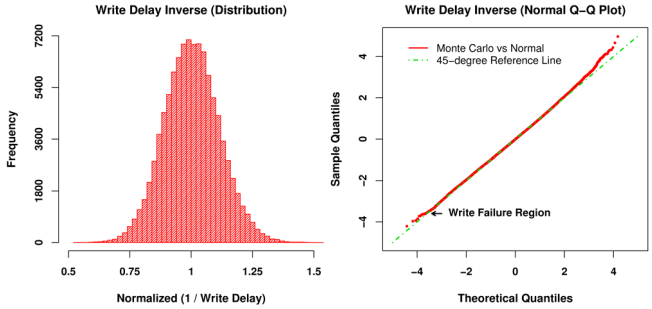


Figure 11: The distribution of write delay inverse. The normal Q-Q plot shows the Gaussian nature of the distribution.

The write failure analysis can now be performed in the transformed domain with an advantage that the timing variable in the write stability constraint varies linearly with the threshold voltages. For example, for exponent α=1, a simple transformation ($T : D \rightarrow 1/D$) is sufficient to achieve linearity. In this work, we use this inverse transformation but other transformations with non-unity values of α can also be used in a similar manner.

Figure 11 shows the distribution of $(1/T_W)$ and compares it to a normal distribution. The figure shows that $(1/T_W)$ can be approximated with a normal distribution. The observed Gaussian nature of the inverse of write delay indicates that it can be modeled with a simple linear model:

$$\frac{1}{T_W} = \left(\frac{1}{T_W}\right)_{nom} + k_W^{AL}\Delta V_T^{AL} + k_W^{NL}\Delta V_T^{NL} + k_W^{PL}\Delta V_T^{PL} + k_W^{AR}\Delta V_T^{AR} + k_W^{PR}\Delta V_T^{PR} + k_W^{NR}\Delta V_T^{NR} \quad (17)$$

The above model can be characterized by evaluating the nominal value and the sensitivities of $(1/T_W)$ with respect to the threshold voltages. The write failure probability (P_W) can now be expressed and computed in the transformed domain.

$$P_W = Prob\left(\frac{1}{T_W} < \frac{1}{T_{WL}^W}\right) = \Phi\left(\frac{\frac{1}{T_{WL}^W} - \left(\frac{1}{T_W}\right)_{nom}}{\sigma_W}\right) \quad (18)$$

Here σ_W represents the standard deviation of $(1/T_W)$ and can be calculated from Equation 17.

V. READ ACCESS FAILURES

During the read operation, the wordline is activated for a limited duration as determined by the cell access time. Read access failures occur if the contents of the cell cannot be read within this duration. In

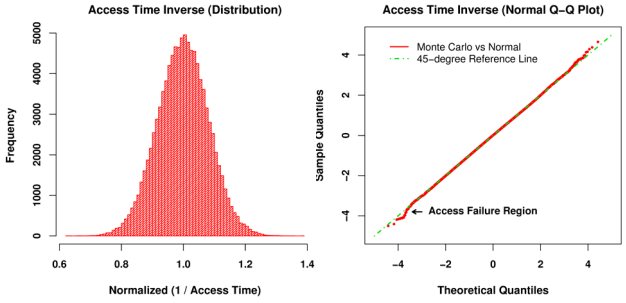


Figure 12: The distribution of access time inverse as obtained from Monte-Carlo simulations. The normal Q-Q plot shows the Gaussian nature of the distribution.

sense amplifier based memory architectures, the contents of a cell are read by sensing the voltage differential between bitlines. The read operation is successful if a precharged bitline discharges by a value large enough to trigger the sense amplifier within the wordline duration. Read access fails are timing failures and can be modeled like write failures. Figure 12 shows that the inverse of access time $(1/T_A)$ can be approximated with a normal distribution. The inverse of access time can therefore be modeled as:

$$\frac{1}{T_A} = \left(\frac{1}{T_A}\right)_{nom} + k_A^{AL}\Delta V_T^{AL} + k_A^{NL}\Delta V_T^{NL} + k_A^{PL}\Delta V_T^{PL} + k_A^{AR}\Delta V_T^{AR} + k_A^{PR}\Delta V_T^{PR} + k_A^{NR}\Delta V_T^{NR} \quad (19)$$

Here T_A represents the access time of a cell. Similar to Equation 18, the access failure probability (P_A) can be easily calculated.

$$P_A = Prob\left(\frac{1}{T_A} < \frac{1}{T_{WL}^A}\right) = \Phi\left(\frac{\frac{1}{T_{WL}^A} - \left(\frac{1}{T_A}\right)_{nom}}{\sigma_A}\right) \quad (20)$$

Here σ_A represents the standard deviation of $(1/T_A)$ and T_{WL}^A represents the wordline duration for the read operation.

VI. JOINT FAILURE PROBABILITY

The stability criteria proposed in Sections III, IV and V express each failure probability as a linear function of the independent sources of variation. The joint failure probability of an SRAM cell can be computed by combining the different criteria in a multivariate normal distribution. For read stability, write, and read access failures, the trivariate density function can be expressed as:

$$f_X = \frac{1}{(2\pi)^{3/2}|\Sigma|^{1/2}} \exp\left(-\frac{1}{2}(x-\mu)^T \Sigma^{-1}(x-\mu)\right) \quad (21)$$

Here, X represents a vector consisting of *RNM*, $(1/T_W)$ and $(1/T_A)$ as its elements, μ is the corresponding mean vector and Σ is the *3x3* covariance matrix with its determinant expressed as $|\Sigma|$. The joint failure probability can be computed by evaluating the corresponding cumulative density function at the point $(0, (1/T_{WL}^W), (1/T_{WL}^A))$.

VII. EXPERIMENTAL RESULTS

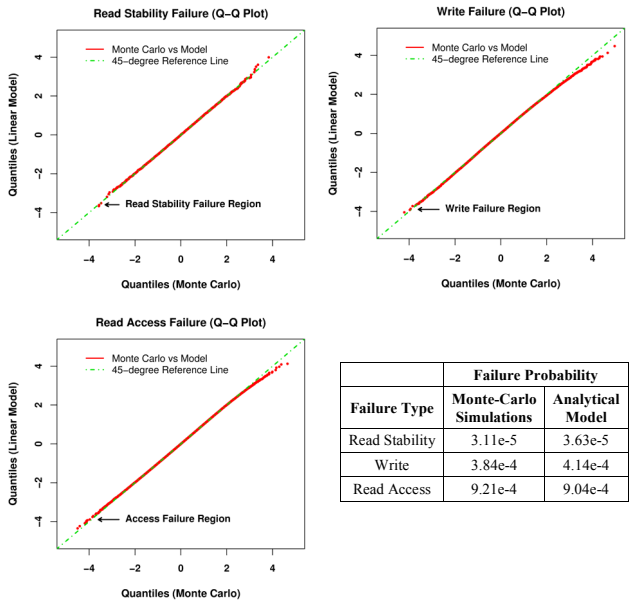
The models proposed in the paper were verified on an SRAM design in an industrial 65nm, 1V, SOI technology [18]. In our simulations, we modeled the V_T of each device in the cell as an independent random variable. The threshold tolerances were chosen from the technology specifications and include the dependence of sigma-V_T on device width. The models were characterized by computing the nominal values and the sensitivities of the read noise

margin (Equation 13), the inverse of write delay (Equation 17), and the inverse of access time (Equation 19) with respect to V_T variations in all six transistors. We computed the sensitivities by varying the V_T of one transistor at a time while keeping the threshold voltages of other devices in the cell fixed at their nominal values. Alternatively, the sensitivities can also be computed by performing linear regression on a small number of Monte-Carlo simulations. The number of simulations required to generate linear models is significantly smaller than the Monte-Carlo simulations needed to verify the stability of an SRAM design. Table I shows the computed sensitivities when attempting to read a zero at node *L* or write a zero at node *R*. The sensitivities represent the relative importance of each transistor in analyzing the three failure mechanisms discussed in the paper. The table shows that while it may be possible to analyze the read access failures by considering only the corresponding access and the pull-down device, both the read stability and the write failures must consider the V_T variations in all six devices for accurate prediction of the failure probabilities.

The proposed models were verified through SPICE based Monte-Carlo simulations. To ensure that the cell stability criteria are checked at larger than 3-sigma corners, we performed 500,000 Monte-Carlo simulations. The Q-Q plots shown in Figure 13 demonstrate that the models match well with the SPICE simulations. Figure 13 also shows a comparison of the failure probabilities. The low failure probabilities of a SRAM cell are hard to verify due to computationally prohibitive number of Monte-Carlo simulations. However, the table shows that even at the very low probabilities, the models track the Monte-Carlo results very well.

Table I: Sensitivities of the stability metrics with respect to the V_T variations in a 6-T SRAM cell. All nominal values are normalized to one and the sensitivities are expressed in V^{-1} units.

	AL	NL	PL	AR	NR	PR
RNM	1.9	-2.13	0.12	-0.4	5.04	-1.39
$1/T_W$	-0.55	0.64	-0.19	-1.31	-0.77	0.70
$1/T_A$	-1.27	-0.26	0.001	0.003	0.06	0.001



	Failure Probability	
Failure Type	**Monte-Carlo Simulations**	**Analytical Model**
Read Stability	3.11e-5	3.63e-5
Write	3.84e-4	4.14e-4
Read Access	9.21e-4	9.04e-4

Figure 13: A comparison of the proposed cell failure models against Monte Carlo simulations.

VIII. CONCLUSIONS

We proposed a framework to model the impact of random variations on SRAM yield. The paper developed several new criteria for characterizing the stability of a SRAM cell in the presence of external DC noise, and also during read and write operations. The proposed models provide a measure of the robustness of a cell and enable efficient estimation of the cell failure probability. The methods discussed in this work can be very useful in optimizing a memory cell to achieve better stability and higher yield.

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