Low Voltage Swing Logic Circuits for a Pentium® 4 Processor Integer Core

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Abstract
The Pentium® 4 processor architecture uses a 2x frequency core clock[1] to implement low latency integer ops. Low Voltage Swing logic circuits implemented in 90nm technology[2] meet the frequency demands of a third generation integer-core design.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles - *Advanced technologies*, *Microprocessors and microcomputers*, *VLSI (very large scale integration.*

General Terms
Performance, Design, Verification

Keywords
Pentium® 4 processor, integer core, sense-amp, adder, rotator, microprocessor, Low Voltage Swing, LVS

1. INTRODUCTION
Microprocessor performance can be defined as the product of latency and parallelism. Since parallelism has been well exploited in previous microprocessor generations, integer performance in the Pentium® 4 processor architecture is achieved using ultra low latency integer operands. This is accomplished by running the integer core at twice the core frequency of the microprocessor. At today's clock rates, this operating frequency is in-of-itself notable. For example a 3.4 GHz processor would have the integer logic functioning at 6.8 GHz. Such a frequency target is on the low end of 90nm technology capabilities - that is at the beginning of process life. End of life process technology frequency expectations are far higher. Described in this paper is the implementation of the newest Pentium 4 microprocessor integer logic core using Low Voltage Swing (i.e.: differential small signal) logic. This circuit topology, referred to as "LVS", is designed explicitly to take advantage of the frequency headroom enabled by 90nm process technology. This paper orginally published as part of the ISSCC 2004 conference [3] will cover the over-all circuit topology, the pre-silicon verification approach, and a pair of implementation examples. Finally, post-silicon data will be shown.

2. CIRCUIT TOPOLOGY
Figure 1 shows the chosen LVS circuit topology [6]. Inverters drive complementary data into a dual rail N-channel diffusion connected network (DCN). The DCN is reset low and equalized.

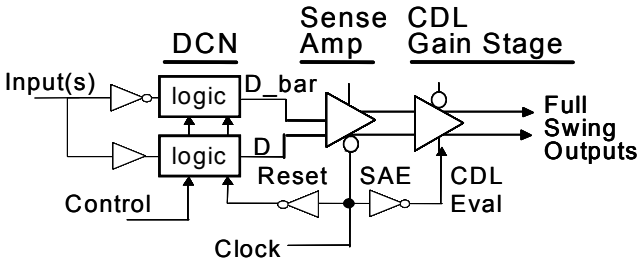

Figure 1. Basic Circuit Topology Used

During small signal development, one side evaluates high with transistors operating primarily in the linear region. The higher N channel linear region current compared to P makes this the system of choice. The DCN gates are driven by either static or domino circuits. The first logic level control is always qualified with DCN reset, to avoid contention.

The DCN ends in a high-speed low-gain ratio'd P-type sense amplifier feeding a final high-gain stage implemented as a cross-coupled domino logic (CDL) gate (Figure 2). Together these stages amplify 10% VCC differential (average) to full rail outputs.

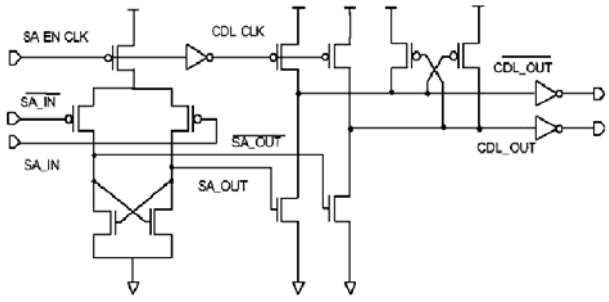

Figure 2. Sense-Amp and CDL Pair

The DCN logic function signal development is allocated less than 35% of a 2x clock phase, equivalent to 2 nominal inverter delays; during this time it implements up to 6 effective logic stages. The

gain stages cost less than two stage delays and a 7th logic stage can be implemented in the CDL itself.

Figure 3 shows the timing sequence. The DCN reset killing differential immediately after the sense amp trigger is the only functional race.

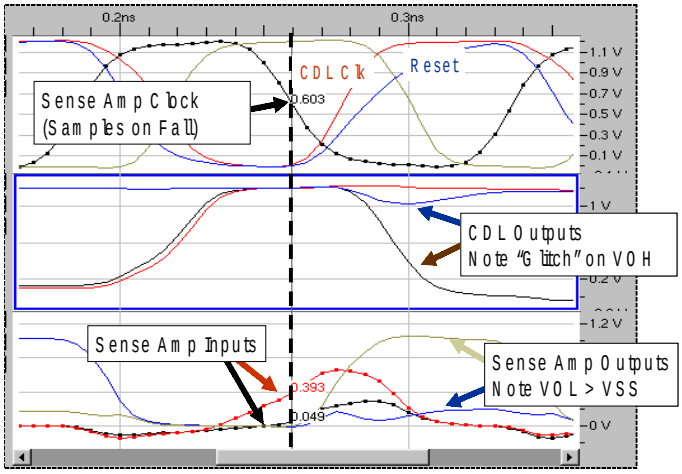

Figure 3. Timing Sequence

3. PRE-SI VERIFICATION

As shown in Figure 3 above, the non-zero offset level on the sense amp '0 output induces a glitch on the non-switching CDL output mitigated by the CDL's cross-coupled P-keepers. Below a minimum input differential, the glitch induces a domino false-discharge failure on the CDL output. This glitch magnitude is a criterion used by an in-house LVS Timing and Noise Tool (LVSTNT) to calculate the circuit setup time. A second criteria is a minimum input differential, typically 8-10% of supply, needed to overcome noise, sense amp V-offset and process variation.

The LVSTNT tool uses a patented pruning algorithm[4] to exhaustively search all circuit paths constrained by logic equations embedded as schematic properties. RTL codes equivalent equations that are formally verified against the schematic versions. As illustration, the rotator/shifter described later exceeds 42,000 paths for verification. Including all differential noise scenarios increases the path count 10X.

Matching analog layout rules are required in three dimensions up to the layer above the last metal used for small signal interconnect. An in-house analog layout rule checker was built to enforce adherence to matching rules. In this way, essentially random logic is proven, by post layout extraction tools, to have minimal differential noise.

4. IMPLEMENTATION EXAMPLES

The integer core has four main LVS structures. The L0 data cache alignment mux uses the core clock to produce 32:1 data alignment in less than one phase of a 2x frequency clock. There are two ALUs. ALU0 has a 32 bit adder and Boolean logic functions. ALU1 has the same 32 bit adder and has a fast 32 bit shifter/rotator [5]. Low latency integer shifts and rotates were enabled by LVS technology and are new to the architecture. The fourth structure is the address generation unit. The pipeline of this block cascades back to back LVS circuits thru four phases of the 2x frequency clock. There are several LVS adders and carry chains in the block all of which share a common topology with the ALU adder. These four LVS structures make up over 20% of the integer core being described. The scope of this presentation will allow us discuss only briefly details of two structures – the LVS alignment mux and the LVS 16 bit adder.

4.1 32:1 Data Alignment Mux

LVS technology enables a non-traditional implementation of the L0 Data Alignment Mux shown in Figure 4. The circuit topology includes 128 individual 32 to 1 dual rail muxes. This function is accomplished in a single stage of logic by distributing the 'mux' node over the height of the L0. The large capacitance of the mux node and the large resistance of the distributed network results in small signal that is amplified to rail by the two gain stages described previously. Duplicating and distributing the mux reset and select logic along the height of the block ensure signal integrity. This single stage Alignment Mux operating in less than one 2x clock phase reduced the critical load pipeline in the integer core.

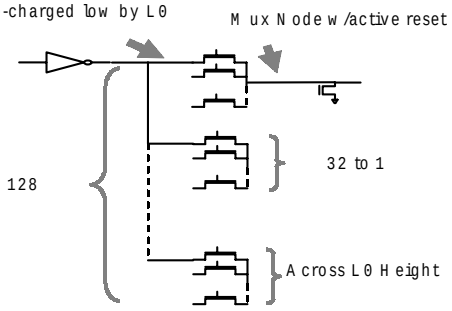

Figure 4. Single Stage L0 Data Alignment

4.2 Adders

The LVS carry chain for a 16-bit adder is shown in Figure 5. It is built upon 16-cascaded LVS PGK cells "0-F" with carry-skip pass-gates "S0-S9" positioned such that any carry propagation path traverses through no more than 6 series devices. The LVS cells that make up the LVS carry-chain are basic pass gate logic configurations with generate and kill transistors at each bit position.

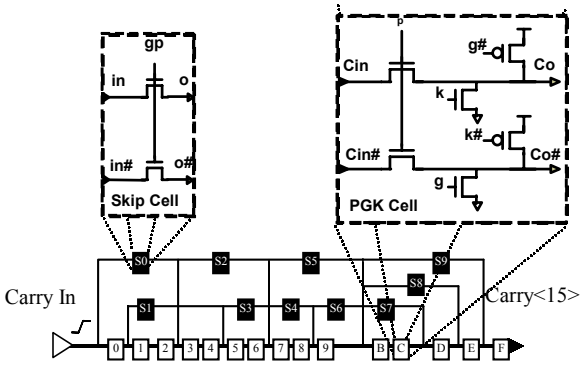

Figure 5. 16-bit Adder Carry Skip Chain

The LVS XOR gates hookup to each polarity of the carry[n] nodes along the chain to produce the sum [n+1] result. The typical critical path begins with the turning ON of the "s0" skip pass-gate that allows the "Cin" to charge up the reset-low carry-chain and develop differential at the inputs of 17 PMOS sense-amplifiers that sense the 16 sum and final carry results along this structure.

The carry propagation RC delays for a 32-bit LVS adder are too slow to sustain the frequency targets of the integer core. For this reason all IA32 ALU and AGU adders are built upon a common 16-bit LVS adder core. The 32-bit ALU for example employs 3 of these cores in a carry-select configuration. This common core is allocated only one 2x clock phase to compute a 16-bit add. Thus the add portion of the AGU and ALU operations on Si are operating at 2x the quoted frequency of the integer core. Fast P-Interrupt Ratio'd NOR gates are employed to generate the controls for the carry-skip pass-gates that initiate the carry propagation critical paths through the LVS adder.

5. RESULTS

The described LVS integer core has been fabricated on 90nm technology. The processor includes test hardware that isolates the integer core on Si. Figure 6 shows the isolated core's voltage vs. frequency schmoo running all tests.

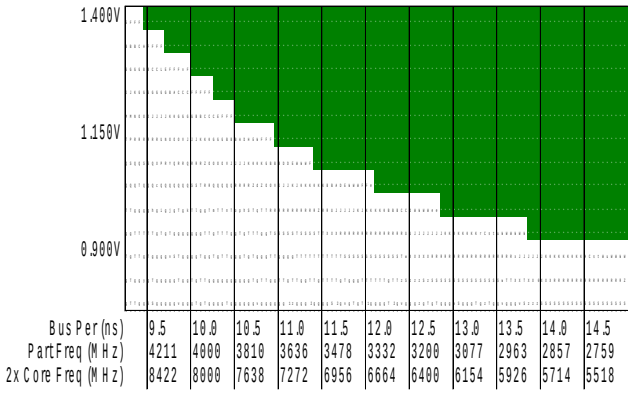

Figure 6. Post Silicon Integer Core Data

The LVS integer core exceeds 8.0 GHz on initial Si at 70C junction and 1.30V pin. The core is expected to reach >10GHz with process & post Si optimizations. The integer core contains over 6.8 millon non-array physical transistors, exceeding the original Pentium® Pro microprocessor. The core area is 14070.8 a die photo of the chip is shown in Figure 7.

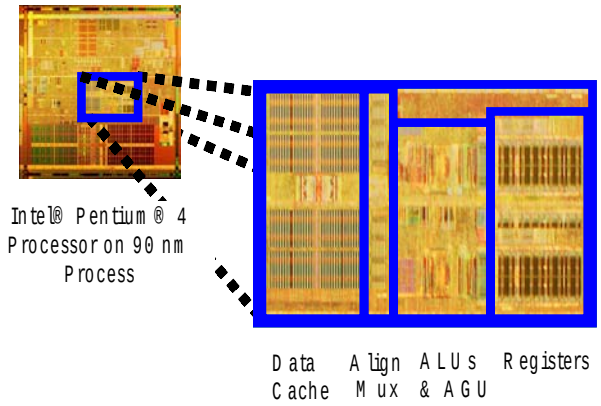

Figure 7. Die Photo with Integer Core Magnified

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