Modeling and Minimization of PMOS NBTI Effect for Robust Nanometer Design

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ABSTRACT

Negative bias temperature instability (NBTI) has become the dominant reliability concern for nanoscale PMOS transistors. In this paper, a predictive model is developed for the degradation of NBTI in both static and dynamic operations. Model scalability and generality are comprehensively verified with experimental data over a wide range of process and bias conditions. By implementing the new model into SPICE for an industrial 90nm technology, key insights are obtained for the development of robust design solutions: (1) the most effective techniques to mitigate the NBTI degradation are V_{DD} tuning, PMOS sizing, and reducing the duty cycle; (2) an optimal V_{DD} exists to minimize the degradation of circuit performance; (3) tuning gate length or the switching frequency has little impact on the NBTI effect; (4) a new switching scenario is identified for worst case timing analysis during NBTI stress.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids– *performance analysis and design aids*; B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids.

General Terms

Performance, Design, Reliability, Experimentation.

Keywords: NBTI, Reliability, Threshold Voltage, Temperature, Performance Degradation, Variability.

1. INTRODUCTION

The 2005 ITRS projects the scaling of CMOS technology to 32nm and 22nm nodes in ten years, with equivalent oxide thickness as thin as 5Å [1]. In the nanometer regime, physical factors that previously had little impact on circuit performance are now becoming increasingly significant. This is especially true for variability and reliability concerns that require careful attention during the design stage. In particular, there has been a recent escalation in interest on the reliability impact of PMOS negative bias temperature instability (NBTI) [2-5]. NBTI occurs under negative gate voltage (e.g., $V_{gs}= -V_{DD}$) and is measured as an increase in the magnitude of threshold voltage. It mostly affects the PMOS transistor and degrades the device drive current, circuit speed, noise margin, and the matching property. Indeed, as gate oxide gets thinner than 4nm, the threshold voltage change caused by NBTI for the PMOS transistor has become the dominant factor to limit the life time, which is much shorter than that defined by hot-carrier induced degradation (HCI) of the NMOS transistor [2]. Furthermore, different from HCI that occurs only during dynamic switching, NBTI is caused during static stress on the oxide even without current flow. Consequently, the situation of the NBTI degradation is exacerbated in the nanoscale design as advanced digital systems tend to have longer standby time for lower power consumption. As the NBTI effect becomes more severe with continuous scaling, it is critical to understand, simulate, and minimize the impact of NBTI in the early design stage to ensure the reliable operation of circuits for a desired period of time.

To date, research works on NBTI have been active only within the communities of device and reliability physics. Partly due to its complexity and emerging status, design knowledge and CAD tools for managing the NBTI degradation are not widely available [1, 6]. Leading industrial companies do develop their own models and tools to handle this effect. These tools, however, are usually proprietary and empirical to a specific technology. In this case, a more general and SPICE compatible model that can accurately predict the degradation would be very useful. This predictive model will further serve as a cornerstone to circuit design and optimization in the presence of the NBTI degradation.

Such a *predictive NBTI model* is presented in this work. It is based on the physical understanding and published experimental data for both DC and AC operations. The dependence of NBTI on key process (e.g., L, V_{th}, T_{ox}) and design parameters (e.g., V_{DD}, V_{ds}, duty cycle, etc.) are captured in this model framework. Representative model coefficients are extracted from silicon data across a wide range of process and stress conditions. Comparisons between published data and model predictions verify the generality and scalability of this approach. Details of the model development are presented in Section 2. Using this scalable model, the increasing impact of NBTI on transistor performance is extrapolated towards the 32 nm node (Section 2.3).

The compact model of NBTI bridges the gap between the technological community and CAD tool developers. The new model can be conveniently customized and implemented into the circuit simulation environment, such as SPICE, to perform design explorations and extract *design guidelines*. As the first step towards robust design under NBTI, Section 3 investigates the sensitivity and tradeoffs of various design techniques to minimize the degradation of circuit performance. Examples include the simulation studies on 90nm NAND and NOR gates. It is identified that V_{DD} tuning and PMOS sizing are the most effective techniques to mitigate the impact of NBTI (Sections 3.2 and 3.3). In particular, an optimal V_{DD} exists for the minimum performance change during static stress. In the case of a PMOS stack (e.g., a NOR gate), a new switching pattern for worst case timing analysis is revealed due to NBTI (Section 3.3.3). At the system level, the NBTI effect can be reduced by tuning the duty cycle; its effectiveness, however, decreases at higher temperature (Section 3.3.4).

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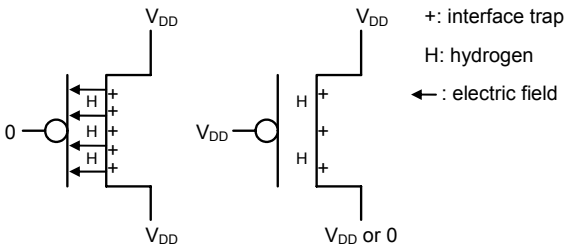


Figure 1. Two phases of PMOS NBTI (V_b=V_{DD}).

Overall, the *predictive model* of PMOS NBTI effect enables efficient design examinations within the standard CAD environment. Based on the newly developed model, this work identifies important *design guidelines* that will lead to further development of design solutions and optimization strategies, in order to improve nanoscale circuit reliability.

2. MODEL DEVELOPMENT

The instability of PMOS transistor parameters, i.e., threshold voltage (V_{th}), saturation current (I_{on}), etc., under negative bias and high temperature has been known since the 1970's [7]. It is the recent aggressive scaling of CMOS technology that makes NBTI as one of the foremost reliability concerns in nanoscale design [1-2]. Although there is no single physical mechanism that is comprehensive enough to explain all the behaviors, it is arguably believed that NBTI is caused by broken Si-H bonds, which are induced by positive holes from the channel. Then H, in a neutral form, diffuses away; positive interface traps (N_{it}) (i.e., from Si^+) are left, which cause the increase of V_{th} [8-10]:

$$\Delta V_{th} = qN_{it}/C_{ox}, \text{ where } C_{ox} = \varepsilon_{ox}/T_{ox} \quad (1)$$

Due to the difference in the flat band voltage, the NMOS transistor has a negligible level of holes in the channel and thus, does not suffer from the NBTI degradation.

For a PMOS transistor, there are two phases of NBTI, depending on its bias condition. These two phases are illustrated in Fig. 1, assuming the substrate is biased at V_{DD}. In Phase I, when V_g=0 (i.e., V_{gs}= -V_{DD}), positive interface traps are accumulating over the stress time with H diffusing towards the gate. This phase is usually referred as "stress" or "static NBTI". In Phase II, when V_g=V_{DD} (i.e., V_{gs}=0), holes are not present in the channel and thus, no new interface traps are generated; instead, H diffuses back and anneals the broken Si-H. As a result, the number of interface traps is reduced during this stage and the NBTI degradation is recovered. Phase II is usually referred as "recovery" and has a significant impact on the estimation of NBTI during the dynamic switching.

In this section, compact models for both phases are developed and verified with experimental data. Meanwhile, typical values of model coefficients are concluded.

2.1 Static NBTI

In Phase I, interface traps are generated by the reaction to break Si-H and then H leaves the Si-oxide interface through diffusion. This process can be generally described by the reaction-diffusion model [11]. The solution to that model provides such dependence:

$$N_{it} = \left(K^2 \cdot t^{1/2} + c^{1/2n}\right)^{2n} \quad (2)$$

where c is N_{it} at the starting point; n is about 0.25, which is the signature of neutral H diffusion [9, 11]. Note that n equals to 0.16 if the diffusing species is H_2, instead of H [9]; in this work, the focus

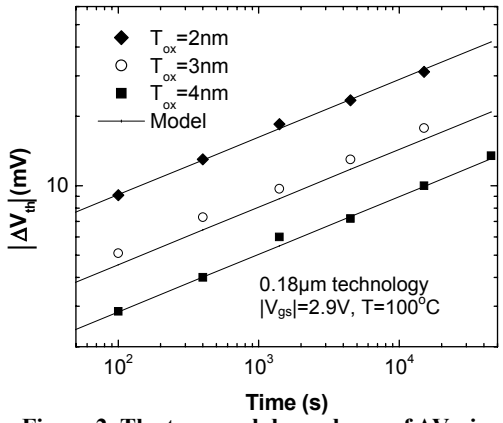


Figure 2. The temporal dependence of ΔV_{th} in static NBTI [2].

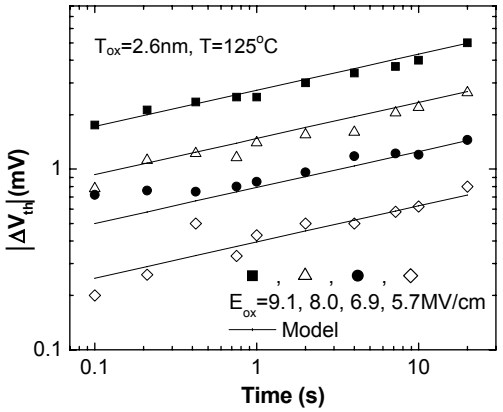


Figure 3. Static NBTI under various E_{ox} [10].

is H-dominated diffusion, while the entire modeling framework is extendable to H_2-dominated diffusion by changing the value of n. Considering the reaction of breaking Si-H, the generation rate of N_{it}, K, is linearly proportional to the hole density and exponentially dependent on temperature (T) and the electric field (E_{ox}) [9-10]. Therefore, for V_{ds}=0:

$$K \propto \sqrt{C_{ox}\left(V_{gs} - V_{th}\right)} \cdot \exp\left(E_{ox}/E_0\right) \cdot \exp\left(-E_a/kT\right) \quad (3)$$

where E_{ox}=(V_{gs}-V_{th})/T_{ox} and k is the Boltzmann constant. Using this model and Eq. (1), Figs. 2 and 3 verify the change of V_{th} under static NBTI for two different technologies at various process and stress conditions. The fitted values of coefficients do converge from the verification: E_0 is 1.9-2.0 MV/cm and E_a is around 0.12 eV. This convergence confirms that E_0 and E_a are technology-independent characteristics of the reaction. Furthermore, if V_{ds} does not equal to 0 (e.g., due to sub-threshold leakage), E_{ox} at the drain end is smaller than the source end, which alleviates NBTI stress. The dependence of K on V_{ds} can be derived from Eq. (3) as:

$$K \propto 1 - V_{ds}/\left[\alpha\left(V_{gs} - V_{th}\right)\right] \quad (4)$$

where α is around 1.3, as extracted from a 0.25μm technology [12].

2.2 Dynamic NBTI

In a realistic circuit operation, the gate voltage switches between 0 and V_{DD}. For a PMOS transistor, the condition of V_g=V_{DD} removes NBTI stress and anneals interface traps. Such a process solely relies on the diffusion of neutral H and thus, has no

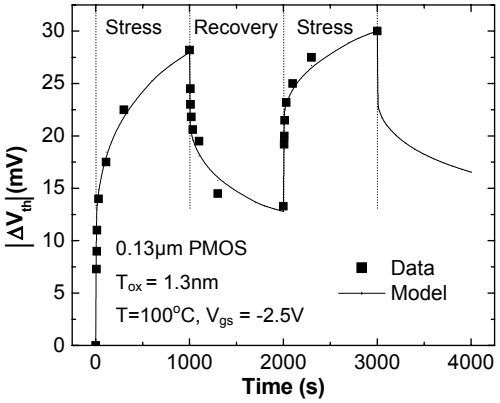


Figure 4. ΔV_{th} during dynamic NBTI [14].

field dependence [13]. Assuming the recovery happens at $t=t_0$ with $N_{it}=N_{it0}$, the change of N_{it} can then be modeled as [10]:

$$N_{it} = N_{it0} \cdot \left[1 - \sqrt{\eta(t-t_0)/t}\right] \quad (5)$$

Fig. 4 evaluates this model by verifying the dynamic behavior with data from a 0.13μm technology [13]. In this example, η=0.35 and again, E_0 and E_a converge to the values in Section 2.1. When the next cycle of stress comes back, the reaction-diffusion process continues as described by Eq. (2). V_{th} change during continuous stress is also verified in Fig. 4.

In reality, the stress and recovery processes are more complicated. They may involve oxide traps and other charged residues [13-16]. These non-H based mechanisms may have faster response time than the diffusion process. Without losing generality, their impact can be included as a constant of δ:

$$\text{Stress: } N_{it} = \sqrt{K^2 \cdot (t-t_0)^{1/2} + N_{it0}^2} + \delta \quad (6)$$

$$\text{Recovery: } N_{it} = (N_{it0} - \delta) \cdot \left[1 - \sqrt{\eta(t-t_0)/t}\right] \quad (7)$$

The change of V_{th} (ΔV_{th}) is then proportional to N_{it} (Eq. (1)). No matter what the value of δ is, there is an interesting behavior predicted by these models: the final ΔV_{th} is independent on switching frequency. This behavior is confirmed by experimental data and one example is shown in Fig. 5 [13-14, 17]. With the recovery in dynamic switching, ΔV_{th} due to NBTI may be reduced by 2-3 times as compared to that purely under static NBTI stress.

As the above models are well verified over a wide range of process and design conditions, they provide a solid basis for further simulation studies and tool development.

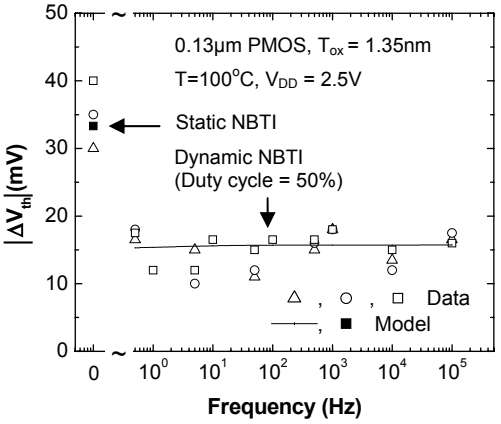


Figure 5. Frequency-independence of NBTI [14].

2.3 Predictive Modeling and Extrapolation

For the direct calculation of V_{th} change under NBTI, the entire suite of formulas and representative model parameters are summarized in Table 1.These models are scalable with key process and design parameters, such as T_{ox}, V_{gs}, V_{th}, V_{ds}, T, L, and time. Even though the gate length (L) is not explicitly expressed in the N_{it} model, L is still able to affect the degradation through its impact on V_{th} (i.e., the DIBL effect).

Based on the newly developed model, the trend of NBTI is extrapolated toward the 32nm node. Technology specifications are taken from the Predictive Technology Model [18]. Due to the slow scaling of V_{th} (for leakage control) and T_{ox}, the electric field across gate oxide, $E_{ox}=(V_{gs}-V_{th})/T_{ox}$, actually decreases for future technology. Consequently, ΔV_{th} due to NBTI is reduced with such a trend of scaling. Fig. 6 shows this trend for static NBTI. On the other hand, with lower ratio of V_{DD}/V_{th}, the transistor performance has increasing sensitivity to V_{th} change. Thus, the change of I_{on} due to NBTI still increases with technology scaling, even though ΔV_{th} decreases (Fig. 6). If the amount of ΔV_{th} is relatively small, such as the case of dynamic NBTI, then the change of I_{on} also follows the trend of ΔV_{th}.

3. DESIGN EXPLORATION

The compact model for NBTI facilitates the design practice and tool development to enhance circuit reliability in the nanometer regime. In this section, a number of key design insights are extracted using this model. These insights help to identify the direction of design solutions in the presence of NBTI.

Table 1. Summary of the predictive model.

$\|\Delta V_{th}\|$ under NBTI			
Stress	$\sqrt{K_v^2 \cdot (t-t_0)^{1/2} + \Delta V_{th0}^2} + \delta_v$		
Recovery	$(\Delta V_{th0} - \delta_v) \cdot \left[1 - \sqrt{\eta(t-t_0)/t}\right]$		
K_v	$A \cdot t_{ox} \cdot \sqrt{C_{ox}(V_{gs}-V_{th})} \cdot [1 - V_{ds}/\alpha(V_{gs}-V_{th})] \cdot \exp(E_{ox}/E_0) \cdot \exp(-E_a/kT)$		
A (mV/nm/$C^{0.5}$)	1.8	α	1.3
E_0 (MV/cm)	2.0	η	0.35
E_a (eV)	0.13	δ_v (mV)	5.0

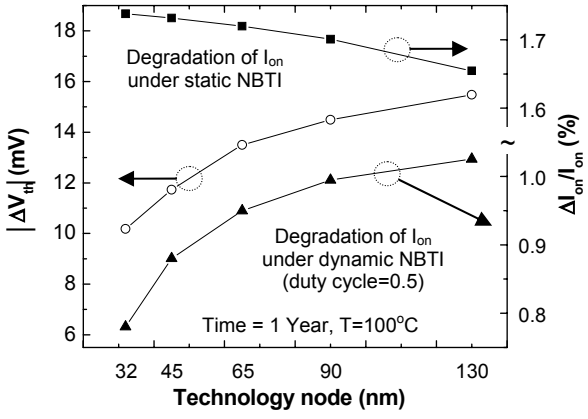


Figure 6. Larger impact of NBTI for future nodes.

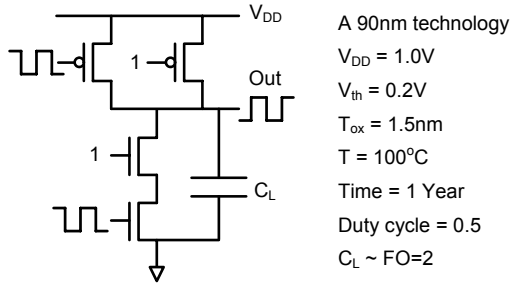


Figure 7. Simulation setup with a NAND gate.

3.1 Experimental Setup

The newly developed models are implemented into HSPICE. An industrial 90 nm technology is used throughout this section. Most of the studies employ a 2-input NAND as the object, with load capacitance equal to that of the Fanout=2 case. The circuit structure and technology specifications are listed in Fig. 7. The stress time is one year and the duty cycle is 0.5 for the dynamic NBTI, except specified otherwise. It is not necessary to specify the switching frequency due to the independence of NBTI on it (Fig. 5).

3.2 Process Sensitivities

The first study is to understand the sensitivity of NBTI to key process parameters. The results of this study would not only help to identify the most sensitive parameters for design optimization, but also provide insights to the interactions between reliability and process variations.

The simulation results of static NBTI are shown in Fig. 8. Due to the exponential dependence of NBTI on E_{ox} (Eq. (3)), the change of V_{th} is most sensitive to V_{DD} and V_{th}, especially to V_{DD} due to its larger magnitude in super-threshold operations. Increasing V_{DD} by 30% may lead to an increase of 30mV in ΔV_{th}. Such a circuit has very pessimistic durability, if the life time is defined as the time when V_{th} shifts by 30mV [8]. Reducing V_{th} has similar impact on V_{th} change. In both cases, the improvement of circuit speed by tuning V_{DD} and V_{th} contradicts the requirement of circuit reliability. The NBTI effect is relatively insensitive to L tuning, since in a static condition (Phase I in Fig. 1), V_{ds} is usually 0 and thus, the dependence of V_{th} on L (i.e., DIBL) is weak.

3.3 Circuit Design Techniques

With the change of V_{th}, circuit speed degrades over the time. This degradation needs to be tolerated during the design stage to ensure sufficient product quality. To date, this is usually achieved by oversizing of the circuit. With the increase of NBTI as well as other design corners, such a strategy has to sacrifice an excessive amount of design margins and loses the benefit of technology scaling. To overcome this barrier, it is critical to integrate these physical effects into the early stage of design exploration, such that their impact can be mitigated up front. The model developed in this work serves well for this purpose. In this section, various design techniques are investigated at both circuit and system levels, in order to obtain design guidelines for effective control of NBTI.

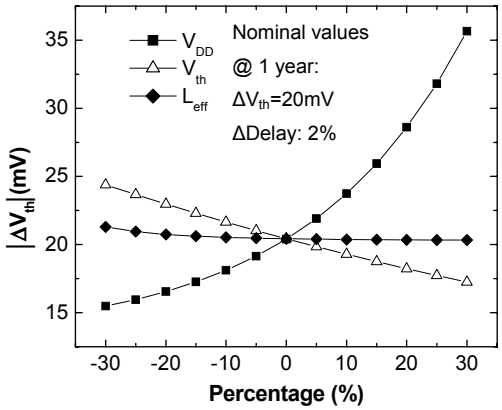


Figure 8. Sensitivities on V_{DD}, V_{th}, and L.

3.3.1 V_{DD} and V_{th} Tuning

V_{DD} and V_{th} would be quite effective to compensate the performance degradation due to NBTI, since ΔV_{th} is very sensitive to them (Fig. 8). For a NAND gate under static stress, Fig. 9 illustrates the amount of voltage overhead needed to guarantee the circuit performance over years. As ΔV_{th} accumulates with longer stress time ($\sim t^{0.25}$), larger margin of V_{DD} or V_{th} is required. For this purpose, tuning V_{DD} may be more beneficial because of its larger sensitivity and easier control.

Although ΔV_{th} increases with higher V_{DD} (Fig. 8), the degradation of performance actually exhibits a non-monotonic behavior, as shown in Fig. 10 [19]. Given the stress time, there exists an optimum V_{DD} that achieves the minimum amount of performance degradation. When V_{DD} is lower than that value, the sensitivity of transistor performance to V_{th} change increases and larger degradation is observed; when V_{DD} is higher, the amount of ΔV_{th} dominates the performance degradation. The exact value of the optimum V_{DD} also depends on the amount of ΔV_{th}: if ΔV_{th} is small (e.g., in dynamic NBTI), then a lower V_{DD} is preferred.

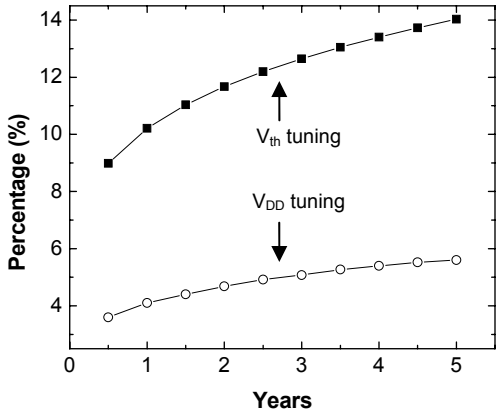


Figure 9. V_{DD} and V_{th} adjustment to compensate the degradation of circuit speed.

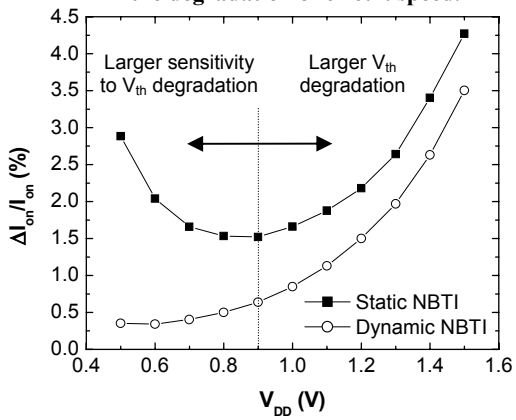


Figure 10. Optimal V_{DD} for minimum degradation of transistor performance.

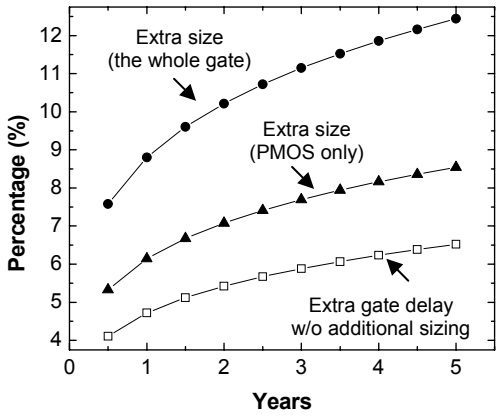


Figure 11. Gate sizing to mitigate NBTI.

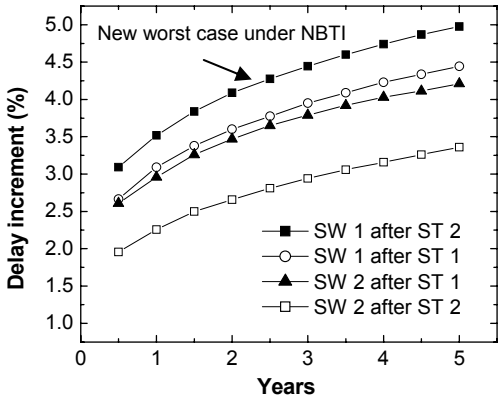
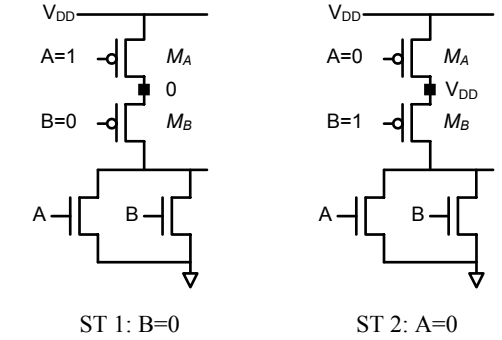


Figure 13. New worst case for timing analysis.

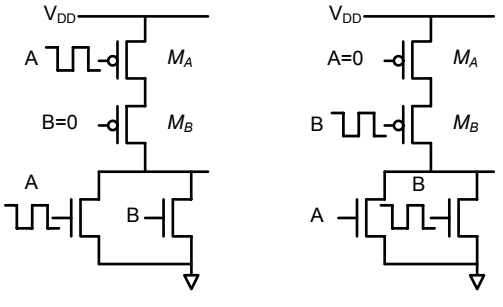
3.3.2 Gate Sizing

Gate sizing has been a widely used technique to tolerate performance uncertainties. By appropriately oversizing the entire gate, sufficient design margin can be set before the fabrication. This is also true in the case of design for reliability. Fig. 11 shows that in order to tolerate potential delay change due to NBTI, as much as 12% oversizing is needed across five years of operations.

On the other hand, since NBTI does not affect the NMOS transistor, oversizing PMOS only may work out for the same purpose. For the same amount of performance degradation, Fig. 11 shows that only 8% is needed if tuning the PMOS transistor, as compared to 12% if tuning the entire gate. While this technique is effective, it may introduce mismatching between NMOS and PMOS during regular operations. Detailed circuit analysis and optimization can be supported by the new NBTI model.



(a) Two static stress cases.



(b) Two switching cases.

Figure 12. Basic stress and switching cases.

3.3.3 Stack Effect

The circuit stack refers to transistors in series. In this case, V_{th} of a transistor may be larger than the nominal value due to the body effect. The stack effect is exploited in design to reduce the leakage current. Since the NBTI effect has an exponential dependence on V_{th}, the stack effect also affects V_{th} degradation under NBTI. To clarify this behavior, a NOR gate with a stack of two PMOS transistors is implemented (as shown in Fig. 12). There are two basic stress cases (ST 1 and ST 2) and two switching cases (SW 1 and SW 2). These are two stress cases refer to V_g of B = 0 (ST 1) and V_g of A = 0 (ST 2). They are not identical during NBTI stress, because of the difference in the threshold voltages. In ST 1, M_B is the on-transistor (i.e., V_s=V_d=0) and thus, V_{th} of M_B is higher than the regular value because of the body effect. In ST 2, the on-transistor, M_A, is not affected by the body effect and has a regular V_{th}. Since higher V_{th} alleviates the impact of NBTI, M_B in ST 1 has a lower ΔV_{th} after a period of static NBTI stress.

The two switching cases represent the switching of A or B (SW 1 or SW 2). In conventional static timing analysis, the switching of A (SW 1) is the worse case, while the switching of B (SW 2) has a shorter delay. The situation gets more complicated when NBTI is involved. If A switches (SW 1) after being stressed in ST 2, it has a longer delay than that after ST 1, due to larger increase of V_{th} in ST 2. This observation is confirmed in Fig. 13. Gate delay from the new worst scenario (the switching of A after ST 2) is significantly longer than that of the conventional case (the switching of A after ST 1). The case for the shortest delay is still the same. Overall, since static NBTI leads to more severe V_{th} degradation, the worst case for timing is a switching after a long dormancy period.

3.3.4 Duty Cycle

The duty cycle can be defined as the percentage of a period that the state stays high. In this study, it refers to the time when V_g=0 for a PMOS transistor, i.e., the static stress condition. At the system level, the adjustment of the duty cycle and the switching frequency is an effective technique for power management. However, tuning the switching frequency may not affect the NBTI degradation, since NBTI is relatively independent on the frequency[1].

Different from the frequency, the duty cycle does have an influence of the NBTI degradation since it changes the relative time

[1] Some experimental data reports the reduction of V_{th} degradation at higher frequencies (>100MHz) [16]. Even so, the amount of reduction is insignificant. Thus, it is safe to assume the frequency-independence for typical operation conditions.

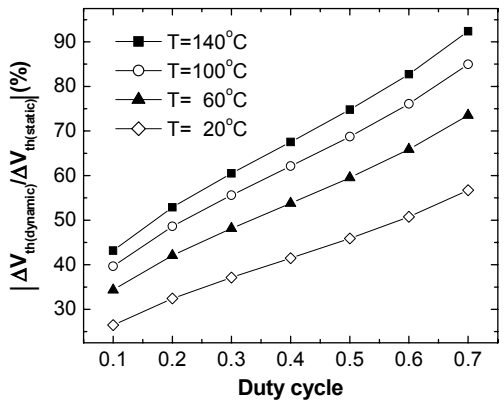


Figure 14. The effectiveness of tuning the duty cycle.

that a PMOS transistor stays in the stress phase or the recovery phase (Fig. 1). The longer it is under recovery (i.e., the lower the duty cycle is), the smaller ΔV_{th} the transistor suffers. This behavior is reported by experiments in [20] and can be well predicted by the compact model. Simulation results are shown in Fig. 14. Under the room temperature, ΔV_{th} can be reduced to less than 30% of that under static stress, if the duty cycle is 0.1. The overall effectiveness of this technique needs to be evaluated together with other design metrics, such as the leakage power, to achieve optimal design.

Furthermore, Fig. 14 indicates that the effectiveness of tuning the duty cycle decreases at higher temperature. The reason is that while the reaction in NBTI stress is exponentially dependent on the temperature (Eq. 3), the recovery, which is purely a diffusion process, does not. Therefore, with increasing temperature, the NBTI degradation is escalated, but not the recovery. From this perspective, lower temperature is desirable to reduce the reaction process of static NBTI stress.

4. CONCLUSIONS

In this work, a predictive model for PMOS NBTI degradation is developed for robust design explorations. Excellent model scalability and generality have been comprehensively verified with experimental data. The convergence of model parameters among various technologies confirms the validity of this predictive model. By implementing the newly developed model into the SPICE simulator, efficient design explorations are enabled.

Based on the simulation studies with an industrial 90nm technology, it is observed that the degradation of circuit performance due to NBTI can be effectively mitigated by V_{DD} and V_{th} tuning, PMOS sizing, as well as reducing the duty cycle. Specifically, an optimal V_{DD} exists to minimize the performance degradation. Lower temperature is also desirable for robust nanoscale design. On the other hand, tuning L or the switching frequency has little impact on the NBTI effect, since the change of V_{th} is relatively independent on L and the switching frequency. As the impact of NBTI on circuit performance has become pronounced in nanoscale design, these design insights are valuable for further development of robust design solutions and CAD tools.

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