A 24 GHz Phased-Array Transmitter in 0.18μm CMOS

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ABSTRACT
A fully-integrated 4-element phased array transmitter at 24 GHz with on-chip PAs is demonstrated in 0.18μm CMOS. It has a beam-forming resolution of 10°, a peak-to-null ratio of 23 dB, and 28 dB isolation between paths. Each PA can deliver up to +14 dBm into 50 Ω in saturation. The die size is 6.8mm x 2.1mm. The transmitter bandwidth is more than 400MHz and supports up to 1Gbit/s QPSK, facilitating a Gigabit wireless LAN solution.

Categories and Subject Descriptors
B.4.1 [**Data Communication Devices**] Transmitters

General Terms
Performance, Design, and Experimentation.

Keywords
Wireless, Transmitters, Phased-Array, 24GHz, CMOS, IC.

1. PHASED ARRAY TRANSMITTER
Integrated phased-array systems at high frequencies promise a future of low-cost radar and gigabit-per-second wireless communication networks. The improvements in the signal-to-noise-plus-interference ratio provided by phased-arrays and the larger bandwidths available at high frequencies motivate the implementation of phased-arrays at 24GHz. In this paper, we present an integrated 24GHz 4-element phased-array transmitter in 0.18μm CMOS, capable of bit-rates more than 500Mb/s (limited by measurement setup). On-chip power amplifiers (PA), with integrated 50Ω output matching, make this a fully-integrated transmitter.

Each element in a phased-array transmitter radiates the same signal delayed by different time intervals. The transmitted outputs add up coherently in the desired direction, increasing the signal power. Incoherent addition of the outputs in other directions attenuates the signal power resulting in reduced interference at receivers that are not targeted. Electrical variation of the delay in each element permits steering of the main transmitter beam.

The architecture and the floorplan of the 4-element CMOS transmitter are detailed in Figure 1. The 24GHz transmitter is based on a two step up-conversion architecture with an IF frequency of 4.8GHz. The delay required in each element is approximated by a phase-shift in the LO path. The first set of mixers up-convert the base-band signal to 4.8GHz. A symmetric H-tree structure distributes the outputs of the 4.8GHz buffers to the 4.8GHz-to-24GHz up-conversion mixers in each path. The outputs of the second up-conversion mixers are buffered and fed to the PA drivers.

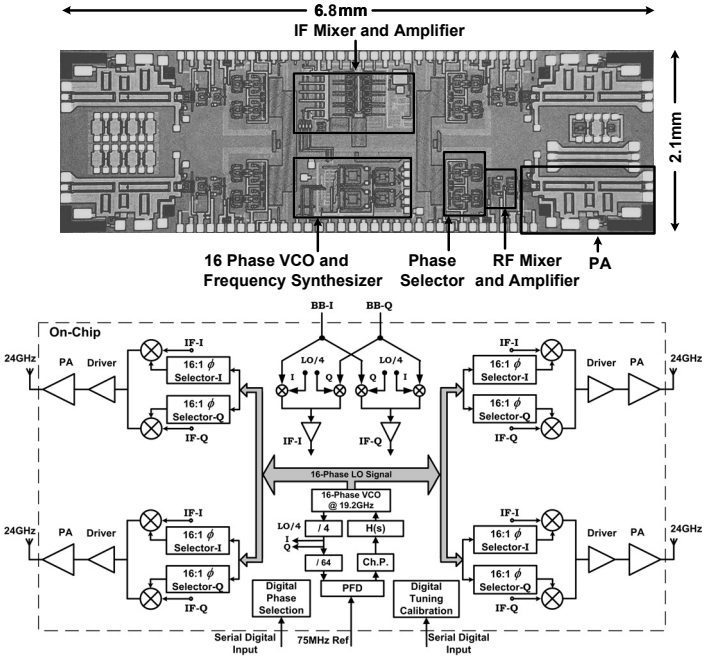

Figure 1. Insert caption to place caption below figure.

The four on-chip PAs are matched to 50Ω. The matching networks in both stages of the PA are designed using low-loss shielded-substrate coplanar waveguides with an effective wavelength nearly twice smaller than that of silicon dioxide. Consequently, there is almost 50% reduction in matching network size resulting in lower loss.

A 16-phase 19.2GHz CMOS VCO consisting of eight differential amplifiers with tuned loads connected in a ring structure generates 16 phases of the LO signal with steps of 22.5° for LO phase-shifting. The same frequency synthesizer loop generates LO frequencies for both up-conversion stages (19.2GHz and 4.8GHz) from a 75MHz reference.

The phase selectors in each transmitter path have independent access to all the phases of the VCO. Symmetric floorplanning and an H-tree based distribution structure ensure symmetry of the LO signals at each transmitter path, as any asymmetry in the LO signal increases the power in the transmit side-lobes, generating interference and clutter for communication and radar systems. The

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digital frequency calibration data and the beam-steering information are loaded onto the chip through a digital serial interface.

The peak-to-null ratio with 4 elements active was larger than 23dB. The fully saturated output power for each PA is 14dBm. The PA output power with driver output of 0dBm is 7dBm. The transmitter was implemented using 0.18μm CMOS and occupies an area of 6.8mm x 2.1mm.