A Fully Physical Model for Leakage Distribution under Process Variations in Nanoscale Double-Gate CMOS

Hari Ananthan and Kaushik Roy
Dept. of ECE, Purdue University
West Lafayette, IN 47907
(hanantha,kaushik)@ecn.purdue.edu

ABSTRACT

Double-gate CMOS is projected to replace classical bulk and SOI technologies around the 32nm node. Predicting the impact of process variations on yield for these novel devices is necessary at an early stage of the design cycle, to enable optimal technology and circuit design choices. This paper presents a fully physical model for double-gate leakage distribution due to gate length (L) and body thickness (t_{si}) variations, both for single devices and stacks. The model is derived directly from the solution of Poisson's and Schrödinger's equations, and thus captures the effect of unique double-gate phenomena such as volume inversion and quantum confinement. It is scalable to $L = 13$nm and $t_{si} = 3$nm, with less than 2% error for 3σ variation as large as 20% of nominal process parameters.

Categories and Subject Descriptors

B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids; B.7.2 [**Integrated Circuits**]: Design Aids

General Terms

Design, Theory

Keywords

Double-gate, Multiple-gate, FinFET, Tri-gate, Process Variations, Leakage Distribution

1. INTRODUCTION

Multiple-gate technologies are the forerunners to replace classical bulk CMOS for the ultimate scaling of silicon MOSFETs to 10nm [1]. The reasons include the ability to use a thicker gate insulator, superior short channel characteristics, improved mobility in the undoped body and elimination of random dopant effects. Quasi-planar structures such as the double-gate (DG) FinFET [8], Tri-gate [6] and Omega-FET [15] are among the most popular device structures, chiefly because of their relative ease of manufacturability.

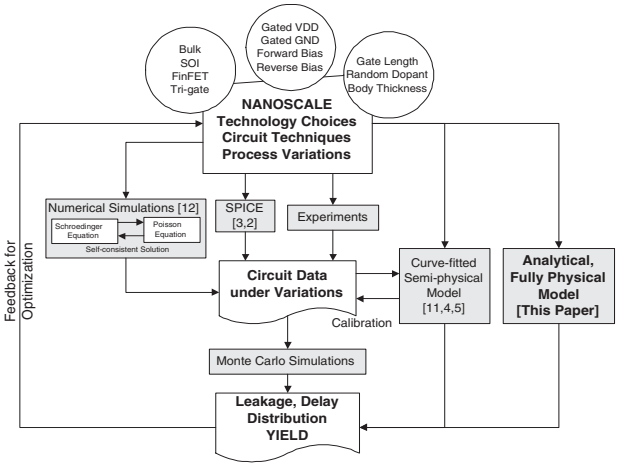

Figure 1: Enabling variation-aware technology and circuit design.

As these novel technologies loom over the scaling roadmap, systematic and random variations in process parameters are beginning to impact yield significantly in ICs. Yield is determined by the number of *failing* parts – those that exceed a given leakage upper bound or fall short of a given frequency lower bound. Designers account for these variations either through a corner-based approach or a statistical approach. Designing for worst-case corners usually results in an overly conservative design that does not meet specifications, and a statistical approach is widely regarded as the best solution. Fig. 1 outlines the various ways in which a designer can evaluate the impact of process variations on technology and circuit design choices in the nanoscale regime. Full-fledged Monte Carlo simulation is computationally too expensive even when compact SPICE-like models [3, 2] are used, and is impossible using exact device simulators. Thus, analytical models for distributions of circuit metrics under process variations are necessary to make statistical analysis tractable.

Existing analytical approaches for variations approximate *threshold voltage* as a polynomial function of gate length (and other parameters such as doping concentration), and then use this to derive the near-lognormal distribution of leakage, assuming gate length is distributed normally [11, 4, 5]. These approaches require technology characterization (either through measurements or simulations) and calibra-

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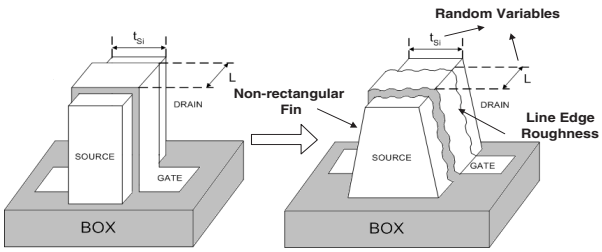

Figure 2: (a) Ideal Quasi-planar Multiple-gate MOSFET structure, and (b) the effect of variations.

tion to obtain the coefficients of the V_t model. Firstly, the V_t so defined by these semi-physical models does not account for unique physical effects in nanoscale devices, for example, effects such as volume inversion and quantum confinement in double-gate MOSFETs, and the associated effect on MOSFET properties due to body thickness variations [14]. More importantly, these approaches work well when a technology is designed independently, and the circuit designer only needs to analyze the effect of variations and optimize the design for yield. However, in the nanoscale regime, an integrated approach to technology and circuit design is not only required, but inevitable to meet system specifications []. As shown by the feedback loop in Fig. 1, the impact of variations on yield must be estimated at an early stage of the design cycle, to enable optimal technology and circuit design choices. Thus, there is a need for a model for variations that is both analytical and physical.

This paper makes the following contributions, and is the first attempt to our knowledge, to:

- Derive a fully physical model for double-gate leakage directly from the solution of Poisson's and Schrödinger's equations, that can be used for process variation analysis (Section 3);
- Develop a model for single device leakage distribution due to gate length and body thickness variations in double-gate technology, that is scalable to devices at the end of the roadmap – with 13nm gate length and 3nm body thickness (Section 4);
- Extend the model to multiple-device stacks to enable logic-gate simulation (Section 5).

2. NANOSCALE DOUBLE-GATE : BACKGROUND

Double-gate CMOS has gained popularity as an alternative to single-gate bulk technology for ultimate scalability of silicon CMOS to 10nm. Essentially, the short channel effect reflects the extent of drain-bias influence on channel potential. In order to increase gate-control, the entire channel needs to be "brought closer to the gate". Technologies such as Fully-depleted SOI, Ground-plane and Double-gate achieve this by using a thin undoped silicon film controlled by one or more gates, with V_t set by the metal gate workfunction. These devices thus have better SCE, higher mobility and negligible random dopant effects compared to classical devices [10].

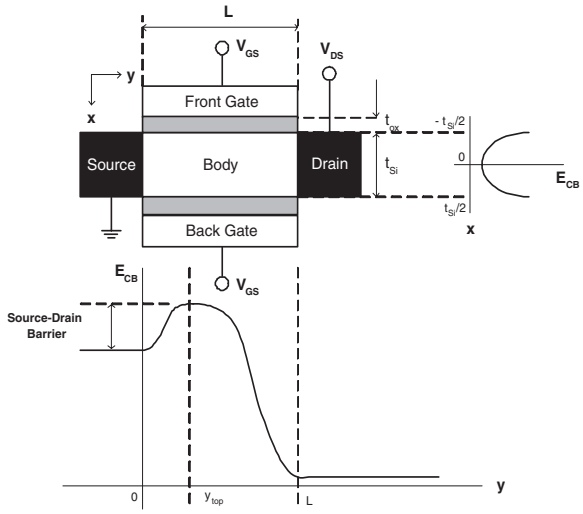

Figure 3: Double-gate device structure, and band diagram in the weak inversion state (E_{CB} is the conduction band edge).

2.1 Device Structure

Fig. 2(a) shows the ideal device architecture of a quasi-planar multiple-gate SOI FET (such as FinFET, Tri-gate and Omega-FET). An undoped silicon fin of thickness t_{Si} is patterned on an SOI wafer. The gate wraps around on either side of the fin (over the gate insulator), and t_{si} is the body-thickness of the resulting double-gate structure, where both gates are tied together. Current flow is parallel to the wafer plane, just as in bulk, but occurs in an orthogonal crystal plane. Channel width is perpendicular to the plane – fin height represents the effective channel width of a single fin. Higher widths are achieved by patterning multiple fins in parallel.

Fig. 3 shows a 2-D cross section of a DG device (top view of Fig. 2). The process parameters of interest are L, t_{si}, t_{ox}, and Gate workfunction ($\Delta\phi_{MS}$). A generic DG MOSFET can have different front and back gate workfunctions and/or oxide thicknesses, and the two gates can be independently controlled. In this analysis, we consider a symmetric three-terminal DG MOSFET, that is, t_{ox} and $\Delta\phi_{MS}$ are symmetric, and the two gates are electrically connected. The three independent terminals are thus gate, source and drain.

2.2 Device Physics

The device physics for a DG MOSFET is different from a traditional bulk MOSFET. The two primary physical phenomena that affect leakage are the short channel effect, and the quantum confinement effect.

2.2.1 Short Channel Effect (SCE)

Leakage current in a bulk MOSFET is dominated by surface conduction and some sub-surface punchthrough current. A DG device on the other hand is nearly *volume-inverted*, that is, current flows throughout the ultra-thin body. In the weak-inversion state ($V_{gs} << V_{dd}, V_{ds} = V_{dd}$), the potential in the undoped body of the DG device (Fig. 3) is nearly flat (equal to $V_{gs} - \Delta\phi_{MS}$) for a long-channel device. When channel length is decreased, the potential at the center of the body, which is the region least controlled by either

gate, increases due to the drain influence. Equivalently, the source-drain barrier (shown in Fig. 3) is lowered, and leakage increases. This is the classical short channel effect. The maximum current flows along the region of maximum potential, that is, at the centre of the body. The 2-D potential distribution is derived as a solution of Poisson's equation [9].

2.2.2 *Quantum Confinement Effect (QCE)*

Confinement of carriers in the ultra-thin body leads to quantization of energy levels, and the finite probability of occupation of these levels given by the wavefunction solution. The quantized levels are at higher energy than the classical levels. This increases the source-drain barrier, thus decreasing leakage. Both the wavefunctions and quantized energy levels are solutions of the 1-D Schrödinger's equation. In fact, the problem can be approximated to the well-known case of a particle in an infinite potential well [13].

As shown in Fig. 1 (Numerical Simulations),the self-consistent solution of Poisson's and Schrödinger's equations is required for any device, in order to properly account for classical and quantum effects.

2.3 Process Variations

Fig. 2(a) shows the ideal structure of a multiple-gate device. Fig. 2(b) gives a glimpse of the likely device structure after fabrication. Parameters such as gate length (L) and body thickness ($t_{\rm si}$) vary from lot-to-lot, wafer-to-wafer, die-to-die, FET to FET on one die, and within an FET due to non-rectangular fin and line edge roughness effects. While L, $t_{\rm si}$, $t_{\rm ox}$, and $\Delta\phi_{\rm MS}$ are the process parameters of interest, $t_{\rm ox}$ and $\Delta\phi_{\rm MS}$ are maintained at their nominal values in order to simplify the analysis in this work. This is justified because, while L and $t_{\rm si}$ are defined lithographically and are susceptible to variations, $t_{\rm ox}$ and $\Delta\phi_{\rm MS}$ are defined by thermal steps that can be controlled much better.

Variation in L affects leakage through SCE – shorter channel length increases drain influence on the channel and lowers the source-drain barrier, thus increasing leakage. Variation in $t_{\rm si}$ on the other hand affects leakage through both SCE and QCE. A thicker body increases the volume of the channel that is not *well-controlled* by the gates, thus increasing drain influence and leakage. Further, thicker $t_{\rm si}$ also lessens the impact of QCE, thus lowering the source-drain barrier and increasing leakage. The quantitative impact on each component is described in the following sections.

3. DOUBLE-GATE LEAKAGE MODEL

3.1 Exact Solution

The analysis in this paper begins with the 2-D Poisson's sultion by Liang [9], supplemented by the 1-D Schrödinger's solution by Trivedi [13], both for symmetric DG devices. These solutions account for both SCE and QCE. However, the model presented in this paper is not restricted to these potential/wavefunction solutions, and can be extended to other solutions such as those by Young [16], and Chen [7]. In fact, the outlined method can be extended to all thin-body fully-depleted devices.

The expression for diffusion current from source to drain in the weak-inversion regime, in a DG MOSFET, can be written as:

$$I_{\rm sub} = \frac{\mu W k T (1 - e^{\frac{-qV_{\rm ds}}{kT}})}{\int_0^L \frac{dy}{\int_{-t_{\rm si}/2}^{t_{\rm si}/2} n_{\rm c}(x,y)dx}}. \quad (1)$$

The term inside the integral $n_{\rm c}(x,y)$ represents the effective carrier concentration at a given position (x,y):

$$n_{\rm c}(x,y) = n_{\rm i}^{\rm QM}(x) {\rm e}^{\frac{q\psi(x,y)}{kT}}, \quad (2)$$

$$\psi(x,y) = V_{\rm gs} - \Delta\phi_{\rm MS} + X(x)Y(y), \quad (3)$$

$$X(x) \sim \cos\frac{\pi x}{\lambda}, \quad (4)$$

$$Y(y) \sim b_1 \sinh\frac{\pi y}{\lambda} + c_1 \sinh\frac{\pi(L-y)}{\lambda}, \quad (5)$$

$$\epsilon_{\rm si} \tan\left(\frac{\pi t_{\rm ox}}{\lambda}\right) = \epsilon_{\rm ox} \cot\left(\frac{\pi t_{\rm si}}{2\lambda}\right), \quad (6)$$

$$n_{\rm i}^{\rm QM}(x) = {\rm e}^{\frac{-Eg}{2kT}} \frac{kT}{\pi\hbar^2} \sum_{ij} g_i m_{\rm di}^* {\rm e}^{\frac{-qE_{ij}}{kT}} |\Psi_j(x)|^2, \quad (7)$$

$$|\Psi_j(x)|^2 = \frac{2}{t_{\rm si}} \left[\sin\left(\frac{j\pi(x + t_{\rm si}/2)}{t_{\rm si}}\right)\right]^2, \quad (8)$$

$$E_{ij} = \frac{j^2 h^2}{8 m_i^2 t_{\rm si}^2}. \quad (9)$$

The 2-D potential $\psi(x,y)$ in the silicon body is derived as a solution of Poisson's equation by separation of variables [9]. λ, the solution of the transcendental Eq. 6, represents the scale length parameter. The equivalent intrinsic carrier concentration $n_{\rm i}^{\rm QM}(x)$ is calculated from the density of states, and the probability of occupation based on the the 1-D wavefunction solution. $\Psi(x)$ and the energy eigen values $E_{\rm ij}$ are derived from a solution of Schrödinger's equation, assuming the carriers are confined in an infinite potential well of width $t_{\rm si}$ [13]. Here, the index i represents the valley (longitudinal or transverse), and j the subband index. The reader is referred to [9] and [13] for a more detailed description of this current model.

3.2 Compact Solution

Eqs. 1-9 involve integrals and complex functional forms, and cannot be used directly to derive an analytical model for variation study. The key observation here is that the physical dependence of $I_{\rm sub}$ can be captured by accounting just for the potential at the centre of the ultra-thin body ($x = 0$), and at the top of the source-drain barrier ($y = y_{\rm top}$). This is because the *x-integral* in Eq. 1 is dominated by the value of the integrand at $x = 0$, and the *y-integral* by the integrand at $y = y_{\rm top}$, the location of the top of the source-drain barrier (Fig. 3). Physically, the maximum current flows at the center of the body (farthest away from the gate, at $x = 0$), and its magnitude is determined primarily by the smallest carrier concentration in the y direction, at the top of the source-drain barrier [9]. Thus, the current can be expressed as:

$$I_{\rm sub} = \mu W k T n_{\rm i}^{\rm QM}(0) e^{\frac{q\psi(0,y_{\rm top})}{kT}} (1 - e^{\frac{-qV_{\rm ds}}{kT}}). \quad (10)$$

It is also noteworthy that the two terms $e^{\frac{q\psi(0,y_{\rm top})}{kT}}$ and $n_{\rm i}^{\rm QM}(0)$ represent SCE and QCE respectively.

Fig. 4 shows that the analytical model of Eq. 10 (normalized) matches results obtained from 2-D numerical simulations using TAURUS-DS [12] well, for a wide range of gate

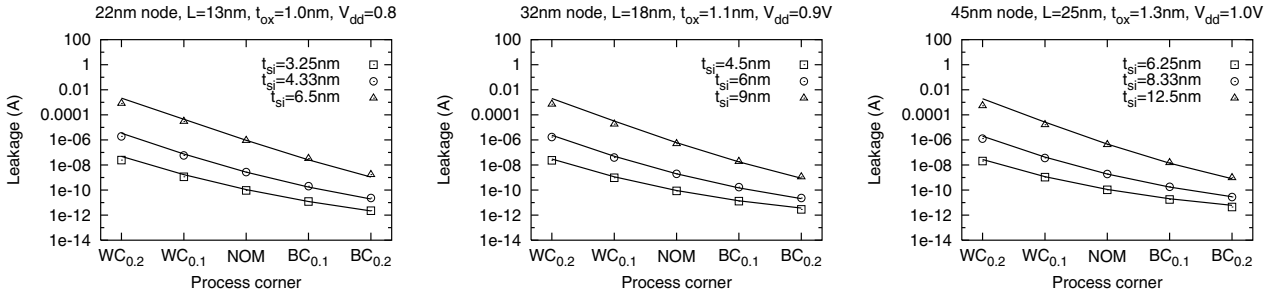

Figure 4: Comparison between Numerical (points) and Analytical model (lines) for (a)13nm, (b)18nm, and (c)25nm devices. Worst-case (WC) and best-case (BC) corners correspond to L and $t_{\rm si}$ variation, and subscripts indicate fractional change in parameters.

length and body thickness values. The x-axes indices denote the process corner: $\mathrm{WC}_{0.2}$ denotes 20% decrease in L and 20% increase in $t_{\rm si}$ (highest leakage), while $\mathrm{BC}_{0.2}$ denotes 20% increase in L and 20% decrease in $t_{\rm si}$ (lowest leakage).

This simplified model captures the essential physics of double-gate leakage current, and is used for process variation analysis in the following sections.

4. LEAKAGE DISTRIBUTION

The dependence of $I_{\rm off}$ on L and $t_{\rm si}$ is through the factors $\mathrm{e}^{\frac{q\psi(0,y_{\rm top})}{kT}}$ and $n_{\rm i}^{\rm QM}(0)$ in Eq. 10. These in effect represent the short channel effect and the quantum confinement effect respectively, as was previously noted. To further simplify the analysis, we consider $\Delta \log I_{\rm off}$, that is, $\log\left(\frac{I_{\rm off}}{I_{\rm off}^{\rm nom}}\right)$:

$$\begin{aligned}\Delta \log I_{\rm off} &= \frac{q\Delta\psi(0,y_{\rm top})}{kT} + \log\frac{n_{\rm i}^{\rm QM}(0)}{n_{\rm i-nom}^{\rm QM}(0)} \qquad (11)\\ &= \Delta(\mathrm{SCE}) + \Delta(\mathrm{QCE}).\end{aligned}$$

Each of these terms is expanded as a 2-D Taylor series about the nominal values $L^{\rm nom}$ and $t_{\rm si}^{\rm nom}$. For example,

$$\begin{aligned}\frac{q\Delta\psi(0,y_{\rm top})}{kT} &= f_L^1(L-L^{\rm nom}) + f_t^1(t_{\rm si}-t_{\rm si}^{\rm nom}) +\\ &\quad \frac{f_L^2}{2!}(L-L^{\rm nom})^2 + \frac{f_t^2}{2!}(t_{\rm si}-t_{\rm si}^{\rm nom})^2 +\\ &\quad f_{Lt}^2(L-L^{\rm nom})(t_{\rm si}-t_{\rm si}^{\rm nom}) + ..., \qquad (12)\end{aligned}$$

where f_L^i is the i-th partial derivative of $\frac{q\Delta\psi(0,y_{\rm top})}{kT}$ with respect to L, f_t^i with respect to $t_{\rm si}$, and so on, evaluated at $(L^{\rm nom}, t_{\rm si}^{\rm nom})$. This analysis is repeated for the other term in Eq. 11. This approximation is justified because L and $t_{\rm si}$ values are assumed to be concentrated around their nominal values ($\leq 20\%$ variations), and the variation in $\Delta \log I_{\rm off}$ is slow enough to be captured using the fist few terms of the Taylor series. Thus, we have:

$$\Delta \log I_{\rm off} = \sum_{i,j} \alpha_{\rm ij} \Delta L^i \Delta {t_{\rm si}}^j, \qquad (13)$$

where $\Delta L = L - L^{\rm nom}$, and $\Delta t_{\rm si} = t_{\rm si} - t_{\rm si}^{\rm nom}$. The mean of

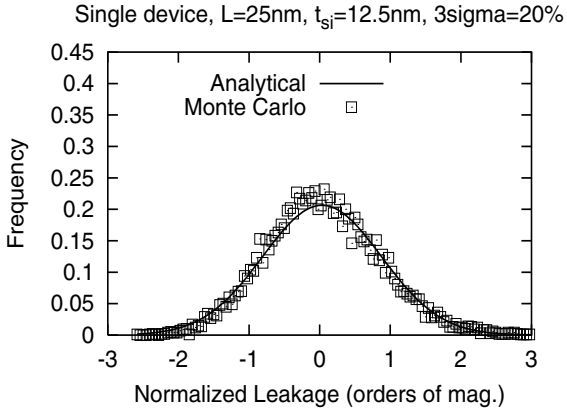

Figure 5: Comparison of Leakage distribution between Monte Carlo (points) and Analytical model (line) for a single device. Both L and $t_{\rm si}$ are assumed to vary normally.

this random variable can then be calculated as:

$$\begin{aligned}E(\Delta \log I_{\rm off}) &= \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \Delta \log I_{\rm off} p_{\rm L} p_t dL dt_{\rm si}\\ &= \sum_{i,j} \alpha_{\rm ij}\mu_{\rm i}(L)\mu_{\rm j}(t_{\rm si}), \qquad (14)\end{aligned}$$

where $p_{\rm L}$ and p_t are the probability density functions, and $\mu_{\rm i}(L)$ and $\mu_{\rm j}(t_{\rm si})$ are the i-th and j-th central moments of the L and $t_{\rm si}$ distributions respectively. The distributions are assumed to independent. If L and $t_{\rm si}$ are distributed normally, then their central moments can be evaluated as:

$$\mu_{2n} = \frac{(2n)!}{2^n n!}\sigma^{2n}, \qquad (15)$$

$$\mu_{2n+1} = 0, \qquad (16)$$

where σ is the standard deviation. The variance of $\Delta \log I_{\rm off}$ can similarly be calculated by taking the square of Eq. 13 and repeating the analysis. The final distribution is assumed to be normal; this is verified through Monte Carlo simulations to be fairly accurate.

Fig. 5 shows a good match between the distribution derived from a Monte Carlo simulation and from the analytical model, for a sample case. For simplicity, yield is defined as the percentage of devices which meet $I_{\rm off} < I_{\rm off}^{\rm max} = M.I_{\rm off}^{\rm nom}$.

Table 1: Error between Monte Carlo simulations and Analytical model for yield, for a single device (all numbers in %).

Variation →	$3\sigma = 10\%$ (L and t_{si})			$3\sigma = 20\%$ (L and t_{si})		
Technology ↓	Y_{MC}	Y_{anal}	Error	Y_{MC}	Y_{anal}	Error
$L = 13$nm						
$t_{si} = 3.25$nm	85.8	86.2	0.54	70.1	70.5	0.57
$t_{si} = 4.33$nm	80.2	81.2	1.3	66.1	67.0	1.4
$t_{si} = 6.5$nm	76.5	76.6	0.06	63.8	64.1	0.44
$L = 18$nm						
$t_{si} = 4.5$nm	87.9	88.7	1.0	71.6	72.5	1.3
$t_{si} = 6$nm	81.4	82.3	1.1	67.1	67.7	0.94
$t_{si} = 9$nm	76.4	76.4	0.03	63.8	64.0	0.39
$L = 25$nm						
$t_{si} = 6.25$nm	89.6	90.4	0.92	73.1	74.0	1.2
$t_{si} = 8.33$nm	82.7	83.5	1.0	68.0	68.5	0.71
$t_{si} = 12.5$nm	76.3	76.3	0.03	63.7	63.9	0.40

We account only for inter-die variations in this analysis, but the approach can be extended to include intra-die variations as well. Table 1 shows the error in estimating yield using this model compared to Monte Carlo simulation, for $M = 2$. The error is negligible – less than 1.4% – for the entire range of gate length and body thickness values, both using $3\sigma = 10\%$, and $3\sigma = 20\%$ of nominal values. The analysis is repeated for different different M values, and the error is found to remain smaller than 1.4%.

5. MULTIPLE-DEVICE STACKS

In order to analyze the leakage distribution in realistic circuits, multiple-device structures such as NOR (parallel) and NAND (series) gates must be considered. Clearly, the only structure of concern is the series-connected stack (NMOS devices in a NAND gate, or PMOS devices in a NOR gate). This is because parallel structures can be analyzed as separate devices. This subsection develops the framework for analyzing a two-input stack. The method can be easily extended to larger stacks. The input vector for a two-input *off* stack can be 00, 10, or 01, with the first bit indicating the top device (closer to the output). The 01 case can be assumed to be equivalent to the single device case, because the intermediate node voltage is almost 0. Thus, only 00 and 10 need to be considered.

The voltage at the intermediate node is calculated by equating the currents in the two devices:

$$I_{sub}(V_g = -V_2, V_{ds} = V_{dd} - V_2) = I_{sub}(V_{gs} = 0, V_{ds} = V_2), \quad (17)$$

where I_{sub} is defined in Eq. 10. It is noteworthy that both devices are in the sub-threshold region for input vectors 00 and 10; thus, using Eq. 10 is justified. Assuming the two devices are identical (except for width) and the variations are perfectly correlated (because of spatial proximity), we have

$$W_1 e^{q\psi_1/kT}(1 - e^{-q(V_{dd}-V_2)/kT}) = W_2 e^{q\psi_2/kT}(1 - e^{-qV_2/kT}), \quad (18)$$

where ψ_1 and ψ_2 are functions of V_2 besides L and t_{si}. It is not possible to solve for V_2 from this transcendental equation. So, Eq. 18 is recast as

$$g(L, t_{si}, V_2) = \text{LHS(Eq.18)} - \text{RHS(Eq.18)}. \quad (19)$$

Expanding $g(L, t_{si}, V_2)$ as a 3-D Taylor series about (L^{nom}, t_{si}^{nom}, V_2^{nom}), and recognizing that $g = 0$, we have

$$g(L, t_{si}, V_2) = g_L^1(L - L^{nom}) + g_t^1(t_{si} - t_{si}^{nom}) + g_V^1(V_2 - V_2^{nom}) = 0. \quad (20)$$

V_2^{nom} is separately evaluated as the solution of Eq. 18, and Eq. 20 is used to evaluate V_2 at a give (L, t_{si}). Essentially, the transcendental Eq .18 is solved only for the nominal point. Since L and t_{si} are concentrated near their nominal values, V_2 is expected to remain close to the nominal value V_2^{nom} too, and thus the first-order Taylor series approximation is justified. Now, the value of V_2 from Eq. 20 is substituted into the correspoing I_{sub} expression, and the mean and variance of the leakage are calculated as in Section 4. The same procedure is used for both input vectors 00 and 10.

Fig. 6 shows that the analytical model for two-device stack I_{off} derived in this section (normalized) matches results obtained from 2-D numerical simulations using TAURUS-DS [12] well, for a wide range of gate length and body thickness values. Table 2 shows the error in estimating yield using this model compared to Monte Carlo simulation, assuming maximum leakage allowed is $2I_{off}^{nom}$. The error is negligible – less than 2.1% – for the entire range of gate length and body thickness values, for $3\sigma = 20\%$.

The above approach can be applied to derive the distribution for longer stacks as well. In fact, the same algorithm was used to solve for λ from the transcendental Eq. 6, for the analysis in Sections 4 and 5.

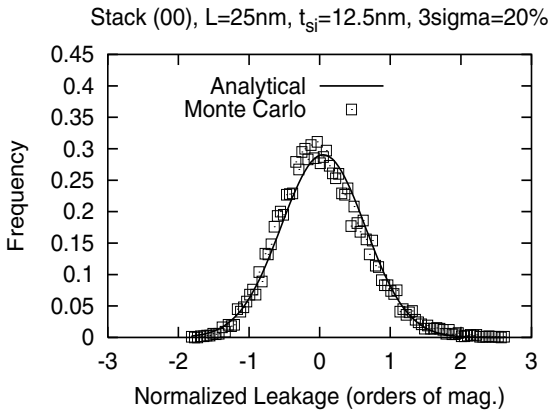

Figure 7: Comparison of Leakage distribution between Monte Carlo (points) and Analytical model (line) for a two-device stack (Input = 00). Both L and t_{si} are assumed to vary normally.

6. CONCLUSION

Systematic and random variations in process parameters from die-to-die, FET-to-FET within a die, and within a FET, are likely to remain, and probably worsen (as a fraction of nominal parameter values) as technology scaling enters the *nano era*. Under this scenario, it is imperative that process, technology and circuit design decisions made at

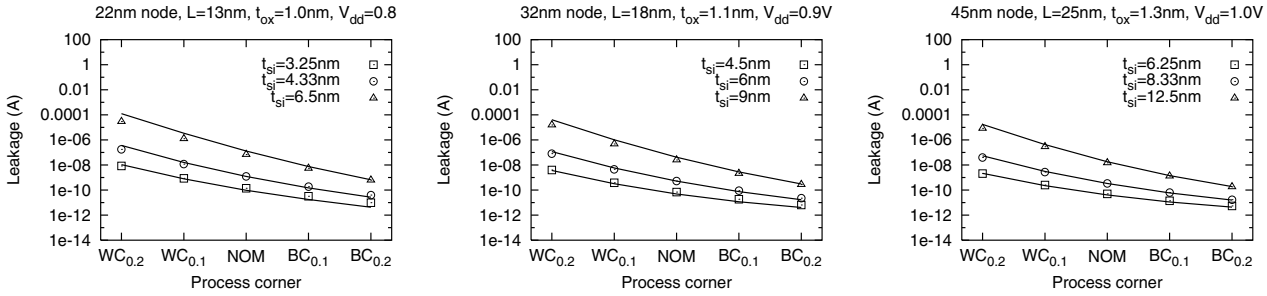

Figure 6: Comparison between Numerical (points) and Analytical model (lines) for (a)13nm, (b)18nm, and (c)25nm two-device stack (Input = 00). Worst-case (WC) and best-case (BC) corners correspond to L and t_{si} variation, and subscripts indicate fractional change in parameters.

Table 2: Error between Monte Carlo simulations and Analytical model for yield for a two-device stack (all numbers in %). The σ value shown applies to both L and t_{si}.

Variation →	Stack "00", $3\sigma = 20\%$			Stack "10", $3\sigma = 20\%$		
Technology ↓	Y_{MC}	Y_{anal}	Error	Y_{MC}	Y_{anal}	Error
$\underline{L = 13nm}$						
$t_{si} = 3.25nm$	76.3	77.5	1.6	71.6	73.0	2.0
$t_{si} = 4.33nm$	71.5	73.0	2.1	68.0	69.3	1.8
$t_{si} = 6.5nm$	67.1	68.0	1.3	65.5	66.5	1.4
$\underline{L = 18nm}$						
$t_{si} = 4.5nm$	79.0	80.7	2.1	73.6	75.2	2.2
$t_{si} = 6nm$	73.4	74.6	1.7	68.8	69.9	1.7
$t_{si} = 9nm$	67.7	68.6	1.4	65.3	66.2	1.5
$\underline{L = 25nm}$						
$t_{si} = 6.25nm$	81.2	82.9	2.2	75.3	76.9	2.2
$t_{si} = 8.33nm$	75.3	76.5	1.6	69.7	70.8	1.7
$t_{si} = 12.5nm$	68.1	69.2	1.5	65.1	66.1	1.5

an early stage of the design cycle incorporate as elaborate a model to account for the impact of variations as possible. This necessitates a fully physical and analytical model that can be used for statistical analysis on large circuits. The leakage distribution model presented in this paper captures most of the key physical mechanisms associated with nanoscale double-gate MOSFETs, because it is derived directly from the solution of fundamental device equations. It can be used both for single devices (INVERTER-like gates) and multiple-device stacks (NAND/NOR-like gates). This framework can be used to perform a full-fledged analysis considering inter- and intra-die variations, with both random and systematic components. It can also be used to evaluate the usefulness of leakage saving techniques such as Gated-Ground, Gated-Supply, Dual-V_t and Sleep-mode V_{dd}, in the presence of process variations. The method used to derive this model can, in principle, be extended to other nanoscale devices such as Fully-depleted SOI MOSFET and Independent-gate DG MOSFET.

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