4.25 Gb/s Laser Driver: Design Challenges and EDA Tool Limitations

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ABSTRACT

This paper describes the design methodology, simulation, and tools used to design a 4.25 Gb/s high output swing laser driver (LD) and the electrical to optical interface from the LD to the laser diode. The quality of the optical output of a fiber optic communication channel is mainly determined by the LD and the electrical interface from the LD to the laser diode. Of particular importance in the interface is how well the LD overcomes the impact of the parasitic, resistive, capacitive, and inductive elements associated with the bondpad, bondwires, package, PCB transmission lines, passive components, and laser diode and its bondwires. The EDA tools used to model the electrical parasitics focus on RF and microwave applications and provide high frequency S-parameter models. This environment requires a stable time domain model of the electrical to optical interface. The presented LD integrated circuit operates from 155 Mb/s to 4.25 Gb/s with rise and fall times of 70 ps or less and a wide output voltage range, and a modulation current range of 5 mA to 85 mA.

Categories & Subject Descriptors

B.4.1 [**Input/Output and Data Communications]** Data Communications Devices

General Terms

Measurement, performance, design, reliability, verification.

Keywords

Laser driver, laser diode, electrical to optical interface.

1. INTRODUCTION

The information revolution is driven by low-cost computing, communication and data storage. The extraordinary increase in the speed of integrated circuits enables similar increases in the data rate of the communication channels connected to these devices. Consequently, electrical communication is increasingly being displaced by optical communication.

Since most information manipulation takes place in the electrical domain, it is necessary to transform the electrical signals to optical signals at the transmitter and to return optical signals into the electrical domain at the receiver. This transformation is implemented by using a LD to modulate the coherent light output of a laser diode. An optical fiber is used to guide the coherent optical signal to the receiver where the optical signal is transformed to an electrical signal by a photo diode and a transimpedance amplifier. Here, we describe the design challenges and tool limitations encountered during design and evaluation of a 4.25 Gb/s LD that directly modulates the laser diode.

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1.1 Application Environment: Classical versus Proposed LD

The function of translating a signal from the electrical domain to the optical domain is performed by a laser diode. The function of the LD is to receive the digital data signal and generate a digital output current that modulates the light output of the laser diode. The high speed data path of the LD can be viewed as a digital current switch. The following sections describe the LD and laser diode application and explain the challenge of modulating a laser without causing excessive timing jitter and inter-symbol interference in the optical signal.

1.2 Laser Driver/Laser Diode Application

The conventional LD architecture is shown in Figure. 1.

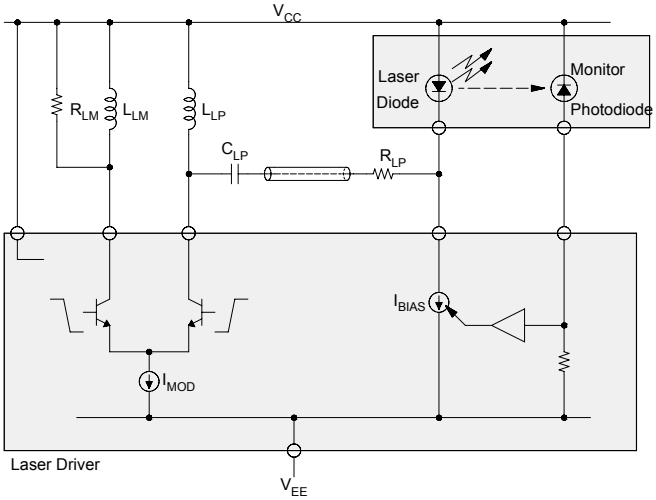


Figure 1. Conventional circuit diagram.

During normal operation, the laser diode is forward biased with a typical operating current of 30 mA. The dynamic impedance of the forward biased diode is 0.3 to 6 Ω; the parasitic series resistance is approximately 2 Ω. The external resistor of 10 to 15 Ω(R_{LP} in Figure 1) is used to critically damp the ringing

associated with the laser diode capacitance and bondwire/package inductance. It also increases the characteristic impedance of the transmission line connecting the output to R_{LP} to 20 Ω. (See Figure 1.)

The LD delivers a DC current (I_{BIAS}) that biases the laser diode so that when the switched current mirror is turned off, the laser is at the threshold and emits almost no coherent light. When the switched current mirror is turned on, the laser emits coherent optical light. The coherent light is sensed by the monitor photodiode, which is used to control the average optical power emitted by the laser diode.

The conventional architectures provide high speed symmetric rise/fall times and the back termination resistor damps any reflections and ringing caused by the laser diode bondwire inductance. However, half of the modulation current is wasted in the back termination resistor; furthermore, external AC coupling capacitors and inductors are required for level shifting. These high frequency components cause reflections and are expensive.

1.3 Advantages and Challenges of the New Design

A proposed architecture, which reduces modulation current by half, is shown in Figure 2. It saves about 85 mA (280 mW).

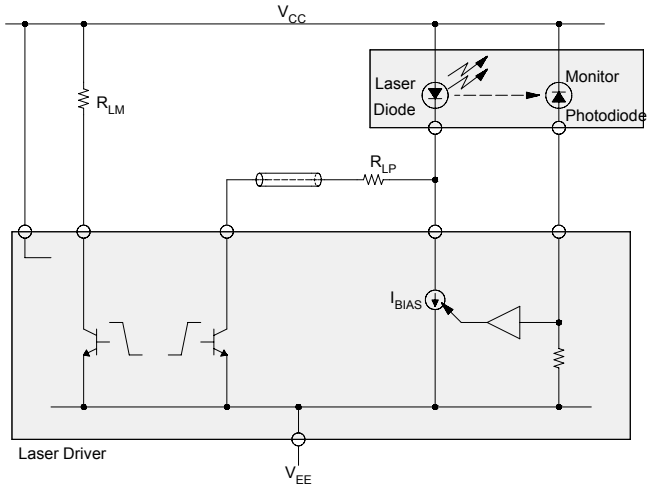


Figure 2: New laser driver architecture.

Additionally, external AC coupling capacitors and biasing inductors are not needed, thus avoiding reflections and cost. Further, a single external damping resistor is sufficient to critically damp the rise and fall time. Finally, an on chip, low power, active termination circuit absorbs reflections from the laser diode's bondwire and package. This LD architecture is described in more detail in [1] and [2].

There are challenges associated with the new architecture. First, the output driver must be able to swing from 0.4 V to V_{CC}. However, some applications may use AC coupling capacitors and biasing inductors, which require the output to swing from 0.6 V to V_{CC} + 2 V (5.6 V max.). This mode of operation is needed to allow the LD to be evaluated in optical modules that were designed for conventional LD architectures. Additionally, rise time, fall time, and overshoot/undershoot are sensitive to the LD output bondwire and package inductance. Further, removal of the passive back termination allows the LD to have an increased output current range, which requires the output driver to deliver 5 mA to 85 mA to the laser diode with constant rise and fall time.

1.4 Modeling the IC Package and the Bondwires

The design objective of reducing power by eliminating the passive back termination resistor causes increased sensitivity to the bondwire inductance, PCB board transmission line characteristics and laser diode package reflections. The LD bondwire inductance, in particular, causes overshoot and undershoot in the output current waveforms. Any overshoot in the current turn-on waveform causes additional overshoot in the optical signal, even when the laser diode is turned on by a current waveform without overshoot as shown in the measured optical output signal from a laser diode in Figure. 3. This overshoot results in "chirping" (unwanted frequency modulation) of the optical signal, which in turn encounters dispersion in the optical link and appears as undesired timing jitter at the receiver.

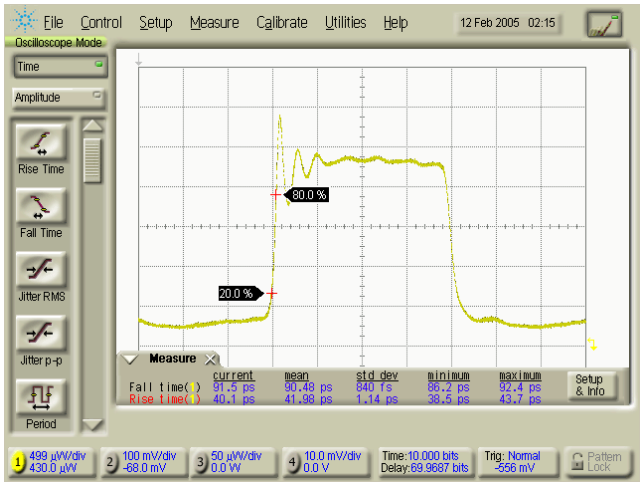


Figure 3. Measured laser diode optical output.

The most critical parameters that determine the LD overshoot/undershoot rise/fall times are the bondwire/package inductance, the output stage current density, and the emitter follower pre-driver bias current. Consequently, it is essential to model the bondwire/package parasitics accurately. A 3-D electromagnetic field solver was used to extract the resistance, capacitance, self and mutual inductance for the bondwires, package and leadframe. The model uses the die location, the bondpad locations, and the physical description of the package and leadframe to accurately determine the SPICE model. The 24 pin QFN package has an exposed leadframe at the back of the package and the typical values for the bondwire inductance are 1.2 nH. The adjacent pin mutual inductance coupling was K=0.7.

2. CIRCUIT AND DESIGN METHODOLOGY

2.1 Laser Driver Integrated Circuit Design

The new LD architecture achieves the low overshoot/ undershoot and fast rise/fall times by using a trimmed reference current and an approximately constant current density in the output NPN devices. The constant density is implemented using a segmented output architecture which turns on additional NPN output devices as the modulation current is increased.

This LD architecture achieves the low power supply voltage and the wide output voltage compliance range by using a grounded emitter NPN as the output device. This allows the output compliance voltage to be just one $V_{CE(sat)}$ above ground or 0.4 V.

The process was a Si-Ge BiCMOS technology with NPN f_T = 90 GHz. This was chosen because of the wide voltage swing from 0.4 V to VCC + 2 V [5.6 V], which is greater than the maximum allowed for high speed CMOS technologies.

2.2 Laser Driver Integrated Circuit Design Methodology

A challenging part of the design of a LD is the lack of a high speed electrical-optical SPICE model for the laser diode/monitor photo diode component. Consequently, the LD is defined with a series of specifications on the electrical performance in terms of rise and fall time, overshoot/undershoot, and random and deterministic jitter. Thus, when these electrical specifications were achieved, the optical performance was excellent.

The LD not only modulates the coherent optical light, but also biases the laser into the desired region of operation. Also, the LD protects the laser diode from destruction during startup, power-down and fault modes. The startup, fault, and disable simulations take a significant amount of time to run, and are simulated with longer timesteps. However, the eye diagrams require extremely fine timestep resolution.

2.3 Modeling the LD IC Parasitic RLCK Components

The areas of the circuit that required particular attention during design were the parasitic capacitance, resistance and the self- and mutual inductance of the high speed signal path. The entire power supply network series parasitic resistance and self- and mutual inductance were also extracted and the LD was simulated. The parasitic resistances associated with the contacts required the layout to be modified and transistors to be resized to allow a reduced contact resistance at the emitter.

2.4 Automated Laser Driver IC Simulation Test Bench

A script was used to automatically run the simulations using the parasitic netlist, the data sheet parameters were extracted and compared to the specification. A suite of eye diagrams were generated for comprehensive set of operating conditions.

2.5 IC EDA Tool Limitations and Proposed Improvements

Existing EDA tools output a flat parasitic extracted netlist which makes it very difficult to access the signals more than two levels down in the hierarchy, because of the unusual characters used to denote hierarchy in the signal names. An EDA tool that seamlessly maps hierarchical signal names between the design tool, scripting languages, and simulators would be a significant improvement. The ability to select signals names for accurate parasitic extraction from various levels of hierarchy would help limit parasitic netlist size. Current tools use an exclude list of signals not to be extracted.

3. EVALUATION BOARD DESIGN AND RESULTS

3.1 Laser Driver Electrical Evaluation

The electrical parameters are measured on an electrical evaluation board and the optical measurements are performed on a customer-designed fiber optic transceiver module.

The LD output active termination circuit was designed to drive a differential 20 Ω transmission line with an output signal range of 0.4 V to VCC + 2 V. However, the available test equipment requires lines with a 50 Ω characteristic impedance, and the signals must be referenced to the ground. Figure 4 is the schematic of the circuit used to transform the signal from a 20 Ω to a 50 Ω transmission line characteristic impedance.

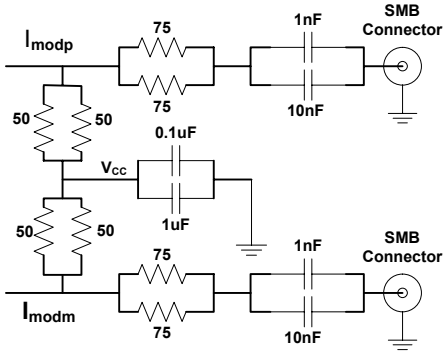


Figure 4: Schematic of LD output external components.

The evaluation board layout is shown in Fig. 5. Parallel resistors and capacitors are used to minimize the parasitic self inductance of the passive components.

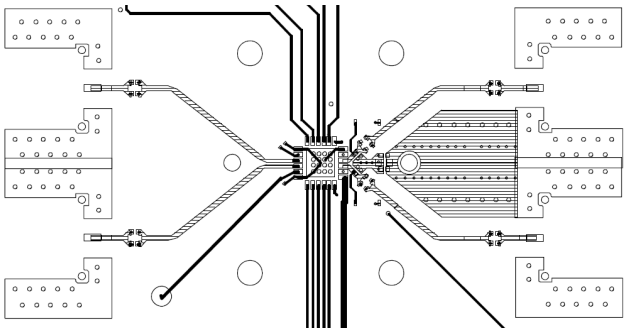


Figure 5. LD input (LHS) and output (RHS) board layout.

3.2. Evaluation board design, modeling and simulation

A 4-port s-parameter model was generated for the differential transmission lines using a 2½-D electromagnetic field solver (Agilent/ADS) and the evaluation board frequency response was simulated. A time domain simulation of the evaluation board was attempted but artifacts in the 4-port s-parameter model resulted in numerical oscillation and non-convergence causing the transient simulations to be in error. However, the measured frequency response of the evaluation board did not agree with the simulated frequency response because of unintended vias connecting two critical power supply decoupling capacitors and a recessed ground plane. Fortunately, test structures built on the evaluation board facilitated fully differential, 4-port S21 S-parameter measurements of the LD output transmission lines and passive components. The schematic for the LD output test structure is shown in Figure 6.

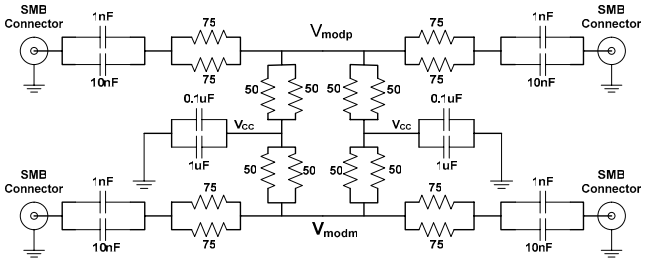


Figure 6: LD output test structure.

The LD output differential S21 S-parameter measurements for the original structure and for the corrected board are contrasted in Figure 7. A recessed ground plane caused the cable connectors to

appear inductive. The original board contained these two errors which caused the null of -30dB at 14.5 GHz in the SDD21 measurement shown in Figure 7. The ground plane was extended to the edge of the board immediately beneath the cable connectors and the decoupling capacitors were moved to the top layer. The corrected board measurement of the SDD21 is also shown in Figure. 7.

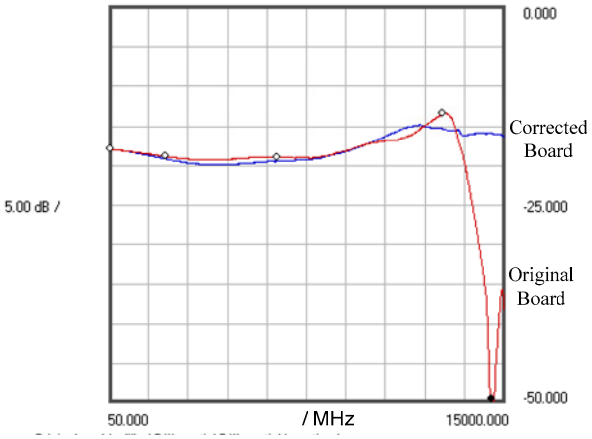


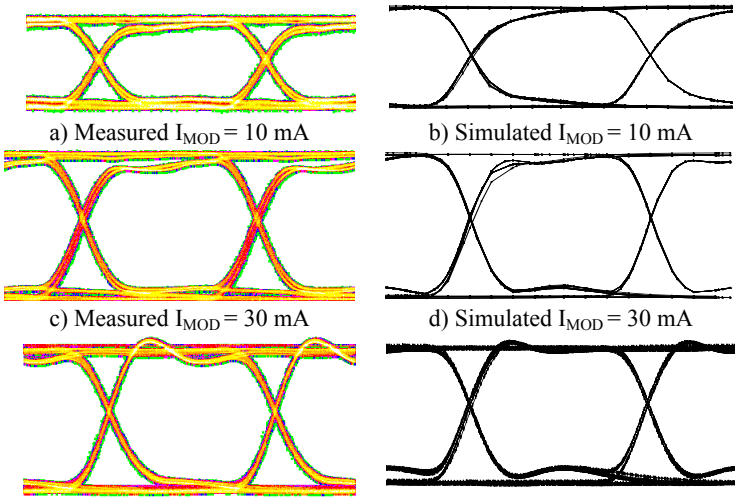
Figure 7. Measured SDD21 original & corrected test structure

3.3 PCB Modeling, Simulation and Parasitic Extraction Tools

Cost effective EDA modeling and simulation tools are not well integrated with the PCB layout tools. It would be useful to be able to extract the passive elements and transmission lines for specified nodes, generate a SPICE model, and then simulate the parasitic extracted circuit as is done with the IC tools. This would avoid the assumptions and errors inherent in manual extraction.

3.4 Laser Driver Simulation and Measurement Results

Figure 8 shows the measured and simulated eye diagrams as a function of modulation current (I_{MOD}). The careful work of parasitic extraction has helped achieve good agreement between measurement and simulation as shown in the eye diagrams.



a) Measured I_{MOD} = 10 mA b) Simulated I_{MOD} = 10 mA
c) Measured I_{MOD} = 30 mA d) Simulated I_{MOD} = 30 mA
e) Measured I_{MOD} = 85 mA f) Simulated I_{MOD} = 85 mA

Figure 8. Measured and simulated 4.25 Gb/s eye diagrams.

3.5 Laser Driver Optical Measurement Results

The optical measurements were performed by the customer on a production transceiver module. The optical eye diagram meets and exceeds the transmit mask at 4.25 Gb/s (Figure 9).

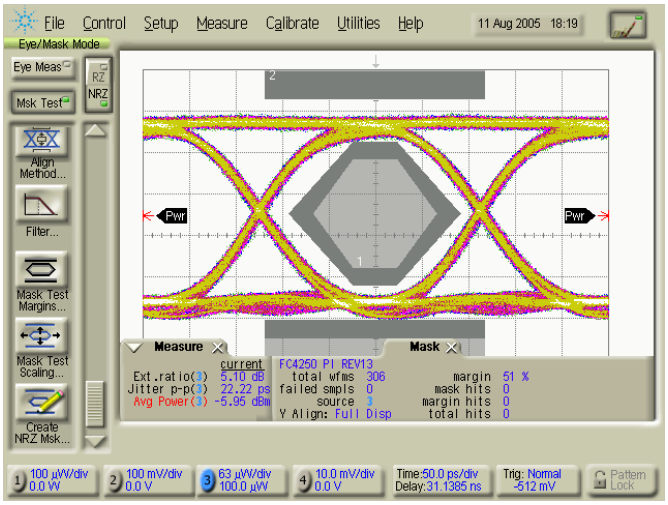


Figure 9. Measured 4.25 Gb/s Optical Eye Diagram

Table 1. Measured performance summary.

Supply voltage	3.0 V to 3.6 V
Ambient temperature range	-40°C to +85°C
Supply current (I_{MOD}=60 mA,I_{BIAS} = 100 mA)	44 mA
Modulation current range	5 mA to 85 mA
Modulation output voltage range	0.4 V to 3.6 V
Bias current range	1 mA to 100 mA
Bit rate	155 Mb/s to 4.25 Gb/s
Rise, fall times	<70 ps
Overshoot, undershoot	<12%
Deterministic jitter (k28.5 pattern)	<15 ps
Random jitter	640 fs

CONCLUSION

Given the challenges of designing a 4.25 Gb/s LD, it is essential for EDA tools to emerge that accurately extract the electrical properties of printed circuit board interconnect and vias and provide an accurate and stable time domain model as well as the traditional frequency domain S-parameter model.

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