A Design Approach for Radiation-hard Digital Electronics

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ABSTRACT

In this paper, we present a novel circuit design approach for radiation hardened digital electronics. Our approach is based on the use of shadow gates, whose task it is to protect the primary gate in case it is struck by a heavy cosmic ion. We locally duplicate the gate to be protected, and connect a pair of transistors (or diodes) between the outputs of the original and shadow gates. These transistors turn on when the voltages of the two gates deviate during a radiation strike. Our experiments show that *at the level of a single gate*, our circuit structure has a delay overhead of about 4% on average, and an area overhead of over 100%. At the circuit level, however, we do not need to protect all gates. We present a methodology to selectively protect specific gates of the circuit in a manner that guarantees radiation tolerance for the entire circuit. With this methodology, we demonstrate that *at the circuit level*, the delay overhead is about 4% and the placed-and-routed area overhead is 30%, compared to an unprotected circuit (for delay mapped designs)

Categories and Subject Descriptors: B.8.2 [Performance and Reliability]: Reliability, Testing, and Fault-Tolerance

General Terms: Design, Reliability

Keywords: SEU, Radiation-hard

1. INTRODUCTION

In recent times, there has been an increased interest in the radiation immunity of electronic circuits [1, 2, 3, 4, 5, 6, 7, 8, 9]. This has been an area of significant interest and research for space or military electronics [8, 7, 10, 11] for many years, due to the significantly larger rate of radiation bombardment in such applications. For space application, neutrons, protons and heavy cosmic ions which are trapped in geomagnetic belts [10] produce intense showers of such radiation. When such ions strike diffusion regions in VLSI designs, they can deposit charge, resulting in a voltage spike on the affected circuit node. If the magnitude of this spike is sufficiently large, an erroneous value may be computed by the circuit. This is particularly problematic for memories, which can flip their stored state as a result of such a radiation strike. Combinational logic may also be affected by such strikes, if the resulting glitch occurs at the time the circuit outputs are being sampled. Such bit reversals are referred to as Single Event Upsets (SEUs) [12], or soft errors in the case of memory.

The charge deposition rate is also referred to as the Linear Energy Transfer (LET). Cosmic ions have varying LETs, and they result in the deposition of a charge Q in a semiconductor diffusion region of depth t by the following formula [11].

$$Q = 0.01036 \cdot L \cdot t$$

Here L is the LET of the ion (expressed in MeV/cm^2/mg), t is the depth of the collection volume (expressed in microns), and Q is charge in pC. The amount of charge that is required to cause a bit to be sampled incorrectly is referred to as the critical charge, Q_C [13]. With diminishing process feature sizes and supply voltages, SEU problems are a concern even for terrestrial electronics today, particularly for mission critical applications. Atmospheric neutrons as well as alpha particles which are created by unstable isotopes in the IC packaging materials can also cause SEU problems. For reference, the LET of a 5 MeV alpha particle is 1 MeV/cm^2/mg [5]. Also, the probability distribution of energetic particles drops off rapidly with increasing LETs [2]. The largest population of particles have an LET of 20 MeV/cm^2/mg or less, and particles with an LET greater than 30 MeV/cm^2/mg are exceedingly rare [2, 3].

The current pulse that results from a particle strike is traditionally described as a double exponential function [14, 15]. The expression for this pulse is

$$I(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

Here Q is the amount of charge deposited as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment constant. Based on the values used in [9], for the simulations reported in this paper, we used values of τ_β = 5ps, and varied the values of τ_α from 10ps to 100ps, and Q from 1fC to 10fC.

The remainder of this paper is organized as follows: Sec-

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tion 2 discusses some previous work in this area. In Section 3 we describe our radiation hardened design approach for digital electronics. In Section 4 we present experimental results, while conclusions and future work are discussed in Section 5.

2. PREVIOUS WORK

There has been a great deal of work on radiation hardened circuit design approaches. Several papers report on experimental studies in this area [11, 13, 4, 16, 8], while others have focused on memory design [12, 13, 9, 17, 6, 7]. Since memories are particularly susceptible to SEU events, these efforts were crucial to space and military applications. Yet other approaches perform modeling and simulation of radiation events [15, 2, 5]. In [1], the authors address the sizing of transistors in a digital design in order to improve the radiation hardness of the design. In [9], the authors provide a built-in current sensor (BICS) to detect SEU events in an SRAM. A radiation hardened DRAM design was proposed in [17], while a FLASH memory based FPGA was introduced in [8].

Other radiation hard design approaches tackle the problem of correcting errors at the system level, such as triple modulo redundancy. In contrast to these approaches, we provide a method to design radiation hard combinational logic. It can be used for memory elements as well. Our approach uses the notion of a clamping circuit which protects the output of a gate from an SEU incident. We also present a methodology to selectively protect a standard-cell based design, in a manner which requires a minimum number of gates to be modified. Our experimental results demonstrate that the area and delay overheads of our approach (compared to an unprotected circuit) are 30% and 4% respectively, for delay mapped circuits.

3. OUR APPROACH

Radiation strikes cause charge to be dumped on a diffusion node, which results in voltage glitches on these nodes. We are concerned with those glitches that cause nodes to change their logical value (i.e. those that cross the switch-point of the gate in question). Our solution to the SEU problem involves a novel circuit design technique which ensures that such a glitch is clamped before it reaches the switch-point.

This section is divided into three subsections. In Section 3.1, we discuss two circuit structures (shown in Figures 1 and 2) that we investigated, in order to create a radiation-hardened standard cell. Section 3.2 discusses the notion of *critical depth* for any protected library cell. A larger critical depth for any cell indicates that we require more logic stages for this cell to erase the effects of a radiation-induced glitch. Based on the notion of critical depth, Section 3.3 describes our algorithm to selectively protect cells in a standard-cell based circuit, so as to minimize the delay and area overhead.

3.1 Working of the Clamping Devices

A clamping diode can be used to suppress a glitch. However, this clamping diode should not prevent (or delay) the switching of the logic during its normal functional operation when no radiation strike has occurred. We hence need another similarly sized driver (logic gate) in parallel with the gate we are trying to protect (shown in Figures 1 and 2). When the outputs of these drivers deviate significantly

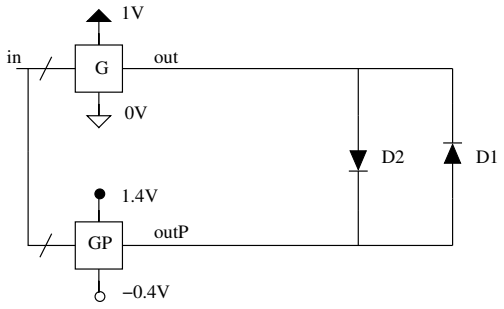

Figure 1: Diode based SEU Clamping Circuit

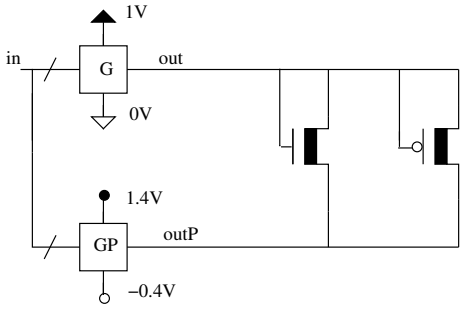

Figure 2: Device based SEU Clamping Circuit

(which would occur when one of the gates undergoes a radiation strike), the clamping circuit turns on, thereby protecting the gate from an SEU event. Note that the supply voltages for the protecting gate are higher (VDD = 1.4V and VSS = -0.4V). The devices used in the protecting gate have a higher V_T (V_T^p = -0.42V and V_T^n = 0.42V) compared to the regular devices in our design (which have $V_{T_n} = 0.22V$ and $V_{T_p} = -0.22V$). This is to minimize the leakage through the protecting gate. The devices used for clamping also have a higher V_T to make sure that they are off during regular operation (in the absence of SEU events). This is important since their inputs are the same as those of the protected gate. In fact the clamping devices are on the verge of conduction (since V_T^p = -0.42V and V_T^n = 0.42V). Ideally we would want the protecting gate to have an even higher V_T (to minimize the leakage through this gate), but we restrict ourselves to two V_T values in this paper. The clamping diodes used can either be regular PN junction type diodes or diode connected devices. We investigated both options.

3.1.1 PN Junction Diode

Consider the circuit in Figure 1. Let us first consider an SEU event that causes a rising pulse on the output node of a protected gate which is at logic 0. This means that the steady state output of the protected gate is at 0V and that of the protecting gate is at -0.4V. When the voltage on the protected node starts rising and when the voltage across the diode D2 (in Figure 1) reaches the diode turn-on voltage, it begins to clamp the voltage across it. In this way the glitch due to the SEU event is suppressed.

Now let us consider the case of an SEU event striking at the output (outP) of protecting gate which is at logic 0. In this case the protected node is still protected (remains at logic 0). This is because the protecting node is initially at

a much lower voltage (-0.4V) and as the voltage at the protecting node rises, the diode D2 remains turned-off. Diode D1 turns on only when the voltage at the protecting node rises to a value greater than the diode turn-on voltage (i.e. voltage glitch = 0.4 + diode turn-on voltage). However, the cosmic particle which can cause such a glitch would have to have a very high energy.

The working of the clamping structure for falling pulses when the output node is at logic 1 is similar to that discussed above.

3.1.2 Diode Connected Device

Consider the circuit in Figure 2. Let us once again, consider a radiation event that causes a rising pulse on a node at logic 0. This means that the steady state output of the protected gate is at 0V and that of the protecting gate is at -0.4V. When the voltage on the protected node starts rising, the clamping NMOS device starts to turn on and turn on more strongly if the voltage on the protecting node continues to rise, thus clamping the protected node. If the radiation event strikes at the protecting nodes, the protected node remains at logic 0. This is because the protecting node is initially at a much lower voltage (-0.4V) and as the voltage at the protecting node rises, the clamping NMOS device turns off more. It is only when the voltage of the protecting node rises above 0.4V that the clamping PMOS device starts turning on. This could cause the voltage of the protected node to rise. As discussed in section 3.1.1 a radiation event to cause such a glitch would have to be very large.

In a similar manner, the clamping PMOS device helps protect a gate from a falling pulse due to a radiation event.

Both the device-based and diode-based clamping structures were implemented, and had very similar protection characteristics, as shown in the sequel. The layout area penalty of the device-based clamping structure was determined to be lower than that for a diode-based clamping structure. As a consequence, the experiments reported in the sequel are all based on the device based clamping structure.

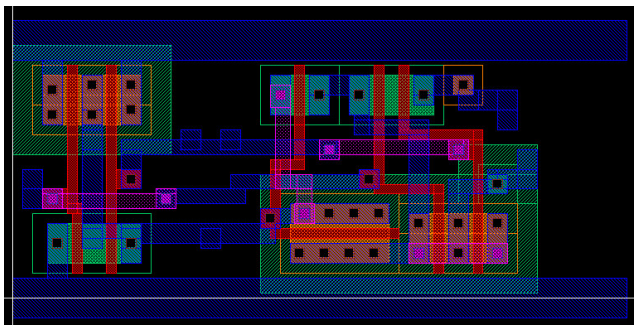

Figure 3: Layout of SEU-tolerant NAND2 gate (uses Device based Clamping)

3.2 Critical Depth for a Gate

. For each of the cells in our library, we designed counterpart cells which were radiation hardened, using diode connected devices to achieve radiation hardening. For each such radiation hardened cell, we computed its *critical depth*.

Consider a sequence of n copies of the same library cell C, with the output of the i^{th} cell being one of the inputs of the $(i+1)^{th}$ cell. Let all the other inputs of the $(i+1)^{th}$ cell be assigned to their non-controlling values. Assume that the radiation strike occurs on the output of the cell at the first level, and corresponds to a charge Q being dumped on the output node at the first level, with a collection time constant τ_α, and a ion track establishment constant of τ_β. Based on Equation 1, we can compute the effective current source that is connected to the corresponding output. Then the critical depth of library cell C, denoted as $\Delta(C)$, is defined as the number of levels of logic that are required for the magnitude of the glitch due to the radiation event to become smaller than $\gamma \times VDD$, where $\gamma < 1$. Note that $\Delta(C)$ is a function of Q, τ_α, and τ_β. The vaules of as $\Delta(C)$, were estimated using SPICE simulations.

3.3 Circuit Level Radiation Hardening

A simplistic approach would be to protect each gate in the design using our approach. However, this would result in an exorbitant delay and area overhead for the circuit. Instead, we propose a method where the delay and area overhead is minimized, while guaranteeing radiation hardness for the circuit.

Let $\Delta = max_C(\Delta(C))$. Given any circuit, we can protect all gates that are topologically Δ or less levels away from any primary outputs of the circuit. In this case, if there is a radiation strike on any protected cell, it would be eliminated because the cell is protected. If there is a radiation strike on an unprotected cell, it would be eliminated since it needs to traverse through Δ or more levels of protected gates before it reaches the output. In either case, the circuit is tolerant to the radiation event.

A variant of the above approach, which is slightly more efficient, is based on *variable depth protection*, and is described in Algorithm 1. It is based on the a reverse topological traversal of a circuit η from its primary outputs. Let $deptharray()$ be the array of critical depths of all the library cells used in the implementation of the circuit η. The algorithm starts with a requirement to protect gates up to a reverse topological depth $D = \Delta$. Whenever a gate C with critical depth $\Delta(C)$ is encountered, the algorithm updates the depth to be protected as $D = min(D-1, \Delta(C))$.

Algorithm 1 Variable Depth Radiation Hardening for a Circuit

```
variable_depth_protect(η, deptharray)
for each p ∈ PO(η) do
  D = Δ
  for each cell C such that p ∈ fanout(C) do
    D = min(D − 1, Δ(C))
    if D > 1 then
      Replace C by C_hardened
    end if
  end for
end for
```

4. EXPERIMENTAL RESULTS

The SEU tolerance of both our circuit structures was simulated in SPICE [18]. We used a 65nm BPTM [19] model card, with $VDD = 1V$ and $V_{T_N} = |V_{T_P}| = 0.22V$. The radiation strike was modeled as a current source described as $I(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta})$.

Based on [9], we used a value of $\tau_\beta = 5ps$. We varied the values of τ_α and Q, to test our design against a variety of ra-

diation conditions. Figure 4 describes the current injection waveform for various values of Q and τ_α.

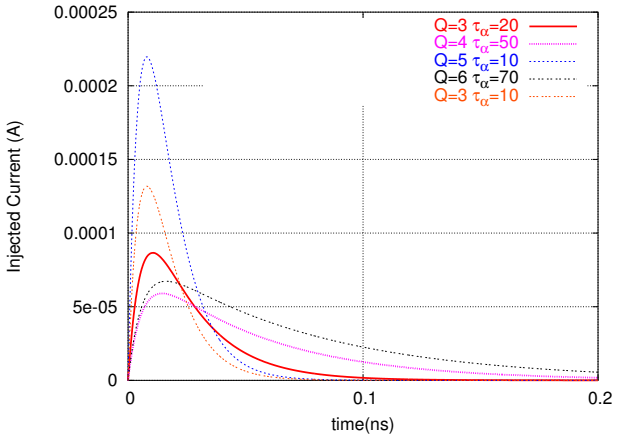

Figure 4: Current Injection Waveform as a Function of Q and τ_α

The performance of both our designs is summarized in Tables 1, 2, 3 and 4. These tables report the protection results for the INV-2X gate, which is the most radiation sensitive gate in our library. The first two tables report the simulation results for diode based clamping, and the latter two describe the results for device based clamping. For both styles, we report the glitch magnitude for varying values of τ_α and Q. The first and third tables report values of glitch magnitudes when the output is at logic 0, while the second and fourth correspond to an output at logic 1.

Q(fC)	Decay time τ_α (ps)				
	10	20	30	40	50
1	0.0674	0.0513	0.0422	0.0358	0.0300
2	0.1400	0.1069	0.0869	0.0737	0.0651
3	0.2152	0.1640	0.1335	0.1149	0.0978
4	0.2883	0.2224	0.1810	0.1538	0.1332
5	0.3553	0.2788	0.2280	0.1945	0.1692
6	0.4242	0.3313	0.2737	0.2355	0.2037
7	0.4951	0.3829	0.3196	0.2714	0.2363
8	0.5704	0.4386	0.3601	0.3088	0.2710
9	0.6425	0.4979	0.4094	0.3480	0.3026
10	0.7139	0.5574	0.4551	0.3837	0.3355

Table 1: Performance of PN Junction Clamping Diode for Rising Pulses (output at logic 0)

Q(fC)	Decay time τ_α (ps)				
	10	20	30	40	50
1	0.0572	0.0005	0.0004	0.0003	0.0003
2	0.1219	0.0959	0.0778	0.0647	0.0006
3	0.1934	0.1460	0.1231	0.1046	0.0912
4	0.2477	0.1973	0.1741	0.1412	0.1244
5	0.3015	0.2493	0.2069	0.1794	0.1571
6	0.3629	0.2963	0.2493	0.2179	0.1899
7	0.4250	0.3387	0.2892	0.2498	0.2199
8	0.4823	0.3859	0.3214	0.2802	0.2493
9	0.5460	0.4287	0.3627	0.3147	0.2775
10	0.6116	0.4801	0.3977	0.3443	0.3062

Table 2: Performance of PN Junction Clamping Diode for Falling Pulses (output at logic 1)

Q(fC)	Decay time τ_α (ps)				
	10	20	30	40	50
1	0.0793	0.0580	0.0497	0.0399	0.0335
2	0.1646	0.1224	0.0983	0.0810	0.0769
3	0.2572	0.1894	0.1508	0.1276	0.1087
4	0.3502	0.2579	0.2061	0.1719	0.1482
5	0.4536	0.3315	0.2633	0.2189	0.1879
6	0.5663	0.4105	0.3235	0.2698	0.2291
7	0.6789	0.4925	0.3852	0.3185	0.2726
8	0.7960	0.5810	0.4558	0.3728	0.3164
9	0.9183	0.6742	0.5275	0.4302	0.3640
10	1.0432	0.7715	0.6009	0.4897	0.4152

Table 3: Performance of Diode-connected Clamping Device for Falling Pulses (output at logic 0)

Q(fC)	Decay time τ_α (ps)				
	10	20	30	40	50
1	0.0753	0.0627	0.0484	0.0410	0.0338
2	0.1582	0.1204	0.0963	0.0811	0.0701
3	0.2438	0.1835	0.1502	0.1248	0.1111
4	0.3335	0.2509	0.2009	0.1689	0.1463
5	0.4246	0.3180	0.2555	0.2146	0.1851
6	0.5229	0.3881	0.3124	0.2612	0.2273
7	0.6249	0.4621	0.3691	0.3081	0.2652
8	0.7319	0.5397	0.4281	0.3567	0.3076
9	0.8436	0.6200	0.4909	0.4070	0.3493
10	0.9579	0.7055	0.5559	0.4595	0.3934

Table 4: Performance of Diode-connected Clamping Device for Falling Pulses (output at logic 1)

Based on these tables, we find that the regular PN junction diode tended to have better protection performance than the diode connected device for the same active area. However, implementing the PN junction diodes could require a larger area on account of the spacing requirements of the wells which are at different potentials. The diode connected devices on the other hand share their well with the devices in the protecting gate, and can be implemented efficiently. Figure 3 describes the device-based clamping approach, applied to an inverter gate. The area of the resulting layout is slightly larger than twice the area of a regular inverter. We created the layouts of the protected versions of all gates in our standard-cell library, which consisted of the cells INV-2X, INV-4X, AND2, AND3, AND4, OR2, OR3, OR4, NAND2, NAND3, NAND4, NOR2, NOR3 and NOR4.

Figure 5 describes the voltage waveform at the output of a gate, when a current corresponding to $Q = 4$ fC and $\tau_\alpha = 10ps$ is injected into this node. The voltage waveform of the unprotected design experiences a large glitch. If it were part of a memory element, the element could have erroneously flipped. Our device based clamping circuit successfully clamps the voltage to a safe level.

Figure 6 shows the voltage waveform at the output of a gate, when a current corresponding to $Q = 4$ fC and $\tau_\alpha = 10ps$ is injected into *the protecting* node. The voltage waveform of the output node is well within the noise margins of the gate.

Based on the fact that we utilize the device-based protection scheme due to its better layout characteristics, we find the largest value of Q, for the most aggressive value of $\tau_\alpha = 10ps$ that our INV-2X cell can tolerate (from Tables 3 and 4). For $\gamma = 0.35$ (i.e. we can tolerate a glitch magnitude of 0.35×VDD), we find that $Q = 4$fC.

Based on the values of $\tau_\alpha = 10ps$ and $\tau_\beta = 5ps$, we computed the critical depth $\Delta(C)$ for each gate C in our stan-

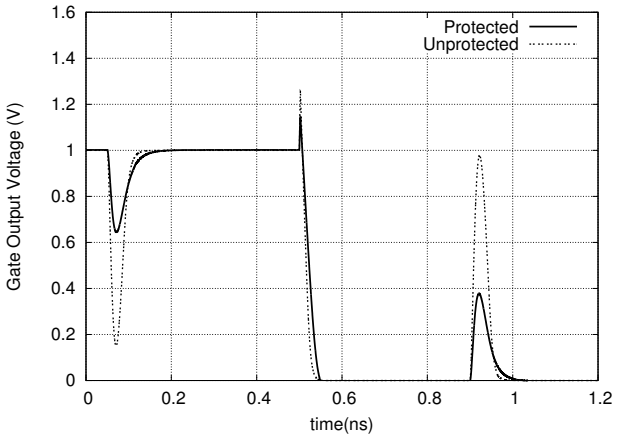

Figure 5: Output Waveform during a Radiation Event on Output

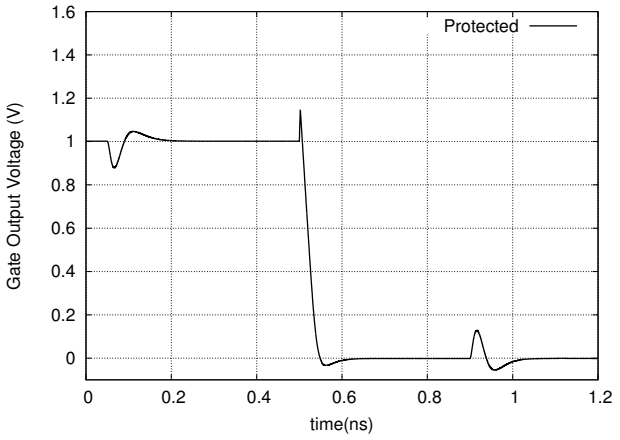

Figure 6: Output Waveform during a Radiation Event on Protecting Node

dard cell library. We used a value of $Q = 5$fC, a quantity which is larger than the charge which results in a glitch magnitude of 0.35×VDD. The results of this exercise are presented in Table 5 in Column 5. In addition to critical depth, Table 5 also reports the worst-case delay of each cell (in picoseconds), for the protected (Column 3) and unprotected (Column 2) versions of the cell. Column 4 reports the percentage overhead in the worst-case delay of the hardened version of each cell compared to the regular version. Note that the worst-case delay of the protected cell is on average just slightly larger than that of a regular cell.

The delay penalty associated with applying our variable depth protection algorithm are presented in columns 2 to 6 of Table 6. Delays were computed using the *sense* [20] package in SIS [21], which computes the largest sensitizable delay for a mapped circuit. In Table 6, Columns 2 and 3 report the delay (in picoseconds) of a regular design and a radiation-hardened area-mapped design. Column 4 reports the percentage delay overhead for the radiation-hardened design. Similarly, Columns 5 and 6 report the delay (in picoseconds) of a regular design and a radiation-hardened delay-mapped design. Column 7 reports the percentage delay overhead

Cell	Regular	Hardened	% Ovh.	Depth
inv2AA	24.614	28.012	3.40	5
inv4AA	23.914	23.576	-0.34	1
nand2AA	31.416	34.993	3.58	1
nand3AA	44.92	48.39	3.47	1
nand4AA	62.436	66.259	3.82	1
nor2AA	45.617	49.902	4.29	1
nor3AA	77.151	82.786	5.64	1
nor4AA	92.80364	95.38472	2.58	1
and2AA	57.476	61.911	4.44	2
and3AA	76.902	82.722	5.82	1
and4AA	98.752	107.329	8.58	1
or2AA	71.161	74.678	3.52	1
or3AA	112.871	116.304	3.43	1
or4AA	125.165	128.543	3.38	1
AVG			3.97	

Table 5: Characteristics of Hardened Cells

for the radiation-hardened design. We note that the circuit-level delay overhead of our radiation-hardened approach is as low as 3.3% on average for delay mapped designs, and about 4.2% for area mapped designs. Note that our radiation hardened designs are generated by replacing regular gates (which are topologically close to the outputs) by hardened gates. This results in a large increase in the load capacitance of the regular gates that drive the hardened gates. As a consequence, the circuit level delay penalty in Table 6 is sometimes larger than the gate-level delay penalty reported in Table 5. We technology mapped both the regular and the radiation hardened circuits using the library of cells mentioned earlier. The resulting designs were placed and routed using SEDSM [22]. The area penalty associated with applying our variable depth protection algorithm is presented in columns 8 to 13 of Table 6. In Table 6, Columns 8 and 9 report the placed-and-routed area (in μ^2) of a regular design and the radiation-hardened area-mapped design. Column 10 reports the percentage area overhead for the radiation-hardened design. Similarly, Columns 11 and 12 report the area (in μ^2) of a regular design and a radiation-hardened delay-mapped design. Column 13 reports the percentage area overhead for the radiation-hardened design. We note that the area overheads on average are larger for area-mapped designs, which is reasonable since the designs were mapped with an area-based cost function. The average area penalty was about 53% and 30% for area and delay mapped designs respectively. This is significantly lower than the area overheads associated with alternate radiation hardening approaches, which commonly require logic duplication or triplication. Some designs (such as *frg2*) have a low logic depth and large number of inputs, and consequently, their area overheads are higher.

5. CONCLUSION

In this paper, we have presented a novel circuit design approach for radiation hardened digital electronics. Our approach uses shadow gates to protect the primary gate in case it is struck by radiation. We locally duplicate the gate to be protected, and connect a pair of diode-connected transistors (or diodes) between the outputs of the original and shadow gates. These transistors turn on when the voltages of the two gates deviate during a radiation strike. The delay overhead of our approach per library gate is about 4%. The area overhead of our approach is greater 100% per library gate.

Ckt	Delay Overhead						Area Overhead					
	Area Mapping			Delay Mapping			Area Mapping			Delay Mapping		
	Regular	Hardened	% Ovh.	Regular	Hardened	%Ovh.	Regular	Hardened	% Ovh.	Regular	Hardened	%Ovh.
alu2	1057.99	1068.913	1.03	959.113	976.987	1.86	1045.88	1728.90	65.31	1439.44	1728.90	20.11
alu4	1318.652	1357.851	2.97	1247.762	1259.695	0.96	2019.60	2830.24	40.14	2470.09	3343.15	35.35
C1355	887.619	920.186	3.67	711.149	720.345	1.29	1592.01	2252.45	41.48	1728.90	2279.11	31.82
C1908	1301.522	1349.072	3.65	1085.28	1093.79	0.78	1569.74	2252.45	43.49	1799.46	2279.11	26.66
C3540	1546.819	1625.472	5.08	1414.443	1424.782	0.73	3136.00	4763.76	51.91	4022.10	5077.99	26.25
C499	887.619	920.186	3.67	711.149	720.345	1.29	1569.74	2265.76	44.34	1728.90	2279.11	31.82
C880	1489.53	1643.51	10.34	1405.322	1554.847	10.64	1045.88	1883.56	80.09	1397.26	2252.45	61.20
dalu	1167.817	1252.608	7.26	1056.534	1077.134	1.95	2470.09	3540.25	43.32	3310.85	3986.66	20.41
des	1725.922	1452.655	-15.83	1615.74	1645.817	1.86	9964.03	14496.16	45.48	12139.63	15074.93	24.18
frg2	825.852	912.605	10.50	792.849	836.477	5.50	1994.52	4725.19	136.91	2611.21	4057.69	55.40
i2	451.879	463.949	2.67	363.611	382.298	5.14	686.61	745.29	8.55	872.61	948.64	8.71
i3	172.865	184.777	6.89	172.865	184.777	6.89	495.51	586.61	18.39	495.51	566.44	14.32
C7552	2012.924	2100.094	4.33	2005.371	2070.491	3.25	7032.50	12638.26	79.71	7953.07	9576.58	20.41
i10	1997.302	2253.81	12.84	1931.211	2002.74	3.70	6845.90	9604.00	40.28	7705.32	11291.18	46.53
AVG			4.22			3.28			52.81			30.22

Table 6: Delay and Area Overhead of Our Radiation Hardened Design Approach

In addition, we present an approach to perform *circuit-level radiation hardening with very low delay and area overheads*. In this approach, we minimize the number of gates that need to be protected in the manner described above. The resulting circuit is made radiation hardened, with a very low area and delay penalty (30% and 4% on average, for delay mapped designs) compared to an unprotected circuit. In practice, however, a very small fraction of gates needs to be protected. We anticipate that our approach could be used in memory elements, or even the gates that drive memory elements. In this way, our approach can protect both combinational and sequential circuits from SEU events.

In the future, we plan to incorporate radiation hardening into the technology mapping step.

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