An Up-stream Design Auto-fix Flow for Manufacturability Enhancement

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ABSTRACT

Although many physical limitations have been reached in modern micro-lithography, printed critical dimensions continue to shrink according to the International Technology Roadmap for Semiconductors (ITRS) [1]. To meet the demands imposed by this guideline, the traditional separation between design and manufacturing communities is being bridged. Many EDA tools package manufacturing data for delivery into established simulation engines for design *verification*. However, none of them provide practical implementations of design *optimizations* at an early stage in the design flow.

This paper presents an automated layout modification flow for metal layers with the goal of enhancing manufacturability. It can easily be deployed in a current custom design flow in a way that is visible to designers. The result of this scheme is improvements to process windows and yield, while minimizing circuit performance detractors. The flow is verified through analyses of both the impact on circuit performance and the benefit to manufacturability. It has been implemented in a state-of-the-art 65 nm chip design. Both silicon yield and electrical performance data are currently being collected and analyzed.

Categories and Subject Descriptions: B.7.2 [Integrated Circuits]: Design Aids −*layout, verification*; B.8 [Hardware]: Performance and reliability −*Performance, analysis and design aids*

General Terms: Design, Algorithms, Performance

Keywards: DFM, OPC, layout, design flow

1. INTRODUCTION

As Moore's Law continues to guide technology node shrinking, manufacturing yield has been an increasingly problematic issue. Various design optimization techniques have been deployed that have proven to be essential for yield enhancement. Such yield enhancement practices include optical proximity correction (OPC), adjustments made to the design layout before OPC to accommodate non-linear technology "shrinking" [2] and redundant via insertion. However all of these optimizations are applied after design sign-off, and are invisible to designers. Various approaches to providing performance guardbands with different variability modeling have been proposed [3, 4, 5, 6]. Process variation inherently gives rise to circuit performance uncertainty. A recent study shows the worst-case slack may increase by 36.4% due only to gate CD OPC side-effects and inaccuracies[7]. As techniques altering layout after design sign-off have become standard in the design flow, there have been requests from the design community to provide design-time visibility and controlability of the modifications.

Restrictive design rules [8] have been utilized on critical layers to improve pattern printability and reduce variations introduced by lithography distortions. As a result, variations on metal layers have become more critical. This has placed an increased emphasis on methods to improve metal printability and process margins.

In this paper we present an automated up-stream DFM layout modification flow for metals that is intended to enhance process latitudes. The flow allows designers to review modifications and corresponding parasitic impact on circuit performance prior to sign-off. It is scalable to large designs or components. The layout modifications are intended to complement "recommended" rules in custom designs by providing an automated framework in which to apply them. The flow is verified from simulations in terms of its impact on both manufacturability and circuit performance. Electrical data is being collected on chips developed with this flow.

In the next section, we describe the overall methodology of the up-stream DFM metal auto-fix flow including the manufacturing issues that are addressed and how the flow is integrated in a standard design flow. Section 3 describes our experiments and results based on a 65nm design. Section 4 summarizes our findings and discusses future approaches for feasible DFM methodologies in volume production.

2. DFM METAL AUTO-FIX ALGORITHMS

Several pervasive manufacturing issues can be alleviated by algorithmically modifying large layouts. This section describes the functionality and parameter optimizations of four such algorithms, their interactions, and their application within the current industry design flow.

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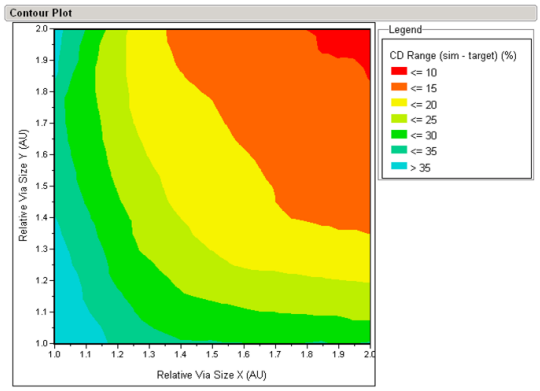

Figure 1: Via CD variation as a function of via size across the focus/exposure matrix simulation as a percent of the total via size.

2.1 BEOL Manufacturing Concerns and Corresponding DFM Treatment

Algorithms to address four metal layout events will be discussed in this section: metal enclosure of upsized vias, notch fill, metal line end extensions, and jog segment widening. Although some of these operations are available in commercial DFM-aware routers, this flow provides the advantage of performance impact visibility to the designers as well as application to lower BEOL layers, which are not typically touched by routers. All of the algorithms are governed by sets of parameters, which allow control of how much metal is inserted and ensure that the output will receive appropriate OPC treatment. All added geometries must pass embedded DRC checks as a precondition to placement, eliminating the possibility of introducing DRC violations.

Metal Enclosure of Upsized Vias. Via doubling has long been proposed as a low-cost back-end-of-line (BEOL) yield improvement technique. However, the number of vias enhanced by this practice is limited by the space available in the layout. Alternatively, expanding individual via edges based on neighboring feature proximity affords a far greater number of improved vias. E.g., in a representative microprocessor layout, via doubling affected 7.37% of the via1 features while the via edge movement approach modified 98.65% of via1's. Enlarged vias print more predictably across lithography focus and exposure variations, and result in lower resistance connections. Figure 1 shows the simulated process window for a range of via sizes. Note the dramatic improvement in CD control from ∼43% of the drawn via dimension at the nominal size vs. only 20% if the via size is enlarged to 1.4 times the nominal dimension in both directions.

The size of a design footprint is heavily influenced by the drawn contact and via dimensions. Typically, most contacts and vias are patterned near the lithography resolution limit to minimize die size. The manufacturing process is usually tuned to achieve sufficient CD control, and therefore consistent via resistivity at nominal via pitch. With off-axis illumination, looser pitches manifest additional variability and a greater risk of open vias than do dense vias. The via edge movement algorithm is well suited to address this issue because it upsizes vias according to their degree of isolation. The results are reductions in both CD variation and risk of open vias.

The algorithm evaluates each via edge independently with respect to its distance from other vias as well as top and bottom metals on different electrical nodes. If enough space exists to accommodate spacing design rules as well as their respective margins, then an edge is moved a prescribed distance. Otherwise the edge remains stationary. This scheme results in a limited set of possible via shapes and sizes. In cases where a via edge is moved beyond its underlying metal, that metal feature is grown an identical amount to ensure proper landing.

Metal Notch and Gap Fill. One consideration of the metal enclosure algorithm is the introduction of unlanded vias where the enlarged via falls off of the underlying metal. Since the via upsizing algorithm guarantees that this distance is sufficiently spaced from neighboring features, the underlying metal enclosure of via is forced in order to prevent any issues with unlanded vias etching into the underlying dielectric. This practice results in many new metal vertices (notches). Those that are placed near line ends may prevent adequate fragmentation for OPC and will cause additional reticle write time. This issue can be addressed by a notch fill algorithm. Established notch fill algorithms exist in many shapes and forms. This algorithm is custom designed to allow parametric control of appropriate dimensions to ensure compatibility with prevailing layout practices and with output from the preceeding algorithm.

Metal Line End Extension. Another common manufacturing issue is insufficient metal enclosure of contacts and vias. Line-end shortening and narrowing can cause nominally enclosed vias and contacts to have elevated resistances or to open completely. Design rule compliant layout typically contains a majority of metal line ends that enclose vias and contacts using minimum design rules despite an abundance of space to neighboring metal features. Algorithmic selection of metal line ends to extend, and determination of extension length represents a low-cost opportunity to enhance yield.

In this routine, relatively narrow metal line ends are identified as candidates for extension based on their enclosure of a contact or via as well as proximity to neighboring metal features. Candidate line ends are extended such that they are less than or equal to a maximum extension parameter. In cases where metal extensions would interfere with one another, the space between them is shared equally such that the design rule value plus a margin parameter spacing is obeyed. Growing metal area can cause an increase in bridging critical area. The algorithm parameters allow balance between susceptibility to high resistance vias and contacts, and to bridging and leakage.

Metal Bend Segment Widening. Metal jog segments tend to incur large CD deviations and therefore have an elevated risk of pinching and bridging. This is especially true at subnominal process conditions. Addressing these metal features during mask preparation (often with OPC) is a typical approach. However, this practice adds to OPC complexity and increases the run time, which can vary from a few days to a month from layer to layer. Pushing these corrections to an earlier design stage reduces mask preparation time and allows designers to see any introduced parasitic effects.

To implement this modification, nominal wire bends in a long metal line are widened where sufficient space exists. Metal bend segments drawn at minimum design rule width, and that contain jogs less than or equal to a bend length parameter are identified as candidates for bend widening. The widths of candidate segments are grown to equal a pre-

Table 1: Capacitance sensitivity analysis for parameter optimizations.

Algorithm	Variable Name	Normalized Variable Value	% Cap Increase	% Delay
Global Sizing	Metal Upsize	-1	-2.63%	-2.39%
		1	3.88%	3.94%
Via Edge Movement	Edge Movement Distance	1	0.94%	0.00%
		2	0.85%	0.00%
		3	0.86%	0.00%
Metal Jog Jog/Notch Fill	Notch Depth	1	0.94%	0.00%
		1.714	0.83%	0.00%
		2.286	0.80%	0.00%
	Max Fill Length	1	0.94%	0.00%
		1.667	1.05%	1.18%
		2.667	1.19%	1.32%
		33.333	1.32%	1.38%
		66.667	1.58%	1.72%
Metal Line End Extension	Max Metal Extension	1	0.63%	0.00%
		3.5	0.94%	0.00%
		6	1.10%	1.04%
		8.5	1.30%	1.30%
	Metal Space Margin	0	1.20%	1.09%
		1	0.94%	0.00%
		2	0.84%	0.00%
Metal Bend Widening	Segment Width	1	0.94%	0.00%
		2.5	0.94%	0.00%
		4	0.94%	0.00%

determined value. This growth can occur on either side of the segment (or shared by both sides) based on proximity to neighboring metal features.

Algorithm Sequence. The aforementioned algorithms must be executed in the order described in order to exploit synergies among them and to avoid unexpected results. The via upsizing routine is seen as the best opportunity to enhance yield and is therefore performed first. This designation gives that algorithm the most operation space, maximizing the count of affected vias. The most important interaction is between the algorithm for metal enclosure of upsized vias and the notch fill routine. Since the first algorithm can generate unwanted metal notches, it is important that the notch fill algorithm follow it. Otherwise, the metal enclosure routine will generate many notches and jogs that will not benefit from the notch fill routine. The metal bend segment algorithm addresses a less critical issue than the others. Therefore, we apply this routine last to allow the most possible operating space to the other algorithms.

A second iteration of the entire sequence will not have an effect on the layout since all addressible events will already have been corrected. The auto-fix algorithms operate on GDS inputs and apply design modifications as flat geometries in the top cell. It is intended to allow execution after DRC and LVS sign-off, but prior to the extraction/characterization step. However, the flow can be applied at any step in the design flow. It is intended for customized macro designs but can also be applied on a full chip to react quickly to process updates or new process constraints. It will not introduce any DRC or LVS issues since the algorithms account for the design rules and connectivity.

2.2 Parameter Optimizations in Auto-fix Algorithm

Each layout modification is controlled by a set of variables. In determining appropriate values for these parameters, it is important to establish that the automated layout modifications do not impose negative parasitic effects on circuit performance. Capacitance and timing simulation experiments were performed on a representative layout sample. Simulation data shows that capacitance and timing metrics are impacted less than from a simulated metal CD process shift.

A range of variables was selected to determine circuit capacitance and timing sensitivity to parameter variations. Separate versions of a single layout were generated with modifications applied according to several values of the parameters described below.

Via Edge Movement - *Edge Movement Distance*: Distance by which a single via edge is moved provided sufficient room considering all design rule spaces with margins.

Metal Jog/Notch Fill - *Notch Depth*: Length of metal jog segment by which the algorithm recognizes candidate notches and jogs. *Max Fill Length*: Length of additional metal applied to candidate notches and jogs.

Metal Line End Extension - *Max Metal Extension*: Maximum extension of metal beyond the original line end. *Metal Space Margin*: Additive margin to metal space design rules.

Metal Bend Segment Widening - *Bend Segment Width*: Amount by which candidate segments are widened.

We ran extraction and simulation programs for each set point with all other variables set to a nominal value. Simulation results were reduced to show changes in capacitance and signal delay from primary input to primary output. We considered both capacitance and signal delay as percentage changes of those from the unmodified layout. Table 1 shows the selected variable set points and simulation results. For comparision, capacitance and timing delays associated with upsized metals simulating a process CD shift are included in the first two rows in Table 1.

Larger vias resulting from the via enlargement algorithm will result in lower resistance vias. However, the RC benefit of this effect is not reflected by the timing simulations in this study since the extraction flow assigns a single resistance value to each via, regardless of size. From these findings we conclude that the routine can be considered relatively harmless.

In general, the capacitance and timing responses display a low sensitivity to algorithm parameter perturbations and little harmful parasitic effect when compared to the simulated process shift. Although the trends indicate that prohibitively large parasitic effects can result from very large parameter values, those used in this study have been optimized beyond which no further yield improvement is expected. The largest capacitance increase of 1.58% and the largest timing delay increase of 1.72% correspond to an extreme parameter value of 66.67 times the nominal set point. The relatively small parasitic effect of these automated layout modifications is an important factor in determining where to integrate them into a design flow.

3. EXPERIMENTS AND RESULTS

We evaluated a representative macro design (i.e., customized design block) from 65 nm technology, based on the following criteria: relatively large area, high frequency of occurrence, and self-contained functionality. We performed the DFM auto-fix flow on metal layers in this macro within the production design flow, and analyzed the impact of the additional metal features on circuit performance and process margins. The experimental results support the feasibility of this approach. The DFM auto-fix scheme has been implemented in a current 65 nm design to enable silicon data verification.

3.1 Impact on Parasitic Extractions

The average densities of four metal layers, before and after application of the DFM auto-fix flow are listed in Table 2.

Table 2: Average density for metal layers in the sample macro.

Metals	Pre-DFM	Post-DFM	Post-DFM Normalized
M01	7.15%	7.90%	1.11X
M02	34.47%	34.75%	1.01X
M03	26.52%	26.71%	1.01X
M04	26.47%	27.31%	1.03X

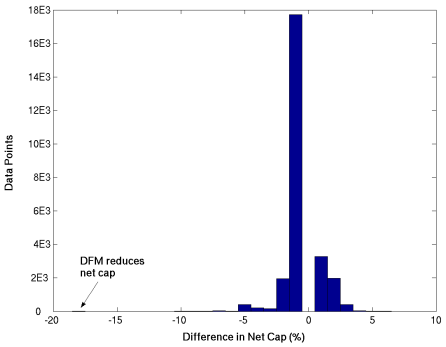

Figure 2: Cap comparisons between post DFM auto-fix version and original version. Only nets with greater than 1% cap differences are shown.

The total area of added metal features is within 11% across all four metal layers. We extracted parasitics after the DFM auto-fix, and compared results with those of the unmodified design. Total capacitance was increased by 0.36%, corresponding to an absolute increase on the order of hundreds of fF. Figure 2 illustrates a histogram showing capacitance changes greater than 1%, by net. A set of nets displayed a capacitance decrease of up to 18% due to the DFM modifications. We identified the net with the largest capacitance reduction as a diffusion node, which is marked as node Z in Figure 3. The total capacitance to VSS associated with node Z is reduced by 11% because more fringe capacitance couples to $M01$ due to the added metals on node $xs0$ and node $s0$ marked in Figure 3. This leads to a 23% increase in total coupling capacitance associated with node Z. Although these capacitance changes seem large when expressed as percentages, all are on the order of $1-3$ fF, which is insignificant to circuit performance.

3.2 Impact on Timing and Noise

By comparing all specifications associated with the critical path for the sample macro including noise margin, bit fall time, bit slew, clock to Q, etc., we find there are either no changes or changes within 0.3%. These shifts are negligible when considered in the context of noise resolution in the extraction and simulation tools. We also investigated the impact on circuit noise due to the increase in total coupling capacitance. The results indicate that a slight improvement in noise response (less than 0.1%) is derived from the DFM auto-fix flow due to a total cap reduction achieved on the layout structure.

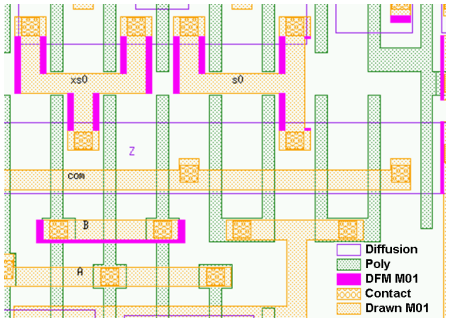

Figure 3: Layout location for node Z with 17% capacitance reduction post DFM auto-fix.

3.3 Impact on Process Margins

We performed a set of print-image contour based DFM rule checks before and after application of the DFM auto-fixes. We generated print image contours based on lithography simulations at focus and exposure corners. We then applied DRC-like spatial rule checks. The results show consistent reductions in violation counts for these checks. In particular, the number of violations of the minimum spacing check is reduced by 80%. Such improvements are the result of reduced litho-induced variations due to the additions made to those features or to their neighbors.

4. CONCLUSIONS AND FUTURE WORK

The DFM auto-fix flow is a scalable, efficient, and low-cost method to improve yield while avoiding performance degradations. The flow has a modular construction, affording the flexibility of adding or removing algorithms and changing control parameters as needed. Also, it allows designers to react to any parasitic effects imposed by the DFM modifications. The flow should help speed process ramp to maturity and provide additional process latitude in stable processes.

The auto-fix flow can be extended to allow the designer to control the extent of the DFM modifications. This functionality could be implemented with various drawn layers which would indicate the parameter values for different regions of the design. Aggressive parameter values can be applied to non-critical regions and conservative parameters to critical paths, matched pairs, etc.

Another promising DFM methodology lies with the print image based simulations which were used only for verification in this work. Generation of print variability contours and application of rule checks can be used as an additional verification step for layout blocks. This would provide designers access to current lithography models in time to correct their designs accordingly.

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