Modeling and Analysis of Circuit Performance of Ballistic CNFET

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ABSTRACT

With the advent of carbon nanotube technology, evaluating circuit and system performance using these devices is becoming extremely important. In this paper, we propose a quasi-analytical device model for intrinsic ballistic CNFET, which can be used in any conventional circuit simulator like SPICE. This simple quasi-analytical model is seen to be effective in a wide variety of CNFET structures as well as for a wide range of operating conditions in the digital circuit application domain. We also provide an insight how the parasitic fringe capacitance in state-of-the-art CNFET geometries impacts the overall performance of CNFET circuits. We show that unless the device width can be significantly reduced, the effective gate capacitance of CNFET will be strongly dominated by the parasitic fringe capacitances and the superior performance of intrinsic CNFET over silicon MOSFET cannot be achieved in circuit.

Categories and Subject Descriptors

I.6.5 [Simulation and Modeling]: Model Development – modeling methodologies.

General Terms – Design, Performance.

Keywords

Ballistic carbon nanotube FET (CNFET), circuit compatible model, parasitic capacitance, circuit performance.

1. INTRODUCTION

As silicon technology is approaching to its limit, several emerging devices are studied to find a suitable alternative to silicon. Carbon nanotube FETs (CNFET) are shown to have potential of taking this place in the post silicon era. Its interesting structural and electrostatic properties (e.g., near ballistic transport) make it attractive for the future integrated circuit applications [1]. Consequently, interests have grown to predict the performance of these devices in circuits and systems [2-6]. However, circuit simulation using CNFET at present is a difficult task, because most of the developed device models are numerical [2, 7], which conventional circuit simulators like SPICE can not handle. A good analytical model to express the electrostatic properties (e.g., I-V and C-V characteristics) of these devices is thus extremely necessary for circuit simulation.

A recent attempt has been made to achieve empirical analytical expressions to represent electrostatic properties of CNFET [6]. However, because of its underlying assumptions, this model cannot accurately predict the device characteristics at all operating conditions.

In this paper, we propose a circuit compatible quasi-analytical device model, which can be used for different semiconducting CNFET structures at all operating conditions in the digital circuit application domain. This compact model will greatly facilitate the circuit simulation using any conventional simulator like SPICE. The model is developed assuming the ballistic transport of CNFET [2] and shown to have close agreement with physical model.

We further provide in this paper, a quantitative analysis on the geometry dependent parasitic capacitances of state-of-the-art CNFET structures and their impact on the circuit performance. Because of its high drive current (due to ballistic transport) the intrinsic performance of CNFET has been predicted to be as high as in the range of Terahertz [3, 8, 9]. The effective circuit performance in reality, is however, governed by the effective gate capacitance of the device, which includes both (1) the intrinsic and (2) extrinsic (parasitic) capacitances. While the intrinsic capacitance of CNFET has theoretically been shown to be only a few atto-farads [8-11], the parasitic capacitance, however, is a strong function of the device geometry. We show that the performance of CNFET is limited by the process (the current technique to fabricate CNFET) and that the device width needs to be significantly reduced, in order to achieve the superior performance of intrinsic CNFET over silicon MOSFET in circuits. This analysis not only provides a realistic estimation of the performance of CNFET circuits but also draws a very effective guideline to device design and optimization as well as process development.

The rest of the paper is organized as follows. In section 2 we describe the proposed compact model of CNFET for circuit simulation. Section 3 discuses the parasitic capacitances in state-of-the-art CNFET structures and its impact on circuit performance followed by a conclusion in section 4.

2. COMPACT MODEL OF CNFET

For circuit simulation using conventional simulator like SPICE we need an analytical expression for device (e.g., *I-V* and *C-V*)

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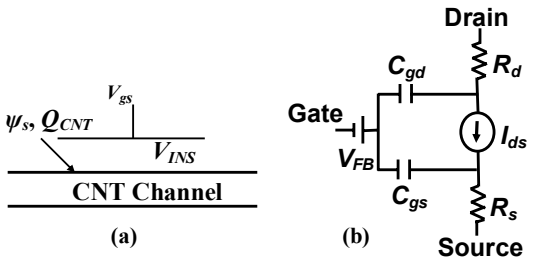


Figure 1. (a) Schematic of a carbon nanotube transistor; (b) Equivalent circuit of a ballistic one dimensional CNFET for circuit simulation. R_s and R_d are the source and drain contact resistance, respectively.

characteristics in terms of applied terminal voltages (e.g., V_{gs}, V_{ds}: see Fig. 1). However, it is impossible to obtain exact closed form expressions directly by solving self consistent device equations [2, 7]. We therefore, employ appropriate approximations to analytically solve the device equations. We assume ballistic transport in MOSFET like single-walled CNFET with one-dimensional (1D) electrostatics [12]. Short channel MOSFET like CNFETs are of particular interest because they are shown to provide near ballistic current, thereby indicating maximum performance [13, 14]. The carrier density for any sub-band (pth) of such nanotube transistor can be expressed as [2],

$$n_p = \int_{E_{c,p}}^{\infty} \frac{D_p(E)}{2}\left[f(E-\mu_s)+f(E-\mu_d)\right]dE \qquad (1)$$

where $\mu_{s(d)}$ is the source (drain) Fermi level, $E_{c,p}$ be the conduction band minimum for the pth sub-band, $f(E)$ is the probability that a state with energy E is occupied and $D(E)$ is the nanotube density-of-states, which can be approximated as $D_0 \mid E \mid / \sqrt{E^2 - E_{c,p}^2}$ for low bias [15]. $D_0 = 8/(3\pi V_{\Pi} b)$, where V_{Π} and b are respectively, the carbon-carbon bonding energy and the distance. Normalizing all energies and voltages by β ($k_B T/q$) and substituting $\varepsilon^2 - \varepsilon_{c,p}^2 = z^2$ ($\varepsilon = E/\beta$), Eq. (1) can be written as,

$$n_p = N_0 \sum_{v_i = v_s, v_d}\left[\int_0^{\infty} \frac{dz}{1+e^{\left(\sqrt{z^2+\varepsilon_{c,p}^2}-(\varphi_s - v_i)\right)}}\right], \quad N_0 = \frac{\beta D_0}{2} \qquad (2)$$

where φ_s (ψ_s/β), v_s and v_d are the normalized surface, source and drain potentials, respectively. Though solving Eq. (2) analytically is not possible, an approximate closed from solution can be obtained by dividing the operating condition into two parts. For $\psi_s < \psi_T$ (below threshold), when $\sqrt{z^2+\varepsilon_{c,p}^2} - \varphi_s >> 1$ (for all 'z': $0 \to \infty$), Eq. (2) can be approximated to calculate the charge as,

$$Q_{CNT} = qN_0\left[\sum_p \int_0^{\infty} e^{-\left(\sqrt{z^2+\varepsilon_{c,p}^2}\right)} dz\right]\left(1+e^{-v_{ds}}\right)e^{\varphi_s}$$

$$= e^{\alpha_0 + \varphi_s} \qquad (3)$$

We consider the source potential as the reference potential and V_{ds} is the drain potential with respect to source. It is observed that $\psi_T = E_{c,p}/q - 2\beta$ is a good choice for the above approximation. The integral of Eq. (3) can be precomputed numerically and α_0 can be analytically obtained for any drain voltage. For $\psi_T < \psi_s \le E_{c,p}/q$ (above threshold), Eq. (2) can be rewritten as,

$$n_p = N_0 \sum_{v_i = 0, v_{ds}}\left[\int_0^{\infty} e^{-[x-(\varphi_s - v_i)]}\left(1+e^{-[x-(\varphi_s - v_i)]}\right)^{-1} dz\right]$$

$$x = \sqrt{z^2 + \varepsilon_{c,p}^2} \qquad (4)$$

Further expanding Eq. (4) into binomial series, which is now a converging series for all values of 'z', and e^{φ_s} into infinite series and neglecting the higher order terms we can obtain Q_{CNT} as,

$$Q_{CNT} = qN_0 \sum_p \sum_{n=1}^{\infty}\left[(-1)^{n-1} e^{n(\varphi_s - \varphi_T)}\left(1+e^{-nv_{ds}}\right)\int_0^{\infty}\left(e^{-n\cdot(x-\varphi_T)}\right)dz\right]$$
$$\approx \lambda_0 + \eta_1\lambda_1(\psi_s - \psi_T) + \eta_2\lambda_2(\psi_s - \psi_T)^2 \qquad (5)$$

λ_0, λ_1, λ_2 can be obtained with simple algebraic calculation, while all integrations can be performed numerically. Note that the reason for approximating Q_{CNT} into polynomial form is to obtain an analytical V_{gs}-ψ_s relation, which is derived below. Further, though one can obtain an accurate expression by considering higher order terms (without using any correction factor), we however, use the above polynomial of order two with constant correction factors η_1 and η_2 to obtain simpler V_{gs}-ψ_s relation. For $\psi_s > E_c/q$, though a similar approximate solution can be achieved following the above approach with carefully expanding in series, we however, observed that Eq. (5) also efficiently predicts the charge. Fig. 2 shows Q_{CNT} verses ψ_s obtained from physics model [numerical solution of Eq. (2)] and the above approximate analytical model [Eq. (3) and (5)]. It can be seen that the analytical models (with [Eq. (5)] and without correction factors [polynomial of order 4]) closely match with physics model in both below [Fig. 2(a)] and above threshold [Fig. 2(b)].

Q_{CNT} is further related to terminal voltage, V_{gs} (neglecting the flat-band voltage; see Fig. 1(a)) as,

$$\psi_s = V_{gs} - V_{INS} = V_{gs} - \frac{Q_{CNT}}{C_{INS}} \qquad (6)$$

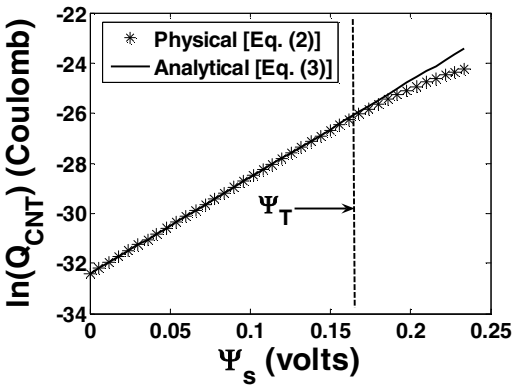
where C_{INS} is the insulator capacitance. Substituting Q_{CNT} in (6) an analytical closed form expression for V_g-ψ_s can be obtained as

$$\psi_s = V_{gs} - \beta \cdot lambertw\left[\frac{1}{\beta \cdot C_{INS}} e^{(\alpha_0 + V_{gs}/\beta)}\right]$$

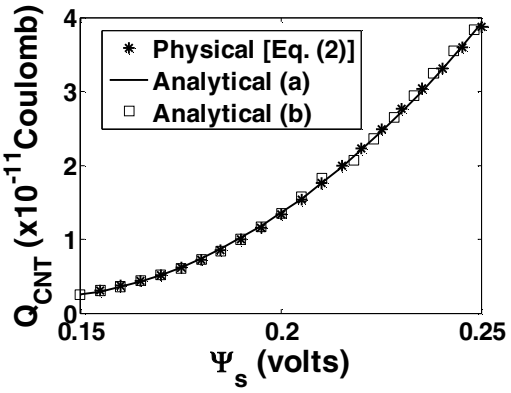
for $V_{gs} \le V_T$

$$\psi_s = \psi_T - \frac{(\eta_1\lambda_1 + C_{INS})}{2\eta_2\lambda_2}$$
$$+ \frac{\left[(\eta_1\lambda_1 + C_{INS})^2 - 4\eta_2\lambda_2[\lambda_0 - C_{INS}(V_{gs} - \psi_T)]\right]^{1/2}}{2\eta_2\lambda_2} \qquad (7)$$

for $V_{gs} > V_T$



(a)



(b)

Figure 2. Charge vs. channel potential of a ballistic carbon nanotube FET. Physical model represents the numerical solution of Eq. (2). (a) $\psi_s < \psi_T$; (b) $\psi_s > \psi_T$; the curve '*Analytical (a)*' represents the charge obtained from Eq. (5) (with correction factors), and '*Analytical (b)*' is the charge obtained from the polynomial expression of order 4 without using any empirical parameter.

where V_T is the gate voltage (threshold voltage) corresponding to ψ_T and can be obtained from Eqs. (3) and (6) with $\psi_s = \psi_T$. Knowing ψ_s in terms of the terminal voltages the drain current, I_{ds} and gate input capacitance, C_G (Fig. 1) can be easily obtained as follows [6].

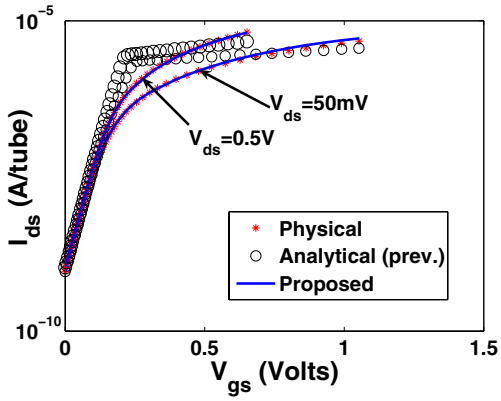
$$I_{ds} = \frac{4qk_BT}{h}\sum_p \left[\ln(1+e^{-\xi_s}) - \ln(1+e^{-\xi_d})\right] \quad (8)$$

and $C_G = \frac{\partial Q_{CNT}}{\partial V_{gs}}$

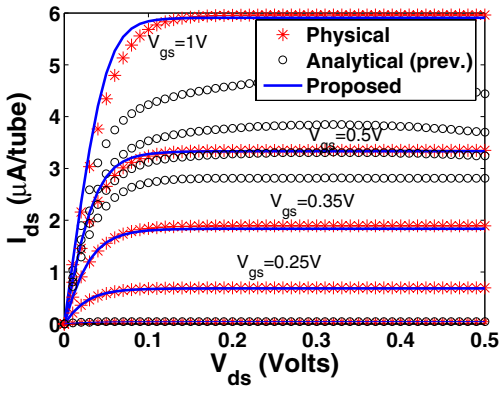
where $\xi_i = \frac{q\psi_s - E_{c,p} - qV_i}{k_BT}$ ($i = s, d$) and h is the Planck's constant. Further, typical values for R_s and R_d (Fig. 1) can be used based on the experimental results for circuit simulation.

Fig. 3 shows the *I-V* (I_d-V_g and I_d-V_d) characteristics of a CNFET with 2nm diameter and 48.3 pF/m insulator capacitance. It can be seen from the figure that while the model proposed in [6] does not match with the physical model for large bias conditions, our proposed model matches closely for a wide range of bias conditions. Also note that since we did not make any abrupt approximation in our model, no discontinuity arises around the threshold. We also verified our model for different nanotube diameters (1, 1.6, 1.7, 2 and 3nm) and obtained close match with physical model in all cases. Note that we used physical model with numerical solutions to compare our model due to the unavailability of adequate experimentally measured data with different nanotube dimensions.

Fig. 4 shows the SPICE simulation result of a two input NAND gate driving three identical gates [CNT: diameter=2nm and L_{ch}=20nm (V_{dd} = 0.9V)]. We used one nanotube for PCNFET and two parallel nanotubes for series connected NCNFETs. As can be seen from the figure, a considerably fast response time (2.52ps) was obtained using the intrinsic devices compared to the conventional ITRS 45nm CMOS technology prediction.



(a)



(b)

Figure 3. *I-V* characteristics of CNFET with diameter = 2nm and C_{INS} = 48.3 pF/m, V_T=0.3V (T=300^{o}K); (a) I_{ds}-V_{gs} for different V_{ds}; (b) I_{ds}-V_{ds} for different V_{gs}.

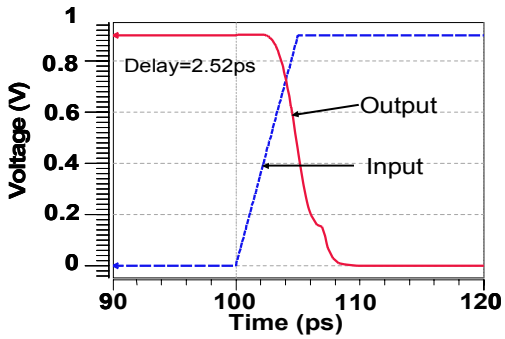


Figure 4. Input/Output waveform of a 2 input NAND driving three identical gates.

3. IMPACT OF PARASITICS ON CIRCUIT PERFORMANCE

In this section we analyze the impact of parasitic capacitances on the CNFET circuit performance. We first describe the effective geometry dependent parasitic components in state-of-the-art CNFET structures followed by a discussion on the overall circuit performance with parasitics.

3.1 Geometry Dependent Parasitic Capacitance

Fig. 5(a) shows the schematic cross-section of a state-of-the-art top gated CNFET structure [16, 17]. In this self aligned process the gate electrode metal (height, T_g) is separated from the source/drain (length, L_{sd}) metal approximately by $T_{ox} - H_{sd}$ in the vertical direction (T_{ox}: oxide thickness, H_{sd}: source/drain metal thickness) and by the thin oxide (L_{un}) in the horizontal direction, that is used to isolate the gate metal during source/drain metal deposition. The cross-sectional view of the electrostatic geometry of the device can be represented as shown in Fig. 5(b). The parasitic capacitance in this structure, hence, consists of mainly the gate/source and gate/drain fringe capacitances. The other components such as gate to substrate and source/drain to substrate capacitances are expected to be very small (due to large SiO_2 thickness) and hence, are neglected in this analysis. The fringe capacitance (C_{fr}) of this geometry can be analytically calculated using the following equation [18].

$$C_{fr} = \frac{2\varepsilon W}{\pi}\ln\left[\frac{T_{g,s/d} + \eta T_g + \sqrt{L_{un}^2 + (\eta T_g)^2 + 2T_{g,s/d}\eta T_g}}{L_{un} + T_{g,s/d}}\right] + \frac{k\varepsilon W}{\pi}\ln\frac{\pi W}{\sqrt{L_{un}^2 + T_{g,s/d}^2}}e^{-\left|\frac{L_{un}-T_{g,s/d}}{L_{un}+T_{g,s/d}}\right|} \quad (6)$$

Where $\eta = \exp\left[\left(L_{sd} + L_{un} - \sqrt{L_{un}^2 + T_g^2 + 2T_{g,s/d}T_g}\right)/\tau L_{sd}\right]$ and $T_{g,s/d} = T_{ox} - H_{sd}$. ε is the permittivity of medium, W is the device width and k and τ are constants. A detail description about the above formulation can be found in [18]. In this analysis, we used SiO_2 as the medium outside the device.

3.2 Analysis of Fringe Capacitance

Fig. 6 shows the variation in C_{fr} with T_g (gate height) and T_{ox} (oxide thickness). C_{fr} has two components; outer (C_{of}) and inner

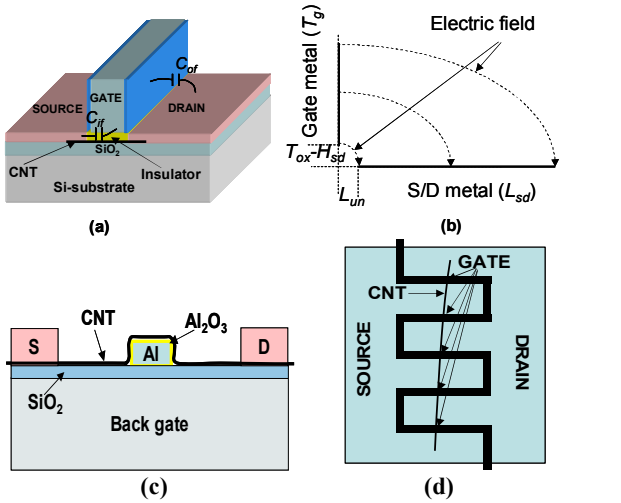


Figure 5. (a) Schematic of a self-aligned top gated carbon nanotube transistor. (b) Electrostatic geometry for the fringing field of the device. (c) Schematic of a dual-gate (bottom) CNFET. (d) Schematic of a multiple FIN CNFET equivalent to five parallel CNT channel.

(C_{if}) fringe capacitances. Unlike conventional MOSFET, in CNFET both C_{of} and C_{if} will substantially contribute to the total fringe capacitance due to very narrow channel region (typically one nanotube in one micrometer width). C_{of} and C_{fr} are calculated following Eq. (6). It can be seen from the figure that for a typical geometry (T_g~30nm, T_{ox}~8nm, L_{un}~1nm, L_{sd}~250nm, H_{sd}~7nm), C_{fr} is about two orders of magnitude larger than the typical device intrinsic capacitance (~1.5aF for 50nm gate [8]). The typical width (W) of a state-of-the-art CNFET device is about 1µm. This is necessary to ensure the nanotube channel under the gate. Hence, the circuit performance will be dominated by the parasitic fringe capacitances and the effectiveness of very low intrinsic capacitance of CNFET can not be utilized in reality. Further, due to the logarithmic dependency, C_{fr} is not a very sensitive function of T_g [Fig. 6(a)]. T_g also can not be very thin since it increases the gate resistance drastically [18]. C_{fr} has a similar dependency on L_{sd} due to the geometric symmetry and hence, varying L_{sd} will not impact C_{fr} significantly [Fig. 6(b)]. C_{fr} however, has a strong dependency on the gate oxide thickness (T_{ox}) of the transistor. It can be seen from Fig. 6(c) that C_{fr} reduces steeply with the increase in T_{ox} around 8nm. This is because the electric flux strongly depends on the nearest distance between the electrodes. This implies that the use of high-K gate oxide will lead to lower effective gate capacitance by employing larger T_{ox} while still having good gate control. Separating source and drain from the gate has also been tried by means of doping the nanotube outside of gate region [19]. We studied the impact of this structure (analogous to underlap device) on C_{fr} by varying L_{un}. Though C_{fr} can be reduced significantly by increasing L_{un}, it still remains significantly higher than intrinsic device capacitance [Fig. 6(d)]. It is hence, evident from Fig. 6 that C_{fr} can not be reduced to the order of intrinsic device capacitance by optimizing T_g, T_{ox}, L_{sd} and L_{un}. One way to effectively reduce C_{fr} is to reduce the width of the device (W). However, this not only calls for the improvement in the control of nanotube fabrication but also requires improvement in lithography process. With present lithography equipment achieving such small W (order of 10nm) is extremely difficult.

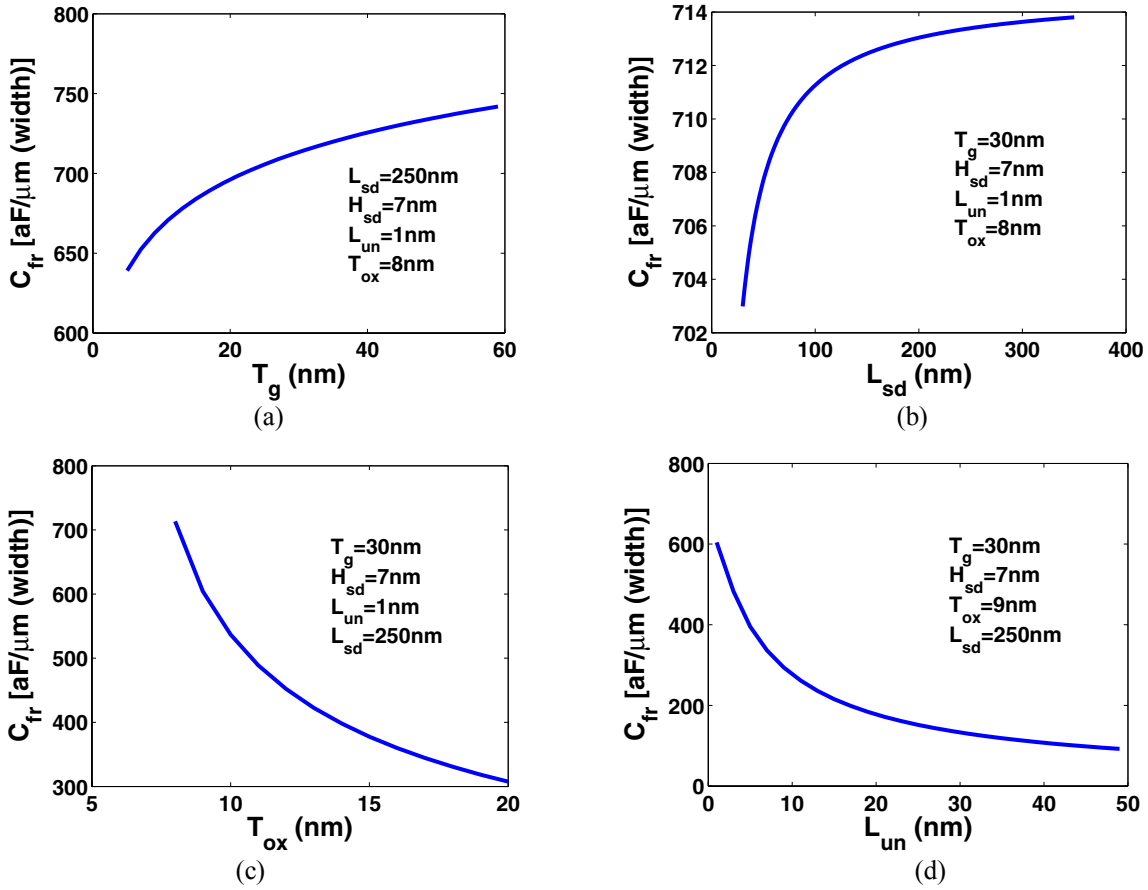


Figure 6. Variation in fringe capacitance with device geometry; (a) with gate metal thickness, (b) with source/drain length, (c) with oxide thickness and (d) with underlap.

A dual (bottom) gate CNFET structure is also recently proposed for improved performance [8, 20], in which the active gate is deposited on top of the back SiO_2 gate (below the nanotube channel) and separated from the source and drain by a large distance [Fig. 5(c)]. In this structure though the gate to source/drain parasitic capacitances are expected to reduce considerably, the parasitic capacitance between the active and the back gates is however, expected to be large if the back gate is controlled independently. It will consist of both overlap and fringe capacitances as shown in Fig. 5(c). For a typical structure with gate length 50nm and height 20nm, the parasitic capacitance was found to be 2.8×10^{-16} F with 1μm width, which is much larger than the intrinsic capacitance. On the other hand, if the back gate switches with the active gate, though the capacitance between them will be negligible, the overlap and fringe capacitances between back gate and source/drain will be significantly high.

Efforts have also been put into increasing the transistor drive current by introducing multiple nanotubes between the source and drain (parallel nanotube channels). One such geometry has been proposed in [16] (see Fig. 5(d)). In this self-aligned process one nanotube acts as multiple channels between the source and drain. We analyzed one such structure to understand its effectiveness in improving the circuit performance. In a typical process, the gate

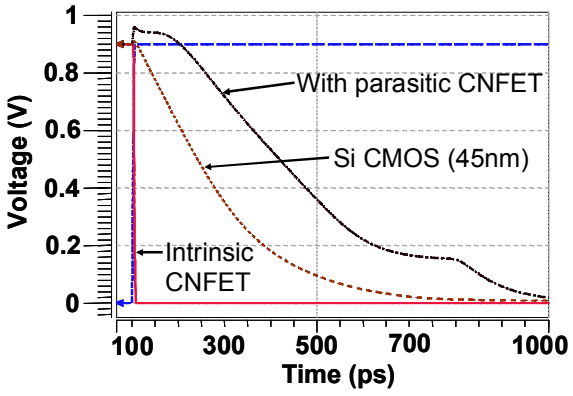


Figure 7. Input/Output waveform of a 2 input NAND gate with fanout 3 using CNFET (20nm gate length) and CMOS BPTM 45nm technology.

FINs are separated by approximately 250nm and hence, besides each individual gate FIN, the gate metal connecting the FINs also contributes to the total fringe capacitance. Hence, the improvement in drive current will be masked by the increase in capacitance degrading the overall performance.

To further analyze the impact of parasitic capacitance we simulated a 2 input CNFET (20nm gate length) NAND gate driving 3 identical gates and compared the same with silicon BPTM 45nm technology. The circuit simulation with CNFET was performed with the developed compact model discussed in section 2. It can be seen from Fig. 7 that while the intrinsic delay of CNFET NAND gate is very small (2.52ps) the delay with parasitics (344ps) is much larger than silicon CMOS delay (165ps). This is because in 45nm technology the minimum transistor size (NMOS transistor width=240nm in 2-input NAND) was much smaller than CNFET width (~1μm). Further, the junction capacitance was not considered in Si CMOS transistors. The above result confirms that the performance will be indeed dominated by the fringe capacitance, which is also expected to dominate the effective gate capacitance in silicon [18].

In the above analysis we have not taken interconnect into account. Interconnect may further limit the performance of CNFET circuits. However, a quantitative analysis of performance with interconnect, we feel, is too abstract at this point when there is too little information available about CNFET circuit layout configuration.

4. CONCLUSIONS

In this paper, we provided a quasi-analytical circuit compatible model for intrinsic ballistic CNFET. This model is seen to be very effective for various CNFET structures with a wide range of bias conditions, which can be used in conventional circuit simulators. We also provided a quantitative analysis on the parasitic capacitance of state-of-the-art CNFET structures. We show that the parasitic capacitance cannot be significantly reduced by optimizing gate metal thickness, gate oxide thickness or source/drain length and that it can be effectively reduced only by decreasing the width.

5. ACKNOWLEDGEMENT

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