DFT for Controlled-Impedance I/O Buffers

Ahmad A. Al-Yamani
King Fahd University of Petroleum and Minerals
PO Box 3, Dhahran 31261, Saudi Arabia
+966-3-860-3186
aaa@ieee.org

ABSTRACT

This paper presents an architecture that enhances the testability of controlled-impedance buffers (CIBs). By testing CIBs digitally, the new architecture overcomes most of the problems with the traditional testing method. Most of these problems are test cost related. While reducing the test cost, the new architecture allows for higher test quality that even includes delay testing capabilities.

Categories and Subject Descriptors

B.7.3 [**Integrated Circuits**]: Reliability and Testing – *built-in tests, testability*.

General Terms

Design, Measurement, Reliability.

Keywords

Built-in self test, design-for-testability, I/O test, I/O characterization.

1 INTRODUCTION

Controlled-impedance buffers (CIB) are widely used in transmission lines. CIBs are special input/output buffers that adjust their impedance based on the impedance of the transmission line they are driving.

Information travels through transmission lines as electromagnetic waves. Such waves are formed by a magnetic field and an electric field. These two fields exchange energy continuously. Other than the small energy dissipated as heat, the sum of the magnetic and the electric field must be constant due to conservation of energy.

The characteristic impedance of the transmission line (Z_0) is determined by the ratio of the maximum voltage to the maximum current.

$$Z_0 = \frac{V}{I} \qquad (1)$$

By conservation of charge, the current flowing through the transmission line is equivalent to the current flowing through the input buffer. Let's call the impedance of the driving (output) buffer Z_1 and the impedance of the driven (input) buffer Z_2. If Z_2 is not the same as the impedance of the transmission line Z_0, there will be a voltage drop at the boundary of the buffer. This voltage drop results in an electric field that needs some of the energy of the signal. This energy is reflected back in the transmission line with magnitude Γ:

$$\Gamma = \frac{Z_0 - Z_2}{Z_0 + Z_2} \qquad (2)$$

Notice that the voltage from the driving buffer is dropped to half due to the voltage divider formed by the impedance of the driving buffer and the transmission line. This is shown in Figure 1.

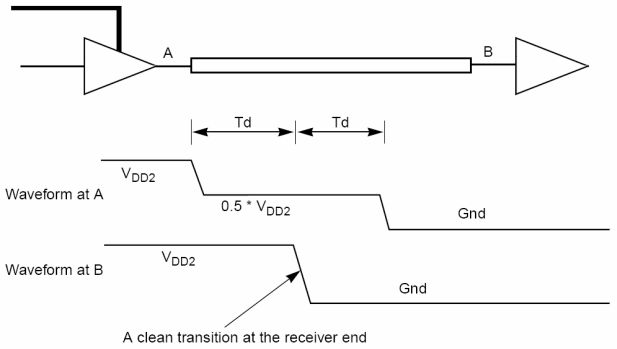

Figure 1 A wave transmitted by an impedance matching driver.

The traditional way of testing controlled-impedance buffers is by configuring them to different driving strengths and measuring the current using the ATE. For every impedance value in the operational range, the appropriate configuration is loaded into the CIB, and the driving current of the CIB is measured using a parametric measurement unit (PMU) on the automatic test equipment (ATE).

There are several problems with the traditional testing methodology. First, it requires a tester channel per CIB. It is well-known that the cost of testers is a linear function of the number of channels. Second, PMUs are expensive units on the tester. If it's possible to test without them, the cost of test will be significantly lower. Also, there are usually many more CIBs on the device than there are PMUs on the tester.

DAC 2006, July 24–28, 2006, San Francisco, California, USA.

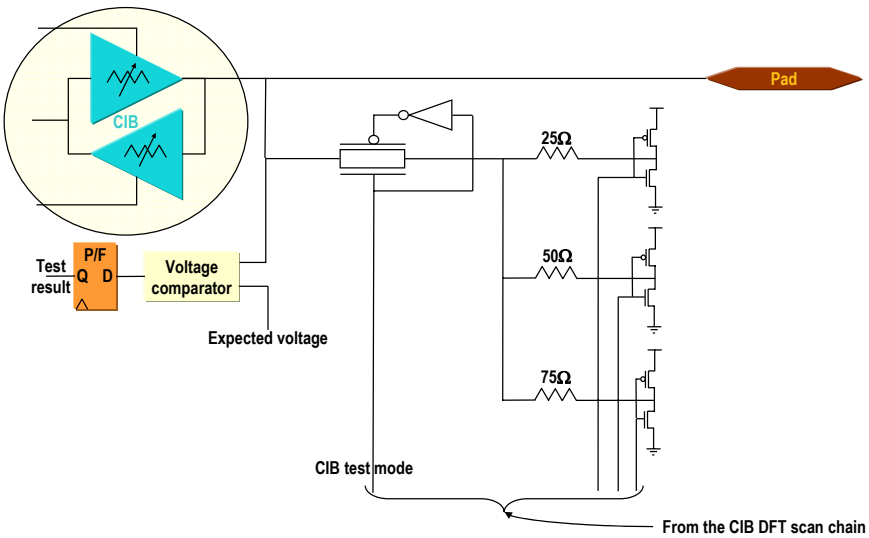

Figure 2 DFT architecture for controlled-impedance buffers.

So, the CIBs are tested serially in groups that can be accommodated by the number of PMUs on the tester. Third, testing using PMUs is a time consuming process. Test time is a recurrent cost and is of very high impact on overall test cost. Fourth, Most low-cost testers don't support PMUs. So, migrating to such testers is not going to be possible if CIBs are to be tested the way they are tested today.

This paper presents some architectures that can be used for testing CIBs. The architectures presented do not only eliminate most of the existing disadvantages but also improve the quality of test of the CIBs by providing a more thorough test. The cost of these DFT structures is the hardware per CIB.

Section 2 of this paper presents the CIB DFTarchitecture. Section 3 presents the delay DFT architecture. Section 4 presents the testing algorithm. Section 5 gives credit to previous related work. Section 6 shows some simulation results and Sec. 7 concludes the paper.

2 CIB DFT ARCHITECTURES

For testing CIBs, our architecture relies on the very well-known technique of converting the driving current into voltage to make it easy for measurement. The basic idea is to insert an external resistance to act as a voltage divider together with the configured resistance. The same idea has been used for testing leakage in I/O pins [1][5].

As shown in Figure 2, we can add multiple resistors (for the multiple possible configuration resistances of the CIB). These resistors act as voltage dividers together with the configured resistor. There is a pass gate for the DFT circuitry. This pass gates is put in connection mode during test and is disconnected during normal operation. The controlling value for the pass gate comes from a flip-flop that controls the mode of operation (normal vs. test mode). When in test mode, an appropriate resistance is selected by activating the path either to Vdd or to GND by activating the right transistor for that resistance. If the CIB is configured to drive the transmission line high, we activate the nMOS transistor. If it is configured to drive the transmission line low, the pMOS transistor is activated.

By selecting the right voltage as the expected voltage going into the voltage comparator, we can find out if the configured resistance inside the CIB was set to the right value. With some changes to the gating circuitry, this structure is similar to that used for I/O leakage testing in [5].

Some CIBs have an internal voltage comparator that is used during functional mode. The same comparator could be used for the DFT circuitry. If the resulting voltage matches (to some extent) the expected voltage, the flip-flop shown will latch a value of 1 which corresponds to a fault-free CIB. Otherwise, a value of 0 will be latched, which corresponds to a faulty CIB. All of the controlling signals come from flip-flops except the expected voltage which is controlled directly from the ATE. By testing the CIBs simultaneously through loading the appropriate values in the controlling flip-flops, we can use a single pin for all CIBs to supply the expected voltage simultaneously.

The above architecture can be enhanced such that only a single DFT resistor is necessary. This resistor can be chosen as the median value between the possible configurations (50Ω for the example in the figure). By controlling the expected voltage to represent the ratio of the DFT resistor to the configured internal CIB resistor, we can achieve the same thing as by using multiple resistors. The enhanced architecture shown in Figure 3 achieves significant advantage over the original architecture in terms of hardware overhead. Both architectures eliminate the need for expensive PMUs and allow testing CIBs without using tester channels (except for the expected voltage signal).

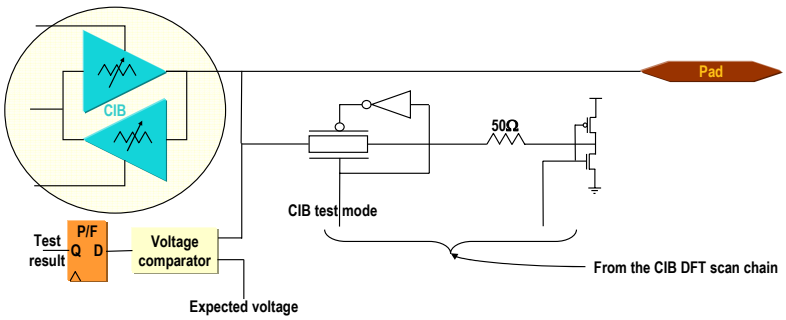

Figure 3 DFT enhanced architecture for CIBs.

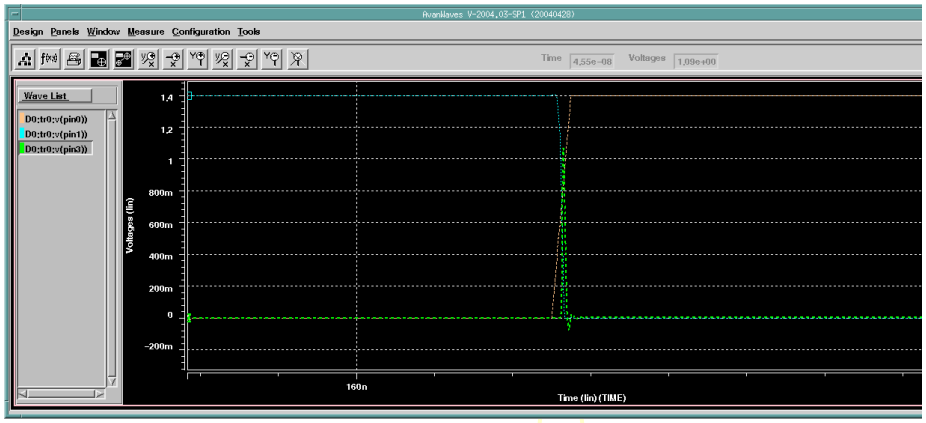

Figure 4 Voltage across the inductance for a defect-free CIB.

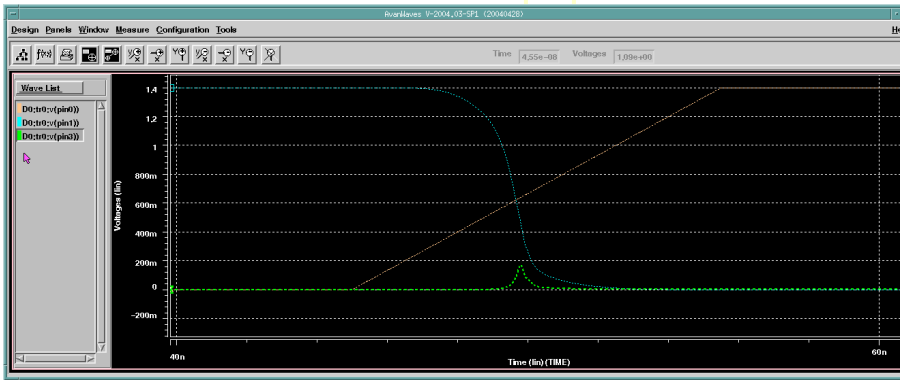

Figure 5 Voltage across the inductance for a CIB with a delay defect.

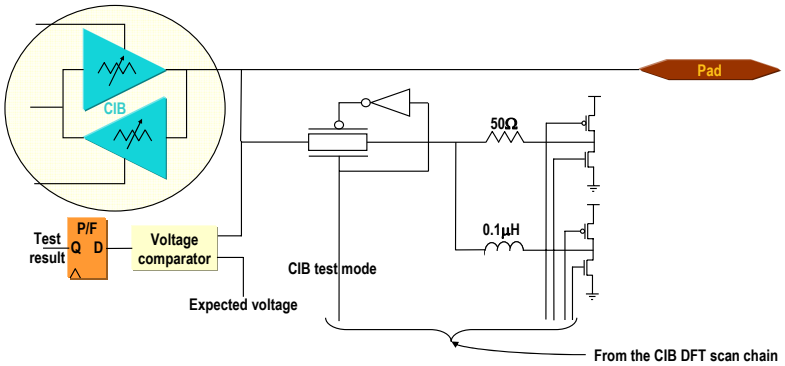

Figure 6 Delay DFT enhanced architecture for CIBs.

3 CIB DELAY DFT ARCHITECTURE

In today's ICs, delay defects cause a significant threat to test and DFT engineers. It has been widely confirmed that delay testing achieves higher test quality that wouldn't be achievable otherwise.

The question that comes up is: "how if the CIB has a delay defect?" The ATE in many cases won't be able to detect such a defect. Using PMUs, it's hard to detect such a fault because PMU testing is slow by nature. Using our DFT architecture, it's still hard to detect such defects because the tester speed often is much slower than the speed at which the CIB can switch.

We wanted to add a device to our DFT circuitry such that the voltage across the device is a function of the time needed for the required strength to be achieved by the CIB. By definition, the voltage across an inductor is the derivative of the current over time.

$$v_L = L\frac{di}{dt} \qquad (3)$$

By connecting an inductor at the output of the CIB, we can measure how long it takes for the driving strength to be adjusted simply by reading the voltage across that inductor.

Using Hspice simulations, we wanted to find out how the voltage across the inductance would look like for a faulty and a fault-free CIB. Figure 4 shows the voltage across the added inductance for a fault-free CIB and Figure 5 shows the voltage across the inductance for a CIB with a delay defect. It's clear that the fault-free CIB has a much larger voltage amplitude than the faulty signal. In both cases the voltage change is a spike that disappears shortly. This is expected because once the signal stabilizes, the voltage across the inductance drops to 0.

In order to utilize this spike for distinguishing between good and faulty CIBs, we connect the inductance voltage to the clock input of a flip-flop as shown in Figure 6. For delay testing of the CIB, we reset the flip-flop to 0, and configure the CIB for any driving strength. The value latched in the delay test flip-flop will tell us if the CIB has a delay defect or not. If the voltage across the inductance is high enough, the 1 input will be latched in the flip-flop meaning that there is no delay defect. If the voltage across the inductance is not high enough, the value 1 will not be latched meaning that the CIB has a delay defect. Notice that we need separate controlling inputs in this case for the n-Mos and the p-Mos transistors. This is because if we are activating the inductance path, we need to deactivate the resistance path and vice versa.

The overall architecture of a DFTed CIB cell is shown in Figure 7. As shown in the figure, there is a scan chain for the controlling values and another chain for the response. The controlling values scan chain can be shared across many or all of the CIB cells because we can apply the same test simultaneously to all cells. There are two flip-flops for the cell response. One of those flip-flops is for detecting the correctness of operation and the other is for the delay test. These cells are stitched together with the output scan cells for all CIBs and are shifted out for every test session.

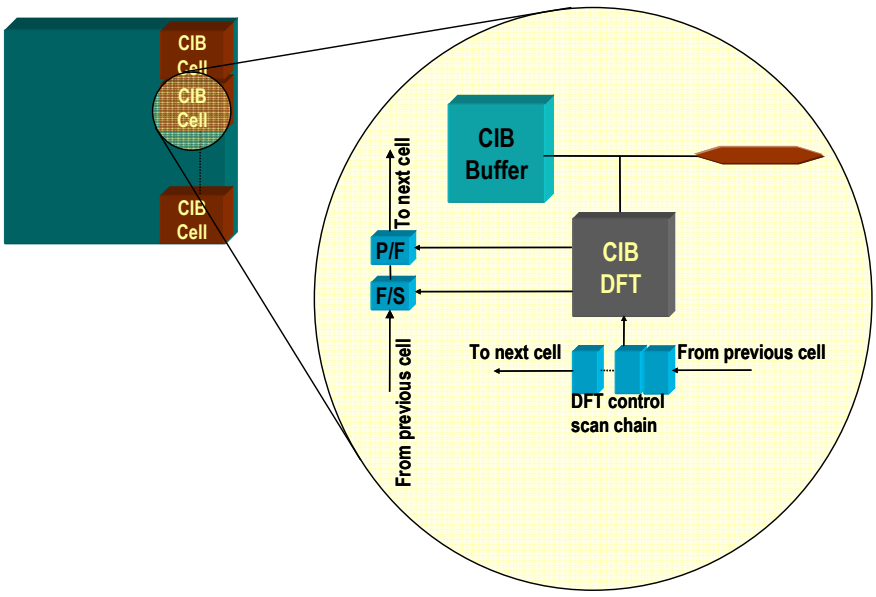

Figure 7 CIB DFTed cell architecture.

4 CIB TESTING ALGORITHM

Testing the CIB using the proposed architectures has two parts. In the first part, the CIB is tested for correctness and then for switching delay. Algorithm 1 is used to test the CIB for correctness of operation and is applied for both values of 1 and 0.

```
1. For each operational resistance R
2.     Load the test configuration
       into the CIB DFT chain.
3.     Load the proper configuration
       into the CIB.
4.     Set the expected voltage.
5.     Clock the pass/fail flip-flop
```

Algorithm 1 CIB operation testing algorithm.

Algorithm 2 is used to test for switching delay. Notice that this type of testing is not possible using the traditional PMU-based testing of CIBs. Also notice that there is no need to clock the F/S flip-flop because the voltage spike due to the inductance will clock it for the fault-free CIB. A CIB with a delay defect will not have a sufficient spike to clock the F/S flip-flop.

```
1. For each operational resistance R
2.     Reset the F/S flip-flop.
3.     Load the test configuration
       into the CIB DFT chain.
4.     Load the proper configuration
       into the CIB.
5.     Shift out the response.
```

Algorithm 2 CIB delay testing algorithm.

5 PREVIOUS WORK

This section is intended to give credit to the previous work on the subject. The work in [3] and [4] presented a BIST architecture for controlled impedance I/Os. In his technique, Haulin avoids connecting the pins to the tester. Instead, he connects them to 3 common controllable power rails. He also inserts load resistances that are equivalent to the characteristic resistance of the I/O. In the technique we present, we avoid the additional power rails which could be costly to be driven around all CIBs. We instead use control scan chains that gate the added load. Also, our technique has the unique inductance-based switching delay testing feature.

[1] presented a technique for I/O leakage testing. The technique is based on the fact that high leakage pins change state quickly due to the leakage. A low leakage pin would change state much slower. By sampling the state of the pin at the right time, we can find out about leakage problems. In the same year, LogicVision came up with a similar technique that utilizes the same large difference between a good pin and a bad pin to test for leakage using only 1149.1 access [7]. Although the two papers are about I/O leakage testing and not about CIB test, they are relevant to this paper because they avoid using a tester channel per pin. The work in [6] implements a loop back solution for testing the IOs of a microprocessor. The solution is also based on the difference in delay for state switching between different driving strengths.

The work in [5] presents another technique for testing I/O leakage based on the work in [2]. It is relevant to this work because it is also based on voltage division. The technique in that paper deserves a lot of credit for being an eye opener for this work. Our simple CIB test technique is similar to the technique presented in [5] with some architectural changes and the change in the application (CIBs instead of I/O leakage). The enhanced technique presented in this paper greatly reduces the required overhead for achieving the same result. Finally, the switching delay test architecture gives the technique in this paper a significant advantage.

6 EXPERIMENTS AND RESULTS

The CIB DFT circuitries presented in this paper were simulated using Spice with different driving strengths and driving voltages using a 0.13µ technology.

The first simulated parameter was the delay for the desired voltage to be reached on the pin. For this experiment, we matched the configured resistance with the external resistance and simulated the time it takes from the 50% voltage change on the input of the driving buffer till the stable voltage was reached by the pin. The simulations were performed for a buffer with driving strength of 1. It was also assumed that the distance between the DFT circuitry and the CIB is negligible and the driving voltage is 1.4v.

Figure 8 shows that for different resistance values, the stabilization time was less than 0.3 nanosecond. This means that the values could be sampled at 3Gbps, which allows for quick testing of the CIBs.

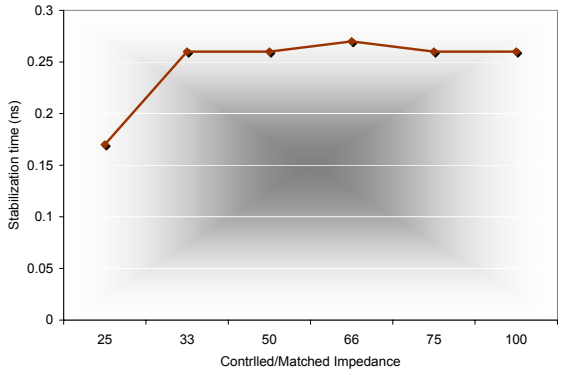

Figure 8 Stabilization time for CIB DFT circuitry.

The second experiment was targeted at finding the impact of the size of the driving buffer on the measured voltage at the voltage comparator of the DFT circuitry. If the expected voltage is too low the voltage resolution of the voltage comparator may be insufficient. As shown in Figure 9, the expected voltage can be brought up to desired levels by increasing the size of the driving transistor. This is applicable to different driving voltage values.

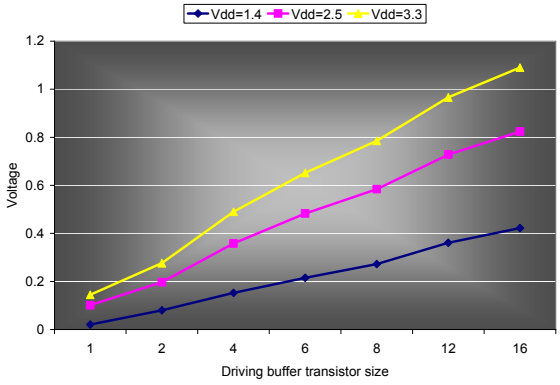

Figure 9 Increasing the expected voltage by increasing the driving transistor size.

The next experiment was targeted at finding the deviation between the ratio of the DFT resistance to the CIB configured resistance and the ratio of the expected voltage to the driving voltage. As shown in Figure 10, the voltage ratio very closely follows the resistance ratio for all combinations of configured resistance and DFT resistance. It is this result that makes it possible to use the enhanced DFT architecture because it implies that for testing purposes, we don't have to match the configured resistance to the DFT resistance. As long as we put the right expected voltage at the voltage comparator, the results should be thorough enough.

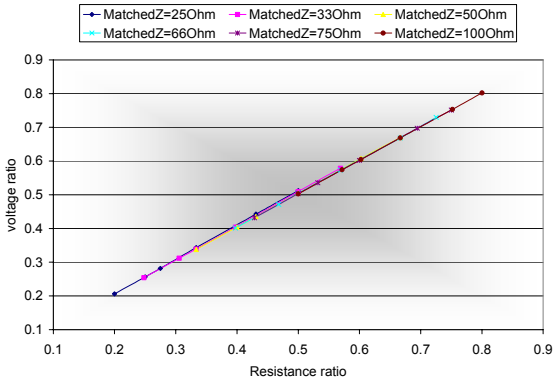

Figure 10 Voltage ratio vs. resistance ratio.

The next experiment was targeted at finding how the voltage ratio changes with the size of the driving buffer. So, the CIB resistance and the DFT resistance were set to 50Ω both. As shown in Figure 11, the size of the driving transistor has a minimal impact on the voltage ratio. This implies that it would be safe to use different transistor sizes and just compare the voltages. This is true with different transistor sizes and different driving voltage levels. The variation is within 10% boundaries of the actual ratio. So, the comparator should be designed to tolerate a change of 10% in this case.

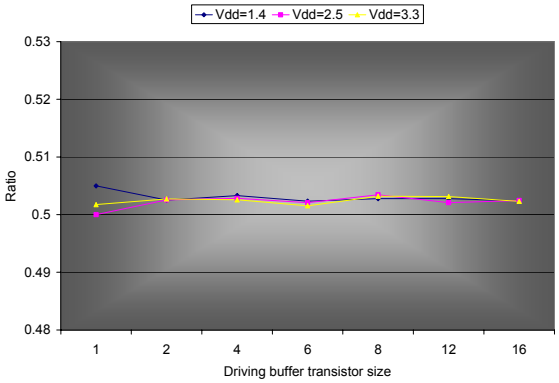

Figure 11 Voltage controllability with size of driving buffer.

One of the very important parameters on this technique and the previous techniques too is the distance between the DFT circuitry and the CIB. We simulated this distance and

tried to find the impact of the distance on the voltage ratio. As seen in Figure 12, a distance of up to 10 microns had no impact at all and a distance of 50 microns had a 10% impact. So, the DFT circuitry should be very carefully placed close to the CIB.

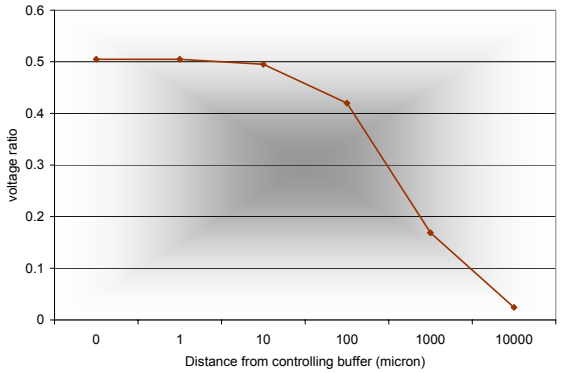

Figure 12 Impact of distance on voltage ratio.

7 CONCLUSIONS

This paper presented a DFT technique for controlled-impedance buffers. The technique aims at overcoming the disadvantages of the existing methods for CIB testing. It eliminates the need for PMUs and for a separate tester channel per CIB. While providing a higher quality of test, the technique significantly reduces the test cost for CIBs. The technique also provides a very unique delay testing circuitry to be able to test for delay defects in CIBs with a very low speed tester.

8 ACKNOWLEDGMENTS

The author would like to thank King Fahd University of Petroleum and Minerals and LSI Logic for supporting this research.

9 REFERENCES

[1] Arabi, T., and G. Taylor, "A JTAG Based AC Leakage Self Test," *Symposium on VLSI Circuits* (VLSI'01), pp. 205-206, 2001.

[2] Frodsham, R, and D. O'Brien, "Apparatus for I/O leakage self-test in an integrated circuit," *US Patent 6,262,585*, July, 2001.

[3] Haulin, T., "Built-In Parametric Test for Controlled Impedance I/Os," *VLSI Test Symposium* (VTS'97), pp. 123-128, 1997.

[4] Haulin, T., "Assembly and method for testing integrated circuit devices," *US Patent 5,996,102*, November, 1999.

[5] Muhtaroglu, A., B. Provost, T. Arabi, and G. Taylor, "I/O Self-Leakage Test," *International Test Conference* (ITC'04), pp. 903-906, 2004.

[6] Provost, B., T. Huang, C. Lim, K. Tian, M. Bashir, M. Atha, A. Muhtaroglu, C. Zhao, H. Muljono, "AC IO Loopback Design for High Speed uProcessor IO Test," *International Test Conference* (ITC'04), pp. 23-30, 2004.

[7] Sunter, S., C. McDonald, and G. Danialy, "Contactless Digital Testing of IC Pin Leakage Currents," *International Test Conference* (ITC'01), pp. 204-210, 2001.