A High Density, Carbon Nanotube Capacitor for Decoupling Applications

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ABSTRACT
We present a novel application for carbon nanotube devices, implementing a high density 3-D capacitor, which can be useful for decoupling applications to reduce supply voltage variations. The capacitor consists of staggered layers of interleaved carbon nanotubes, alternately connected to anode and cathode contacts. The device can realize a capacitance/area, significantly larger than the ITRS's projected requirements for year 2018. The capacitance per unit area can exceed 1pF/μm^2, with a quality factor greater than 100 at 1GHz.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – *Ad-vanced Technologies.*
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B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids.

General Terms: Performance, Design.

Keywords
Carbon nanotube, interconnect, capacitor, three-dimensional.

1. INTRODUCTION
Capacitors are important components in nanoscale processor circuits [1]. They are used in a variety of applications including the suppression of supply voltage variation (decoupling circuits) and analog/radio frequency signal processing (i.e. switched capacitor circuits). Today's semiconductor capacitors are based upon a parallel plate topology with different electrode materials. Their capacitance is determined by their parallel plate area (A), dielectric thickness (t) and dielectric permittivity ($\in$):

$$C = \in A/t \quad (1)$$

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For several technology generations, the placement and sizing of integrated capacitors for decoupling applications has been studied [2] [3]. Placement algorithms must balance the conflicting requirements of reducing the supply voltage variation while minimizing the amount of die area and leakage power consumed by the capacitors [4]. Because of their parallel plate topology, however, today's semiconductor capacitors face numerous challenges in the near future [5]. First, as component dimensions are scaled down, decreasing parallel pate capacitor area will result in a marked reduction in capacitance. Reducing t will offset the decreasing capacitance, but can lead to higher levels of leakage current. Finally, while new dielectric materials are being explored, their manufacturability is yet to be determined [5]. Therefore, new semiconductor capacitor candidate materials and topologies are being investigated for improved decoupling capacitors in future nanotechnology generations.

Carbon nanotubes (CNTs) are cylinders of very small diameter formed by rolling sheets of graphite [6]. When rolled correctly, a CNT can exhibit metallic properties, without a distinct bandgap. When CNTs are rolled with a single wall, ballistic transport of the electrons is possible in the presence of small and moderate electric fields. In addition, the current density of CNTs has been shown not to degrade even under extreme operating conditions (350 hours for J~10^{10}A/cm2 at 250 C [7]).

We propose a novel capacitor, CNCAP (Carbon Nanotube CAPacitor), consisting of multiple layers of interleaved CNTs, alternately connected to the cathode and anode. Each CNT electrode is surrounded by four CNTs connected to the opposing electrode (Figure 1). The proposed CNCAP can provide a very high capacitance/area, in excess of 1pF/μm^2. This is two orders of magnitude greater than the International Technology Roadmap for Semiconductors (ITRS) projected capability (11fF/μm^2) of MOS decoupling capacitor devices in the year 2018 [5]. CNCAP's quality factor is sufficient for use in analog and radio frequency applications. It can be used as a general replacement for metal-insulator-metal (MIM) capacitors. CNCAP's large capacitance per unit area makes it an excellent candidate for supply voltage variation decoupling circuits, greatly simplifying CAD decoupling capacitor placement algorithms. Finally, the unique CNT structure of the CNCAP permits it to be fabricated as an add-on module in the top layers of traditional silicon manufacturing processes.

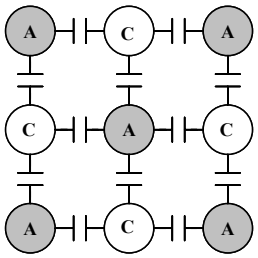


Figure 1. (a) High density capacitor composed of interleaved carbon nanotube cathodes (C) and anodes (A).

In this paper, we present the structure and model of CNCAP suitable for decoupling applications. In Section 2, we introduce the geometry and electrical model of individual cathode and anode CNT pairs. In Section 3, we develop the electrical model for the entire CNCAP structure. Finally, we present a comparison of our CNCAP structure to existing MIM capacitors in Section 4 and present our conclusions in Section 5.

2. CARBON NANOTUBE CAPACITOR UNIT CELL

Figure 2 shows two parallel CNTs. The physical parameters are: r (CNT radius), s (spacing between CNTs), and ℓ (CNT length). An electrical model of the two parallel CNTs [8] is shown in Figure 3. In Section 2.1, we will present the resistance of the CNTs. We will present the inductance of the CNTs in Section 2.2. Finally, we will introduce the various capacitance components of the cathode-anode CNT pair in Section 2.3.

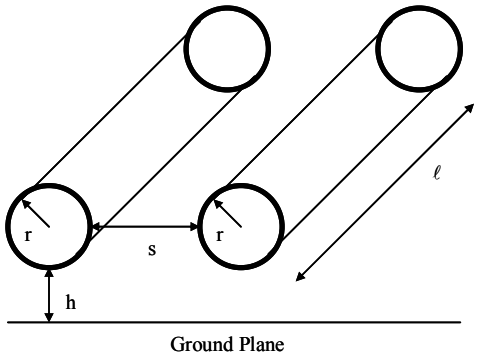


Figure 2. Geometry of two parallel carbon nanotubes.

2.1 Carbon Nanotube Resistance

One of the hallmarks of 1-D conduction is the limiting quantum resistance (characteristic of CNTs). As such, Ohm's Law does not hold for CNTs [9]. When the length of the conductor is scaled to the lengths less than the mean free path of scattering of electrons, we enter a regime of ballistic transport. However, the current flowing through the CNTs even in the limit of ballistic transport is limited by the fundamental resistance of 1-D transport, namely, the quantum contact resistance.

Because of their band structure, CNTs have two modes of propagation. In addition, in each of the two modes, the electrons can be either spin up or spin down resulting in four channels of conduction. When the CNT is modeled as a one dimensional conductor, these channels can be considered as four separate, but parallel, non-interacting channels of transport. For each channel

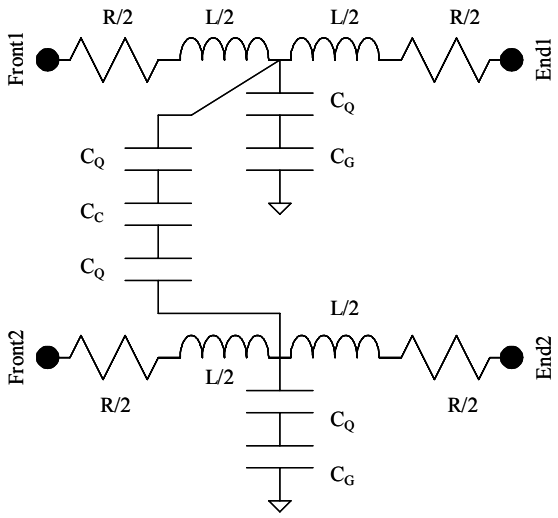


Figure 3. Electrical model of two parallel carbon nanotubes.

of transport, the quantum contact resistance has a value of h/e^2 [9]. Therefore, the quantum contact resistance for a CNT is:

$$R_{Q,CONTACT} = \frac{1}{4}\left(\frac{h}{e^2}\right). \tag{2}$$

However, when the channel length of a one-dimension conductor is increased beyond the mean free path of scattering of electrons, its resistance will increase. Below a critical bias threshold, the principle scattering mechanism in a CNT is due to acoustic phonons. From [10], [11], the resistance of a single CNT (under low bias conditions) is given by:

$$R = R_{Q,CONTACT} + \frac{1}{4}\left(\frac{h}{e^2}\right)\left(\frac{\ell}{\lambda_{acc}}\right) \tag{3}$$

$$R = \frac{1}{4}\left(\frac{h}{e^2}\right)\left(1+\frac{\ell}{\lambda_{acc}}\right) \tag{4}$$

where ℓ is the length of the CNT and λ_{acc} (approximately 1.6μm) is the mean free path due to acoustic phonon scattering.

For higher biases, other scattering mechanisms (optical phonon and zone boundary phonon) occur, and the CNT resistance increases appreciably. Therefore, the CNT resistance is not only a function of its length, but also its bias voltage. The resistance of the same CNT under high bias conditions is given by:

$$R = \frac{1}{4}\left(\frac{h}{e^2}\right)\left[1+\ell\left(\frac{1}{\lambda_{acc}}+\frac{1}{0.16\ell/V+\lambda_{high\ field}}\right)\right]. \tag{5}$$

where $\lambda_{high\ field}$ (approximately 30nm) is the mean free path at high electric fields, and V is applied bias.

2.2 Carbon Nanotube Inductance

To effectively model the CNT inductance, we need to consider both the magnetic inductance and the kinetic inductance. The magnetic and kinetic inductance of a CNT per unit length is given by [12]:

$$L_{MAGNETIC} = (\mu/2\pi)\cosh^{-1}(h/r) \approx 1pH/\mu m \tag{6}$$

$$L_{KINETIC} = (0.25)h/2e^2v_F = 4.07nH/\mu m. \quad (7)$$

where v_F is the Fermi velocity in graphite (approximately 7.96x10^{5}m/s). Because $L_{KINETIC}$ is several orders of magnitude larger than its magnetic counterpart, $L_{MAGNETIC}$ is usually neglected.

2.3 Carbon Nanotube Capacitance

Next, we address the three capacitances inherent in parallel CNTs (Figure 4) [12]. Each CNT has an associated quantum capacitance (C_Q) in series with the electrostatic coupling capacitance (C_C).

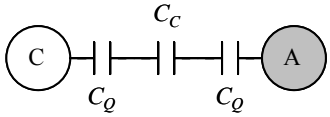


Figure 4. Capacitance of Parallel CNTs.

The electrons in a CNT can be thought of as a quantum electron gas in one dimension. Following Pauli's exclusion principle, it is not possible to add an electron with energy less than the Fermi energy of the system. For a CNT, the energy required to add an extra electron is given by:

$$\delta = hv_F/\ell \quad (8)$$

Equating δ with the energy stored in the quantum capacitance, we find:

$$C_Q = 4(2e^2/hv_F) = 388aF/\mu m \quad (9)$$

where v_F is again the Fermi velocity in graphite.

For the coupling (electrostatic) capacitances between neighboring CNT cathodes and anodes in our CNCAP, silicon dioxide was assumed for the dielectric. We numerically solved the Laplace equation for the subset interconnect structure (Figure 5) in the metallic limit (conductivity $\rightarrow \infty$), neglecting the fringing field at the ends of CNTs (a valid assumption for ℓ >>s).

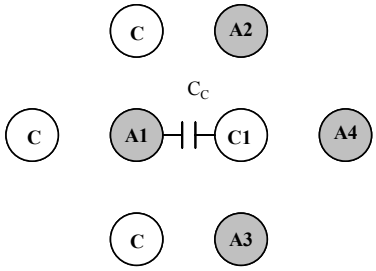


Figure 5. Subset of our proposed carbon nanotube structure with an individual electrostatic coupling capacitor (C_C).

We assume all of the electric field emanating from cathode C1 terminates on the four "nearest neighbor" anodes (*A1 - A4*). In addition, these electric field lines are equally distributed between *A1 - A4*. Therefore, the structure in Figure 9 gives an accurate estimate of the capacitance (C_C) between the CNTs *C1* and *A1* in our CNCAP structure. For r=0.5nm and s= 4.0nm; C_C is 15.6aF/μm, and the total capacitance between any CNT cathode-anode pair is:

$$C_T' = \left[(2/C_Q) + (1/C_C)\right]^{-1} = 14.4aF/\mu m. \quad (10)$$

3. PROPOSED CAPACITOR MODEL

With the resistance, inductance, and capacitance characteristics determined, we are now ready to develop the electrical model of our proposed CNCAP structure. It consists of multiple layers of interleaved CNTs, alternately connected to the cathode and anode (Figure 1). Each CNT is surrounded by four CNTs connected to the opposing electrode. This provides a very high ratio of electrode surface area to volume spacing and a very high capacitance/area device. Assuming the staggered, interleaved CNT interconnect structure is uniform, the coupling capacitance between each of the interior nanotubes is assumed to be equal. The capacitive coupling between fringe nanotubes will be larger than the coupling between interior nanotubes. To the first order, the capacitances can be assumed to be equal. We will address the magnitude of the coupling capacitance in the next sub-section.

Next, we assume a distributed model for any two opposing electrode CNTs (Figure 6). Therefore, the average equivalent series resistance for the capacitor is $R+\Delta R$. The average equivalent series inductance for the capacitor is $L+\Delta L$. As ΔR and ΔL go to zero, the series resistance and series inductance for any cathode-anode CNT pair will be given by R and L, respectively.

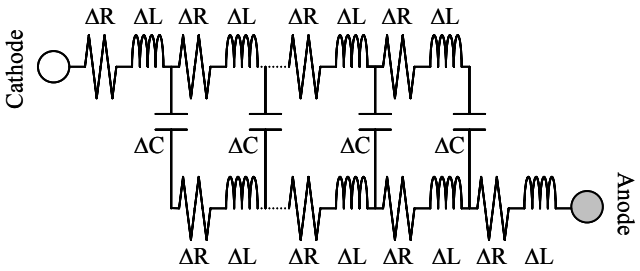
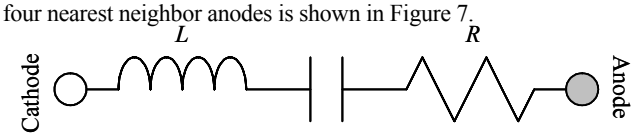


Figure 6. Distributed model of parallel carbon nanotube system showing the average parasitic resistance and inductance values are $R+\Delta R$ and $L+\Delta L$, respectively.

Using the above information, we developed an electrical model of our proposed CNCAP. The model for each CNT cathode and its four nearest neighbor anodes is shown in Figure 7.



$C_T = 4C_T'$

Figure 7. Electrical model of our proposed capacitor structure for each carbon nanotube interconnect cathode.

4. ANALYSIS OF CNCAP

Armed with our electrical model, we are now ready to compare the performance of our proposed CNCAP with MIM capacitors. We calculated the resistance (R) and inductance (L) of our CNCAP constructed of N CNTs of length ℓ. (This results in a capacitor with N/2 cathodes and N/2 anodes). The results are shown in Figure 10 for an applied bias of 1V.

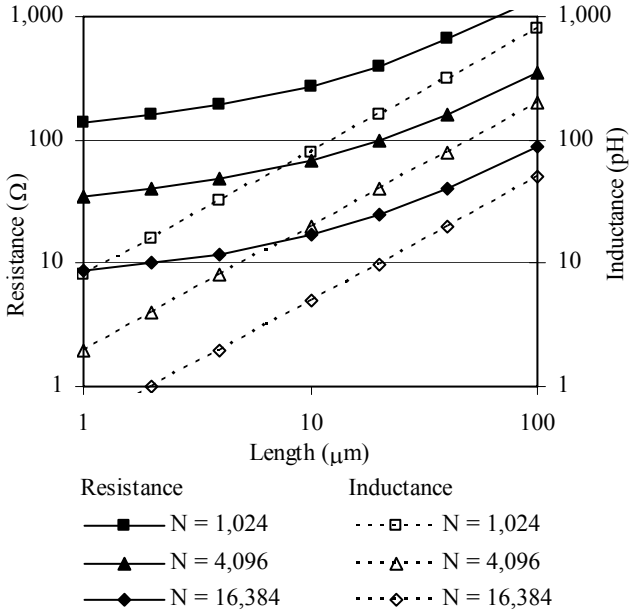


Figure 10. Carbon nanotube capacitor's equivalent series resistance (*R*) and inductance (*L*) vs. nanotube length (ℓ) and number of nanotubes (N) with a 1V applied bias.

We compared the capacitance per unit area of our CNCAP (varying the CNT separation, *s*) and the projected future capability for MOS capacitors (Table 1). In 2018, MOS capacitors are expected to exhibit a capacitance per unit area of 11fF/μm^2 [5]. For a CNCAP with 200 layers of interleaved CNTs, a capacitance per unit area of 1,160 - 2,710 fF/μm^2 can be achieved. Varying the number of interleaved CNT layers would linearly change the capacitance per unit area. Note, the capacitance per unit area would even be higher for dielectric materials with an increased permittivity.

In addition, the leakage current for each of the CNCAP configurations was calculated in the metallic limit (conductivity $\rightarrow \infty$). The WKB approximation [13] was used to calculate the electron tunneling probability for the silicon dioxide dielectric. The results were compared to the 2018 projected requirements for MOS capacitors (less than 2μA/cm^2 [5]). The results are again shown in Table 1. Therefore, to meet the expected leakage current requirements, inter-CNT separation distances of 4nm or more can be used while still increasing the capacitance per unit area by more than an order of magnitude.

Table 1. Projected Capacitance/Area for MOS Capacitor vs. 200 Layer CNCAPs

Capacitor Technology	Capacitance (fF / μm^2)	Leakage (/ μm^2)
2018 MOS Capacitor	11	< 20 fA
CNCAP, *s* = 2nm	2,710	1.83μA
CNCAP, *s* = 3nm	1,660	27.5pA
CNCAP, *s* = 4nm	1,160	0.586 fA

At 1GHz, CNCAP can achieve a Q of more than 100 for $s \geq 4$nm. (Note, Q is not a function of the number of CNTs in the CNCAP. As the number of CNTs is increased, the series resistance decreases linearly as the capacitance increases linearly.)

5. CONCLUSIONS

We presented a novel, three-dimensional capacitor structure composed of metallic, single wall carbon nanotubes. Because of their high capacitance per unit area (and low leakage current) the proposed carbon nanotube capacitor would provide increased flexibility in placement of large values of decoupling capacitance close to large current loads mitigating di/dt event supply voltage variations. We showed the structure can exhibit more than 1pF/μm^2 of capacitance per unit area, with an acceptable quality factor in excess of 100 at 1GHz. Both the capacitance per unit area and the quality factor exceed the 2018 International Technology Roadmap for Semiconductors's roadmap projections. The three-dimensional carbon nanotube capacitor is suitable for integration in future technology nodes (featuring directional carbon nanotube growth and quality metal-to-nanotube contacts). It can be implemented in the upper layers of traditional silicon wafer processing as an add-on module for improved performance in decoupling, analog, and radio frequency signal processing applications.

6. REFERENCES

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, New York: McGraw-Hill, 2001.

[2] H. H. Chen, "Minimizing chip-level simultaneous switching noise for high-performance microprocessor design," *Proc. Int. Symp. Cir. Sys.*, May, 1996, vol. 4, pp. 544-547.

[3] A. B. Kahng, B. Liu, and S. X. Tan, "Efficient decoupling capacitor planning via convex programming methods," *Proc. Int. Symp. Phy., Apr. 2006, pp. 102-107.*

[4] H. H. Chen, J. S. Neely, M. F. Wang, G. Co, "On-chip decoupling capacitor optimization for noise and leakage reduction," *Proc. Symp. Int. Cir. Sys*., Sep. 2003, pp. 251-255.

[5] International Technology Roadmap for Semiconductors. [Online]. Available: http://public.itrs.net/.

[6] M. S. Dresselhaus, G. Dresselhaus, and P. Avouris, *Carbon Nanotubes: Synthesis, Structure, Properties and Applications*. New York: Springer-Verlag, 2001.

[7] B. Q. Wei, R. Vajtai, and P. M. Ajayan, "Reliability and current carrying capacity of carbon nanotubes," *Appl. Phys. Lett.*, vol. 79, Aug. 2001, pp. 1172-1174.

[8] A. Raychowdury and K. Roy, "A circuit model for carbon nanotube interconnects: Comparative study with Cu interconnects for scaled technologies," in *Proc. Int. Conf. Computer Aided Design*, 2004, pp. 237-240.

[9] P. L. McEuen, M. S. Fuhrer, and H. Park, "Single-Walled Carbon Nanotube Electronics," *IEEE Trans. Nano.*, vol. 1, no. 1, Mar. 2002, pp.78-85.

[10] S. Salahuddin, M. Lundstrom, and S. Datta, "Transport Effects on Signal Propagation in Quantum Wires," *IEEE Trans. Elec. Dev.*, vol. 52, no. 8, Aug, 2005, pp. 1734-1742.

[11] J. Y. Park, *et al.*, "Electron-phonon scattering in metallic single-walled carbon nanotubes," *Nano Lett.*, vol. 4, no. 3, pp. 517-520, 2004.

[12] P. J. Burke, "Luttinger liquid theory as a model of the gigahertz electrical properties of carbon nanotubes," *IEEE Trans. Nanotech.*, vol. 1, no. 3, pp. 129-144, Sep. 2002.

[13] Taurus Device Simulator, Synopsys Inc., v2004.09.