High-Level Simulation of Substrate Noise in High-Ohmic Substrates with Interconnect and Supply Effects

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Abstract

Substrate noise is a major obstacle for mixed-signal integration. In this paper we propose a fast and accurate high-level methodology to simulate substrate noise generated by large digital circuits. The methodology can handle any substrate type, e.g. bulk-type or EPI-type, and takes into account the effects of interconnect and supply. For each standard cell a substrate macromodel is used in order to efficiently simulate the total system, which consists of a network of such macromodels. For a 40K gates telecom circuit fabricated in a 0.18 μm CMOS process, measurements indicate that substrate noise is simulated by using our methodology within 20% error but several orders of magnitude faster in CPU time than a full SPICE simulation.

Categories and Subject Descriptors

I.6.5 [**Computing Methodologies**]: SIMULATION AND MODELING – Model Development, Modeling methodologies. B.7.2 [**Hardware**]: INTEGRATED CIRCUITS – Design Aids, Simulation; Verification

General Terms

Design, Verification

Keywords

model order reduction, modeling, substrate noise

1. INTRODUCTION

The integration of the digital and the analog circuits on the same die brings some difficulties that endanger the gains in performance and form factor. One of the most important problems is the parasitic supply coupling and substrate noise coupling, which is caused by the fast switching of the digital gates [1].

Methodologies that check at the same time generation, propagation and immunity of analog designs to the substrate noise, are not yet mature. Typically, this problem is studied after the layout, which is too late in the design flow. Very often, only the isolation efficiency is checked without usually knowing the amount of noise injected into the substrate.

Previous work on gate-level characterization of substrate noise is very limited. For substrate noise the first effort to model gates with a lumped equivalent model has been made in [2] where a digital gate is modeled by a current source in parallel with its circuit and n-well capacitance. Methodologies that make use of real substrate noise waveforms extracted for each standard cell are presented in [3][4][5]. For every gate, a substrate noise current signature is extracted for every switching activity at the inputs. In [3][4], only switching at the outputs, which is coupled into the substrate via the drain capacitance, is taken into account, not at the inputs and the effects of the noisy power supply.

We have presented a methodology named SWAN (Substrate Waveform ANalysis) [6][7], which accurately simulates the actual waveform of the substrate noise voltage of a large digital circuit by considering both power supply coupling (*Ldi/dt*) and capacitive coupling (*CdV/dt*). SWAN can simulate the actual time domain waveform of the substrate noise voltage, related to the real circuit operation. Its accuracy has been demonstrated with EPI-type substrates. For such substrates, the bulk can be considered as one bulk node such that the individual macromodels can be combined in parallel to construct a chip-level substrate macromodel. However, nowadays bulk-type substrates are more used. In this case a simple parallel combination of the macromodels may not be feasible for bulk-type substrates. Instead a three dimensional resistive (or *RC*) mesh might need to be considered, in combination with a multiple-input-multiple-output system formed by a network of switching noise sources and many sensing nodes in the analog circuits. The extension of SWAN to high-ohmic substrates, which is the subject of this paper, circumvents this complex problem by macromodeling the problem, making the approach applicable to large digital circuits.

The interconnect is an important part of the circuit capacitance between V_{DD} and V_{SS}. For a 0.18 μm CMOS technology it was demonstrated that neglecting the interconnect underestimates the circuit capacitance by around 30 %. Interconnect will become more dominant in the future technologies. In this paper we take into account interconnect as part of this circuit capacitance as well as its impact on the supply current and resulting ground bounce.

The paper is organized as follows. In section 2 we present the different sources of substrate noise. We also formulate conditions for which the substrate can be neglected for ground bounce in high-ohmic substrates. In section 3 we describe the extensions of the high-level substrate noise simulation methodology to bulk-type substrates. In section 4 the accuracy of the methodology is demonstrated on a 40K gates telecom circuit fabricated in 0.18 μm CMOS process and compared to measurements.

2. SOURCES OF SUBSTRATE NOISE

In digital CMOS circuits substrate noise is caused by three mechanisms: coupling from the digital power supply, coupling from switching source–drain nodes and impact ionization in the MOSFET channel.

DAC'04, June 7–11, 2004, San Diego, USA.

Noise on the digital power supply is caused by voltage drops due to the inductance and resistance in the power supply connections to the chip. The combination of the inductance in the power supply connection and the on-chip capacitance between power and ground causes ringing of the power supply voltage. These effects are also called ground bounce or simultaneous switching noise [8]. Typically, the digital ground is connected to the substrate in every CMOS gate, which results in a very low impedance between digital ground and substrate, and all digital ground noise and ringing will also be present on the substrate. Therefore, this noise coupling mechanism is often the dominant cause of substrate noise [6].

The second origin of substrate noise is capacitive coupling from switching source and drain nodes of the MOSFETs.

The third source of substrate noise is impact ionization.

2.1 Effect of a bulk-type substrate on the V_{DD}-V_{SS} circuit admittance

Assuming that all gates under consideration belong to a single power domain, it is possible to combine the V_{DD}-V_{SS} admittances ($Y_{11}(j\omega)$) of each gate in the same power network to a single admittance [7]. The contribution of the substrate, which can be modeled by a resistive network extracted with SubstrateStorm [11], to the overall $Y_{11}(j\omega)$ is negligible for high-ohmic substrates [10] (see Fig. 1 for a 2-input NAND gate) for any digital gate. Further, the effect from the PMOS devices inside the n-well is negligible due to the shielding of the reverse-biased n-well. In the figure the symbol C_c refers to the circuit capacitance, which is computed using the V_{DD}-V_{SS} admittance.

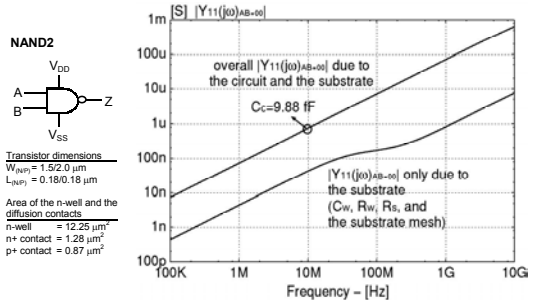

Fig. 1: Contribution of the substrate in the overall V_{DD}-V_{SS} admittance ($Y_{11}(j\omega)$) of a NAND2 gate in a 0.18 µm CMOS process on a bulk-type substrate with 18 Ωcm resistivity.

2.2 Comparison of the parasitic bulk current with the charge/discharge current

Besides the impedance division in the substrate the high ratio of the total drain-source current to the substrate current through the NMOS transistor further justifies the assumption of neglecting the substrate in $Y_{11}(j\omega)$. The ratio of the drain junction capacitances of the NMOS transistor to the load will give the proportionality between the peak value of the substrate current $i_{DB}(t)$ (I_{DB}) through the NMOS and the peak value of the digital ground ground current $i_{DS}(t)$ (I_{DS}), which charges/discharges the load seen by the driver. The effect from the PMOS is neglected due to the shielding by the n-well. The ratio I_{DS}/I_{DB} is defined by λ:

$$\frac{I_{DS}}{I_{DB}(NMOS)} = \frac{C_{load} + C_{pdrive}}{C_i(NMOS)} = \lambda \qquad (1)$$

where C_{load} is the sum of the oxide capacitances of the fanout logic and the interconnect capacitance seen at the output. C_{pdrive} is the sum of all capacitances of the switching driver, which need to be charged by the driver itself. The capacitance C_{pdrive} consists of several contributions, as will be discussed below. Note that C_{pdrive} also contains $C_j(NMOS)$.

Without loss of generality, the ratio I_{DS}/I_{DB} is now demonstrated for an inverter (W_P/L_P=2.0/0.18 µm and W_N/L_N=1.1/0.18 µm) in 0.18 µm CMOS process on a bulk-type substrate (resistivity of 18 Ωcm). The conclusions for other gates are similar. The inverter drives another identical inverter. When the inverter output switches from LOW to HIGH, the inverter is mostly in the states (PMOS=Saturation, NMOS=Saturation) and (PMOS=Cut-off, NMOS=Linear). In this case the average value of λ is found to be 13.01. For the inverter output switching from HIGH to LOW, λ equals 10.47. For larger load values λ becomes larger. The worst-case (minimum λ) occurs when the gate is unloaded since C_{load}=0. In this case λ becomes 8.52 and 6.95 for the rising and falling output respectively.

The current $i_{DB}(t)$ injected from the junction splits into two parts: $i_{CW}(t)$ represents the part taken away via the substrate contacts, whereas $i_{BG}(t)$ is the part that is picked up by the grounded backside contact (see the π-circuit of Fig. 2). There is also the impact ionization current $i_{DI}(t)$ but it is not significant for deep submicron technologies with low supply voltages. So we neglect the impact ionization current $i_{DI}(t)$. Using this π-network the ratio between the peak values of the digital ground return current $i_{DS}(t)$ (I_{DS}) and the current $i_{BG}(t)$ (I_{BG}) is found to be:

$$\frac{I_{DS}}{I_{BG}} = \lambda.\frac{R_{ds} + R_{cw}}{R_{cw}} \qquad (2)$$

For this technology I_{DS}/I_{BG} is found to be 672 and 541 for the LOW-to-HIGH and HIGH-to-LOW switching output respectively. Further, we find I_{BG}/I_{DB} ≈0.02, which means that only 2% of the current injected by the NMOS device via the junction, goes deeper into the substrate. A worst-case condition occurs when the substrate contacts are placed very far from the noisy digital gate ($Rc>>Rb1,2$). In this case, $I_{DS}/I_{BG}=I_{DS}/I_{DB}=\lambda$. However, this situation is very extreme and it never occurs in practice

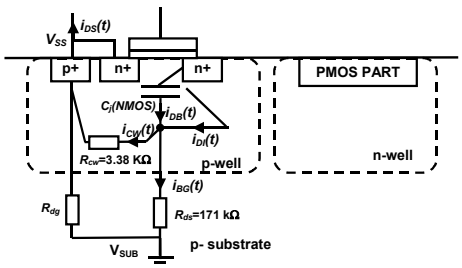

Fig. 2: Substrate current from the NMOS device for 0.18 µm CMOS process on a bulk-type substrate.

The ratio I_{DS}/I_{BG} tends to increase with technology downscaling. Indeed, this ratio depends on a ratio of resistors (namely $(R_{ds}+R_{cw})/R_{cw}$) and a ratio of capacitors (namely λ). The resistor ratio, which depends on the ratio between the doping of the substrate and the p-well, tends to increase as the p-well doping increases with technology scaling. This yields an almost linear decrease of R_{cw} with the increase of doping. On the other hand, λ

decreases due to an increase of the junction capacitance with doping. However, this increase is sub-linear for an abrupt junction, such that in total the ratio I_{DS}/I_{BG} increases.

The above analysis of the substrate current injection due to capacitive coupling has been carried out for an inverter. The resistive division from equation (2) has about the same value for other standard cells in the same library since the resistances R_{cw}, R_{dg}, and R_{ds} scale down at the same rate as the rate of increase of the cell width. This means that the resistive ratio as well as the ratio of capacitors (namely λ) do not change significantly from one cell to another.

By these findings we conclude that the bulk current injected from the substrate contacts is not significant and it tends to get smaller in future technologies. So the bulk current injected from the junctions can further be neglected. On the other hand coupling from the noisy power supply via substrate contacts remains the dominant mechanism, as previously demonstrated by measurements [10].

3. ANALYSIS METHODOLOGY

The macromodel shown in Fig. 3 is now used to analyze substrate noise generation in bulk-type (high-ohmic) substrates. The different components of this linear macromodel are [7]:

1. passive models of the non-switching gates, mainly capacitive, between V_{DD} and V_{SS};
2. a current source modeling the active gates, drawing a current from V_{DD} and sinking it to V_{SS};
3. a package model, i.e. bondwires and a damping resistance
4. a substrate mesh connecting the on-chip power grid to the substrate, which is the primary source of substrate noise as explained in previous section.

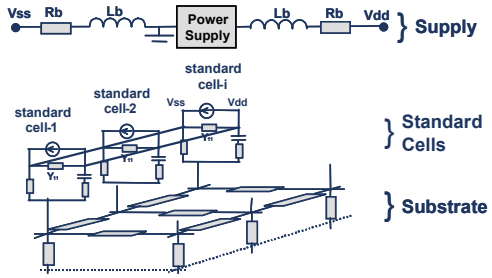

Fig. 3: Macromodel used for simulating substrate noise generation in high-ohmic substrates.

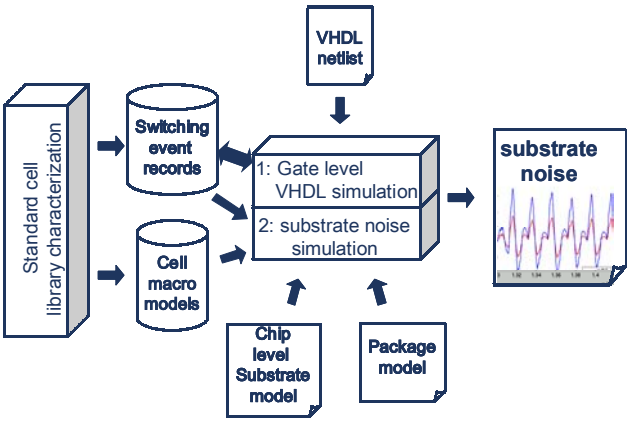

Fig. 4: Substrate noise generation analysis flow.

In Fig. 4 the proposed analysis flow is shown for substrate noise generation on high-ohmic substrates. It consists of two steps: (1) a standard cell library characterization, which is a one-time effort for a technology, and (2) an evaluation of the macromodel at design time. The latter also consists of two tasks as indicated on the figure. First the switching activity of the design is extracted by using a VHDL gate-level simulation [6]. In a second step the macromodel is excited with the supply current derived from the switching activity.

3.1 Standard Cell Library Characterization

Standard cell characterization extracts two components of the macromodel, namely a circuit admittance between V_{DD} and V_{SS} for every logic gate and the supply current signature for each type of switching event.

As shown in [10] the circuit admittance (mainly a capacitance) is logic-state dependent. For a single gate the variation can be up to 6 %. However, due to the large number of gates the circuit admittance varies only a few percentages between different clock cycles. Hence, it is sufficient to extract the admittance for all logic states of all types of gates and combine them, weighted with the relative occurrence of the logic states, based on information from the switching activity file.

The supply current of the gates is extracted for all types of switching activity [6]. The following paragraphs explain how this extraction procedure has been improved compared to [7] and extended to include interconnect effects.

3.1.1 Load modeling at the Driven Gate's input

In Fig. 5 (left) a typical characterization setup of a gate is shown. Important to note is that all input sources and load are referenced to ground. For supply current modeling this ground-referenced setup has important disadvantages as will be explained below.

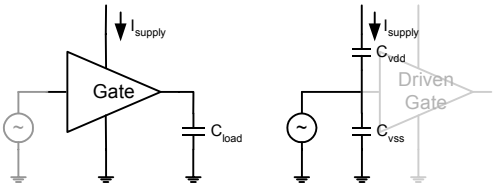

Fig. 5: Ground-referenced supply current characterization (left) and input capacitance model of a driven gate (right).

Consider a rise event at the output of the gate. Then the circuit charges the load and I_{supply} will contain a load current contribution. On the other hand, for an output fall event the load is discharged through the gate and I_{supply} will not contain a load contribution. In reality the load of a gate consists of interconnect (see next paragraph) and driven logic, i.e. not a pure ground referenced capacitance.

In Fig. 5 (right) this driven logic gate is shown with an equivalent input capacitance model. The input capacitance is partly referenced to ground and partly to supply. For a rising input event (i.e. the output of another gate has produced a rise event), the ground referenced input source charges both the ground referenced and the supply referenced input capacitance, returning current to the supply line (negative supply current). The total contribution to the supply current of the cascade of a driver and driven gates for a rise event on a net is obtained by subtracting from the load current at the driver gate all input capacitance currents referenced to supply at the driven gates.

For falling input events the ground referenced input source discharges the ground referenced capacitance and charges the supply-referenced capacitance. The contribution of the driver gate load is counted at the driven gate in this case and is a pure addition (i.e. all positive quantities).

This analysis shows that for rising events any error in load modeling at the driver or timing error between the driver and driven gates will introduce errors in the total supply current, while for falling events such error is impossible.

With the above considerations in mind, the classical characterization model (Fig. 5) is better replaced by the one shown in Fig. 6a and b. The load capacitance is always referenced such that it is discharged (this depends on the state at the output). The input source is referenced such that it charges the relevant capacitance of the driven gate (this depends on the state at the input). This is what we define as modeling load current at the driven gate's input. This approach has the following advantages:

- pure addition of positive quantities to find the total supply current, the load current is only counted where it charges a capacitor.
- supply current dependence of a driver gate to its load value is greatly reduced: only the short circuit current in the driver gate is influenced by the load value. This is typically a second-order effect. Hence there is much less variation of supply current on the load value, making the modeling easier.
- interconnect modeling. The interconnect load is directly added to the load of the driver gate, it will correctly influence the short circuit current.

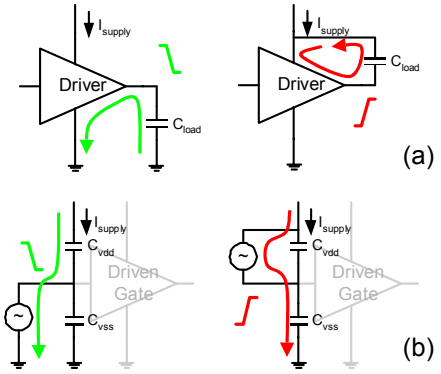

Fig. 6: Reference to determine supply current depends on type of event: (a) at the output of a gate the capacitor is discharged, (b) at the input the relevant capacitor is charged.

3.1.2 Interconnect Modeling

In deep-submicron technologies the impact of interconnect on supply current is increasing. For nanometer technologies it is predicted to be the dominating factor in power consumption [12]. It is thus essential to include interconnect effects.

The attentive reader will have remarked that although the impact of interconnect on the short circuit current is now included, the actual charging current of the interconnect has not been included.

Fig. 7a shows a model of the interconnect capacitance. It is partly referenced to ground, partly to supply. It resembles the input model of a logic gate, and thus an implementation is straightforward. For every net in the design an instance of the interconnect model is added to circuit, where the total value of the interconnect capacitance is divided between the ground and supply capacitance. The total value is obtained by layout extraction tools.

The capacitance division between ground and supply is a parameter for the cell and can be adjusted for individual nets.

3.1.3 Comparison of transistor-level simulations with macromodeling

In Fig. 7b the supply current calculated by summing the extracted currents is compared to a transistor-level simulation (Spectre) of a 0.18 µm CMOS clock buffer driving two other clock buffers. Extracted layout parasitics have been taken into account. Since these buffers are placed further apart a large interconnect load is present on the output of the first clock buffer. As shown in the figure, omitting this interconnect load causes a big error in the peak value of the current and in the total charge (expressed in pC in Fig. 7b) consumed by the circuit. Omitting the interconnect load would cause an error of approximately 12% on the total charge consumed.

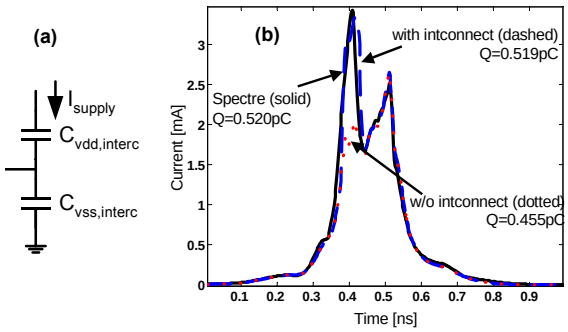

Fig. 7: (a) Interconnect load model and (b) comparison of simulated supply currents, Spectre versus SWAN with and w/o interconnect.

3.2 Macromodel evaluation

A model extraction for high-ohmic substrates results into a large mesh of capacitors and resistors (Fig. 3) with multiple inputs and multiple outputs (MIMO), which is too large for efficient high-level simulations. A model-order reduction strategy is required to obtain accurate and efficient high-level simulations. These high-level simulations are performed using highly optimized digital filter approximations of the reduced model.

Two approaches can be followed to generate such reduced order model:

1. Projection techniques. These start from the complete netlist representation and applies well-chosen project techniques to reduce the model order. In this way, passivity of the system can be guaranteed [13]. However, only the stability of the transfer functions is required when determining the equivalent digital filter for substrate noise simulations. This implies that only stability (and not passivity) is an issue in our case.
2. Modeling techniques that start from table-based frequency-dependent transfer functions obtained by either AC-simulations or measurements. Identification techniques are then used to fit a model onto the table-based transfer functions. The extraction of stable filters can be obtained using different strategies [13][14].

The use of identification techniques has another important advantage over model-order reduction techniques by projection:

identification techniques are able to fit the wanted frequency response function directly in the z-domain. This is not possible when using projection-based model-order reduction since a Laplace-domain model is transformed into a (reduced-order) Laplace-model. This requires an additional translation step from the Laplace domain towards the discrete-time domain. Such transformations (e.g. bilinear transformation) introduce additional distortion (e.g. frequency warping). A subspace identification technique [15] with regularization [13][14] is used to determine a discrete-time MIMO state-space model that is fitted onto the frequency response of the substrate:

$$\begin{cases} zX = AX + BU \\ Y = CX + DU \end{cases} \quad (3)$$

with

$$Y = \left[C(zI - A)^{-1}B + D\right]U \quad (4)$$

where z denotes the z-variable in the discrete-time domain; A,B,C and D are the system matrices and U, Y and X represent the vector of inputs, outputs and n state variables, respectively. Hence, the order of the system is n.

The simulation efficiency of the subspace model can be increased by determine a band-diagonal representation of A [15]. This is always possible since one can always find a regular matrix T such that (A, B, C, D) and (TAT^{-1}, TB, CT^{-1}, D) represent the same transfer function. Hence, A can be made band diagonal such that the computational efficiency can be increased.

Subspace identification algorithms are basically three-step algorithms [15]:

1. An estimate of the extended observability matrix O is obtained by applying a projection onto the output spectra, Y, which is constructed such that the influence of the input spectra, U, are projected away. The resulting extended observability matrix therefore contains only information on A and C since the influence of BU and DU are projected away.
2. An estimate of the matrix A is found as the linear least-squares solution of the over-determined set of equations given by a shift property of the extended observability matrix O. An estimate of C can be extracted directly out of the extended observability matrix O.
3. Once A and C are determined, it is possible to estimate the matrices B and D using a linear least-squares solution.

In step 2 of the subspace identification, i.e. during the estimation of A and C, stability is imposed with two techniques. A first method moves the instable poles into the stable region using a projection into the unit circle in the z-domain [15]. A second method is only applicable to the z-domain and uses a regularization of the linear least-squares problem to compute A such that all poles are within the unit circle [16]. The modeling errors that result from imposing stability can be corrected in Step 3 during the least-squares estimation of B and D.

4. EXPERIMENTAL RESULTS

The accuracy of our high-level simulation methodology has been verified with measurements on a 40K gates telecom circuit (circuit L1 in Fig. 8), fabricated in a 0.18 µm 6 M CMOS process on a high-ohmic substrate with 18 Ωcm resistivity. It contains a 20-bit maximum-length-sequence Pseudo-Random-Binary-Sequencer (PRBS) circuit driving two cascaded sets of the IQ modulator and demodulator chains (Fig. 9). The PRBS circuit generates a trigger signal (TRIGOK) to synchronize the measurements. There is a checksum comparator circuit comparing the output of the data path with the expected output in order to check whether the circuit is running properly or not. Whenever the circuit functions correctly the signal (FUNCOK) becomes continuously HIGH, else it remains LOW.

A SPICE computation of the AC model of a 40K gates telecom circuit takes 6 hours for the netlist extraction from the layout and around 5 days for the AC simulation itself. The netlist of circuit L1 contains 119762 transistors and 58939 interconnect capacitances. With our method the computation of the same circuit capacitance by superposition of the one-time characterized macromodels takes less than a second. The macromodels are constructed in around 10 minutes, including the time for netlist extraction from the layout of each gate.

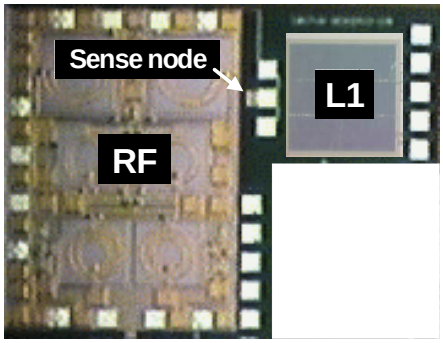

Fig. 8: Microphotograph of the test circuit (L1), 40K gates telecom circuit and the analog victim with the sense node in between.

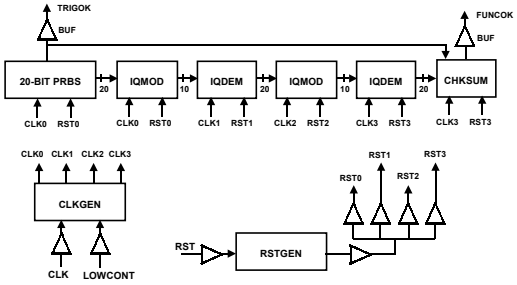

Fig. 9: Schematic of the test circuit.

At a supply voltage of 1.8 V, the calculated value of the circuit capacitance is 271pF. This is composed of 236pF logic gate capacitance, 20pF well capacitance and 15pF interconnect capacitance assuming that all interconnect capacitance is coupling capacitance. The measured value at that voltage is 261pF, which is an error of less than 4%.

A final verification of the analysis methodology is the comparison of measurements and simulations of the generated substrate noise. This noise is measured at a sense node (Fig. 8) in between the telecom circuit and the analog circuit. Using SubstrateStorm [11] a substrate netlist was extracted modelling the digital to sense node coupling, representing for instance the back node of a transistor.

In Fig. 10 a simplified macromodel representation of the digital to sense node coupling is shown. The ground bounce of the digital circuit produced by switching current noise is coupled to both the

ground of the analog circuit (R_{dig2an}) and to the sensitive node near the analog circuit ($R_{dig2sens}$). The analog ground and digital ground are connected externally to a common ground. The substrate noise voltage has been measured between the sensitive node and the analog ground using a 50 Ω probe system. It is important to note that resistance $R_{dig2sens}$ is the largest impedance in the system (~350 Ω) and determines the attenuation of the ground bounce noise of the digital circuit (i.e. a simple resistive division between $R_{dis2sens}$ and the 50 Ω measurement impedance).

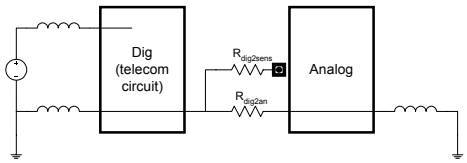

Fig. 10: Explaining the coupling in the substrate noise experiment.

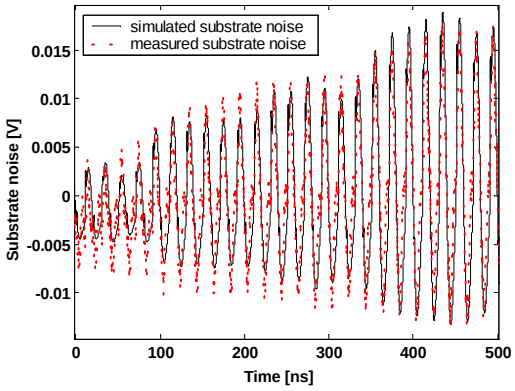

Fig. 11: Simulated versus measured substrate noise at a sensitive node near the analog circuit.

In Fig. 11 a comparison of the measured versus simulated substrate noise voltage is shown. The digital circuit is clocked at 50 MHz, which is close to the resonance frequency of the package (approximately 55 MHz) to maximize the substrate noise voltage (for the experiment's sake). The first 25 clock cycles after end of reset have been plotted. Clearly visible is the start-up of the PRBS that gradually increases the activity of the circuit. The RMS value of the measured substrate noise is 6.5 mV, of the simulated waveform 7.7 mV, an error of 20%. The simulation time of this macromodel is less than 10 minutes on a standard Pentium IV workstation.

5. CONCLUSIONS

To model substrate noise generated in digital CMOS circuits of practical size, processed both with EPI-type and bulk-type substrate technologies, we have developed a fast and accurate macromodeling approach. We have proven that for bulk-type substrates bounce on the digital power supply lines is the main substrate noise injection mechanism and we have presented the conditions on the power supply current for which the significance of the bulk current via the drain junction capacitance is neglected for substrate noise. Since interconnect has a significant influence on the generation mechanisms of substrate noise for future technologies we have taken into account interconnect in the substrate noise macromodel characterization. For a 40K gates telecom circuit fabricated in 0.18 µm CMOS process the measurements have indicated that substrate noise is simulated with our methodology within 20% error but several orders of magnitude faster in CPU time than a full SPICE simulation.

ACKNOWLEDGEMENTS

This work was partially funded by the MEDEA+/Witness project.

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