SOC-NLNA: Synthesis and Optimization for Fully Integrated Narrow-Band CMOS Low Noise Amplifiers

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ABSTRACT

In this paper we present SOC-NLNA, a systematic synthesis methodology for fully integrated narrow-band CMOS Low Noise Amplifiers (LNA) in high performance System-on-Chip (SoC) designs. SOC-NLNA is based on deterministic numerical nonlinear optimization and the Normal Boundary Intersection (NBI) method for Pareto optimization. To enable SoC integration, we simultaneously optimize both devices and passive components to yield integrated inductor values that are significantly less than those generated by traditional design techniques. When the synthesized LNAs are simulated using Cadence SpectreRF, SOC-NLNA yields up to 35 and 58 percent improvement in noise figure and gain. Leveraging the efficiency of our methodology, we are able to generate the Pareto surfaces between LNA performance metrics in seconds.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids

General Terms

Design, Algorithms

Keywords

Low Noise Amplifier, LNA Optimization, Analog Synthesis

1. INTRODUCTION

Given the increasing demand for wireless systems in system-on-chip (SoC) technology, the automated design and optimization of fully integrated CMOS Low Noise Amplifiers (LNA) is vital for meeting power and performance requirements while substantially reducing time-to-market and cost [1, 2, 3]. Successful LNA designs will efficiently balance critical figures of merit including noise figure, gain, power consumption and input and output impedance matching. In addition to these important design considerations, fully integrated LNA designs must also consider the impact of circuit element sizing and the parasitics that are inherently present in the SoC environment. LNA synthesis methodologies that account for these important design constraints will deliver designs with greater functionality, increased performance and improved reliability.

Previous LNA design techniques primarily fall into two categories: (1) equation-based design or (2) numerical design optimization. Equation-based design techniques utilize explicit expressions for the design parameters that optimize certain figures of merit. Due to the simplifying assumptions necessary to create explicit expressions for optimum component values, these techniques may not account for the inductor or device parasitics and typically lack the flexibility to exploit more complex circuits in order to realize component values that are suitable for SoC integration [4, 5, 6, 7].

Numerical design optimization techniques iteratively search the design space in order to find LNA designs that optimize certain figures of merit while meeting performance constraints. Stochastic single objective and multi-objective optimization routines based on simulated annealing [8], particle swarm optimization [9] or evolutionary algorithms [10], while eventually converging to near-optimum solutions, require significant simulation time for problems with nonlinear constraints. Consequently, these algorithms are appropriate for complex optimization problems with many local minima or discrete design variables. Since the objective and constraint functions for many analog design problems are relatively smooth [11], optimization routines based gradient-based nonlinear programming techniques can provide a substantial performance improvement.

In this paper we present SOC-NLNA, Synthesis and Optimization for fully integrated Narrow-band CMOS Low Noise Amplifiers. SOC-NLNA is a systematic synthesis methodology for fully integrated CMOS LNAs in high performance SoC designs based on deterministic single and multi-objective optimization techniques. Leveraging analytical LNA modeling techniques, SOC-NLNA utilizes Sequential Quadratic Programming (SQP) [12] and the Normal Boundary Intersection (NBI) method [11, 13] to simultaneously optimize the LNA's input and output matching networks, transistor sizes and bias voltages to ensure that the LNA meets performance requirements and has passive component values that are suitable for SoC integration. Our results indicate that SOC-NLNA yields up to 35 and 58 percent improvement in noise figure and gain, respectively, on designs simulated using Cadence SpectreRF while providing inductor values that are more than one order of magnitude less than those generated by traditional design techniques. By generating significantly smaller inductor values, we enable the SoC integration of the complete LNA. Finally, leveraging the efficiency of SOC-NLNA, we are able to generate the Pareto surfaces between LNA performance metrics in seconds.

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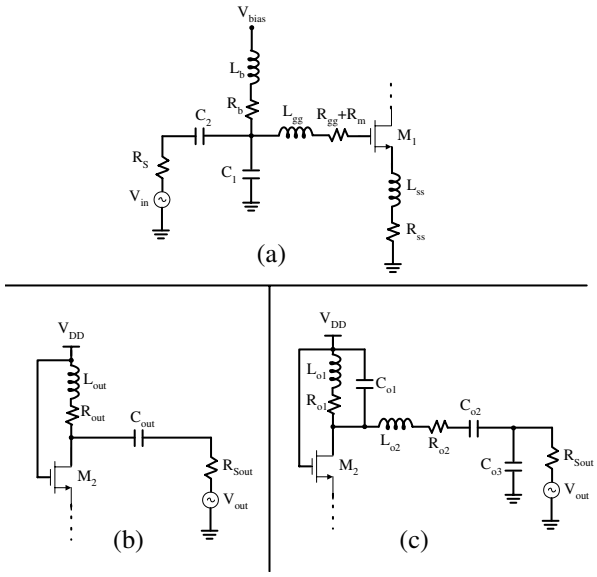

Figure 1: Inductive source degenerated LNA with input (a) and output (b,c) matching networks.

2. LNA MODELING

2.1 LNA Design Considerations

The main function of an LNA is to amplify the weak signal from the receiving antenna. As a result, the LNA affects the performance of the entire RF receiver. To obtain the maximum gain with minimal additive noise, the LNA's impedance should be matched with both the input and output analog blocks to guarantee maximum power transfer. Therefore, the input and output matching networks, depicted in Figure 1, are vital to the LNA's performance. Input and output matching network performance also depends on the parasitics of the transistors M_1 and M_2, respectively, which also effect the LNA's noise figure, gain and the power consumption. Traditionally, portions of the the biasing and input matching networks are realized using off-chip components due to the large inductor and capacitor values that may be required [4, 5, 6]. To enable the SoC integration of the entire LNA, we will exploit and optimize the impedance matching networks to realize suitable passive component values. In this paper we will consider the three input and output impedance matching topologies shown in Figure 1. Note that R_{ss}, R_{gg}, R_b, R_{out}, R_{o1} and R_{o2} are the internal resistances of the inductors L_{ss}, L_{gg}, L_b, L_{out}, L_{o1} and L_{o2}, respectively.

2.2 Modeling of Passive Components

The complete SoC integration of the LNA requires precisely characterized integrated inductors and capacitors in order to match the input and output impedances of the amplifier. Integrated spiral inductors typically have significant parasitic resistances that can impact impedance matching, gain and noise figure [7]. When characterizing the LNA at a particular operating frequency, which is typically the case for narrow-band LNA design, on-chip inductor elements must be accompanied by an equivalent resistance, $R_{eff} = \omega L_{eff}/Q$, where Q the quality factor of the inductor. At a particular operating frequency, R_{eff} and L_{eff} are not just the physical inductance and resistance of the spiral inductor's conductors, but also include the effects of all resistive, capacitative, and inductive parasitics in the substrate and conductors. Note that for time-domain simulation or characterization at multiple frequencies, wide-band inductor models based on the 11-element or 2-π configuration should be used [15]. We utilize the synthesis techniques presented in [15] to determine the quality factor (Q_{max}) achieved by the optimal inductor design for a given effective inductance value (L_{eff}) and operating frequency (f), $Q_{max} = S(L_{eff}, f)$, which can then be used to calculate R_{eff}. The geometric dimensions of the integrated inductors can be determined using an inductor optimization methodology such as [14]. We utilize the modeling techniques in [16] to characterize metal-insulator-metal capacitors.

2.3 Analytical LNA Model

To enable the automated synthesis of integrated LNAs, models that appropriately balance speed and accuracy must be developed to ensure that circuits meet design requirements while maintaining reasonable simulation times. Circuit-level simulators provide the most accurate means for modeling LNAs in deep sub-micron technologies but typically require long simulation times. Since synthesis methodologies may evaluate hundreds of designs during design space exploration, using a circuit-level simulator as the primary modeling engine requires an intractable period of time [17].

We have developed an analytical modeling methodology for fully integrated inductively-degenerated CMOS narrow-band cascode LNAs that captures short channel transistor effects to enable rapid design space exploration in current and future process technologies [17]. Our model efficiently considers integrated passive components, device parameters and their associated parasitic resistances and capacitances. By considering the devices and passive components simultaneously, we can generate more efficient designs. In the noise figure model, we considered the parasitics in the circuit elements and short channel noise sources such as gate induced noise, distributed gate resistance, and channel resistance due to nonquasi-static assumption. Although gate induced noise is not included in BSIM3v3, we include it in the model by dividing every transistor into five segments to generate the gate induced noise effect [18]. While the transistor M_1 is the most significant contributor to the noise figure of the LNA, we also consider the noise generated from the second transistor, M_2. Note that we neglect the noise generated from the internal resistances of the inductors in the output network because the signal will already amplified at this point. To characterize impedance matching, gain, and power dissipation, we use the model presented in [17].

3. LNA SYNTHESIS

3.1 LNA Optimization Problem Formulation

In order to be successfully realized in the SoC environment, fully integrated narrow-band CMOS LNAs must be designed to consider the impact of device and passive component parasitics and ultimately have values that can satisfy performance and area constraints without having to resort to off-chip components. In general, the LNA optimization problem can be formulated as a multi-objective optimization problem where the objective functions include noise figure,

gain and power dissipation and the constraints include input and output impedance matching, and bound constraints on component values. Mathematically, the optimization problem can be expressed as

$$\text{Minimize} \quad \begin{bmatrix} F(\overrightarrow{x}) \\ G(\overrightarrow{x}) \\ P(\overrightarrow{x}) \end{bmatrix}$$

$$\text{Subject to} \quad \begin{pmatrix} \mathrm{Re}(Z_{in}(\overrightarrow{x})) = \mathrm{Re}(Z_{sin}) \\ \mathrm{Im}(Z_{in}(\overrightarrow{x})) = \mathrm{Im}(Z_{sin}) \\ \mathrm{Re}(Z_{out}(\overrightarrow{x})) = \mathrm{Re}(Z_{sout}) \\ \mathrm{Im}(Z_{out}(\overrightarrow{x})) = \mathrm{Im}(Z_{sout}) \\ \overrightarrow{x_{min}} \leq \overrightarrow{x} \leq \overrightarrow{x_{max}} \end{pmatrix} \quad (1)$$

$$\overrightarrow{x} = \left[W_1, W_2, V_{gs}, \overrightarrow{Z_{ic}}, \overrightarrow{Z_{oc}}\right]^T \quad (2)$$

where $F(\overrightarrow{x})$, $G(\overrightarrow{x})$ and $P(\overrightarrow{x})$ are the noise figure; negative gain, since gain should be maximized; and power consumption of the LNA, respectively. The vector $\overrightarrow{x}$ contains the LNA design parameters, where W_1 and W_2 are the widths of transistors M_1 and M_2, respectively, as depicted in Figure 1, V_{gs} is the bias voltage applied to M_1, $\overrightarrow{Z_{ic}}$ and $\overrightarrow{Z_{oc}}$ are vectors of inductor and capacitor component values for the input and output impedance matching networks, and Z_{sin} and Z_{sout} are the input and output source impedances that need to be matched. Other possible objective and constraint functions include the area consumed by the passive components and the IIP^3 linearity of the amplifier. The bound constraints on the passive component values are used to ensure that the optimized LNA design can be fully integrated on-chip. Since $F(\overrightarrow{x})$, $G(\overrightarrow{x})$ and $P(\overrightarrow{x})$ cannot be simultaneously minimized, we need to find the Pareto-optimal trade-off surfaces relating each of these design metrics in order to synthesis an LNA that maximizes overall performance while meeting design constraints based on a particular application's requirements.

3.2 Single-Objective LNA Optimization

In order to deterministically solve the complete multi-objective optimization problem described in the previous section, we need to solve a series of optimization problems to either (1) minimize a single performance objective ($F(\overrightarrow{x})$, $G(\overrightarrow{x})$ or $P(\overrightarrow{x})$) and set the remaining performance objectives as constraints, or (2) minimize a weighted combination of performance objectives. For noise figure minimization, this single-objective optimization problem would be cast as

$$\text{Minimize} \quad F(\overrightarrow{x})$$

$$\text{Subject to} \quad \begin{pmatrix} Gain(\overrightarrow{x}) \geq G_{min} \\ P(\overrightarrow{x}) \leq P_{max} \\ \mathrm{Re}(Z_{in}(\overrightarrow{x})) = \mathrm{Re}(Z_{sin}) \\ \mathrm{Im}(Z_{in}(\overrightarrow{x})) = \mathrm{Im}(Z_{sin}) \\ \mathrm{Re}(Z_{out}(\overrightarrow{x})) = \mathrm{Re}(Z_{sout}) \\ \mathrm{Im}(Z_{out}(\overrightarrow{x})) = \mathrm{Im}(Z_{sout}) \\ \overrightarrow{x_{min}} \leq \overrightarrow{x} \leq \overrightarrow{x_{max}} \end{pmatrix} \quad (3)$$

where $Gain$ is the gain of the LNA, G_{min} is the minimum allowed gain, and P_{max} is the maximum allowed power dissipation. The rest of the variables are defined in Section 3.1.

To solve this optimization problem, we utilize Sequential Quadratic Programming (SQP), a nonlinear programming technique that exploits the gradients of the objective and constraint functions at each iteration to accelerate convergence. SQP requires both objective and constraint functions to be either convex or concave to guarantee that the algorithm will produce the global minimum for the optimization problem. If the design space is not convex, SQP will only converge to a global minimum if the algorithm's start point lies in the convex set containing the global minimum [12]. Our computed Pareto surfaces and their favorable comparison with the Monte Carlo simulation of random designs depicted in Figure 4 and described in Section 4.4 empirically confirm that using our LNA models, we are able to successfully generate near-optimal LNAs using SQP, which has significant computational advantages over stochastic optimization techniques such as evolutionary programming.

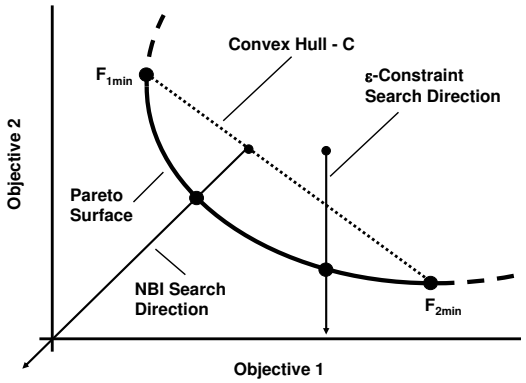

Figure 2: Search directions for NBI and ϵ-constraint methods.

3.3 Generation of Pareto Surfaces

In order to synthesize the LNA to maximize performance and meet the constraints for a particular application, we need to systematically generate the Pareto-optimal trade-off surfaces between different design metrics. In order to generate these Pareto surfaces, we utilize the Normal Boundary Intersection (NBI) method. Originally developed by Das and Dennis, the NBI method is a systematic way to generate the Pareto optimal surface between design parameters with equally spaced evaluation points [13]. In contrast, the ϵ-constraint method [15] forms the Pareto surface by solving a series of single objective optimization problems for each set of constraint values.

NBI first locates the minimum value of each design metric using the technique described in Section 3.2 in order to determine the relevant range of design parameters for Pareto optimization. For instance, if the minimum possible noise figure is 1 dB, then setting the maximum noise figure constraint to any value less than 1dB will cause the optimization algorithm to fail. In practice, we constrain each of the figures of merit to limit the Pareto surface generation to a particular region of interest. Once we know the bounds on the design parameters, we then form an $n-1$ dimensional convex hull C that is defined by the maximum allowed value of each design metric. For each Pareto optimal point required, we search the performance metric space along a vector through the origin that is approximately normal to C until we find the Pareto optimal design. Conceptually, the difference be-

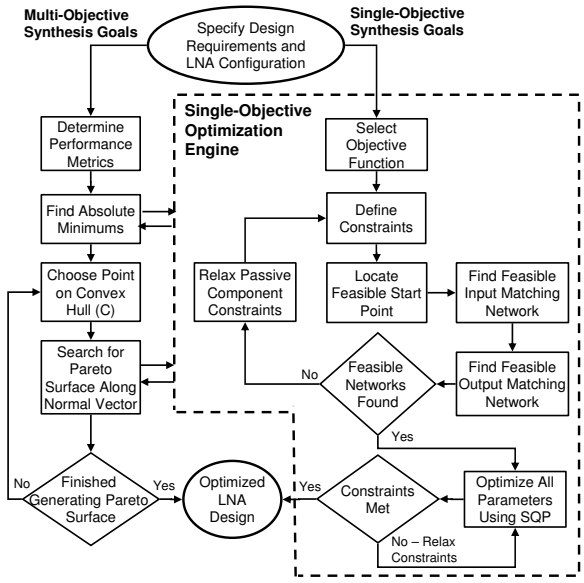

Figure 3: The SOC-NLNA methodology

tween the NBI method and the ϵ-constraint method is that if started at a feasible point, the NBI method searches for a particular Pareto optimal design along a vector through the origin that is normal to C, while the ϵ-constraint method, if started at a feasible point, searches for a Pareto optimal design along a vector that is normal to one of the fixed design constraints as depicted in Figure 2.

3.4 Overall Synthesis Methodology

SOC-NLNA solves (2) utilizing the single and multiple objective optimization techniques described in Sections 3.2 and 3.3, respectively. Figure 3 depicts our overall LNA synthesis methodology. Based on the LNA's application requirements, implementation process technology and performance objectives, we define the type of optimization, either single objective with set constraints or multiple objectives for Pareto surface generation. We also specify constraints on passive components based on the achievable quality factors and component area requirements.

If we want to generate the Pareto surfaces analyzing the trade-off between performance metrics including noise figure, gain and power consumption, we begin by using our single objective optimization engine to determine the minimum achievable value of each metric. We then calculate a set of points on the n-1 dimensional convex hull (C) using NBI. For each point on C, we search for the Pareto optimal point along a vector through the origin using the NBI method and our single objective optimization engine as depicted in Figure 2. Once we have found the specified number of Pareto optimal points, we can approximate the Pareto surface using a surrogate function as described in [15], which can then be utilized in higher-level designs.

Our single objective optimization engine is utilized either at each stage of Pareto optimization or for LNA synthesis with fixed design constraints. We start by defining the appropriate objective and constraint functions for the optimization problem. We then locate a feasible start point for the optimization problem in order to accelerate convergence. For a fixed initial transistor widths and bias voltages obtained from [4, 6], we optimize the input matching network using SQP on the following optimization problem:

$$\begin{aligned} \text{Minimize} \quad & \| \text{Re}(Z_{in}(\overrightarrow{Z_{ic}})) - \text{Re}(Z_{sin}) \\ & + \text{Im}(Z_{in}(\overrightarrow{Z_{ic}})) - \text{Im}(Z_{sin}) \|_2^2 \\ \text{Subject to} \quad & \overrightarrow{Z_{ic,min}} \leq \overrightarrow{Z_{ic}} \leq \overrightarrow{Z_{ic,max}} \end{aligned} \tag{4}$$

where Z_{in} is the input impedance of the LNA, $\overrightarrow{Z_{ic}}$ is a vector of inductor and capacitor component values for the input impedance matching network, $\overrightarrow{Z_{ic,min}}$ and $\overrightarrow{Z_{ic,max}}$ are the minimum and maximum inductor and capacitor component values for the input impedance matching network, and Z_{sin} is the input source impedance that needs to be matched. We utilize an optimization formulation similar to (4) to find a feasible start point for the output matching network. If either input or output impedance matching cannot be realized for the given $\overrightarrow{Z_{ic,min}}$ and $\overrightarrow{Z_{ic,max}}$, we relax the component value constraints based on a percentage of the inductor's maximum attainable quality factor for a given technology and attempt to find input and output matching networks that satisfy our matching requirements.

Once feasible input and output matching networks for the initial transistor parameters are obtained, we then optimize the LNA using a single objective version of the problem formulated in (1) for the specified performance objectives and constraints using SQP. If the performance constraints cannot be met, we relax the constraints and repeat the optimization process. SOC-NLNA combines SQP and NBI in order to create Pareto-optimal LNA designs with component values that can be integrated into the SoC environment while meeting noise, gain and power requirements.

4. RESULTS

4.1 LNA Design Example

To evaluate SOC-NLNA, we perform single-objective LNA optimization using the formulation described in (3) for a design with a 20mW power dissipation constraint, a minimum gain of 20dB, an operating frequency of 2.4GHz, and the output matching topology displayed in Figure 1c. During the optimization process, we enforce the following constrains on the design parameters: $W_1, W_2 \in [100, 1000]\mu m$, $V_{gs} \in (V_T, V_{dd} - V_T)$, $L_{ss} \in [0.05, 0.5]$nH, other inductors $\in [0.05, 10]$nH and capacitors $\in [0.05, 1]$pF. Our optimization methodology required 575 function evaluations and only 22.4 seconds of CPU time.

For this design example, we compare SOC-NLNA with 2 variations of the LNA design methodology presented in [4, 6]. In the first variation, we utilize the W_1, V_{gs}, L_{ss} and L_{gg} values obtained from [4, 6] and assume the other input matching network values are part of an external off-chip biasing network with large L_b and C_2 and small C_1 in order minimize their impact on the input impedance. We call this first variation the *Classic Power Constrained Noise Optimization (CPCNO)* methodology [6]. In the second variation, we utilize the only the W_1 and V_{gs} values from CPCNO and optimize the input matching network based on the formulation in (4). We call this second variation the *Matched Power Constrained Noise Optimization (MPCNO)* methodology. In both cases, we optimize the output matching network using our methodology.

	W_1 (μm)	W_2 (μm)	V_{gs} (V)	L_{ss} (nH)	L_{gg} (nH)	L_b (nH)	Inductor's Total Resistance (Ω)	Noise Figure (dB)	Gain (dB)
SOC-NLNA	458	400	0.99	0.50	0.071	1.90	2.86	0.43	19.8
CPCNO	276	400	1.11	0.29	13.23	Off Chip	18.73	0.66	18.0
MPCNO	276	1500	1.11	1.14	2.23	2.23	6.0696	0.57	12.5

Table 1: LNA designs obtained using our LNA synthesis methodology, CPCNO and MPCNO

Table 1 displays the transistor widths, bias voltage, input matching inductor values and their associated parasitic resistances. In the design example, SOC-NLNA produced an input matching network with passive component values suitable for SoC integration by optimizing the inductors and capacitors in the biasing network in addition to traditional cascode network (L_{ss} and L_{gg}). The inductor values required by the design generated using our full synthesis methodology and our input matching synthesis methodologies yield significantly smaller inductance values than the 13.2nH L_{gg} inductor value required when using the CPCNO methodology. The large valued inductors lead to significantly larger parasitic resistances, which can result in a significant increase in noise figure for the LNA.

The Cadence SpectreRF results for noise figure and gain obtained for the 3 optimization methods are depicted in Table 1. The CMOS model used is BSIM3v3 0.35μm from TSMC. For the design obtained using SOC-NLNA, our predicted noise figure of 0.42dB closely matches the result obtained from SpectreRF of 0.43dB, and our predicted gain of 21.6dB is near the value of 19.8dB collected from the SpectreRF LNA simulation. The CPCNO methodology provides poor input matching since inductor parasitic effects are not considered. This also adversely impacts the LNA's noise figure. The MPCNO methodology provides good input and output matching using our matching methodology, but lacks the low noise figure and large gain obtained by optimizing the complete LNA design.

4.2 Input Impedance Network Optimization

To illustrate SOC-NLNA's propensity to generate input matching networks that are suitable for SoC integration, we synthesized approximately 9,000 designs in different processes with varying M_1 transistor characteristics and operating frequencies, and compare the largest input matching inductor value and its associated parasitic resistance for a given design produced by (1) our synthesis methodology, (2) CPCNO, and (3) the impedance matching methodology in [7], which includes the parasitic resistances of the inductors (L_{ss} and L_{gg}). We call impedance matching methodology (3) the *Resistive Power Constrained Noise Optimization (RPCNO)* methodology. The designs we produce have process parameters from TSMC 0.35, 0.25 and 0.18μm mixed-mode processes as well as an IBM 0.13μm process. The synthesized input matching network designs are for systems with $W_1, W_2 \in [50, 1000]\mu m$, $V_{gs} \in (V_T, V_{dd} - V_T)$ and an operating frequency between 900MHz and 5GHz. We assumed a maximum integrated capacitor value of 2pF in our synthesized input impedance matching networks.

Table 2 shows the mean and maximum of the largest integrated inductor values and their associated parasitic resistance for a given design produced by our input matching synthesis methodology and the CPCNO and RPCNO methodologies. On average our design methodology produces maximum inductor values that are 10.2% and 5.8% of those produced by the CPCNO and RPCNO methodologies. Similarly, on average our design methodology produced parasitic resistance values that are 6.6% and 2.6% of those produced by the CPCNO and RPCNO methodologies. Note that for all of the 9000 designs synthesized, SOC-NLNA produced a 14.91nH maximum inductor value. In contrast, the maximum inductor values produced by the CPCNO and RPCNO methodologies were 669.1nH and 742.5nH, respectively, which are significantly larger than the inductance values that can be realized on-chip.

4.3 Output Impedance Network Optimization

The complex output matching network configuration also provides the flexibility to realize reasonable passive component values in the output matching network. We synthesized 9,000 designs using the methods described in the previous section to evaluate the simple and complex output impedance matching network topologies depicted in Figures 1b and 1c, respectively. Variations of the simple output impedance network are typically used in many LNA designs [4, 5]. Table 3 shows the mean and maximum of the largest integrated inductor value and its associated parasitic resistance for a given design produced by our synthesis methodology for the simple and complex output matching topology. The additional degrees of design freedom provided by the extra elements in the complex impedance matching network allow SOC-NLNA to produce inductors that are suitable for SoC integration, while the simple impedance matching network can produce values as high as 24.38nH.

4.4 Pareto Optimization

In order to locate LNA designs that provide the appropriate design constraints that maximize critical performance metrics for a particular application, the generation of Pareto-optimal trade-off surfaces is crucial. Using SOC-NLNA, we generated the Pareto surface comparing noise figure versus power dissipation with a fixed gain constraint of 20dB, which is depicted in Figure 4. In order to validate SOC-NLNA, we simulated performed a Monte Carlo simulation of 10,000 LNA designs with random W_1, W_2 and V_{gs} values and input and output impedance networks matched using the formulation in (4). The noise figure and power dissipation performance combinations of all of the randomly simulated designs are dominated by the calculated Pareto surface, which demonstrates that our methodology is closely approximating the Pareto surface and that the LNA optimization problem is well-suited for nonlinear constrained convex optimization. Figure 4 also depicts the impact of technology scaling on the Pareto surface. Beyond 0.18 micron technology, transistor scaling produces diminishing returns as the decrease in

	SOC-NLNA	CPCNO	RPCNO
Mean L_{max}	2.55	24.94	43.94
Max L_{max}	14.91	669.1	742.5
Mean R_{max}	2.18	32.69	82.37
Max R_{max}	11.19	498.6	901.0

Table 2: Mean and maximum of the largest input matching network inductor value and its associated parasitic resistance for a given design

	Simple Output Network	Our Complex Output Network
Mean L_{max}	6.18	2.63
Max L_{max}	24.38	12.72
Mean R_{max}	5.90	2.30
Max R_{max}	14.97	6.96

Table 3: Mean and maximum of the largest output matching network inductor value and its associated parasitic resistance for a given design

transistor length begins to increase short channel transistor effects. On average, it took 2,563 function evaluations and 152.7 seconds to produce 11 points on the Pareto optimal surface for each of the 4 technologies.

5. CONCLUSION

In this paper we present SOC-NLNA, a systematic synthesis methodology for fully integrated narrow-band CMOS LNAs in high performance SoC designs based on deterministic single-objective optimization using SQP and multi-objective optimization using NBI. SOC-NLNA yields inductor values that are more than one order of magnitude less than those obtained from existing techniques, which will enable the full SoC integration of the LNA. When the synthesized LNAs are simulated using Cadence SpectreRF, SOC-NLNA yields up to 35 and 58 percent improvement in noise figure and gain, respectively. Given the increasing demand for wireless systems in SoC technology, SOC-NLNA will enable the rapid realization of fully integrated narrow-band CMOS LNAs that meet power and performance requirements.

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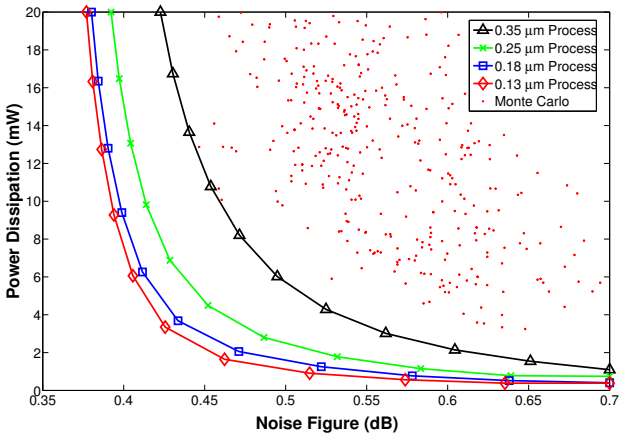

Figure 4: Pareto surface depicting the trade-off between noise figure and power dissipation

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