An Effective DFM Strategy Requires Accurate Process and IP Pre-Characterization

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1. INTRODUCTION

The design methodology called Design for Manufacturing (DFM) includes a set of techniques to modify the design of ICs in order to make them more manufacturable, i.e. to improve their functional yield, parametric yield, or reliability. Traditionally DFM in the pre-nanometer era consisted of different methodologies aimed at relaxing the mask layout shapes of an IC at the full chip level in order to minimize its failure probability, for example, increasing the feature spacing and width, and adding redundant contacts and vias where possible.

In a broader sense we may consider Design Rules (DR) as the first and most fundamental form of DFM; in fact DRs define the space of design variables that should guarantee product manufacturability. In this sense, DRs are in fact a method of "proactive DFM" as opposed to the methods described before that look at opportunistic design modifications at the end of the design process only and that we define as "reactive DFM".

Obviously, proactive DFM has a huge advantage with respect to reactive methods, because it should guarantee that the resulting design is manufacturable by construction and by being embedded in the standard design flow, it also allows to optimize circuit speed, power and area concurrently with yield, hence without requiring additional steps of verification and closure loops.

With the advent of nanometer technologies, namely at 130nm and below, process and design systematic yield loss mechanisms have started to cross over random effects in the yield pareto.

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Random yield loss mechanisms (YLM) are caused by random contaminants or defects (e.g. particles) and are therefore characterized by the absence of strong spatial, temporal or any other kind of correlation. On the contrary, process systematic YLM are usually spatially correlated (e.g. their failure rate shows strong radial wafer patterns) or temporally correlated (e.g. lot to lot variation as a function of equipment). Design systematic YLM are strongly correlated to specific local physical layout patterns, and therefore their failure rate may vary by orders of magnitude as a function of the layout characteristics.

The same physical design feature (e.g. a contact or a via) may yield completely differently depending upon neighboring features (short correlation distance effects) such as the presence or lack of certain shapes next to it, in example the presence of a minimum distance, small area, metal island and via next to it. Other types of design systematic YLM are characterized by medium or even relatively big correlation distances, for example, YLM due to CMP effects. Any design systematic YLM is however characterized by an intra-chip correlation pattern. In other words, they depend on local physical design properties.

This design locality property of design systematic YLM considerably complicates the effectiveness of traditional DR approach because DR are applied globally to every physical design feature in a chip.

In order to cope with the design locality property of design systematic YLM, DRs have proliferated in number and became increasingly complex. Because of this the DRs for sub-nanometer technologies have been split into two sets; a fundamental set of DRs, i.e. rules that, if violated, would cause a products yield to drop to zero; and a set of "Recommended DR" (RDR), i.e. rules that the design tools should try to implement as much as possible based upon design locality. Unfortunately, it would be basically impossible or extremely impractical to include every such complex DR in the design tools to generate maximally manufacturable designs by construction.

For this reason, a large number of rule-driven reactive DFM methodologies have been introduced recently, which have the drawback of modifying the design patterns after timing closure and verification have completed, hence introducing additional risk and delay in the design process.

Moreover, most of the RDRs create some contention between conflicting rules, for example, adding via redundancy which may create a large number of small dielectric regions that are difficult to manufacture and may cause systematic failures.

We claim that the only way to break this tail-spin involution is to radically change the approach from a rule-based reactive to a model-based proactive DFM.

Model-based, proactive DFM philosophy consists in the development of accurate, silicon verified YLM models that can evaluate the relative impact of each YLM and assess trade-offs. These models are then integrated in the design tool's cost function along with other design objectives such as speed, power and signal integrity functions. Design tools are thus able to exploit the design locality property of design systematic YLM as well as global random YLM to achieve the optimal manufacturability compatible with the actual IC design specifications.

2. YIELD LOSS MECHANISMS AND THEIR CHARACTERIZATION

2.1 Random Yield Loss mechanisms

Random defects and contaminants are among the most well-known and deeply studied yield loss mechanisms. They cause electrical feature shorts and opens such as, for example: active, poly and metal shorts and opens due to particle defects, contact and via opens due to formation defectivity. Test structures to characterize random defects have been described in the past, such as the examples in [1] and [2]. The real challenge is to be able to collect enough statistical raw data to achieve a resolution lower than 0.1 ppb which is required to measure defect fail rates that are currently < 1ppb.

2.2 Design Systematic Yield Loss Mechanisms

IC layout has a very strong influence on transistor performance and circuit functionality, such as those due to stress effects on carrier mobility or due to printability effects. Accurate characterization of these effects and their impact on IC yield is crucial for DFM. Some of the most significant systematic effects that cause functional yield loss include: via/via stack failure as a function of interconnect length, poly-metal bridging, metal shorts/opens as a function of width vs. spacing, misalignment and line-end shortening. Characterization of such effects in silicon requires specialized structures and a proper Design Of Experiments around the layout variables, as for example it is shown in [3].

2.3 Parametric yield loss mechanisms

The electrical performances of IC devices are subject to natural random variation. Because of this, every IC performance parameter can be described as a random variable with a specific associated probability distribution. The tails of the probability distribution may fall outside the acceptable device specs and cause parametric yield loss. Parametric yield loss is characterized by inter-die and intra-die level correlation, with the latter also known as device mismatch. Characterization of this type of yield loss requires specific test structures, test methodologies and statistical circuit simulation techniques, such as those described in [4],[5].

3. YIELD-AWARE DESIGN FLOW

Accurate YLM modeling can be used to pre-characterize the design dependent yield loss susceptibility of every IC component, such as standard cells, SRAM arrays and analog IP. These pre-characterized models can then be combined with process characterization information from dedicated test chips in order to obtain the yield cost information for each component that is finally stored in the design database. This component-level yield cost information can be used by design tools in the design flow to enable them as "yield-aware"[6]. For example, standard cell yield cost can be used at the logic synthesis and physical placement level to optimize logic IC blocks layout for yield concurrently with speed, power and area. Other design tools can be made yield–aware, thus achieving significant yield benefits, such as those used for chip floorplanning, routing, and memory generation.

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