Practical Aspects of Reliability Analysis for IC Designs

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ABSTRACT

Voltage analysis is a major part of design-in reliability as voltage is the driver for electric degradation in dielectrics and MOS devices. Particularly, voltage has the largest influence on gate oxide reliability. An important trend designers should be aware of is the planned shift to new gate oxide failure criteria, which will tolerate progressive soft breakdowns in the gate oxide introducing additional gate leakage and noise. With increasing electric oxide fields negative bias instability of pFET devices became a severe problem, which cannot be solved by technology alone but requires also design solutions. Thus, simulation of MOSFETs being degraded by hot carrier stress and negative bias temperature stress becomes mandatory, as well as the control of device properties of circuit elements in a design. Design-in reliability in the metallization levels mainly is related to via placing and therefore, design tools should be able to trade off between increase in size, e.g. due to redundant vias, and benefit in reliability. Analysis of metal lines with maximum potential difference and minimal spacing also becomes mandatory in order to calculate the risk of time-dependent dielectric breakdown in the inter-metal dielectric, particularly for low-k dielectrics. From ESD point of view the following demands exist for future EDA solutions: 1) verification of net oriented ESD rules, 2) IR-drop analysis on layout to check ESD metallization rules, and 3) automatic placement of ESD or I/O cells depending on some formalized ESD guide lines that codify the ESD protection concept.

Categories and Subject Descriptors

B.8.0 [**Performance and Reliability**]: General

General Terms

Reliability

Key Words

Design-in reliability, gate oxide integrity, hot carrier stress, NBTI, electromigration, stress-induced voiding, TDDB of inter-metal dielectric, ESD

1. INTRODUCTION

The reliability of circuit operation for a decade of years or more depends on the degradation mechanisms of the technology and on the robust design of the circuits. Design-in reliability stands for design methods to either reduce the degrading effects on device level and on metallization level, or to implement design techniques to tolerate a reasonable amount of degradation. In this work practical aspects of the following reliability relevant topics during operation of a circuit are addressed: isolating property of gate oxides in MOSFETs, stability of MOSFET device parameters, conducting property of the metallization, isolation property of the inter-metal dielectric, and electro-static discharge (ESD). In semiconductor reliability physics the key mechanisms are known as gate oxide integrity (GDI), hot carrier stress (HCS), negative bias temperature instability (NBTI) of PFET devices, electromigration (EM), stress-induced voiding (SIV), and breakdown of the inter-metal dielectric.

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2. GATE OXIDE INTEGRITY

Any electric stress reduces the life time of gate oxides and all electric stresses applied to a certain gate oxide area are cumulative in time, which means each stress consumes life time. The amount of life time being consumed by a certain electric stress increases with increasing voltage drop across the oxide, increasing temperature, and increasing active gate oxide area. Among these factors the voltage has the largest influence.

2.1. Voltage overshoots

The qualification of gate oxide (GOX) integrity for e.g. 10 years of operation usually is based on a certain operation voltage of the technology plus a voltage tolerance of up to 10%. However, voltage overshoot events, e.g. during switching, are not covered and need to be considered as additional electric stress. These are voltage overshoots between gate and any other terminal of the transistor, in the on or the off stage of the transistor. The following circuit relevant parameters need to be known to calculate the additionally consumed life time: potential difference, involved terminals (e.g. gate and drain), duration or duty cycle of the overshoot event, active GOX area and type of the affected device (e.g. NFET). For example a 1.5 nm-GOX may be qualified for 10 years of safe operation at a voltage of 1.20 V plus 10% voltage tolerance, which is 1.32 V. Let's assume 0.01% of the total active GOX area is affected by a 1.8 V-overshoot event with a duty cycle of 1% of the total operation time. In such a case the cumulative probability for GOX failure increases from 50 ppm to about 80 ppm after 10 years.

2.2. New definition of gate oxide failure criteria

State of the art gate oxide (GOX) reliability evaluation considers the first irreversible increase in gate leakage current as oxide failure criterion, regardless of the first increasing step being small (soft breakdown) or large (hard breakdown). This is the traditional definition of GOX breakdown and the further increase of leakage current through this localized breakdown path in the GOX hasn't been of interest. However, with decreasing GOX thickness below about 1.3 nm the time range of further leakage current increase becomes significantly large compared to the time to formation of

the breakdown path itself. This progressive wear-out of ultra-thin gate oxides [10, 16, 20] gained interest as traditional definition of GOX failure criterion cannot guarantee 10 years of save operation anymore for several square millimeters of active GOX area. Future GOX reliability assessment will have to shift to this new GOX failure criterion, which tolerates all soft breakdown (SBD) paths not exceeding a certain leakage level. It likely will be applied to SiO_2-based gate oxides below about 1.3 nm and also to high-k gate dielectrics.

In the following circuit simulation results of a NOR gate are shown with a voltage-controlled current source between gate and source as well as between gate and drain in each FET. Its characteristic was described by a power law dependence on gate voltage, which simulates a typical soft breakdown (SBD) path [15]. Such a SBD path is not an ohmic leakage path. Two different pairs of parameters (current at 1 V and exponent) were used for simulation: 5E-6 A/3.0 (high level SBD path), and 3.4E-7 A/5.5 (low level SBD path). The technology input parameters, like gate length or threshold voltage, and the number of leakage paths were varied by using a Monte Carlo simulation of 5000 runs. Figure 1 shows the cumulative distribution of rise and fall times of the output signal as well as the delay between two selected transitions of the output level. For each case three distributions are plotted, which belong to simulations using high level SBD paths, low level SBD paths, and without any SBD path in the NOR gate. The statistical distribution of rise times and delays show significant shifts in the case of high level SBD paths. Worth noting, at the extreme edges of the cumulative distribution the effect of extreme deltas in the technology parameters overlap with the effect of minimum or maximum numbers of SBD paths activated in the NOR gate. Maximum number is eight, which is a worst case study, because realistic is a single SBD path.

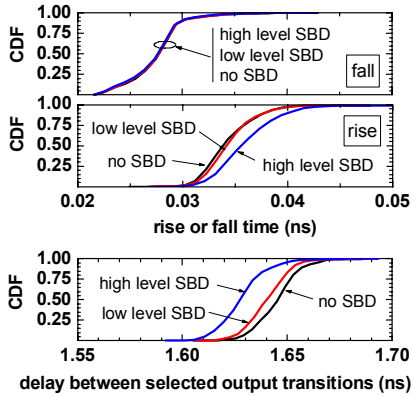

Figure 1. Example of cumulative distributions of fall time, rise time, and delay between two selected transitions in the output signal of a NOR gate. Monte Carlo simulations for three cases were performed: low and high level SBD path (specifications are given in the text), and no SBD path at all.

Whereas the new GOX failure criterion seems to be applicable to digital logic, analog logic may have problems to tolerated similar gate leakage levels. Furthermore, the leakage current after formation of a SBD path not only increases during the progressive phase but also shows noise [21]. This additional source of noise may also be a problem for analog circuits to tolerate a SBD path in the gate oxide. However, many analog circuit elements will be operated at low voltages and will not be affected by GOX soft breakdown within any reasonable life time.

2.3. Design-in reliability for gate oxide integrity

As the voltage drop across the gate oxide (GOX) is the key driver for time-dependent dielectric breakdown (TDDB) and GOX wear-out, design-in reliability requires transient analysis of the node potentials from gate integrity point of view. It is strongly recommended to identify overshoot events of the voltage drop across the GOX between any terminal and the gate. Design solutions for power-down techniques are beneficial for GOX reliability, because the duty cycle of electric stress is reduced.

The new definition of GOX failure criterion will tolerate gate leakage levels well above the direct tunneling current of the fresh GOX as well as an additional source of noise caused by such a progressive soft breakdown spot in the GOX. The following features would be required in circuit simulators in order to test the robustness of circuit elements, particularly analog designs, against such a SBD path: 1) voltage analysis for identifying the spots, where SBD most likely will occur, 2) adding of a GOX leakage path with a power law dependence on the potential drop across the GOX, and 3) adding a source of noise due to this gate leakage path.

In addition to the discussed aspects during operation of a circuit any electric stress due to plasma processes during fabrication will consume life time of the GOX or cause drifts in the MOSFET parameters. Circuit design can prevent or enhance such plasma-induced damage (PID). PID is not only related to circuit design but also to technology processing, and therefore, is beyond the scope of this paper. In 2005 and 2006 tutorials on PID were held at the International Reliability Physics Symposium (IRPS), which included aspects of circuit design and discussed different regimes of oxide thickness down to ultra-thin gate oxides of modern CMOS technology generations [4, 6].

3. DEVICE RELIABILITY

3.1. Comparison between HCS and NBTI with respect to circuit relevance

Since the Hot Carrier Stress phenomenon was the first limiting factor of scaling in the history of CMOS-technology development, HCS is the most explored damage mechanism of device reliability. Nowadays the physics are relatively well understood, and both the technology development engineers and designers can optimize the devices and circuits respectively [7, 11, 26]. Although there is a relief of HCS reliability challenges in the last years because of lower operation voltages and short HCS critical device operation based on duty factors, technology development and circuit designers still have to consider HCS for MOS transistor engineering and circuit design [24, 25].

NBTI became a more and more severe problem and is nowadays the most critical device reliability limiting factor [3, 9, 19, 22]. Since the electric field across the gate oxide is one of the critical stress parameters, the gate oxide scaling without proportional downscaling of the operation voltage leads to a clear aggravation of NBTI by technology development. Figure 2 shows a diagram plotting the electric oxide field of standard pMOS devices in inversion under normal operation condition for different technology nodes. The open hexagons for future technologies represent the ITRS prediction for the electric gate oxide field [8]. For standard logic devices of modern technologies more than 5.5MV/cm is

applied across the gate oxide and with the upcoming shift to metal gates this value will increase further. Elevated operation temperatures and possible stress times close to 100% of the product life times challenge the NBTI problem [24, 25].

Therefore, both HCS and NBTI are relevant effects for device degradation and correspondingly for circuit reliability. Nowadays circuit reliability is not only the task of technology development! Circuit designers have to take into account also reliability issues like NBTI and HCS for competitive products. Especially in modern designs with low power techniques stress induced parameter degradation can lead to timing conflicts (digital applications) or mismatch (analog applications) within the product [5, 23-25, 27]. For this work the designers have to be supported by smart software tools with built-in reliability know how.

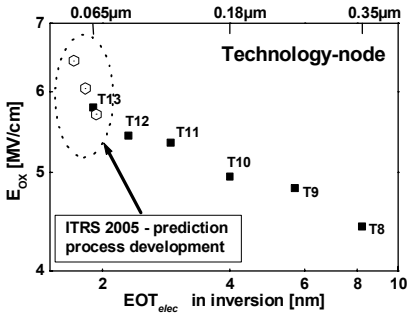

Figure 2. Electric gate oxide field during normal operation of standard logic transistors of different technology nodes (T6-T13). The open hexagons mark the ITRS prediction for future technologies. The degradation due to NBTI becomes more critical due to the increasing electric field.

3.2. Comparison of digital and analog design

The circuit-design for digital applications fundamentally differs from the design of analog or RF-circuits. The transistors are used in different operation points. Therefore, the stress conditions and even the reliability requirements of the electric device parameters vary a lot for analog and digital design [5, 23, 27]. Besides the different requirements on electric device parameters, on stress operation points, and on reliability, another significant divergence has to be pointed out: The need for completely different approaches to simulate the reliability of digital and analog or RF-circuits.

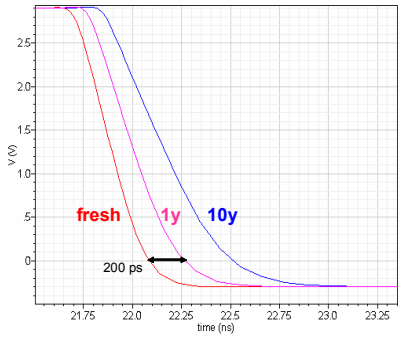

Figure 3. Simulation of an output signal of a driver circuit with the help of a circuit simulator with consideration of stress-induced device parameter degradation. The diagram shows the output signal before and after 1 year and 10 years of continuous normal operation.

Critical analog circuits typically have a relatively low number of transistors. Therefore, it is possible to simulate complete circuit blocks and afterwards to assess each device characteristic. Even in Mixed Signal Applications the analog part of the circuits is relatively small, so full-custom approaches can be used. For full-custom design smart circuit simulators with built-in reliability functionality are available and useful (e.g. [2]). For example Figure 3 shows simulation results of a driver circuit before and after a given operation time. Based on degradation-models and with the help of adequate input patterns the simulator can calculate device parameter degradations for each transistor within the circuit and then simulate the circuit with degraded devices. Subsequently the designer can optimize the circuit design according to the given reliability requirements.

For digital and semi-custom designs a more automated design approach is used. It is mainly based on a limited number of library elements that are placed automatically by the design tool. This directly implicates a further problem regarding reliability simulation: Since the designer does not know in advance where exactly a single library element is going to be placed, it is almost impossible to determine the exact operational pattern for a certain library element in general. Therefore, in a semi-custom design, a completely different approach is needed to consider reliability within the design. A possible way to take the stress-induced parameter degradation into account is for example the calculation as a part of on-chip process variations (OCV). For this purpose stress-induced parameter variations can be transformed in propagation-delays. It's helpful in modern technologies that stress-induced parameter degradation is always one way only. Independently of the occurred damage mechanisms the device becomes slower (lower $|ID_{Sat}|$, higher $|V_{TH}|$) corresponding to increasing propagation-delays. With smart software tools time paths within the chip can be checked and if necessary, due to timing conflicts, gates can be replaced by faster ones, with the disadvantage of higher area demands and larger power consumption.

The huge numbers of transistors in modern semiconductor products makes it rather difficult to simulate the complete chip e.g. a base-band or a DRAM product, especially with respect to reliability. Even if a smart simulator with the capability of millions of transistors is available, it is not manageable to consider all possible input patterns to simulate the different operation conditions of the product. Therefore, in order to identify the most critical operation patterns for a product the interaction between the designers and the customer will become more and more essential.

3.3. Future task in terms for DIR in EDA tools

In order to get valuable simulation results for circuits after a given operation time, the software tools need different inputs. First of all there is the need of a deep understanding of the occurring damage mechanisms of the transistors and their dependencies of different stress conditions. The corresponding degradation model is needed to calculate the change in electric behavior and therefore, simulate the circuit function after degradation. The second important input is the determination of realistic, product relevant patterns to stimulate the simulated circuits. Due to unequal use times and operation points of each device within a circuit, the degradation levels of all devices are different. Without this information the entire simulation of the degraded circuit becomes faulty and worthless. To improve (the generation of) these input patterns is one of the big challenges in simulation work.

In the semi-custom design world one requires a smart balancing between propagation delays, area demands and power consumption. Only if a simulator tool can achieve these demands and considers the mentioned restrictions, the software can help to design suitable reliable products. Otherwise the tools will lead to over engineered technologies and noncompetitive products.

4. INTERCONNECT RELIABILITY

4.1. Critical interconnect structures

In the past, the ITRS roadmap [8] has been described the total length of interconnect structures as a typical parameter for different technology generations. For newer technologies – especially for metal stacks containing copper dual damascene metallization – it turned out that the via-line transitions are the most critical sites for failures in the BEOL [29]. Therefore, the number of critical vias in a product is a much more decisive figure to describe the risk of interconnect failure than the total metal length. The careful and optimal design of vias and their surrounding is the key factor to obtain more reliable products. The use of design-in reliability in BEOL often leads to a loss of chip area. A compromise has to be made for an optimization of reliability as well as area, performance, power and yield. Moreover, the interaction of design measures with BEOL manufacturability has to be taken into account, but is beyond the scope of this paper.

The most important failure mechanisms in BEOL reliability are electromigration (EM), stress-induced voiding (SIV), and time-dependent dielectric breakdown (TDDB) of the inter-metal dielectric. For each of these failure mechanisms, it has to be defined, which kind of structures are the critical ones, i.e. which are most prone to failure during life time.

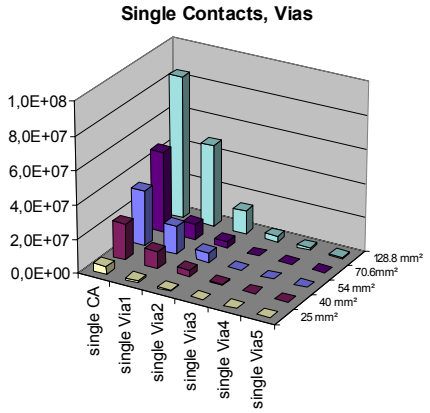

Figure 4. Number of critical vias for different metal levels as a function of the product area.

The crucial parameters, which have to be considered when designing a circuit and performing the metal routing, are the total number of vias connecting two metal levels, the geometry of the connected metal lines like line length and width and the overlap of the metal line around the via. For electromigration an additional criterion besides the geometry is the electrical function. The overall BEOL reliability depends on the duty cycle of current flow, the direction of the current (up-stream versus down-stream) and the type of operation (DC, DC-pulse or AC). For non-DC currents the thermal heating of the metal line and the vias is the limiting factor for the maximum currents [17].

4.2. Electromigration

Electromigration is a material transport induced by high current density in the metal line. It is determined by a current- and temperature-driven metal-ion diffusion process. For aluminum it is dominated by grain boundary diffusion and for copper it is controlled by interface diffusion. Avoiding single vias which have to carry high DC current is the most important measure for improving electromigation reliability. Adding a redundant via helps to lower the current load per via and to improve the EM life time [14]. The expense to eliminate single vias or contacts in designs depends on their frequency of occurrence in certain metal levels. A layout analysis was performed to identify single vias in typical logic products for a 130nm-technology (Figure 4). This analysis shows that the problem of single vias increases on larger products. The total chip size often is limited by the sum of the size of its library elements. Therefore, these elements are usually very small and a lot of single contacts are use due to the lack of space for redundant contacts.

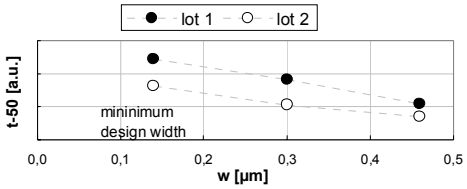

Figure 5. EM life time as function of line width for a via down-stream structure (two different lots) tested with the same current density in the line.

In modern copper technologies the limiting item for the maximal current density, which can be allowed in metal circuits, are vias contacting wide metal lines beneath. The EM life time decreases with increasing metal width (Figure 5). Therefore, especially single vias in connection with wide metal lines have to be avoided. As demonstrated in [12] placing the via at the border of the lines is beneficial due to the surrounding via liner being connected to the liner of the metal line below. This leads to a liner redundancy effect, which prolongs the life time of the via and also explains the higher life times of narrow metal lines.

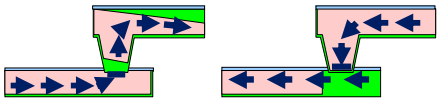

Figure 6. Schematic figures of up-stream and down-stream EM failure.

If the current flow is directed from an upper metal level through a via into the lower metal level (down-stream), this is more critical than the other way round (up-stream). In the down-stream case the diffusion barrier in the bottom of the via is in direct neighborhood to the preferred diffusion path at the metal-to-barrier interface (Figure 6). Therefore, in a design the up-stream direction can carry higher current densities than down-stream. In order to improve the down-stream EM reliability an additional end-cap can be set at the end of the metal line to provide a metal reservoir [14].

4.3. Stress-induced voiding

Stress-induced voiding (SIV) is caused by mechanical stress gradients due to different coefficients of thermal expansion of the

different materials in a metal stack. Vacancy diffusion leads to void growth. Therefore, large metal plate structures are very sensitive to SIV due to their large vacancy reservoir, which can lead to very early fails by voiding. The voiding preferentially occurs below the vias due to the mechanical stress gradients being formed below vias [13, 18]. In the case of SIV redundant vias help to avoid this problem by a) reducing the stress in the metal and by b) providing a redundant current path in the circuit. Since the metal plate serves as a vacancy reservoir the SIV-life time decreases with increasing plate size [18]. The designer may circumvent the rule to place redundant vias on large plates by using a "nose" for connecting via and plate (see inset of Figure 7). For such designs a dependency of SIV-life time on the nose length was observed (Figure 7). The longer the nose (diffusion path of the vacancies towards the via) the better the life time of SIV is. A similar design, in which the plate is replaced by parallel minimal metal lines, is also a critical one for SIV. This structure is more sensitive to grain boundaries as sources for vacancies. Overall, the connected metal volume to the via is the decisive parameter for SIV, which EDA tools should be capable to analyze.

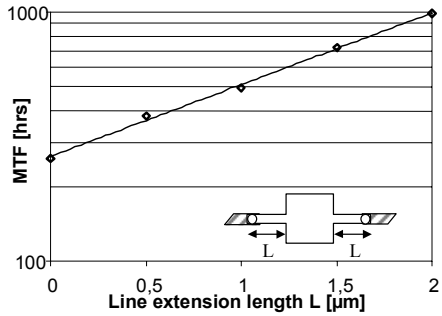

Figure 7. SIV-life time increases with nose length [28]

4.4. Breakdown of inter-metal dielectric

The time-dependent dielectric breakdown (TDDB) of the inter-metal dielectric is becoming more and more important by introducing low-k materials into the BEOL. It is determined by the maximal potential difference between immediately neighbored metal lines, which have minimum spacing between them. Due to the statistical nature of TDDB the total length of such lines within the product and the duty cycle of the full potential difference between theses lines during product life need to be known. Analysis of these two parameters in an EDA tool would enable life time extrapolation from experiment to product.

5. ELECTROSTATIC DISCHARGE

Electrostatic discharge (ESD) effects represent a major threat to IC functionality and therefore, measures on package or chip level have to be taken to prevent any damage [1, 30]. In the following, the focus will be on chip level aspects of ESD and related design issues.

ESD events can occur in a variety of situations, the most prominent examples are touching of a chip or package by a charged human being (described by the so called Human Body Model, HBM) or the discharge of a chip that has been pre-charged during processing or handling via one of its pins (described by the Charged Device Model, CDM). During an HBM ESD event, a current of up to several amps is forced into the IC. Within the model, the human body is idealized by an inner resistance of 1500 Ω, so a human being charged to 2000 V leads to a current around 1.3 A. 2000 V is a usual voltage level chips have to withstand during HBM ESD tests. An HBM pulse lasts for about 150 ns. CDM events are much faster; they last for approx. 1-2 ns. A typical voltage level specified for CDM tests is 500 V. Without appropriate protection concepts, ESD pulses can damage both diffusions and gate oxides of an IC. ESD defects in diffusions result from local melting of the silicon crystal structure usually leading to small polycrystalline regions and increased leakage currents e.g. in I/O circuitry. Gate oxides also show higher leakage after too high ESD stress and they suffer from gate oxide breakdown analogous to DC breakdown.

5.1. ESD-related issues in design

Usually, during the design and layout of an IC a variety of ESD related rules have to be followed by the designer. These rules can range from the recommended usage of special pad cells from I/O libraries and their placement on a power rail around the chip to very detailed layout design rules for single ESD endangered MOS devices. Thus, there are rules applying to the electrical net of the IC as well as rules applying to the concrete physical layout. Like with standard design tools, it is highly desirable to have verification methods available to check for ESD rule violations. In the following, some examples of ESD verification developed and used at Infineon will be discussed.

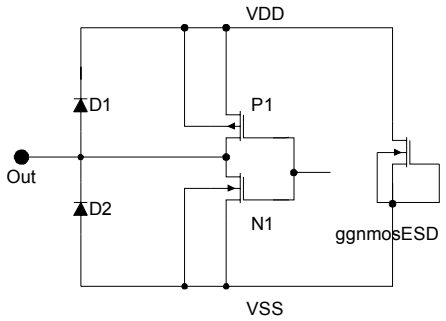

Figure 8. A standard ESD output protection concept with diodes and a power clamp.

In Figure 8, a standard ESD concept for output protection based on diodes and a power clamping device (a grounded gate NMOS, ggNMOS) is shown. Yet a simple concept, there are quite some rules to be followed:

1. There must be special diodes *D1*, *D2* connected correctly to the output pad.
2. The clamp *ggnmosESD* must be connected to VDD and VSS.
3. The output drivers *N1*, *P1* must follow some ESD layout rules (also holds for *D1*, *D2, and ggnmosESD*).
4. The output drivers *N1*, *P1* must match to the supply voltage at VDD (e.g. core devices are usually not allowed at I/O supply voltage).

Rules 1, 2, and 4 are clearly net-oriented whereas rule 3 is a candidate for an ESD design rule check (ESD DRC). An ESD DRC can be implemented in a straightforward manner with existing DRC tools (e.g. Assura, Calibre, etc.). ESD protection devices (like *D1*, *D2* and *ggnmosESD*) and active devices that require special ESD layout (like *N1*, *P1*) can be detected by introducing ESD marking

layers and then be checked for ESD rule violation like for any other design rule. An important example is the fixed drain-contact-to-gate spacing for silicide-blocked drivers *N1*, *P1*. Still, if the marking layers are not in place, no ESD rules will be tested; the mere existence of protection elements can only be checked by verifying the netlist of an IC.

Such a verification of net-oriented ESD rules can either be done on a pre-layout netlist or on an extracted netlist after layout. The latter alternative has some advantages for ESD verification, e.g. rules for CMOS inverter ratios can only be tested on the final layout with transistor fingers (see below).

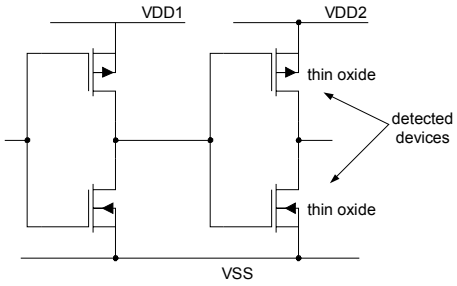

Figure 9. Thin oxide devices at two different power nets might be damaged during an ESD event.

A special in-house tool for hierarchical electrical rule checking is used to check rules like rules 1, 2, 4 mentioned in the example. It operates on Spice netlists and can handle whole IC. Such a netlist is extracted from the layout with an LVS-like runset that can take ESD marking layers and texts into account to extract special ESD devices, e.g. the *ggnmosESD* or the diodes in Figure 8. Thus, one can test for the existence and the connectivity of these devices (rules 1, 2). The ESD verification runset needs to know about the type of a pin of the top level sub-circuit in the netlist, i.e. is the pin a power supply (e.g. 1.5 V or 2.5 V), a ground pin, or an I/O pin. To insure the presence of the correct pin names, one can either use a special naming convention for the pin labels in the layout or apply a mapping on the layout pin labels based e.g. on I/O-cell names (e.g. a VDD pin in a 2.5 V supply cell is renamed to "VDD_2V5"). The pin types on top level of the netlist are then propagated through the net, such that the ESD rules - depending on the pin type - can be checked. In this way, one can find e.g. 1.5 V devices at a 2.5 V supply deep in the net hierarchy (rule 3 above) or prove the existence of a power clamp between specific VDD/VSS nets (rule 2). Thin oxide buffer capacities, which are often forbidden between VDD and VSS, can also be tested along these lines.

An important ESD topic also covered by ESD verification is internal interfaces between different power domains. For example a gate receiving signals from a voltage domain different from the one at drain or source might suffer from ESD damage and can be detected by net verification (see Figure 9). Another issue are neighbouring N-wells on different supply voltages forming a parasitic npn-transistor via the substrate. They can be identified on layout level. If the N-well/N-well distance is too small, ESD problems might arise and an ESD error is issued.

5.2. Future ESD awareness of EDA tools

The focus in the previous section was on verification of ESD reliability topics in design. To a great amount ESD DRC issues can be covered by standard DRC verification tools. On the other hand, net oriented ESD rules cannot be verified by present EDA tools, usually in-house tools have been developed for this task. It's demanded to have an EDA tool generally available that can solve tasks like those described in the previous chapter and that can handle the data of complete ICs. Beyond this, such a tool should be imbedded in the whole design flow, it would need an infrastructure for defining ESD pin types, ESD power domains and ESD endangered interfaces between such domains on some abstract level. This would even allow for early ESD net checks (where applicable) before layout synthesis.

Another topic to be addressed by future ESD-aware EDA tools is IR-drop analysis on layout to check ESD metallization rules. In modern CMOS technologies with operating voltages in the 1 V-regime, the ESD design window between the maximum operating voltage and the breakdown voltage of the thinnest gate oxide can get rather small, such that a good handling of parasitic metal resistances will become a major issue for ESD protection concepts.

A certainly more demanding topic would be automatic placement of ESD or I/O cells depending on some formalized ESD guide lines that codify the ESD protection concept. This would take the burden from standard ESD designers to learn detailed and tedious ESD rules. But maybe this is a topic for EDA tools in a farther future.

6. REFERENCES

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