Computation of Accurate Interconnect Process Parameter Values for Performance Corners under Process Variations

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Abstract
This paper introduces a fast analytical model for determining accurate parasitic values for best- and worst-case delays of a stage under interconnect process variations. The inputs to the model are the nominal values for each interconnect and device parameter and the amount of variation in each interconnect parameter. The outputs of the model are the interconnect parameter dimensions within the range of process variation that yield the best- and worst-case delay of a stage. Simulations show that our model accurately predicts the performance corners of a stage while those predicted by traditional best/worst-case analysis methodologies can have an error of up to 28.42%.

Categories and Subject Descriptors
B.8.2 [Hardware]: Performance Analysis and Design Aids

General Terms: Performance, Verification, Reliability

Keywords: Corners, STA, Delay, Variations, Interconnect

1. Introduction

The continued scaling of the minimum feature size of contemporary chips makes devices and interconnects increasingly susceptible to process variations introduced during manufacturing processes [1]-[3]. It has been shown, for instance, that process variations can cause up to 2000% variation in leakage current and 30% variation in frequency of a chip fabricated in 180nm CMOS technology [4]. Thus, without properly addressing and predicting variations in devices and interconnects, the yield of chips can drop to unacceptably low levels due to timing violations or increased power consumption.

In the past, designers were primarily concerned with device variations. However, as the minimum feature size is further decreased, variations in the interconnect begin to play an important role in delay variations of a chip [6]. This behavior is caused by interconnect parameters which can vary by more than 30% from their nominal values. In recent years, accurate model order reduction and statistical timing analysis techniques have been developed to predict the impact of process variations on interconnects, a stage and/or a die [7]-[10]; but, no fast best/worst-case methodology has been developed that can accurately determine interconnect performance corners. Hence, this paper focuses on a new interconnect performance corner analysis methodology that can be used in conjunction with previously developed device best/worst-case delay techniques.

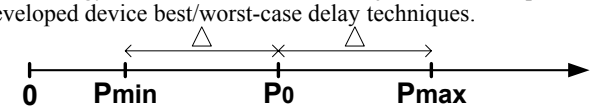

Figure 1: Process Parameter Variation Model

Process corner analysis (PRCA), also known as worst-case corner analysis, was one of the first methodologies employed to account for the impact of variations on the delay of a transistor [11]. PRCA was later adopted to also handle interconnect process variations which is the focus in this paper. PRCA takes as its input the nominal values of process parameters, P_0, for devices and interconnects (e.g. interconnect thickness, T_0, and width, W_0) and a Δ amount by which each of them can vary. This provides PRCA with a spectrum of values for each process parameter ranging from P_{min} to P_{max}, as illustrated in Figure 1. For example, T_0 can vary from T_{min} to T_{max}.

It was demonstrated in [5] that there exists a "context-dependency" for interconnect performance corners. Specifically, the paper showed that the delay of one interconnect structure increased while the delay of another interconnect structure decreased when the metal thickness was increased from T_0 to T_{max}. However, the paper did not derive a revised PRCA methodology to find the true performance corners of a stage. Instead, the authors abandoned the PRCA approach and applied a model-order reduction technique to analyze the impact of process variation on the clock skew at the expense of increased complexity. Furthermore, the notion of context-dependency in the paper is limited to the interconnect structure. However, it is shown in this paper that the driver and receiver gates of a stage also contribute to the context-dependency of the performance corners.

Process corners derive their name from the fact that they are obtained from a combination of P_{max} or P_{min} of each process parameter, i.e., the extreme maximum or minimum variation from P_0 for each process parameter. PRCA assumes that these process corners coincide with the performance corners, i.e., the worst/best-case delay of a stage. It is thus common practice in the industry to use the process corners predicted by PRCA in a pre-extraction step to arrive at two sets of process parameter dimensions, one that yields the best- and one that yields the worst-case delay of a stage under process variation. The RC circuits are then extracted from these two sets of dimensions, after which they are given to an STA tool for timing analysis. *It is shown in this paper, however, that the interconnect process corners may not coincide with the interconnect performance corners of a stage, as assumed in PRCA.* As a consequence, the current industry standard of arriving at the best/worst-case delay of a stage may not yield the correct performance corners. This paper thus proposes a fast STA methodology, called performance corners analysis (PECAN), which determines the correct performance corners of a stage given the nominal process parameters of the devices and interconnect and a Δ amount in which the interconnect parameters can vary. Similar to PRCA, PECAN provides an extraction tool with two sets of process parameter values; however, PECAN's values lie between P_{min} and P_{max} and yield the true performance corners of the stage.

The rest of the paper is organized as follows. Section 2 gives a review of PRCA. PECAN is introduced and explained in Section 3. PECAN is compared to HSPICE simulations and PRCA in Section 4. Section 5 concludes the paper.

2. Process Corner Analysis Review

PRCA uses an independent set of process corners for devices and interconnects to compute the best/worst-case delay of a stage. In this section we explain how PRCA applies to interconnects.

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The best/worst-case propagation delay of interconnect lines is found using 4 values, referred to as process corners: C_{Max}, C_{Min}, RC_{Max}, RC_{Min}. The first two terms are used to model interconnects as being capacitance dominated to calculate the stage delay. The last two terms are used to compute the interconnect delay when the resistance of the wire is significant. For an interconnect with a metal layer cross section of the form shown in Figure 2, PRCA's interconnect corners are found using the parameter values shown in Table 1, where W, T, and H are the interconnect width, thickness and inter-layer-dielectric (ILD) thickness, respectively. The information given in Table 1 can be presented graphically by introducing a rectangular solid, as shown in Figure 3, where each side of the solid represents one of the three interconnect parameters in the range from P_{min} to P_{max}, as indicated in the image. Figure 4 illustrates the fixed location of the PRCA's interconnect performance corners in the rectangular solid.

Table 1: PRPCA Process Corners for W, T, and H

	W	T	H
C_{max}	W_{max}	T_{max}	H_{min}
C_{min}	W_{min}	T_{min}	H_{max}
RC_{max}	W_{min}	T_{min}	H_{min}
RC_{min}	W_{max}	T_{max}	H_{max}

In our subsequent analysis, three problems with PRCA will be discussed. First, it is incorrect to fix the performance corners for any interconnect topology. In particular, it is illustrated that the performance corners may be given by different process corners for different interconnect structures. Second, the performance corners may be different from the process corners. Specifically, it is shown that the best-case corner may not depend on P_{min} or P_{max} for a particular interconnect parameter but on a value within that range. Third, it is incorrect to consider gate and interconnect process corners independently.

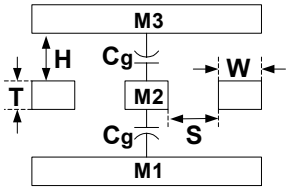

Figure 2: Metal Layer Cross Section

$$C = \varepsilon_{ox} l \left(W/H + T/S \right) \quad (1)$$

$$R = \rho \, l / WT \quad (2)$$

$$RC = \varepsilon_{ox} \rho \left(l^2/(WS) + l^2/(HT) \right) \quad (3)$$

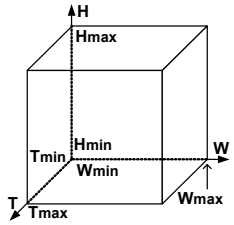

Figure 3: Rectangular Solid

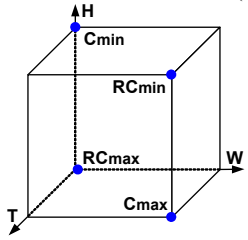

Figure 4: PRCA corners

3. Performance Corner Analysis

PECAN is intended to be used as a fast STA pre-extraction step with the goal of finding the values for each interconnect parameter that *yield* the performance corners of a net given the nominal values of the parameters and the Δ amount each of the parameters can vary. The extraction step following PECAN is then used to arrive at a best- and worst-case RC circuit which can be analyzed by current STA methods for accurate timing analysis. This procedure is, in fact, similar to the one followed by PRCA. However, the main difference between PRCA and PECAN is that PECAN replaces the four PRCA corners with two 50% delay (t_d) corners which are allowed to freely "float" within the cube shown in Figure 3.

3.1 PECAN RC Model

PECAN uses a model in which the driving gates of a stage are replaced by an equivalent total nominal resistor (R_{g0}) and equivalent total nominal output capacitance (C_{g0}), the receiving gates are modeled as a total nominal load capacitance (C_{L0}), and the interconnect is represented as a 1-stage $\prod$-model with resistance R_{int} and capacitance C_{int}. Graphically, the stage shown in Figure 5 is represented by the RC model given in Figure 6. This inaccurate delay model can be used because PECAN's purpose is to find the interconnect parameter values which *yield* the performance corners of a stage; it is not intended to be used to compute the actual best or worst-case delay of a stage.

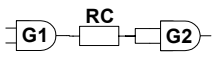

Figure 5: One Gate Stage

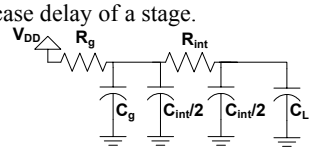

Figure 6: Stage Model

PECAN approximates the delay of the stage shown in Figure 6 by its Elmore delay [12] given as

$$t_d = R_g \left(C_g + C_{\text{int}} + C_L \right) + R_{\text{int}} \left(0.5 C_{\text{int}} + C_L \right). \quad (4)$$

To compute the Elmore delay, all RC values need to be quantified in terms of their process parameters as shown in (5) through (11). The nominal equivalent resistance [13] of each transistor in the driving gate is given by (5) where L_d is the gate length, t_{ox} is the oxide thickness, μ_{eff} is the effective mobility of the gate defined in [15] for the BSIM model, ε_{ox} is the permittivity of the oxide, W_d is the gate width, V_{DD} is the supply voltage, α accounts for short-channel effects [13], and V_{TH} is the threshold voltage of the transistor. The total nominal equivalent resistance of each gate can be found by combining the nominal resistances of each transistor in the gates into a single resistance.

$$R_{g0} = \frac{3}{2} \frac{V_{DD} L_d t_{ox}}{\mu_{eff} \varepsilon_{ox} W_d \left(V_{DD} - |V_{TH}| \right)^{\alpha}} \quad (5)$$

The total nominal gate output capacitance is given by (6) which is the summation of the nominal output capacitances of each transistor of the driving gate given by (7) where C_j is the zero-bias bulk junction bottom capacitance per unit area, A_{diff} is the diffusion area, C_{jsw} is the zero-bias bulk junction sidewall capacitance per unit length, and P_{diff} is the perimeter of the diffusion region.

$$C_{g0} = \sum_{i=1}^{n} C_{g0i} \quad (6)$$

$$C_{g0i} = C_{ji} A_{diffi} + C_{jswi} P_{diffi} \quad (7)$$

The total nominal load capacitance is given by (8) which is the summation of nominal load capacitances for each transistor of the receiver gate given by (9) with Cox = ε_{ox} / t_{ox}.

$$C_{L0} = \sum_{i=1}^{n} C_{L0i} \quad (8)$$

$$C_{L0i} = \frac{2}{3} C_{oxi} W_d L_d \quad (9)$$

The interconnect capacitance is given by [14]

$$C_{\text{int}} = \varepsilon_{ox} l \left(\frac{W_0}{H_0} + 2.04 \left(\frac{T_0}{T_0 + 4.53411 H_0} \right)^{0.071} \right). \quad (10)$$

The interconnect resistance is given by (11) where ρ is the interconnect metal resistance.

$$R_{\text{int}} = \rho l / (W_0 T_0) \quad (11)$$

C_{int} and R_{int} are affected in different ways by W and T, as illustrated by (10) and (11). Specifically, C_{int} increases while R_{int} decreases with increasing W and T. This relationship implies that for small W and T, interconnects are resistance dominated while for large W and T interconnects are capacitance dominated. Since both C_{int} and R_{int} affect the delay of a stage, as shown by (4), there must exist an optimum value for W and T for which the combined impact of C_{int} and R_{int} on the stage delay is minimized. This observation is captured by Figure 7 which plots the change in the

delay of a stage versus W. Figure 7 demonstrates the existence of a minimum global delay point referred to as P_{minGL} for an interconnect process parameter P. It is interesting to note that H only influences C_{int} but not R_{int}. Thus, as illustrated by (11), H needs to be maximized in order to minimize the delay of a stage.

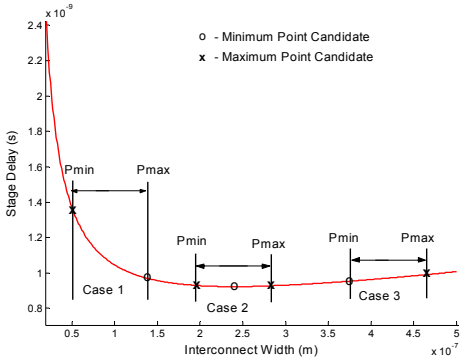

Figure 7: Stage Delay vs. Interconnect Width

3.2 Determining Performance Corners

PECAN uses P_{minGL} to find the performance corners of a stage. Specifically, the location of P_{minGL} in relation to the range P_{min} to P_{max} determines the location of the performance corners. As illustrated by Figure 7, three scenarios may arise in the analysis. For case one labeled in the figure, the worst-case performance corner can be found by setting the interconnect parameter equal to P_{min} and the best-case performance corner can be found with P_{max}. The first case is, in fact, analogous to the performance corners found by PRCA. For case two, the worst-case performance corner may be given by P_{min} or P_{max} while the best case corner is given by P_{minGL}. Specifically, for case two, it is not possible to say beforehand on which side the worst-case corner lies because the slope of the graph shown in Figure 7 may be different on each side, i.e., the slope of the curve on the right to P_{minGL} may be higher or lower than the slope to the left of P_{minGL}. For the third case, the locations of the performance corners are reversed as compared to the first case. The locations of the performance corners predicted by PECAN are summarized in Table 2. A graphical representation of the location of PECAN's performance corners is given in Figure 8. In the figure, the worst-case performance corner can be found in one of four process corners, marked (a), (b), (c), and (d). The best-case performance corner, however, may float around the top surface of the rectangular solid. It is important to note that the locations of the performance corners predicted by PECAN differ substantially from those predicted by PRCA. This observation is due to the fact that, *unlike PECAN, PRCA does not distinguish between the three cases but always assumes the first case*.

Table 2: PECAN Performance Corners for W, T, and H

	Case 1	Case 2	Case 3
Case Criteria	$P_{max} \le P_{minGL}$	$P_{min} < P_{minGL} < P_{max}$	$P_{minGL} \le P_{min}$
Worst Corner	P_{min}	P_{max} or P_{min}	P_{max}
Best Corner	P_{max}	P_{minGL}	P_{min}

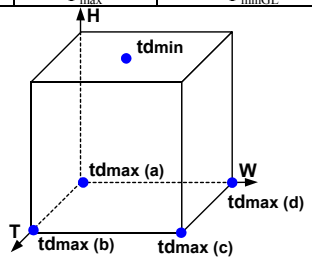

Figure 8: PECAN Performance Corners Locations

3.3 Computation of P_{minGL}

P_{minGL} for each interconnect parameter can be found by taking the partial derivative of (4) with respect to each parameter, setting the equation equal to zero, and solving for the parameter using the nominal values of the remaining parameters. Specifically, W_{minGL} and T_{minGL} can be found by taking the partial derivative of (4) with respect to T and W, respectively, setting each of the equations to zero, and solving for the interconnect parameter. Following these steps, for example, W_{minGL} can be found to be

$$W_{\min GL} = \sqrt{\frac{\rho H_0 \left[2.04 \varepsilon_{ox} l \left(\frac{T_0}{T_0 + 4.53 H_0} \right)^{0.071} + C_{L0} \right]}{2 \varepsilon_{ox} R_{g0} T_0}}. \quad (12)$$

A correction factor, β, was introduced to fine tune W_{minGL} and T_{minGL}, given in (13) and (14) respectively, where R_t is given by (15) and C_t is given by (16). The factors were obtained using regression techniques. In Section 4 it is shown that these correction factors can improve our results slightly by being multiplied to the previously obtained minimum points, as shown in (17).

$$\beta_W = 0.742 + 0.0129 R_t^{-0.275} - 0.0287 C_t^{1.77} + 0.443 \left(C_t / R_t \right)^{0.138} \quad (13)$$

$$\beta_T = -45.27 - 28.11 R_t^{-153} + 46.36 C_t^{0.00178} + 71.14 \left(C_t / R_t \right)^{2.556} \quad (14)$$

$$R_t = R_{g0} / R_{\text{int}} \quad (15)$$

$$C_t = C_{L0} / C_{\text{int}} \quad (16)$$

$$P'_{\min GL} = \beta * P_{\min GL} \quad (17)$$

An important observation that can be made with the aid of (12) is that *P_{minGL} is not only dependent on interconnect parameters but also on the device parameters of the gates on both sides of an interconnect line* due to P_{minGL}'s dependence on C_{L0} and R_{g0}. In the past, this type of context-dependency has not been considered for best/worst-case analysis under process variation. Consequently, it has been believed that best/worst-case corners could be found on interconnects and gates independently. However, we have shown that the performance corners of interconnects are influenced by the interconnect structure, its driving and its receiving gates. This means that the complete context needs to be taken into account to find the correct interconnect performance corners.

4. Simulations

This section compares PECAN to accurate HSPICE simulations. In addition, the improved accuracy of PECAN compared to PRCA is demonstrated. The simulations were done in HSPICE using the BSIM4.0 model and 65nm CMOS technology. Process variations of 30% were assumed in each interconnect parameter which is typical for this technology node [6].

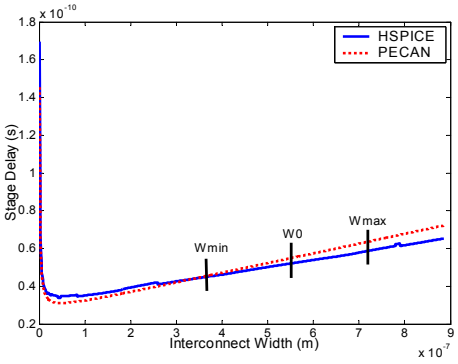

Figure 9: HSPICE & PECAN Simulations

4.1 HSPICE vs. PECAN

Figure 9 shows the delay of a particular stage versus W predicted by HSPICE (solid line) and PECAN (dashed line). For this experiment, T_0=200nm, H_0=200nm, l=100µm, and all (W/L)=10. There are two main observations that can be made from this experiment. First, as explained earlier, the stage delay predicted by PECAN is not accurate compared to the delay found using HSPICE. However, as Figure 9 shows, the shape/fidelity of the HSPICE curve is very well captured by PECAN. This means that PECAN's simple RC model shown in Figure 6 is sufficient to determine the location of P_{minGL}. For this particular experiment, HSPICE gave W_{minGL} at 46nm and PECAN predicted W_{minGL} to be

48nm, as shown in the first row of Table 3. Second, Figure 9 demonstrates that P_{minGL} can lie well below 100nm. As a consequence, there exist feasible designs where the best/worst-case performance corners predicted by PRCA will be wrong.

Table 3 lists more comparisons between HSPICE and PECAN for W. Also given in the table is W_{minGL} determined without the correction factor, β_W, and with the correction factor. Comparing W_{minGL} determined with and without β_W, it is easily seen that β_W reduces the maximum error in W_{minGL}. According to the fifth column of Table 3 the maximum error of W_{minGL} determined with β_W lies below 11%. More importantly, however, the error in the minimum delay computed by HSPICE at W_{minGL} found by PECAN versus the true global minimum delay computed by HSPICE lies below 3% as illustrated in the seventh column.

Table 3: HSPICE vs. PECAN for W_{minGL}

HSPICE		PECAN				
W_{minGL} (nm)	t_{WdGL} (ps)	W_{minGL} w/o β_W (nm)	W_{minGL} w/ β_W (nm)	Err. (%)	t_{WdGL} w/ β_W (ps)	Err. (%)
46	33.739	48	48	4.35	34.729	2.9000
48	31.258	48	43	-10.4	31.264	0.0192
84	93.594	86	79	-5.95	93.597	0.0032
91	99.86	86	89	-2.2	99.864	0.0040
125	257.4	134	134	7.2	257.62	0.0855
193	616.75	229	210	8.81	617.28	0.0895
226	716.6	240	235	2.98	716.8	0.0279
695	11609	721	666	-4.17	11617	0.0689
708	11827	725	715	0.99	11827	0.0000

Table 4: HSPICE vs. PECAN for T_{minGL}

HSPICE		PECAN				
T_{minGL} (nm)	t_{TdGL} (ps)	T_{minGL} w/o β_T (nm)	T_{minGL} w/ β_T (nm)	Err. (%)	t_{TdGL} w/ β_T (ps)	Err. (%)
53	40.734	53	52	-1.89	40.735	0.0025
82	80.102	108	88	7.32	80.104	0.0025
119	25.461	109	107	-10.08	25.465	0.0160
119	3363.3	206	117	-1.68	3363.5	0.0060
180	35.163	192	177	-1.67	35.164	0.0028
204	46.689	213	209	2.45	46.690	0.0021
317	1352.8	582	331	4.42	1352.8	0.0000
688	25.686	642	650	-5.52	25.687	0.0039
1310	18.575	953	1274	-2.75	18.576	0.0054

It is easily shown that no error exists in the worst-case performance corner, provided that the error in W_{minGL} found by PECAN is smaller than Δ; thus PECAN introduces no error in the worst-case corner. It is also easily shown that the worst error in the best-case performance corner is given by the error in t_{WdGL}, the global minimum delay given at W_{minGl}. Overall, we can say that the error of PECAN for W is 0% for the worst-case performance corner and below 3% for the best-case performance corner. Table 4 provides simulation results for T. Using the same analysis for T as done previously for W, we can say that the error of PECAN for T is 0% for the worst-case performance corner and below 1% for the best-case performance corner.

Table 5: PECAN to PRCA Comparison for W_0 = 550nm

	30% Variation in W
PECAN min. Performance Corner	385nm
HSPICE t_d at PECAN Corner	45.56ps
Error of t_d computed by HSPICE at PECAN Corner vs. true global min. t_d	0%
PRCA min. Performance Corner	715nm
HSPICE t_d at PRCA Corner	58.51ps
Error of t_d computed by HSPICE at PRCA Corner vs. true global min. t_d	28.42%

4.2 PECAN vs. PRCA

The greatest difference between PECAN and PRCA arises in the third case given in Table 2 because the location of the best and worst case performance corner is reversed when compared to the first case. An example of such a situation is given in Figure 9. If a nominal width of W_0 = 550nm is assumed, it is possible to quantify the error of PRCA for variations of 30% in W. As summarized in Table 5, when PRCA is used to determine the best-case performance corner for the stage in question, the error in the best performance corner is found to be 28.42%. If PECAN is used to determine the performance corners, however, the location of the corners is correctly found and the error in the best performance corner is 0%. A similar result can be found for the worst-case performance corner. For PECAN's second case shown in Figure 7, the error in PRCA's corner is approximately half of that found for the third case earlier.

5. Conclusions

This paper introduced a fast analytical model for determining accurate parasitic values for best- and worst-case delays of a stage under interconnect process variations. The inputs to the model are the nominal values for each interconnect and device parameter and the amount of variation in each interconnect parameter. The outputs of the model are the interconnect parameter dimensions within the range of process variation that yield the best- and worst-case delay of a stage. Simulations showed that our model accurately predicts the performance corners of a stage while those predicted by traditional best/worst-case analysis methodologies can have an error of up to 28.42%.

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