Entering the Hot Zone — Can You Handle the Heat and Be Cool?

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ABSTRACT

With the latest gaming systems such as X-box, Playstation 3, PSP, IPTV, and H264 requiring more bandwidth, packaged in smaller devices, and providing higher quality, in return they evacuate more heat and consume more power, thus making power consumption and thermal dissipation a major issue for chip designers in the nanometer era

Thermal effects on the chip and package is the next wave. First, there was signal integrity. Then power integrity and now, there is a new first-order effect in the horizon for IC and system designers called thermal integrity. And the traditional design methodology of using uniform temperature across the chip is becoming woefully inadequate and provides insufficient data to the package and system designers, unable to meet the requirement and demands of the consumer. To better understand the impact of temperature variation on chip's performance, both power distribution and package characteristics must be considered in the design and analysis flow. Likewise, a realistic view of the heat distribution across the chip is becoming essential for package and system designers. What makes the analysis of signal, power, and thermal integrity effects challenging is that they must all be considered concurrently across the entire chip, which requires novel approaches to mitigate the issue.

The panel will discuss how urgent is the impact of thermal integrity on system designs and is this a real concern or are we making it up? When and under what condition will it become urgent, and is it related to process nodes, low power applications, type of packaging used, etc.? Is there specific design techniques used for more specific multimedia processing? Can you separate the IC design from package and system designs with some assumptions or is co-design the only way? How accurate is the industry's understanding of the physics of the chip (device), interconnect, and package? Is thermal integrity a first order or second order effect? Given the other variations from nominal, how important is this?

The moderator will conclude with a summary of the panelist comments and be able to make a forward-looking statement about the future of power and heat and their impact on system design.

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Categories and Subject Descriptors

B.6.2 Reliability and Testing
B.7.2 Design Aids
B.8 Performance and Reliability
C.4 Performance of Systems
D.2.2 Design Tools and Techniques

General Terms: Reliability, Performance, Design

Keywords: Thermal effects, Low power, IC packaging

Position Statements:

Panelists have provided their position statements (see below) outlining their opinions. In the panel, each panelist will discuss the new breakthroughs in technology required to address the power and thermal concerns for IC package and system designers and the necessary cooperation between those teams, as well as the EDA companies.

1. Andrew Yang:

When it comes to the issue of "temperature" on IC reliability and manufacturability, there seems to be two camps of opinions. In one camp are those that feel that "thermal" is a future issues being hyped today. But in the other camp, there are designers and foundries that are experiencing thermal integrity is a real issue today. At 90nm and especially at 65nm, over 25% of power consumption is coming from leakage power. And as the temperature increases, leakage increases exponentially impacting timing, power, electromigration, etc. The ability to accurately analyze the impact of temperature and its variations on the silicon is critical to the success of ICs, especially at 65nm and below. Another important point is that when performing thermal analysis, the designers needs to concurrently consider the leakage power, performance — especially clock network, reliability, and packaging. A key factor is the feedback between power and thermal simulation to avoid thermal-runaway condition.

2. Rajit Chandra:

Leakage power is exponentially affected by temperature. Assuming uniform temperature leads to large error margins and high costs--both from chip and package designers' viewpoints. The ability to ship first silicon is limited by leakage. Just as signal integrity solutions were needed to design around signal cross talk issues, thermal integrity is needed to ensure that designs work at specified power, performance and reliability specs. Leaving chip designers to guess the physics of thermal coupling between various heat sources and materials within the IC and the package environment is to repeat the mistakes of yesterday, when cross talk noise-related failures were found in the lab after the chips were manufactured. Only now the cost of such mistakes is even higher.

One of the key capabilities that Gradient offers is the ability to do detailed full 3D thermal analysis of ICs, including heat transfer between devices, metal wires, inter layer dielectric and the package boundaries. Gradient's technology is scalable, efficiently and accurately provides temperature data, and applies to nanometer scale designs with millions of devices and multiple metal layers with different package boundary materials. This data is then used for accurate analysis of hotspots and accurate assessment of leakage power, timing, and other reliability factors such as metal electro-migration. Interfaces with package tools allow verification and optimization of the thermal implications of the package, the system, airflow, the external environment, etc.

Integrating temperature data into existing tools allows designers to reduce their design guardbands and detect any temperature-induced problems. Early analysis, coupled with a range of methods employing thermal-equalization and temperature-aware leakage optimization, must be interoperable at all points with today's physical synthesis and layout tools to ensure convergence of the performance and reliability constraints.

3. Javier DeLaCruz:

Thermal performance of a part can be easily and dangerously be described in standard JEDEC terms like Theta j-a, Theta j-c, and Psi j-b. These are very helpful and important terms that that can help an engineer make an educated package selection initially, but we must remember the assumptions related to these terminologies. Some pitfalls may exist if these metrics are used as a crutch in design.

With some commercial designs, without an airflow condition, the orientation of a part is an important consideration. The locations of the vent holes or other cooling mechanisms are also important. We can use the JEDEC metrics as a starting point, but we must consider the end use and how the part must be cooled. Margin or failsafe conditions may need to be used to prevent thermally induced failures of components. For example, a game system may be mounted onto entertainment center with a glass door that restricts the airflow. Additionally this may be in a cabinet with other power devices such as an amplifier or a DVR. They may also be placed on thick carpeting, which would restrict the airflow to vents that may be on the bottom of the unit. These are conditions that are very different than the theoretical conditions that are delivered on package datasheets. Thermal tracking features built into a die that may reduce power when temperatures are elevated or higher standoffs for components that may be placed on carpets may be possible solutions.

For industrial applications, forced convection usually exists, and while there is typically a benefit of a higher layer-count PCB, other details in the system prohibit proper part cooling. DIMMs are an example of devices that restrict airflow, while other components may locally heat the air. Airflow conditions and direction are critical in heat sink selection. Datasheets tend to show ideal airflow direction conditions which would not normally exist in a true industrial application. Planning the placement and orientation of the fans, power devices and other components will help with power system cooling.

4. Sribalan Santhanam:

In the deep submicron era, power is a fundamental design consideration. Moore’s Law predicts that shrinking geometries relentlessly increase gate density and switching speed, but the accompanying power-density increase places stringent limits on usable gate capacity and operating frequency. Consequently, designers struggle to contain operating power and, increasingly, leakage power, in modern SoC designs.

P.A. Semi’s PWRficient processor illustrates a design implemented with power efficiency in mind from the outset. The designers sought to gain a ten-fold improvement in power efficiency relative to equivalent-performance processors. To achieve this goal, they integrated most system functions into the SoC, thereby gaining control over system power and reducing interconnect power. They then built the entire SoC from first principles, applying a range of power-management techniques pervasively and at all levels from the architecture to physical design.

Leakage, which varies widely across the process range and has an exponential relationship to temperature, presents a unique problem not addressed by this array of power-management techniques. The design team solved the leakage problem by questioning the most basic assumption—that of a fixed operating voltage across process and operating-temperature ranges.

The P.A. Semi team continuously evaluated power dissipation as the design progressed. To validate early estimates, the team triangulated the results of different power estimation methods; as the design progressed, more physical-design data and better simulations improved estimation accuracy. And test silicon in the target process provided the bridge to physical reality, confirming that the models correlated well with silicon. The outcome is a dramatically power-efficient processor and a design methodology that can extend these benefits to 45nm and beyond.