Lookup Table Based Simulation and Statistical Modeling of Sigma-Delta ADCs

Guo Yu
Department of ECE
Texas A&M University
College Station, TX 77843
guoyu@ece.tamu.edu

Peng Li
Department of ECE
Texas A&M University
College Station, TX 77843
pli@ece.tamu.edu

ABSTRACT

Sigma-Delta ($\Sigma\Delta$) ADCs have been widely adopted in data conversion applications due to the good performance. However, oversampling and complex circuit behavior render the simulation of these designs prohibitively time consuming. In this paper, a lookup table (LUT) based modeling technique is presented for efficient analysis of $\Sigma\Delta$ ADCs. In the proposed approach, various transistor-level circuit nonidealities are systematically characterized at the building-block level and the complete ADC is simulated much more efficiently using these table models. As such, our approach can provide up to four orders of magnitude runtime speedup over SPICE-like simulators, hence significantly shortening the CPU time required for evaluating system performances such as SNDR (signal-noise-distortion-ratio). The proposed LUT modeling technique is further extended to assess performance variations due to parameter fluctuations. The resulting parameterized LUT modeling technique not only facilitates scalable performance variation analysis of complex $\Sigma\Delta$ ADC designs, but also allows us to feasibly extract statistical performance correlation models for low-cost test solutions.

Categories and Subject Descriptors: B.7.2 [Integrated Circuits]: Design Aids - *Simulation*

General Terms: Algorithms, Performance, Design

Keywords: Sigma-Delta, Lookup table and statistical modeling.

1. INTRODUCTION

$\Sigma\Delta$ converters offer high resolution and low cost, making them an appealing choice for many applications such as electronic instrumentation and audio signal processing. The application of $\Sigma\Delta$ converts has become increasingly popular because of easy implementation in digital CMOS technology and insensitivity to process variation [1]. By over-sampling the input signal, $\Sigma\Delta$ ADCs achieve high performance through noise-shaping. However, oversampling and complex circuit behavior make the simulation task extremely challenging. SPICE-like simulators can provide good prediction of system performances, however, at the cost of excessive CPU times. For instance, computing the outputs over several ten thousands clock cycles, required for an accurate estimation of SNDR, can easily translate into tens of hours of SPICE run. Given the already lengthy CPU time required for a single analysis run, transistor-level simulation is completely non-scalable for performance variability analysis conducted over a large number of process conditions.

Although high-level simulators (e.g. MIDAS [2] and SWITCAP [3]) are runtime efficient, these techniques are only suitable for architectural-level exploration and determination of building block specifications. The inclusion of very little transistor-level information disqualifies these tools for high-accuracy simulation. Similarly, behavioral-level simulation techniques such as [4] are fast but the accuracy is heavily dependent on the calibration of model parameters, which requires significant human involvement. Therefore, fast behavioral-level simulation is typically not considered as fully automated and accurate unless simulation models can be systematically extracted.

To facilitate efficient design of complex $\Sigma\Delta$ ADCs, simulation techniques employed need to be sufficiently accurate in terms of capturing transistor-level details while being scalable with respect to system complexity. This need is particularly pressing for assessing the impact of process variation, where the analysis complexity tends to explode in a large parameter space. In terms of functional mixed-signal test, statistical models correlating different specifications are also desired in order to replace expensive tests with inexpensive alternatives such that test time and cost can be reduced [5]. Construction of these statistical models requires the simulation of the design at a huge number of process corners.

In this paper, we address the above challenges using a macromodeling methodology. To facilitate feasible whole system analysis, building-block macromodels are extracted from the detailed transistor-level characterization to account for various circuit level nonidealities. Then, the building-block models are used to compose the complete system to perform efficient system simulation, as shown in Fig. 1.

We propose to use lookup tables (LUTs) to characterize each building block. This choice is appropriate since most of analog components of a $\Sigma\Delta$ ADC are clocked and hence their behavior in terms of state-transitions is amenable to lookup table based characterization. Although lookup table based modeling techniques have been used under many different circuit analysis contexts (e.g. [6, 7, 8]), circuit-specific tech-

DAC 2006, July 24–28, 2006, San Francisco, California, USA.

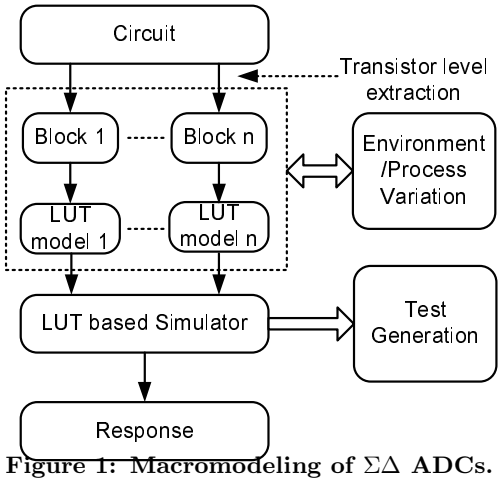

Figure 1: Macromodeling of ΣΔ ADCs.

niques need to be employed in order to appropriately take into account various circuit intricacies. Furthermore, the LUT based techniques need to be extended to address the increased analysis complexity when considering statistical performance variations.

The LUT based macromodeling framework presented in this paper is capable of efficient system simulation, performance variability analysis and statistical performance model extraction of complex ΣΔ ADCs. In this paper the detailed LUT characterization of building blocks is presented wherein the modeling of various circuit-level nonidealities is discussed. To increase the accuracy of the LUT based modeling, specific table extraction techniques are developed. To address the issue of parametric variations, response surface modeling (RSM) is adopted to construct parameterizable LUTs in key process variables, thereby facilitating efficient statistical analysis of ΣΔ ADCs. As an important application of our statistical modeling framework, statistical performance correlation models are feasibly extracted to relate two key linearity specifications, namely THD (total-harmonic-distortion) and INL (integral nonlinearity). The successful extraction of such model indicates that in practice it is possible to use inexpensive THD measurements to predict INL so that the cost of linearity test can be significantly reduced.

2. BACKGROUND

The two basic components of ΣΔ ADCs are modulators and digital filters. The analog input is sampled by a very high frequency clock in the ΣΔ modulator, then the signal is passed through a loop-filter to perform noise-shaping. The output of the loop-filter is quantized by an internal A/D converter, producing a bit-stream at the same speed as the sampling clock. A low-pass digital filter then removes the out-of-band noise and the down-sampler converts the high speed bit-stream to high resolution digital codes.

A widely used second-order ΣΔ modulator is shown in Fig. 2. The major components of a ΣΔ modulator are integrators, internal quantizers and D/A converters. The whole system is clocked by an external sampling clock, which makes it possible to model the performance of each component at sampling intervals. The output of switched-capacitor integrators used in the ΣΔ converter is a function of input signals and their previous states

$$y[k+1] = F(y[k], x[k+1], d[k+1]), \qquad (1)$$

where $y[k+1]$ is the current output of the integrator, $y[k]$ is the previous integrator output, F is a nonlinear function describing the state transfer, $x[k+1]$ and $d[k+1]$ are the current input signal and feedback digital output, respectively. As shown in Fig. 3, since each integrator is clocked by the sampling clock, it is possible to use lookup tables to model the output at the end of each clock cycle, as described in the later sections of the paper.

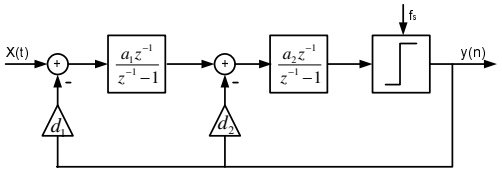

Figure 2: Block diagram of a 2nd-order ΣΔ modulator.

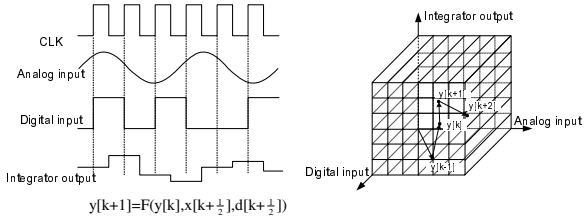

Figure 3: Clocked ΣΔ modulator behavior.

On the other hand, various circuit-level nonidealities such as the finite DC gain, bandwidth and slew rate of the operational amplifies, charge injections of the switches, mismatching of the internal quantizers and D/A converters, etc, are difficult to analyze accurately by hand analysis, neither are their impacts on system performances. For example, as an approximation, the transfer function of an integrator can be written as [4]

$$H(z) = a \cdot \frac{z^{-1}}{1 - \frac{A_0 C_i}{A_0 C_i + C_s + C_{dac}} z^{-1}}, \qquad (2)$$

where a is the integration coefficient, A_0 is the open-loop DC gain of the amplifier, C_i is the integrating capacitance, C_s is the sampling capacitance and C_{dac} is the input capacitance of the DAC. The finite bandwidth, slew rate and saturation of the amplifier also introduce incomplete charge transfer, which shifts the transfer function in equation 2. There is no simple way to calculate the influence of the effects mentioned above in terms of SNDR. Normally transistor-level simulation needs to be employed. Additionally, using transistor-level simulation to predict the linearity of the design can be prohibitively expensive. For example, transient analysis needs to be performed over at least $(2^{14}-1)\cdot 128$ clock cycles to fully characterize a typical 14-bit ΣΔ ADC with 128 OSR (over-sampling-ratio). The process variation analysis is another challenge for the conventional simulators because a large number of long transient simulations are needed to evaluate the performance of the circuit at different parameter corners. In the following sections, it will be shown that these issues can be well addressed by adopting LUT based modeling.

3. LUT-BASED MODELING

The proposed lookup table based simulator is illustrated in Fig. 4. In our fast ADC simulation methodology, various circuit blocks are modeled as follows. The macromodel of each building block of the ΣΔ modulator is extracted at the transistor-level using Cadence Spectre [9]. SNDR and THD are calculated using Fast Fourier transform (FFT) to estimate the performance of the modulator. A two-stage Cascaded Integrator Comb (CIC) filter is implemented as the decimator and the decimation rate (same as OSR) is programmable to adjust for different applications. Since the simulator can run long transient simulation very efficiently (2 seconds for 64k cycles), INL and Differential Nonlinearity (DNL) can be easily calculated by applying an input ramp signal and evaluating the output digital codes.

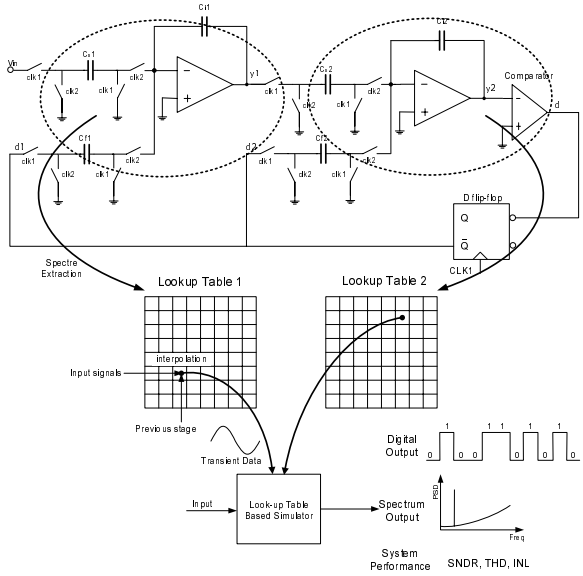

Figure 4: The proposed LUT based simulator.

3.1 Details of Model Extraction Setup

The setup of ΣΔ ADCs for the lookup table generation can be divided into two parts. One consists of integrators and D/A converters, and the other consists of the quantizer. As shown in section 2, the output of the integrator is a function of the input signals and the initial state of the integrator, which are discretized to generate the lookup table. The number of levels depends on the accuracy requirement of the simulation. Since ΣΔ ADCs are quite linear in most cases [1], linear interpolation is good enough. The internal voltage swing discretization is determined by the system architecture. For low-voltage designs, the internal voltages can change from 0 to V_{dd}. To cover the whole range of the voltage swing, we discretize the inputs and outputs of the integrators at N levels (N is in the range of 10), from 0 to V_{dd}.

The extraction setup for an integrator with a 2-bit DAC which is implemented in thermometer code is shown in Fig. 5. A large inductor L together with a voltage source V_s is used to set the initial value of the integrator output. The input of the integrator is also set by a voltage source V_i. The digital output of the quantizer controls the amount of charge to be fed back. The digital codes of 00 to 11 can be represented by counting the number of three voltage sources V_{d1}, V_{d2} and V_{d3} which are set to V_{dd}. For the ΣΔ modulators with 1-bit quantizer, the digital signal can be simply modeled using one voltage source V_d.

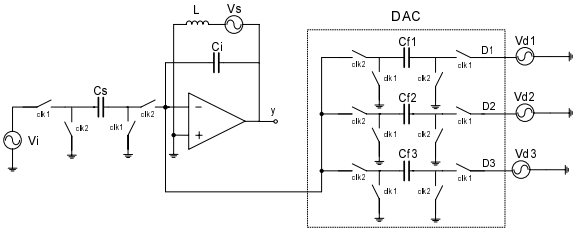

Figure 5: Model extraction setup for integrators.

The nonidealities of the quantizer should also be taken into consideration. For a 1-bit quantizer, we can use Spectre to find the voltage levels where the digital output switches from 0 to 1 (V_{off+}) and 1 to 0 (V_{off-}). The quantizer is then modeled as

$$d[k+1] = \begin{cases} 1 & (V_{in}[k+1] > V_{off+}) \\ d[k] & (V_{off-} \leqslant V_{in}[k+1] \leqslant V_{off+}) \\ 0 & (V_{in}[k+1] < V_{off-}) \end{cases}, \quad (3)$$

where $d[k+1]$ is the current output of the quantizer, $d[k]$ is the output of the quantizer in the previous clock cycle. A 2-bit quantizer can be modeled in a similar way since it is built from three 1-bit quantizers each of which is modeled as in equation 3.

3.2 Controlling of Model Accuracy

To achieve good accuracy for the LUT methodology, several issues regarding modeling must be taken into consideration. When we perform the lookup table generation, the inductor L and the voltage source V_s are used to set the initial condition of the integrator as shown in Fig. 5, redrawn in Fig. 6.

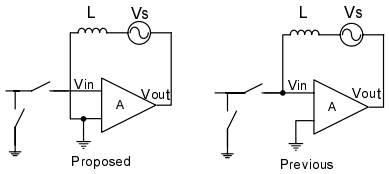

Figure 6: Modified output voltage setup.

As shown in the right part of Figure 6, the initial output voltage of the integrator was not setup correctly in [7]. To see this, suppose that the gain of the amplifier is A, the input voltage is V_{in} and the initial voltage of the amplifier output is V_s, we get

$$A \cdot V_{in} = -(V_s - V_{in}). \quad (4)$$

Therefore, the voltage at the input node can be written as $V_{in} = -V_s/(1+A)$. Suppose that $V_s = V_{dd}/2$ and $A = 60dB$, we will get an offset voltage of $|V_{in}| = V_{dd}/2002$. This offset voltage occurs each time when the table is built and makes the tables generated inaccurate. In our experiments, it has been observed that such an offset voltage can introduce as much as 5dB error in SNDR with the input signal in full voltage swing.

Another issue to be noticed is that, if we take a look into the charging consequence of the integrator in one clock cycle from nT to $(n+1)T$, we can see that the sample-and-hold circuit follows the input signal during the first half clock cycle. So we have to use the input signal at $(n+1/2)T$ instead of $(n+1)T$ as the index to the LUT models during simulation, as shown in Fig. 7. In this case, equation 1 will be rewritten as $y[k+1] = F(y[k], x[k+1/2], d[k+1/2])$, which was not handled correctly in [7]. Since the digital output of the DAC remains the same within a clock cycle, $d[k]$ can be used to replace $d[k+1/2]$.

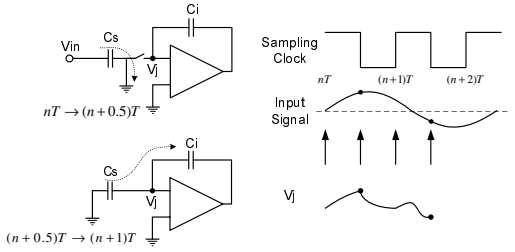

Figure 7: Charging consequence of the integrator.

3.3 Error Analysis

Since the LUTs extracted are of finite size, interpolation needs to be employed during the simulation, which introduces errors. As a reasonable assumption, we can model this type of errors as white noise. Therefore, the interpolation errors can be analyzed in a similar way as the quantization errors. For the $\Sigma\Delta$ modulator in Fig. 2, we consider the interpolation errors for the two integrators as noise injected at the integrator output. Accordingly, we define two noise transfer functions as

$$NTF_{e1} = \frac{a_2 \frac{z^{-1}}{1-z^{-1}}}{1 + a_2 d_2 \frac{z^{-1}}{1-z^{-1}} + a_1 a_2 d_1 \left(\frac{z^{-1}}{1-z^{-1}}\right)^2}, \quad (5)$$

$$NTF_{e2} = \frac{1}{1 + a_2 d_2 \frac{z^{-1}}{1-z^{-1}} + a_1 a_2 d_1 \left(\frac{z^{-1}}{1-z^{-1}}\right)^2}, \quad (6)$$

where NTF_{e1} and NTF_{e2} are the noise transfer functions for the first and the second stage integrators, respectively. The error analysis shows that the interpolation errors of the first stage integrator has more influence than that of the second stage. Such error analysis can guide the LUT extraction to balance between the table size and the accuracy.

4. MACROMODELING FOR STATISTICAL ANALYSIS

Environmental and process variations can introduce noticeable shifts in the performance of $\Sigma\Delta$ ADCs. To allow a feasible variation analysis, we combine the response surface modeling with the LUT based methodology in this section.

4.1 Response Surface Modeling

To find the influence of different circuit parameters to the performance of a system, parameterized lookup tables can be used to approximate the system performance under the circuit parameter variations. Given a set of n observed responses $y_1, y_2, \cdots, y_n$ and n sets of m input variables $x_1, x_2, \cdots, x_m$, we can determine a function to relate x and y as [10]

$$\begin{aligned} \hat{y}_1 &= \hat{h}(x_{11}, x_{12}, \cdots, x_{1m}) \\ \hat{y}_2 &= \hat{h}(x_{21}, x_{22}, \cdots, x_{2m}) \\ &\vdots \\ \hat{y}_n &= \hat{h}(x_{n1}, x_{n2}, \cdots, x_{nm}) \end{aligned}, \quad (7)$$

where
- $\hat{y}_i$ ith approximated response,
- $\hat{h}$ a function relating y and x,
- x_i ith set of circuit variables,
- m number of circuit variables,
- n number of experimental runs.

To construct the parameterized LUTs, a number of simulations should be performed to get enough sets of data. In order to minimize the cost of LUT generation while keeping reasonable accuracy, RSM can be applied to generate a quadratic function relating each entry in the table with the circuit parameters [10]

$$\hat{y} = \hat{\beta}_0 + \sum_{i=1}^{m} \hat{\beta}_i x_i + \sum_{i=1}^{m} \sum_{i=1}^{m} \hat{\beta}_{ij} x_i x_j, \quad (8)$$

where
- x_i ith circuit variable,
- $\hat{y}$ approximated response (an table entry),
- $\hat{\beta}$ estimated fitting coefficients,
- m number of circuit variables.

Since minimizing the number of simulation is a major consideration, a second-order central composite plan consisting of a cube design plan and a star design plan is employed [11]. The cube design plan is a two-level fractional factorial plan which can be used to estimate first-order effects (e.g., x_i) and interaction effects (e.g., $x_i x_j$), but it is not possible to estimate pure quadratic terms (e.g., x_i^2). The star design plan is used as a supplementary training set to provide pure quadratic terms in equation 8.

When we perform variation analysis, the range for each circuit variable is specified at the very beginning. In the two-level factorial experimental design plan, each factor takes on two values -1 and $+1$ to represent the minimum and the maximum values of the circuit variable, respectively. Each factor in the star plan takes on three levels $-\alpha, 0, \alpha$, where 0 represents the circuit variable in the nominal case and $\pm\alpha$ are two standardized values of the circuit variable between the two ends $(-1, +1)$ of the circuit variable. Once the experimental plan has been determined by RSM, the fitting coefficients in equation 8 can be constructed using least-square fitting. In reality, numerically more stable algorithms such as SVD can be used to solve the nonlinear least square problem.

4.2 Statistical Correlation Models

In the previous section, we have built the analysis infrastructure cable of handling process and environmental variations. With the LUT base simulator, we can collect enough data to generate correlation models to predict the specifications that are difficult to measure by using other specifications which are easier to obtain.

INL and DNL are two important linearity specifications for an A/D converter. Since it is time consuming to measure INL and DNL, especially for high resolution ADCs, linearity test can be a significant component of overall test phase [12]. Maximum INL gives an indication of the nonlinearity

in the worst case, so it is wise to use INL_{max} to represent the circuit nonlinearity. Unlike the time-consuming measurement for INL, THD can be much more easily measured in the frequency domain by applying an sinusoidal input [13]. Hence, it is natural to predict INL_{max} using THD by constructing a statistical correlation model relating both, as show in Fig. 8. In this paper, we propose a simulation-based approach for constructing such correlation model for ΣΔ ADCs. By using our efficient LUT based simulator, it is feasible to build a correlation model by collecting a large set of INL_{max} and THD data and performing nonlinear regression. As demonstrated in our experimental results, good correlation between INL_{max} and THD indicates that in practice the linearity test of ΣΔ ADCs can be reduced by using easily obtained frequency-domain measurements.

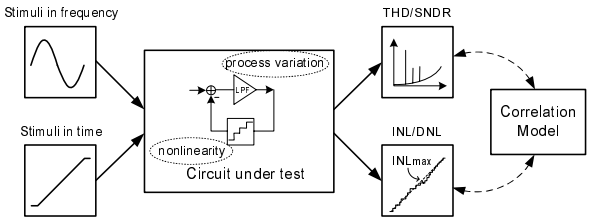

Figure 8: Correlation of INL and THD.

5. EXPERIMENTAL RESULTS

In this paper we will look into two second-order ΣΔ ADCs designed with a 1-bit and a 2-bit quantizer, respectively. Both ADCs are implemented in $0.13\mu m$ CMOS technology with a single 1.5 V supply. The oversampling ratio is set to 128 and the sampling clock used is 1MHz. The test input is a 2kHz $0.8V_{p-p}$ sinusoidal signal and the decimator is configured to 12-bit output. For each ADC, we perform 65,536 (2^{16}) + 100 clock cycles transient simulation with the first 100 points thrown. A Kaiser window is applied to the digital output in FFT analysis. The eight parameters selected to represent the environmental and process variations of the ΣΔ ADC with 1-bit quantizer are presented as follows. Temperature ($Temp$) is swept from $-97C^o$ to $127C^o$, the threshold voltages of PMOS (V_{thp}) and NMOS (V_{thn}), the carrier mobilities of PMOS (μ_{op}) and NMOS (μ_{on}), the effective channel length of PMOS (L_{effP}) and NMOS (L_{effn}), and the oxide thickness (T_{ox}) are all swept ±40% from their nominal values. To build the parameterized LUT models for the ΣΔ ADC with 1-bit quantizer, a Resolution VI 2^{8-2} fractional factorial design plan that includes 64 runs for the cube design plan and 17 runs for the star design plan is used. For the ΣΔ ADC with 2-bit quantizer, we consider three internal DAC capacitance mismatching variations for each DAC. A Resolution VI 2^{6-1} fractional factorial design plan with 45 runs is employed, with 32 runs for the cube design plan and 13 runs for the star design plan.

In Fig. 9, we compare the transistor-level analysis (Spectre) with the LUT based simulation on the nominal design of the ΣΔ ADC with 2-bit quantizer. Two spectra fit very well, especially for the signal and distortions which are of the most interest in the performance analysis, indicating the good accuracy of the LUT simulator.

A comparison of the model extraction time, simulation time, SNDR and THD of the LUT based simulator and

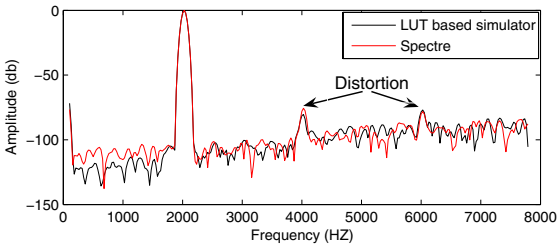

Figure 9: Spectrum of ΣΔ ADC with 2-bit quantizer.

Table 2: Comparison of Spectre and LUT based simulator.

	Spectre	LUT simulator	Error	Speed up
set1	72.4dB	72.1dB	0.3dB	8100X
set2	73.2dB	72.3dB	0.9dB	8100X
set3	74.0dB	73.9dB	0.1dB	8100X
set4	74.8dB	74.6dB	0.2dB	8100X

Spectre in the nominal case are shown in Table 1. Once the LUT models are extracted, the LUT simulator can be efficiently employed to perform statistical performance analysis, which is infeasible for transistor-level simulators. For the 1-bit quantizer ΣΔ ADC, it only takes 20 minutes to conduct 1,000 transient simulations each including 64k clock cycles. For the same analysis, transistor-level simulation is expected to take 4,500 hours to complete. To verify the accuracy of our parametric modeling, four sets of environmental and process parameters are randomly selected and the SNDRs predicted by Spectre and the LUT simulator are compared in Table 2. The error of SNDR is within 1dB, which demonstrates the effectiveness of our method for capturing variations.

The SNDR distribution of the 1-bit quantizer ΣΔ ADC with eight parameters swept randomly in 1,000 runs is shown in Fig. 10. For this particular ADC design, it can be seen that the average SNDR is around 72dB and its derivation is small, indicating the robustness of the design.

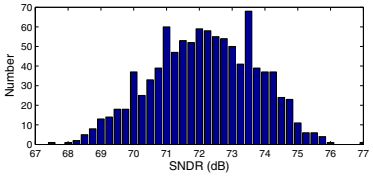

Figure 10: SNDR distribution with random parameter sweeping for the ΣΔ ADC with 1-bit quantizer.

For the 2-bit quantizer ΣΔ ADC, we investigate the impacts of DAC capacitance mismatching. In today's CMOS technology, the mismatching of capacitors can be controlled within ±1%. We set the maximum mismatching to ±2% to completely cover the variation range. Statistical simulations are performed to analyze the influence of the mismatching of the two internal DACs in the ΣΔ ADC with 2-bit quantizer by sweeping the values of the three charging capacitors for each DAC. The distributions of SNDR due to the capacitance mismatching in the two DACs are shown in Fig. 11.

Table 1: Runtime and accuracy of the LUT based simulator.

	LUT based simulator					Spectre		
Design	Nominal extract	Parametric extract	Run time	SNDR	THD	Run time	SNDR	THD
SDM (1bit)	7 min	9.5 hr	2 s	73.8 dB	-63.1 dB	4.5 hr	74.1 dB	-62.6 dB
SDM (2bit)	20 min	15 hr	4 s	86.8 dB	-76.2 dB	9.5 hr	86.2 dB	-76.8 dB

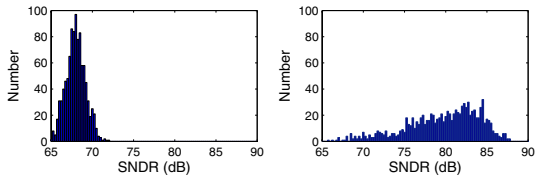

Figure 11: SNDR distributions with mismatching in different DACs for the ΣΔ ADC with 2-bit quantizer.

We can see from the two figures that the mismatching of the DAC connected to the first stage integrator (left figure) has much more influence to the system performance than that of the other DAC (right figure). This can be explained by the fact that the first DAC is connected directly to the input, so the feedback error because of the DAC mismatching will be magnified by the second stage integrator. The result of this analysis indicates that more attention should be paid to the first stage DAC in the design process.

Finally, we demonstrate the correlation model of INL_{max} and THD built based on a set of 1,000 transient simulations. Nonlinear regression is applied to build a third order polynomial correlation model. We compare the INL_{max} predicted by the correlation model and that by simulation for 1,000 circuit samples in Fig. 12.

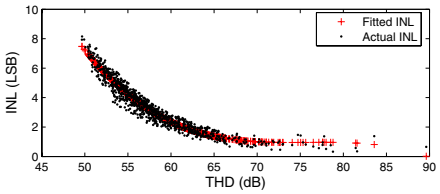

Figure 12: Correlation of INL_{max} and THD

The coefficient of determination is

$$R^2 = \frac{SSR}{SSTO} = \frac{\sum(\hat{y}_i - \bar{y})^2}{\sum(y_i - \bar{y})^2} = 0.9413, \qquad (9)$$

where $\bar{y}$ is the mean value of INL_{max}, $\hat{y}_i$ is the fitted value and y_i the simulated value of ith INL_{max}. The large value of coefficient determination indicates a strong correlation between these two specifications. In practice, we expect that our modeling framework can be employed to identify such correlation so that the alternate test paradigm can be applied to reduce the test cost.

6. CONCLUSIONS

An efficient lookup table based simulation technique for ΣΔ ADCs is presented. By combining RSM, parameterized LUT models in terms of important underlying circuit parameters are constructed. With this methodology we can analyze the circuit performance as well as the influence of parameter variation very efficiently. We have also demonstrated the correlation of maximum value of INL and THD. A correlation model is successfully extracted using our LUT based simulation infrastructure, indicating the possibility of using THD measurements to perform more cost-effective test of INL.

7. ACKNOWLEDGEMENT

This work was funded in part by C2S2, the MARCO Focus Center for Circuit & System Solution, under MARCO contract 2003-CT-888.

8. REFERENCES

[1] S.R. Norsworthy, R. Schreier, and G.C. Temes. *Delta-Sigma Data Converters : Theory, Design, and Simulation*. IEEE Press, Piscataway, NJ, 1997.

[2] S. Babii, L.A. Williams, B.E. Boser, and B.A. Wooley. *MIDAS User Manual*. Stanford University, Stanford, CA, 1997.

[3] S.C. Fang and K. Suyama. *Users' manual for SWITCAP2*. Columbia University, New York, NY, 1992.

[4] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto. Behavioral modeling of switched-capacitor sigma-delta modulator. *IEEE Trans. Circuits Syst. - I*, 50(3):352–364, March 2003.

[5] P.N. Variyam, S. Cherubal, and A. Chatterjee. Prediction of analog performance parameters using fast transient testing. *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, 21(3):349–361, March 2002.

[6] W.M. Goughran, E. Grosse, and D.J. Rose. CAzM: A circuit analyzer with macromodeling. *IEEE Trans. Electron Devices*, 30(9):1207–1213, September 1983.

[7] R.J. Bishop, J.J. Paulos, M.B. Steer, and S.H. Ardalan. Table-based modeling of delta-sigma modulators. *IEEE Trans. Circuits Syst.*, 37(3):447–451, March 1990.

[8] G.T. Brauns, R.J. Bishop, M.B. Steer, J.J. Paulos, and S.H. Ardalan. Table-based modeling of delta-sigma modulators using ZSIM. *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, 9(2):142–150, February 1990.

[9] *Affirma Spectre Circuit Simulator User Guide*. Cadence Design Systems, Inc., San Jose, CA, 2000.

[10] K. K. Low and Stephen W. Director. An efficient methodology for building macromodels of IC fabrication processes. *IEEE Trans. Computer-Aided Design*, 8(12):1299–1313, December 1989.

[11] George E.P. Box, J. Stuart Hunter, and William G. Hunter. *Statistics for Experimenters : Design, Innovation, and Discovery*. John Wiley & Son, Hoboken, NJ, 2005.

[12] S. Cherubal and A. Chatterjee. Optimal INL/DNL testing of A/D converters using a linear model. In *IEEE Int. Test Conf.*, pages 358–366, October 2000.

[13] Nico Csizmadia and A.J.E.M. Janssen. Estimating the integral non-linearity of AD-converters via the frequency domain. In *IEEE Int. Test Conf.*, pages 757–762. Atlantic City, NJ, September 1999.