# DFM: Where's the Proof of Value?

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## ABSTRACT

How can design teams employ new tools and develop response methodologies yet still stay within design budgets? How much effort does it require to be an early adopter and what kind of measurable results compensate for this effort? Panelists discuss how their design-for-manufacture (DFM) tools fit into a fixed design methodology, budget and timeline, and give examples of expected ROI (monetary, quality, reduced time-to-market, and comprehensive yield).

The aim of this panel is to provide a serious comparison of related DFM technologies on the market and some idea of the cost and difficulty of integrating the tools into a fixed design budget and timeline. Specific results will be cited, along with examples of expected ROI (monetary, quality, reduced time-to-market, and comprehensive yield enhancement).

The audience should walk away with enough information to make an informed decision on which companies would make sense for their DFM challenges, to reach their own yield and throughput goals.

## Categories and Subject Descriptors:

B7 Integrated Circuits, D.2 Software Engineering

## General Terms:

Design, Algorithms

**Keywords:** Design for manufacture, DFM, Design for yield, ROI, RET, OPC, Yield optimization

## Position Statements:

Panelists have provided their position statements (see below) outlining their opinions. In the panel, each panelist will give insight into why their technologies offer a good return for investment for the additional effort expended by the design team.

## 1. Raul Camposano:

The killer applications of DFM so far have been in lithography, in particular RET, litho verification and mask data preparation. A mask synthesis flow is indispensable. It is largely transparent to designers as it is typically run by manufacturing. Further downstream, the combination of TCAD, test chips and a yield management system can generate important information for design tools.

Checks and correction for manufacturability however are migrating upstream in the design flow. Incorporating lithography compliance checks and correction into the physical design and verification is emerging as a must for advanced technologies. Other such DFM technologies include dealing with variability to reduce margins, more accurate modeling of CMP for better metal fill and more accurate extraction, modeling mechanical and thermal stress more accurately to predict potential via failure and change in electrical parameters.

The full benefit of "DFM" is only realized by increasingly integrating what needs to happen in the fab (mask synthesis, yield management, test chips, TCAD) with a new generation of manufacturability enabled design tools.

## 2. Mike Gianfagna:

For DFM to work, the effort to adopt new tools and technologies should be low, with a demonstrable improvement in yield, performance or reliability. It is well documented that lithography variation is a significant contributor to yield loss. What is drawn on the layout is no longer what is printed in silicon. At 90nm, this effect can rob 10% of device yield, and it's getting worse as we approach 65nm. Furthermore, excessive guard-banding is robbing circuit performance. Resolution enhancement tools such as optical proximity correction (OPC) reduce the problem, but they are used after the design taped out, causing extremely long run times and huge data volumes. Below 90nm, lithography issues are too widespread and too subtle to all be fixed "after the fact".

We have invented new tools that meet these challenges by providing efficient, robust and circuit-aware incremental and re-usable OPC processing for manufacturing engineers. These same tools are integrated into existing design flows to produce accurate layout views of the design as printed in silicon. (We refer to this as the DFM View™.) Integration into existing flows for both design and manufacturing engineers reduces adoption costs substantially. With a lithography-aware design flow such as this, tape-out essentially becomes a non-event. All design data is verified printable and OPC correct during the physical implementation phase. And because the DFM View is used, timing and power expectations are in line with what can be manufactured. Mask data preparation now becomes a


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process of assembling the chip and performing final verification. No multi-week OPC runs and no massive error reports. This is what a DFM solution should look like.

## 3. Andrew Kahng:

DFM solutions have emerged from the realm of marketing hype and are now providing tangible benefits to chip designers. There are two types of DFM solutions – physical and electrical. Physical DFM solutions, such as RET, have been instrumental in extending the life of photo-lithography. However, physical DFM tools are purely "geometric" in that they work to preserve shape fidelity without any knowledge of the electrical characteristics of the shapes that are manufactured in silicon.

The future of DFM can be seen in a new generation of electrically-aware DFM tools that drive power and timing requirements into the manufacturing process while, at the same time, bringing process awareness forward into design. At 90nm, electrical DFM solutions have already proven their ability to dramatically reduce leakage power and leakage variability, and to improve timing.

An ideal electrical DFM solution does not require any changes to existing design flows, does not require a different hand-off to manufacturing, and does not require detailed proprietary process information from the foundry. Thus, chip designers can reap the substantial benefits of electrical DFM at a very low cost of adoption.

## 4. Naeem Zafar:

Until recently, design engineers had relatively little need to concern themselves with design for manufacture (DFM) or design for yield (DFY); they have relied on their wafer manufacturer to address these issues. As a result, to prevent interruption to today's IC design flow, new, more aggressive RET technologies have been adopted by fabs to "correct" manufacturing issues seen at 90nm and below. However, since manufacturing and yield issues are strongly design-dependent and are affected by how the design is laid out, they are now being pushed upstream into the design process.

Interestingly, today's DFM market mirrors the classical categorization of tools available to designers: design creation, analysis, and verification. As the DFM market evolves, we will see a convergence of these DFM technologies into a cohesive DFM-driven IC design flow. The larger vendors are attempting to bolt these new technologies onto their existing implementation flows. However, new DFM-driven design flows need to be anchored by IC implementation tools with DFM-aware architectures designed to accept DFM analysis data from yield, lithography, and CMP simulators, to create DFM-correct designs.

The effort required to adopt new DFM technologies will reap ROI rewards by employing tools with complex architectures that do a lot more but that simplifies designer's life by simplifying the flows and eliminating post route fix-up methodologies currently deployed.

## 5. Joe Sawicki:

Looking at the ocean of DFM tools being touted on the market today, a designer is faced with the nearly overwhelming task of understanding what will bring value to their design activities. Even eliminating the tools and companies for whom DFM clearly means "design for marketing," a designer is faced with dozens of options that, if all purchased, would constitute a design seat costing several millions of dollars. Making matters even more confusing, DFM today is a lot like flossing your teeth—a bit of annoyance today for a return in the future. Given this, what is a designer to do?

First, look for tools that are a natural fit into the existing design flow. No, everything doesn't (and can't) go into the place and route engine, but they do need to leverage existing interfaces and flow points. Second, look for tools that do not require designers to become manufacturing engineers. The first tools that attempted to do litho-friendly design checking a couple of years ago ran into this problem as they generated very pretty lithography contours for designers that had no idea what to do with them. Third, production-proven matters. The easiest thing in the world is to come up with a tool that fixes problems that aren't production-proven and misses problems that are. Fourth, remember that even with all these issues, the problems are real. Tools are being released now that have significant impact on these problems, and addressing these problems keeps your chip from being the latest yield-disaster in the headlines of EE Times.

## 6. Atul Sharan:

All the angst and buzz associated with DFM is primarily due to discontinuities associated with lithography and, to some extent, chemical mechanical polishing (CMP). While the CMP process is improving, the lithography resolution problem is getting worse. The fundamental assumption in the current design tools -- what you draw is what you get on silicon -- is now broken. This loss of resolution translates into unacceptably large variability in the design, resulting in yield loss (both catastrophic and parametric), dramatically higher design margins and longer design closure cycles. Ultimately, process technology is underutilized. All these have a direct impact on ROI.

Unfortunately none of these variations can be accounted for through design rules. What is required is a new level of abstraction to model and predict these variations across the chip -- not unlike what SPICE models are to transistor behavior for a designer. This must be done for both device and interconnect, and in the context of the each design, as these are proximity affects not restricted to nearest-neighbors geometries.

These new technologies – which move the designer from a primarily rule-based methodology to "rules+model"-based methodology will not themselves fall into any traditional method of adoption. The challenge is to introduce them into design flows without requiring designers to make any change in whichever conventional design tools they are using, and without requiring them to suddenly become manufacturing engineers. These new generation of tools also will require additional and new information from the fabs/foundries - and this is already happening.

Only with such tools in place can proper ROI analysis be done on the real cost of ignoring these "DFM" issues. More importantly, only by using these tools, can designers be assured that they are fully utilizing process technologies without sacrificing time-to-market.