Test Response Compactor with Programmable Selector

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ABSTRACT

The paper presents an efficient method for synthesis of scan chain selection logic. It is capable of acting as a flexible X-control logic for test response compactors. The same circuitry can also be employed to selectively gate scan chains for diagnostic purposes.

Categories and Subject Descriptors

B.8.1 [**Performance and Reliability**]: Reliability, Testing and Fault Tolerance.

General Terms

Algorithms, Design, Reliability, Theory.

Keywords

Compression, scan chain selection, unknown states, VLSI test.

1. INTRODUCTION

It is widely recognized that in scan-based designs a certain number of scan cells may capture unknown (X) states. Sources of unknown states include uninitialized memory elements, bus contentions, non-scan flip-flops, floating buses, internal three-state logic, or multi-cycle paths when generating at-speed tests. Once captured, the unknown states can be subsequently injected into test response compactors, thus affecting resultant signatures. Very often, even if compactors are designed to tolerate certain amount of X states, their ability to preserve test related information quickly deteriorates because error patterns become masked by gross of unknown values.

Since X states may invalidate fault effects recorded in test responses, various test response compaction schemes attempt to reduce a possible impact the unknown states may have on a test quality. In general, compactors fall into one of three different categories. *Combinational* compactors flush out X states, but in order to maximize fault detection and diagnosis they require scan chain masking logic. These compactors may have a non-canceling property by observing each scan chain on two or more outputs to improve handling of small number of X states and to provide the capability to identify failing scan chains [7], [11]. *Finite-memory* compactors flush out X states in a number of cycles [6], [14], [18]. *Time* compactors have infinite memory, and thus an X state, once injected, will stay there until a read out operation. Moreover, time compactors have a fan-out in the feedback that results in a rapid multiplication of X states.

In order to handle circuits with a wide range of X state profiles, a compaction scheme has to be combined with a scan chain masking mechanism. Without it, certain combinations of X states that cannot be eliminated by ATPG would prevent observability of some scan cells and result in a significant coverage drop. Clearly, compactors that do not tolerate unknown values require complete elimination of X states. X tolerant compactors need masking of large clusters of X states. Furthermore, the information required to control scan chain selection has to be optimized as otherwise it will negatively impact the effective test data volume compression.

There is a number of solutions that allow, to a certain degree, for selective observation of scan chains. A circuitry to mask selected unload values so that X states do not reach a compactor is employed by OPMISR technique [2], [3]. A *selective compactor* is proposed in [13]. Its enhanced version [16] masks a given number of scan chains by deploying a register file to encode targeted scan chains. A simple LFSR-based masking circuit is described in [10]. It employs a conventional LFSR reseeding to gate scan chains in a per cycle mode. In X-tolerant deterministic BIST [19], a small percentage of scan chains is observed by means of a *two-stage scan-out selector*. At each stage, each input is connected to two different outputs and every two outputs share only a single input. An *X-masking logic* [17] allows certain amount of over-masking while its structure is obtained as an instance of logic synthesis with don’t cares, where inputs are provided by any logic BIST or test data compression scheme. A test set-dependent masking circuitry is also proposed in [12]. A *channel masking* scheme presented in [5] allows to either disable all scan chains, or to select scan chains belonging to one of two groups at the price of possible over-masking. A weighted random pattern generator can be used [8] to form a stochastic parity matrix of the X-compact approach such that the unknown states are masked with a high probability in so-called *X-tolerant multiple input signature register*. A scheme using LFSR reseeding has also been proposed in [21]. In this case, however, the outputs of masking circuitry are formed by AND-ing several outputs of a phase shifter in order to decrease probability of blocking non-X responses. The *X-filter* [15] removes effects of X states from test responses compacted by means of error correcting codes. Other techniques are also disclosed in several patents, see for instance [4], [10], [20].

The key requirements for a reliable test response compaction scheme include (1) ability to guarantee observability of any scan cell for a wide range of X state profiles, (2) design simplicity, and (3) minimal amount of additional information required to control compactor operations. In this paper, we present a flexible scan

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chain selection scheme which fulfills all these requirements and offers a high quality test, ease of use, and broad applicability with no design impact. The main original contributions of the paper consist of (1) a new synthesis algorithm for generating a linear multiple scan chains selection logic; (2) analysis of a selector encoding efficiency; (3) a new technique to rank scan chains and determine per pattern scan chain selection masks employed to suppress X states; (4) experimental results for a variety of designs showing applicability of the proposed scheme and actual impact of X states on a test pattern count and compaction ratios.

2. SELECTOR SYNTHESIS

Figure 1 shows a programmable selector placed in a typical scan-based design. The selector consists of a mask register (MR) and a combinational logic driven by mask bits stored in a compressed form in MR. The selector outputs provide gating signals to indicated scan chains such that X states or unwanted responses from these chains cannot reach a test response compactor.

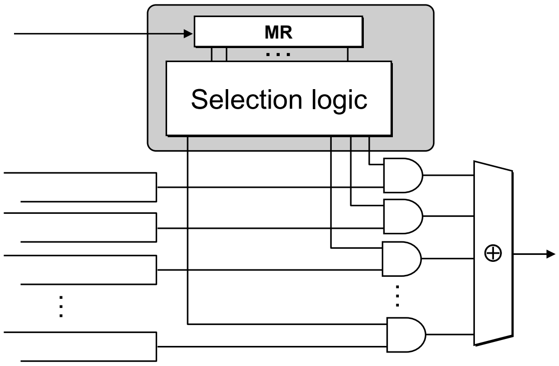

Figure 1. Selector in scan-based designs

It is worth noting that values occurring at the inputs of AND gates (Fig. 1) are threefold:

- 0 – designated scan chains are blocked to suppress unknown states (or to disable scan chains for other reasons such as fault diagnosis and silicon debug),
- 1 – those scan chains are required to feed a compactor as they carry test responses containing errors captured in flip-flops hosted by the chains,
- dc (don't cares) – scan chains whose content is not regarded critical may receive either 0 or 1 as gating signals.

In order to guarantee that all scan chains are enabled or disabled in accordance with the pre-specified requirements, the combinational part of the selector is defined in terms of *selector polynomials* indicating how particular mask bits (stored in register MR) are connected to the outputs. In principle, the selector is designed as an m-input n-output linear mapping circuit, where m is the number of mask bits, n is the number of scan chains, and $m << n$. Each output is then obtained by XOR-ing a given number F of inputs – an example of such a circuit is shown in Fig. 2 for $m = 6$, $n = 12$, and $F = 3$.

Synthesis of the selection logic is primarily aimed at achieving high *encoding efficiency*, which is defined as a ratio of successfully encoded pre-specified gating signals to the number m of deployed mask bits. This objective is of critical importance here as a failure to encode a single gating signal may result in a significant coverage drop by having the entire scan chain unobservable. This is in a clear contrast to test pattern compression where missing one specified bit does not jeopardize quality of test to such extent. Since encoding efficiency is directly related to the probability of linear dependency among selector polynomials, the task of designing selector can be guided by data indicating how likely it is that some of the already accepted polynomials and those regarded as possible candidates may form linearly dependent sets. Using this information, the synthesis is carried out n times by means of a greedy selection as follows.

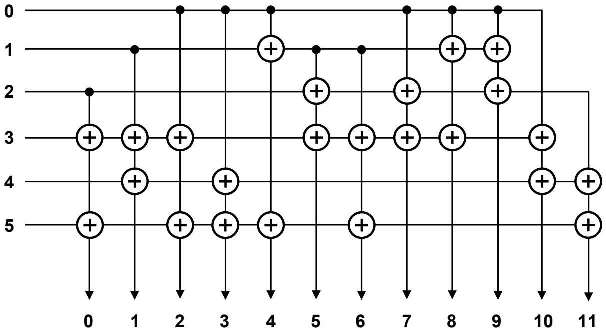

Figure 2. Example of linear selector

Synthesis algorithm.

1. Generate randomly a next candidate polynomial.
2. In order to roughly reduce the linear dependency, check if a new candidate shares at most a given number of the mask bits with all polynomials accepted earlier. If this is not the case, reject the candidate and go back to step 1.
3. Using Gaussian elimination, determine the reduced row-echelon form (and subsequently a rank) of m-element sets of polynomials formed by choosing randomly m – 1 polynomials from the list of polynomials already accepted, and by appending the candidate as the obligatory member of the set. The candidate polynomial can be then associated with the average rank computed over a large number of such m-element sets.
4. Repeat steps 1 ÷ 3 for a given number of candidates (in experiments reported next, this number is equal to 1000).
5. Accept a polynomial with the highest average rank and add it to the solution list.

Table 1. Probability of linear independence (%)

Spec.	Mask register size (m)			
bits	32	34	32 [1]	34 [1]
16	99.74	99.85	98.87	99.50
18	99.53	99.77	97.80	98.68
20	98.82	99.51	96.17	97.42
22	97.75	98.85	91.39	94.05
24	95.34	97.46	77.99	84.79
26	89.37	94.77	54.69	67.22
28	75.47	88.32	26.71	40.24
30	46.70	73.73	7.09	16.48
32	9.34	45.10	0.68	4.48

First results, indicating effectiveness of the above algorithm, are presented in Table 1. It gives the probability of linear independence for two selectors (m = 32, m = 34, F = 3) driving n = 128 scan chains. The number of specified gating signals ranges from 16 to 32. For the sake of comparison, we also include results reported in [1] for purely random linear stimuli decompressors. Superiority of our approach over the scheme [1] is clearly pronounced in the table. For instance, given a likelihood of linear independence, a new selector is capable of encoding approximately four more specified bits than the circuitry of [1] for otherwise the same values of m and n. Also, with the increasing number of specified bits, the probability of linear independence remains much higher once the number of specified bits becomes close to the number of mask bits.

3. CHARACTERIZATION EXPERIMENTS

Comprehensive experiments were run to measure the encoding efficiency of the linear selectors described in the previous section. *Note, that this is the first time such results are presented for linear combinational networks.* Given values of m, n, and F, every experiment is comprised of a number of successive steps. In step k it is verified (by solving the corresponding linear equations) whether k specified bits (gating signals) can be encoded. The specified bits subjected to encoding in step k are obtained by adding a new specified bit to those bits that have already been used in step k – 1. The process continues until the first failure. In such a case, the number of bits that were encoded, i.e., those used in the previous step, is recorded by incrementing a corresponding entry of a histogram. Subsequently, a new combination of gating bits becomes the subject of encoding.

Table 2. The average encoding efficiency (%)

F = 3	Number of outputs			
m	64	128	192	256
12	99.27_2	98.85_2	98.31_2	-
16	98.05_2	96.69_2	95.99_2	96.28_2
24	97.70_1	95.50_2	94.61_2	94.42_2
32	98.23_1	95.97_1	94.17_1	94.17
40	98.59_1	96.02_1	95.22_1	93.96_2
48	99.21_1	96.54_1	95.38_1	94.84_1
56	99.41_1	96.90_1	95.42_1	94.92_1
F = 5	Number of outputs			
m	64	128	192	256
12	100.68_4	100.68_4	100.50_4	100.17_4
16	100.30_3	100.11_3	99.64_3	99.89_4
24	99.91_2	99.88_3	99.58_3	99.52_3
32	99.90_2	99.67_2	99.62_2	99.65_2
40	100.02_2	99.65_2	99.61_2	99.66_2
48	99.99_1	99.88_2	99.59_3	99.65_2
56	100.05_1	99.71_2	99.56_2	99.59_2

The results are presented in Table 2 for F = 3 and 5. Data in the table assume a form E_s, where s indicates in each case how many stages of the mask register are shared (at most) by any pair of the selector polynomials. Clearly, each entry to the table corresponds to the average number of scan chains whose gating signals can be encoded. As an example, consider a 64-output selector using *trinomials* (F = 3) and a 32-bit mask register. The resultant encoding efficiency is equal to 98.23%. In other words, this logic is able to encode, on the average, 32 × 0.9823 = 31.43 gating signals (scan chains). Ability to control such a large fraction of outputs is very promising given the fact that only a small percentage of scan chains usually contain a vast majority of X states [14]. Although the encoding efficiency slightly decreases with the increasing number of scan chains, in all examined cases it always remains well above 90% threshold. At the same time, the encoding efficiency increases with the increasing value of F. It creates an interesting trade-off between the hardware cost of the selector and its performance.

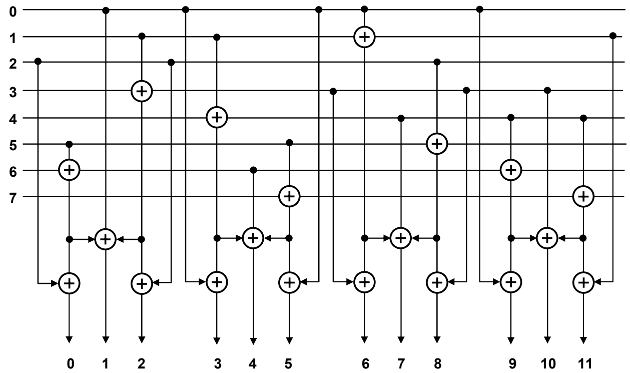

Figure 3. Selector with 3 & 5 linear circuitry

The above observation can also be used to design a new type of selector with further enhanced performance, while the hardware cost would remain the same as that of circuits with F = 3. An example of such a design is shown in Fig. 3. The idea here is to replace certain trinomials with their 5-term counterparts (*pentanomials*) in such a way that the latter items are formed by reusing, in each case, two 2-input XOR gates (say $a \oplus b$ and $c \oplus d$) already used to implement some trinomials. A pentanomial can be then formed by using only two 2-input XOR gates as follows: $(a \oplus b) \oplus (c \oplus d) \oplus e$, where e is the fifth term of a newly created polynomial.

Synthesis of new selectors rests on the Stinson's hill climbing employed here to refine a selector obtained by using the method of Section 2. It is worth noting that when the synthesis step described earlier is completed, one can determine an associated average rank for each selector trinomial. The second step of the proposed synthesis method repeatedly replaces a trinomial having the lowest rank with a pentanomial created based on trinomials with higher ranks (in fact, several candidate pentanomials are formed, and the one with the highest rank is accepted). Notice that the number of pentanomials created this way cannot exceed n/3.

Table 3. The average encoding efficiency, F = 3 & 5

	Number of outputs			
m	64	128	192	256
12	100.62_2	100.04_2	99.95_2	-
16	99.49_2	98.39_2	98.34_2	98.19_2
24	99.09_1	98.06_2	97.60_2	97.69_2
32	99.42_1	98.30_1	97.59_2	97.38_2
40	99.59_1	98.36_1	97.90_1	97.57_2
48	99.89_1	98.68_1	98.06_1	97.78_1
56	100.25_1	98.73_1	98.07_1	97.77_1

Table 3 illustrates performance of the enhanced linear selector for the same parameters as used earlier in Table 2. Also, we adopt the same notation as before.

4. FURTHER EXPERIMENTAL RESULTS

The proposed scan chain selection logic was further tested on several industrial designs. For each design, only a single scan cell was always chosen as a primary fault propagation site. Hence, the proposed approach guarantees a uniform handling of all faults, especially those with a small number of propagation sites which might otherwise be blocked. Indeed, as shown below, the selection algorithm could likely arrive with such masking decisions as faults with a large number of observation points would play a dominant role. A single-output XOR tree was deployed as a combinational test response compactor. The mask register was loaded only once per pattern. Such an approach contributes a negligible amount of data, and thus it does not compromise a compression ratio. It also prevents timing closure violations. With this masking scenario, X states may hinder observability of certain errors in a twofold manner. If a given X state is not suppressed, then it is impossible to observe errors captured at the same scan-out cycle and arriving from scan chains it is XOR-ed with. On the other hand, blocking an X state hides all errors occurring in the same scan chain.

An increase in pattern count was employed as a figure of merit to assess performance of the scheme. Indeed, when original test patterns are applied, several test escapes are observed due to X states and the use of selection logic. Hence, one has to apply a number of top-up patterns until a target fault coverage is restored. Given locations of failing scan cells and unknown state for each test pattern, finding the complete set of stimuli proceeds as follows.

1. For each scan chain compute two coefficients S_i and M_i, where S_i represents the estimated number of errors that will be preserved provided scan chain i is selected, while M_i is a similar number for scan chain i if it were masked. Let $\mathbf{E}(i)$ and $\mathbf{X}(i)$ be the sets of flip-flops in scan chain i that capture errors and unknown states, respectively. Let also E_c and X_c represents the number of errors and X states, respectively, captured by scan cells belonging to scan-out cycle c. Coefficients S_i and M_i are then given by the following formulas:

$$S_i = \sum_{c\in \mathbf{E}(i)} 2^{-X_c} - \sum_{c\in \mathbf{X}(i)} E_c / X_c$$

$$M_i = \sum_{c\in \mathbf{X}(i)} E_c 2^{-(X_c-1)} - \sum_{c\in \mathbf{E}(i)} (X_c+1)^{-1}$$

   It is worth noting that S_i is calculated as a difference between the number of errors occurring in a given scan chain (and calibrated by the probability that X states occurring in the same time frames will all be masked – we assume that a single scan chain is masked with probability 0.5) and the number of errors occurring in the same time frames as those of X states hosted by a given scan chain (again calibrated by the number of corresponding X states to avoid double counting). Similarly, M_i is equal to the number of errors occurring in the same time frames as those of X states (now suppressed) hosted by a given scan chain provided, however, that they are not masked by other unknown states from the same shift cycles. Clearly, this number has to be reduced by errors occurring in the masked scan chain (calibrated by X's from other scan chains, and including the masked chain itself).

2. Find the largest coefficient S_i or M_i, and mark the corresponding scan chain with the masking value of 1 (select) or 0 (mask) depending on whether S_i or M_i was chosen. Note, that this is not the final masking yet, as these signals must be subsequently encoded.
3. Based on a decision made in step 2, update the content of all scan chains by either deleting all errors and X states in a scan which is supposed to be masked, or by deleting all errors and X states in those time frames where a selected scan chain features an unknown state.
4. Assign iteratively the gating signals to the remaining scan chains by repeating steps 1, 2 and 3.

Table 4. Experimental results – I

		m	IPC	IPC (%)	Comp. (x)
Circuit	**C1–d0**	8	922	163	18.62
Scan	50 × 373	12	806	142	19.98
Faults	471362	16	699	123	21.45
Errors	272472	24	596	105	22.88
X's (%)	1.56	32	568	100	22.98
Tests	566	50	578	102	21.81
FC (%)	98.10				
Circuit	**C1–d2**	8	892	252	13.91
Scan	50 × 373	12	654	185	17.01
Faults	471362	16	542	153	18.94
Errors	276906	24	425	120	21.35
X's (%)	2.62	32	397	112	21.71
Tests	354	50	378	107	21.32
FC (%)	98.93				
Circuit	**C1–d3**	8	909	311	11.90
Scan	50 × 373	12	645	221	15.10
Faults	471362	16	512	175	17.41
Errors	313775	24	405	139	19.68
X's (%)	3.45	32	355	122	20.78
Tests	292	50	338	116	20.44
FC (%)	98.98				
Circuit	**C2–d3**	7	98	12.8	13.46
Scan	16 × 112	8	82	10.7	13.49
Faults	81540	12	79	10.3	13.10
Errors	27634	14	75	9.8	12.95
X's (%)	2.60	16	71	9.3	12.81
Tests	765	18	68	8.9	12.66
FC (%)	87.42				
Circuit	**C3.1–d2**	12	516	24	99.61
Scan	128 × 353	16	440	21	101.45
Faults	1147100	24	341	16	103.29
Errors	1458974	32	294	14	103.10
X's (%)	0.04	64	275	13	95.94
Tests	2126	128	275	13	83.18
FC (%)	98.83				
Circuit	**C3.2–d2**	13	535	25	122.25
Scan	160 × 283	16	425	20	126.24
Faults	1147164	24	296	14	129.49
Errors	1499807	32	256	12	128.32
X's (%)	0.04	80	226	11	112.77
Tests	2129	160	211	10	93.00
FC (%)	98.83				

5. By solving linear equations in the order determined in step 2, confirm the desired gating signals for successive scan chains until the first encoding failure.
6. Using the selector network, determine the values of all gating signals that were not the subject of encoding, and then find the resultant fault coverage. Drop detected faults and store the number of test patterns that were effectively used to arrive with this fault coverage.

Repeat steps 1 – 6 until all target faults are detected.

Experimental results are gathered in Tables 4 and 5. For each circuit the following information is provided:

- the name, where label -d*k* indicates the use of depth-*k* sequential patterns,
- the scan architecture and the total number of faults,
- the total number of error bits, i.e., the number of scan cells that capture erroneous signals,
- the X-fill rate computed as a ratio of the total number of captured X states to the number of scan cells multiplied by the number of test patterns,
- the number of patterns which contribute to the fault coverage (FC) assuming that there is no compaction,
- the size *m* of the mask register,
- top-up patterns reported here as absolute and relative numbers in columns IPC (increase in pattern count),
- the effective compaction ratio; since a single-output compactor is used, the compaction is given as the number of scan chains normalized by the ratio of original test patterns to the total number of patterns effectively applied, i.e., those including top-up vectors; in addition a selector control data is also included.

Circuits reported in Tables 4 and 5 feature a wide range of X-fill rates starting from 0.001% (C6) and getting close to 5% (C4). Consequently, the resultant increase in a pattern count significantly varies from less than 1% for circuits with a low X-fill rate (C6) up to as much as 300%, if a design sees a high percentages of X's (C1 and C4). Furthermore, it appears that sites at which unknown states are captured as well as frequency of their occurrence may play a crucial role. We have observed, for instance, that X states populate majority of scan chains in design C1-d3 in a uniform manner across all test patterns. Contrary to this phenomenon, there are only a few patterns with high concentration of X states in design C4-d0. In this case, the majority of patterns has low X-fill rates or do not feature unknown state at all. As a result, design C1-d3 with depth-3 sequential patterns and an 8-bit selector (which gives, on the average, full controllability of 16% of scan chains) needs four times more test patterns than in a no-compaction mode. On the other hand, circuit C4-d0 (here a 12-bit selector provides similar scan chain controllability) requires a 1.3x pattern count increase despite a higher X-fill rate than that of design C1-d3.

All experiments were run by using several values of *m*, starting from the smallest one required by a given scan chain configuration. For all circuits the optimal compaction is achieved for m being roughly 10-20% of the number of scan chains. Possible gains due to larger registers clearly diminish because of necessary control data. Circuits with low X-fill rates (C6.1-d0, C6.2-d0) achieve the best results for the smallest register determined by the scan chain configuration.

Table 5. Experimental results – II

		m	IPC	IPC (%)	Comp. (x)
Circuit	**C4–d0**	11	2623	133	33.34
Scan	80 × 357	12	2575	130	33.60
Faults	677010	16	2161	109	36.56
Errors	476949	24	1240	63	46.05
X's (%)	4.94	32	994	50	48.84
Tests	1975	48	972	49	47.26
FC (%)	88.75	80	907	46	44.79
Circuit	**C5.1–d2**	11	811	63	48.68
Scan	80 × 1081	12	750	58	50.09
Faults	2558220	16	727	56	50.48
Errors	2381823	24	657	51	51.91
X's (%)	0.44	32	639	49	52.01
Tests	1294	48	591	46	52.58
FC (%)	98.91	80	640	49	49.84
Circuit	**C5.2–d2**	13	1260	96	79.58
Scan	160 × 541	16	1061	81	85.80
Faults	2558380	24	865	66	92.22
Errors	2432380	32	805	62	93.51
X's (%)	0.44	40	748	57	94.78
Tests	1308	80	744	57	88.85
FC (%)	98.91	160	691	53	80.80
Circuit	**C6.1–d0**	11	21	0.22	78.90
Scan	80 × 940	12	22	0.23	78.81
Faults	1836531	16	16	0.17	78.53
Errors	1681671	24	15	0.16	77.88
X's (%)	0.001	32	17	0.18	77.23
Tests	9436	48	17	0.18	75.98
FC (%)	96.51	80	15	0.16	73.61
Circuit	**C6.2–d0**	13	112	1.19	153.87
Scan	160 × 470	16	111	1.18	152.93
Faults	1836691	24	111	1.18	150.46
Errors	476949	32	65	0.69	148.78
X's (%)	0.001	80	40	0.42	136.15
Tests	9435	160	39	0.41	118.87
FC (%)	96.51				
Circuit	**C7–d0**	12	90	8.4	99.29
Scan	122 × 138	16	60	5.6	99.74
Faults	279175	24	26	2.4	99.21
Errors	227449	32	12	1.1	96.37
X's (%)	0.60	64	7	0.7	82.71
Tests	1076	122	11	1.0	64.47
FC (%)	98.86				
Circuit	**C7–d2**	12	118	13.0	99.29
Scan	122 × 138	16	87	9.6	99.74
Faults	279175	24	43	4.8	99.21
Errors	305343	32	25	2.8	96.37
X's (%)	1.05	64	7	0.77	82.71
Tests	905	122	4	0.44	64.47
FC (%)	98.85				

5. CONCLUSIONS

The paper presents a new a programmable scan chains selector to be used with a space compactor. It provides very good observability of scan errors even for a very large percentage of X states in test responses. The proposed solution is also very efficient in terms of silicon area and the amount of information required to control it. An extensive set of experimental results obtained on industrial designs indicate that a 12 to 32-bit register is sufficient to control scan chain selection for an entire scan test pattern in designs with tens of thousands of scan cells.

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