Lab 1 : Introduction To Quartus II Design Software

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Group 30

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Preface:

- As the first lab to the course, this lab serves as an introduction to using virtual logic softwares like Quartus II and giving leeway to understand operating the Altera board.
- In this lab we intend to derive logic equations and truth tables from the given logic circuit below.
- Using the pre-lab the logic circuit below is to be re-simulated and compiled in the Quartus II software. Given the output from the software, it must be compared with the output given from the pre-lab. The results should be matching to ensure the lab was performed successfully with minimal errors.

Lab Objectives:

- To initiate the students who are not familiar with the Altera Quartus II Design Software and the Altera FPGA based DE2-115 platform.
- To understand the basics of the Altera environment.
- To design a simple logic circuit and capture its logic diagram using the Graphic Editor.
- To compile, simulate, debug, and test their design.

Required Equipment:

- Quartus II Software

Part I:

Logic Diagram Presentation:

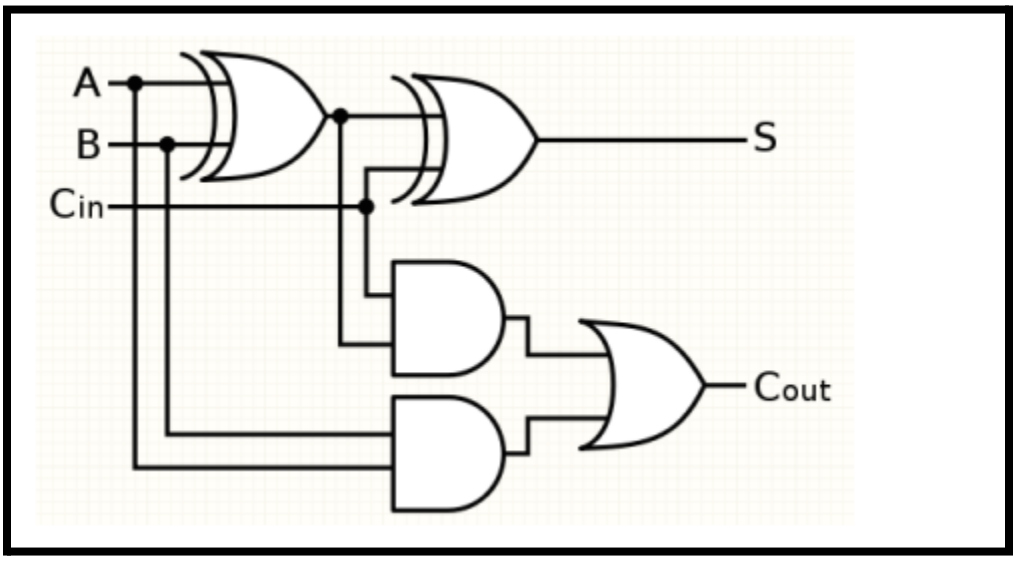

Figure 1

Truth Table (Theoretical - Obtained from pre-lab)

A	B	Cin	A + B	A * B	Sum	Cout
0	0	0	0	0	0	0
0	0	1	0	0	1	0
0	1	0	1	0	1	0
0	1	1	1	0	0	1
1	0	0	1	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	1
1	1	1	0	1	1	1

Table 1

Prelab Derived Equations:

$S = ((A \oplus B) \oplus C)$
$Cout = ((A \oplus B) * (Cin) \oplus (A * B)$

Logic Circuit (Created in Quartus II - Simulation)

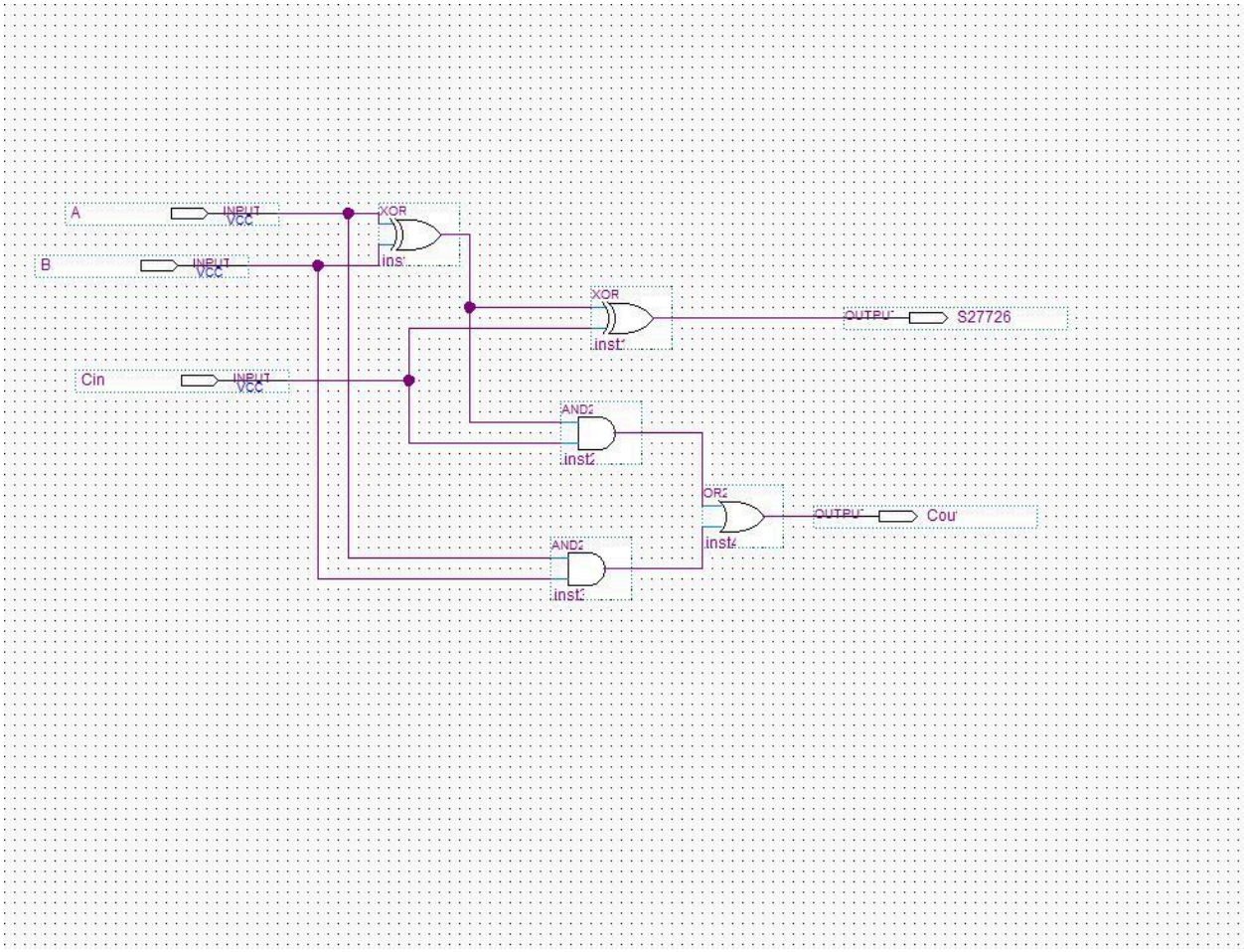

Figure 2

Simulation WVF

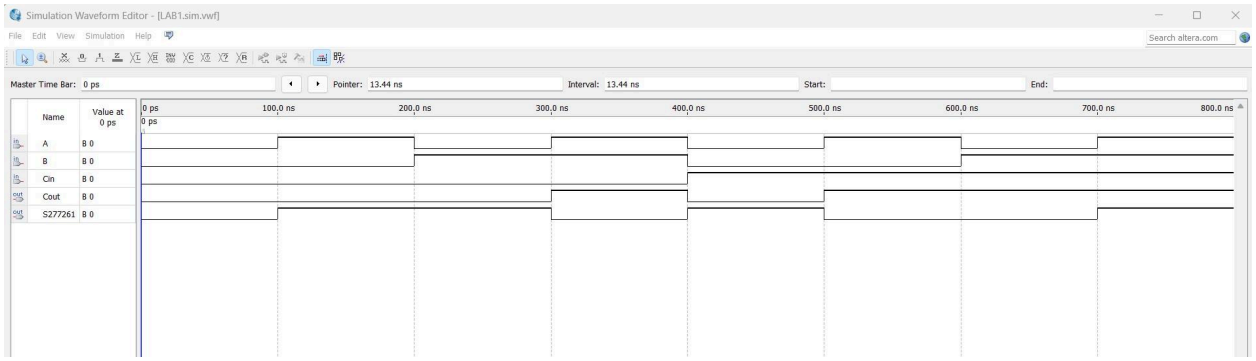

Figure 3

Simulation WVF

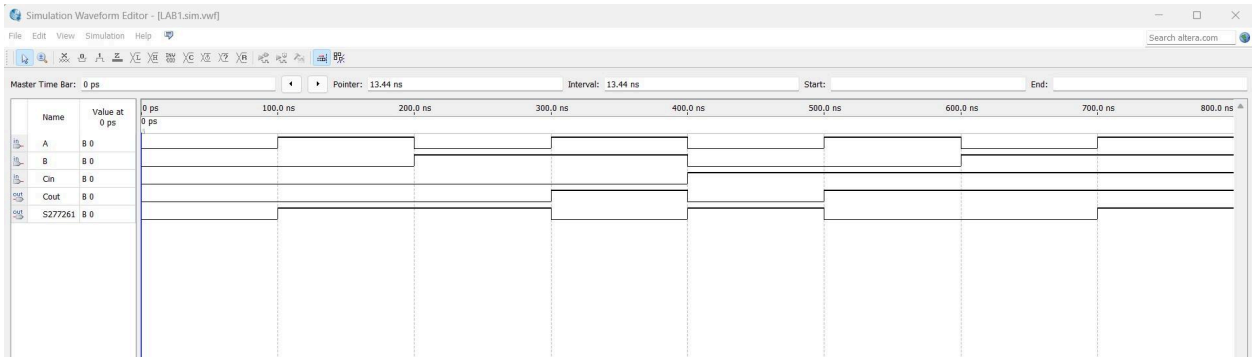

Figure 4

Simulated Output (WVF)

A	B	Cin	Cout	Sum
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

Table 2

Comparison - (S)imulated V (T)heoretical

A	B	Cin	Sum (T)	Cout (T)	Sum (S)	Cout (S)
0	0	0	0	0	0	0
0	0	1	1	0	0	1
0	1	0	1	0	0	1
0	1	1	0	1	1	0
1	0	0	1	0	0	0
1	0	1	0	1	1	0
1	1	0	0	1	1	0
1	1	1	1	1	1	1

Table 3

Discussion:

As seen above in **Fig. 2**, the truth table that was given is the exact same as the simulated. Cout and Sum both have the same values, proving that this lab was successful. The boolean algebra laws explained above are correct in this case as the experimental values equal the simulated values. By making the simulation and the logic diagram on Quartus II, these results correctly match with the theoretical result(s).

Conclusion:

Hence, the goal of the lab, which focused on the introduction to Quartus and simulating a circuit on an Altera FPGA-based DE2-115, was successful, as the given truth table matched exactly with the experimental results.