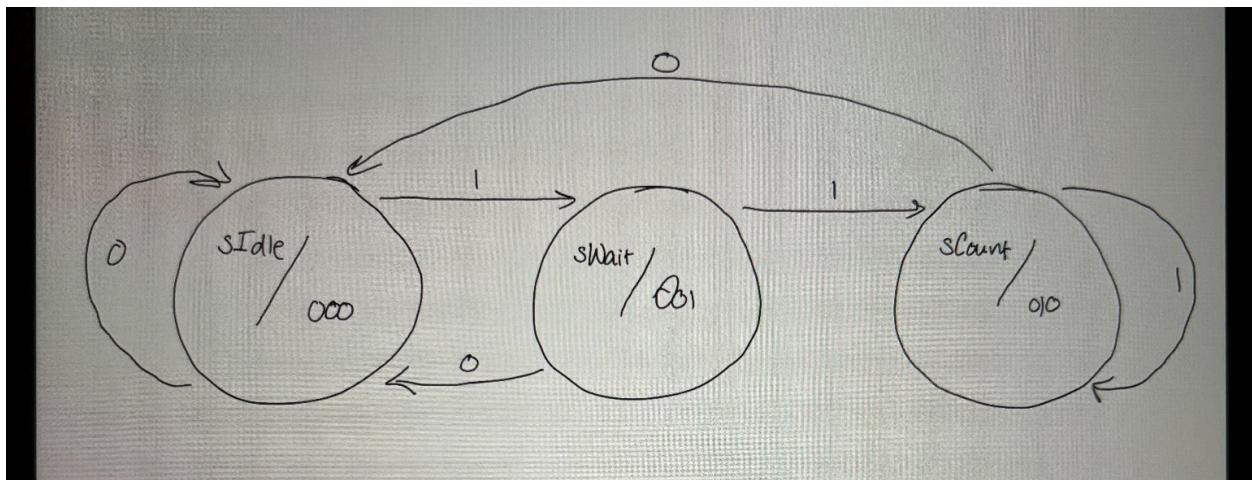


## 1. Testing reaction time

For this task, I made a VHDL file in order to define the timer entity and create a Moore state machine. The state machine's purpose was to manage the timing and the outputs for the simulation. For this, I had to define the clock, reset, start, and react inputs, and the cycle and led outputs. After this was done, I created a testbench file in order to run the simulation with GHDL and GtkWave.

This state machine only had 3 states, which were defined as sIdle, sWait, and sCount. The testbench file had a few functions, like creating a stimulus for all the inputs, and keeping track of the outputs.



## Acknowledgements

I got help from youtube videos online and I also worked with Kamalani Enomoto.