AN70707

EZ-USB® FX3™/FX3S™ Hardware Design Guidelines and Schematic Checklist

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Associated Project: No

Associated Part Family: CYUSB3014, CYUSB3035

Software Version: N/A

Related Application Notes: None

AN70707 discusses recommended practices for EZ-USB® FX3™/FX3S™ hardware design and the critical items that a developer must consider. The Cypress EZ-USB FX3 is the next generation USB 3.0 peripheral controller. With its highly integrated and flexible features, developers can add USB 3.0 functionality to any system. All recommendations apply to FX3 and FX3S, unless specifically mentioned otherwise.

Contents

Introduction

Cypress's EZ-USB® FX3™ is the next-generation USB 3.0 peripheral controller, providing integrated and flexible features. FX3 has a fully-configurable, parallel, general programmable interface called GPIF II, which can connect to any processor, ASIC, or FPGA. It provides easy and glueless connectivity to popular interfaces, such as asynchronous SRAM, asynchronous and synchronous address data multiplexed interfaces, and parallel ATA. FX3 has an embedded 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications. It implements an architecture that enables 375-MBps data transfer from GPIF II to the USB interface.

An integrated USB 2.0 OTG controller enables applications in which FX3 may serve dual roles; for example, FX3 may function as an OTG Host to MSC as well as HID-class devices. FX3 contains 512 KB or 256 KB of on-chip SRAM for code and data. FX3 also provides interfaces to connect to serial peripherals such as UART, SPI, I²C, and I²S. FX3 comes with application development tools. The software development kit comes with application examples for accelerating time to market.

In addition to these features, FX3S has an integrated storage controller and can support up to two independent mass storage devices. It can support SD 3.0 and eMMC 4.41 memory cards. It can also support SDIO on these ports. Feature differences between FX3 and FX3S are listed in Table 1.

You should follow several guidelines for trace width, stack up, and other layout considerations to make sure the system will perform as expected.

A reference schematic for the EZ-USB FX3 DVK is available at CYUSB3KIT-001 EZ-USB® FX3™. Please contact fx3@cypress.com for the EZ-USB FX3S DVK schematics.

Table 1. Feature Differences Between FX3 and FX3S

Feature	EZ-USB FX3	EZ-USB FX3S
GPIF	8/16/32-bit	8/16-bit
Storage ports	No	1 or 2 ports (SD3.0, eMMC4.41, SDIO3.0)
USB 3.0, USB 2.0 Device	Yes	Yes
HS-OTG	Yes	Yes
CPU	ARM9, 200 MHz	ARM9, 200 MHz
Embedded SRAM	256 KB/512 KB	256 KB/512 KB
Serial Interfaces*	I^2C, SPI, I^2S, UART	I^2C, SPI, I^2S, UART
Boot Options	I^2C, SPI, USB, GPIF-based	All FX3 boot options + eMMC-based boot options
Package	121-pin BGA, 10 x 10 mm	121-pin BGA, 10 x10 mm

*All serial interfaces might not be available under all configuration options. Refer to the pin description section in the datasheet for details.

Power System

Overview

The EZ-USB FX3 device power domains are shown in Figure 1. A description and the voltage settings on each of these domains are provided in Table 2.

Figure 1. EZ-USB FX3 Power Domains Diagram

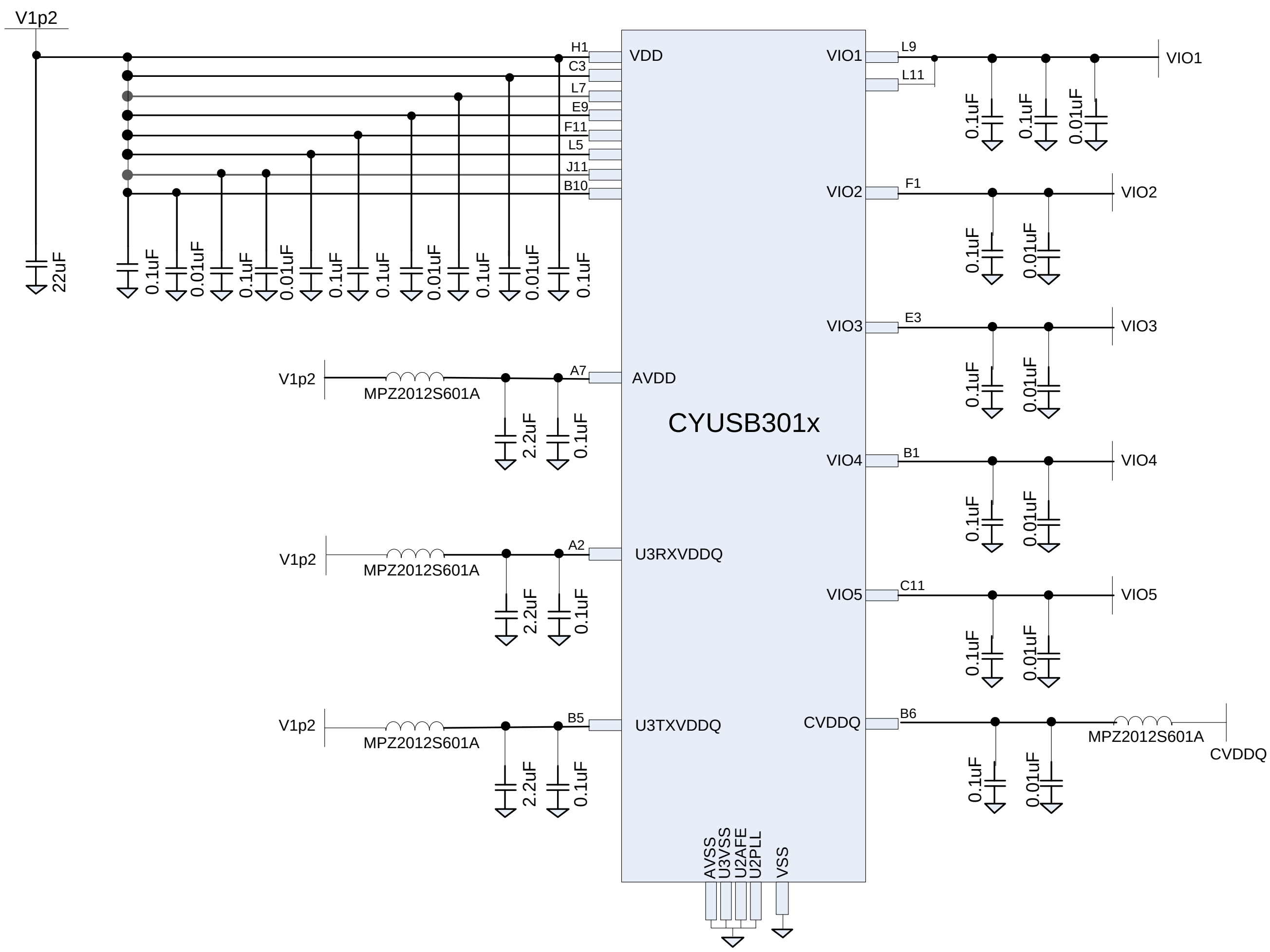


Table 2. EZ-USB FX3 Power Domains Description

Parameter	Description	Min	Typical	Max	Unit
V_{DD}	Core voltage supply	1.15	1.2	1.25	V
A_{VDD}	Analog voltage supply	1.15	1.2	1.25	V
V_{IO1}	GPIF II I/O power domain	1.7	1.8, 2.5 and 3.3	3.6	V
V_{IO2}	IO2 power domain	1.7	1.8, 2.5 and 3.3	3.6	V
V_{IO3}	IO3 power domain	1.7	1.8, 2.5 and 3.3	3.6	V
V_{IO4}	UART/SPI/I^{2}S power domain	1.7	1.8, 2.5 and 3.3	3.6	V
V_{IO5}	I^{2}C and JTAG supply domain	1.15	1.2, 1.8, 2.5 and 3.3	3.6	V
V_{BATT}	USB voltage supply	3.2	3.7	6	V

Parameter	Description	Min	Typical	Max	Unit
V_{BUS}	USB voltage supply	4.0	5	6	V
C_{VDDQ}	Clock voltage supply	1.7	1.8, 3.3	3.6	V
$U3TX_{VDDQ}$	USB 3.0 1.2 V supply	1.15	1.2	1.25	V
$U3RX_{VDDQ}$	USB 3.0 1.2 V supply	1.15	1.2	1.25	V

Power Modes

EZ-USB FX3 supports the following power modes:

Normal mode: This is the full-functional operating mode. In this mode the internal CPU clock and the internal PLLs are enabled.

- The I/O power supplies VIO2, VIO3, VIO4, and VIO5 may be turned off when the corresponding interface is not in use. VIO1 may not be turned off at any time if the GPIF II interface is used in the application.
- The USB I/O requires a 3.3-V regulated power supply. This supply is internally driven from either the VBUS or VBATT external supplies. VBATT/VBUS can be turned OFF if USB is not used. If USB port is used one or both supplies must be present.
- VBATT can be connected to the system battery or a stable 3.2 V–6 V voltage rail from the PMIC. If VBUS and VBATT are both present and in their specified ranges, VBUS becomes the primary supply to the USB I/O unless there is a software/firmware override. If VBUS is less than 4.1 V then FX3 behaves like no VBUS is connected to it. If this happens when the FX3 is powered then FX3 does not enumerate at all. If this happens somewhere during the operation of FX3 then the FX3 firmware will turn off the USB PHY and disconnect from the host.
- EZ-USB FX3 can withstand up to 6 V on the VBUS pin; in applications where this supply can see higher voltages, it is necessary to have an external overvoltage protection (OVP) device to protect the EZ-USB FX3 device. One example of such an application is a Battery Charging application, Battery Charging v1.2 Spec. In this application, the charger (such as a wall/dedicated charger) can supply up to 9 V to the VBUS.
- VBUS pin can be connected to an in-system supply rail that is switched on/off depending on VBUS detect by another processor. A typical scenario is a PMIC that detects VBUS and switches ON a regulated 3.3-V supply to EZ-USB FX3 as a result. In such a case, the system must use the software override to use VBATT as the primary supply.
- EZ-USB FX3 does not contain a charge pump and therefore, cannot source the VBUS supply when used as an OTG-A device. When EZ-USB FX3 is used in an OTG-A mode, an external charge pump, either standalone or integrated in a PMIC, must be used to power VBUS.

Suspend mode with USB 3.0 PHY enabled (L1): Power supply for the wakeup source and core power must be retained. All other power domains can be turned off/on individually.

Suspend mode with USB 3.0 PHY disabled (L2): Power supply for the wakeup source and core power must be retained. All other power domains can be turned off/on individually.

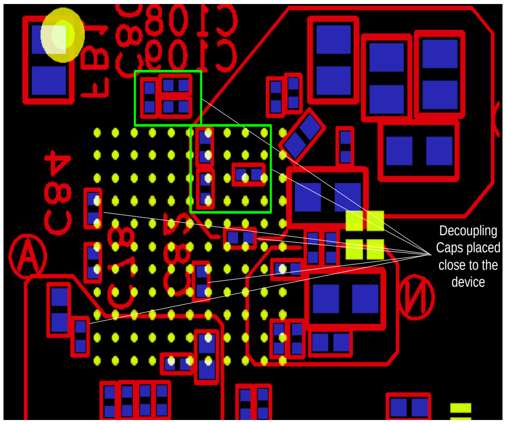
Standby mode (L3): Power supply for the wakeup source and core power must be retained. All other power domains can be turned off/on individually.

Core power down mode (L4): Core power is turned off. All other power domains can be turned off/on individually.

Device Supply Decoupling

Power supply decoupling is critical in ensuring that system noise does not propagate into the device through the power supply. Improper decoupling can lead to jittery signaling, especially on the USB bus, which results in higher CRC error rate and more retries. Decoupling capacitors should be ceramic type of a stable dielectric. It is important to have the decoupling caps as close to the power pins as possible and short trace runs for the power and ground connections on the FX3 device to solid power and ground planes. Figure 2 shows a sample of decoupling caps placement.

Figure 2. Decoupling Caps Placements



The specific recommendation for the ceramic capacitor nearest to each FX3 power pin is given in Table 3.

Table 3. Power Domain Decoupling Requirements

Power Domain (Pin Numbers)	Bulk Capacitors for Group	Decoupling Capacitors Per Pin
VDD (B10, J11)	22 µF	0.01 µF and 0.1 µF
VDD (H1, L7, F11, L5)		0.1 µF
VDD (C3, E9)		0.01 µF
AVDD (A7)	2.2 µF	0.1 µF
U3RXVDDQ (A2)	2.2 µF	0.1 µF
U3TXVDDQ (B5)	2.2 µF	0.1 µF
CVDDQ (B6)		0.01 µF and 0.1 µF
VIO1 (L9, L11)	0.01 µF	0.1 µF
VIO2 (F1)		0.01 µF and 0.1 µF
VIO3 (E3)		0.01 µF and 0.1 µF
VIO4 (B1)		0.01 µF and 0.1 µF
VIO5 (C11)		0.01 µF and 0.1 µF
VBUS (E11)		0.1 µF

Inrush Current and Power Supply Design

When the USB 3.0 Super Speed PHY is enabled for the first time, or a reset event; an initial inrush current is expected on the 1.2 V U3RXVDDQ and U3TXVDDQ supplies for ~10 us. The magnitude of this current can be as high as 800 mA. In order that this inrush current does not cause the common 1.2 V supply to droop to unacceptable levels, care must be taken in the design of the power supply network for these supplies.

If the same 1.2 V supply is also used for the VDD core supply, care must be taken to insure that the level on this supply does not fall too low, as this has the potential to trip the on-chip power-on reset (POR) circuit that will reset the entire chip. The POR circuit can fire if the 1.2-V core VDD voltage falls down to less than 0.83 V for more than 200 ns. The 1.2-V power network must be designed such that the VDD does not drop below 0.83 V when an inrush event occurs. Proper combination of decoupling capacitors (as specified in the datasheet), inductor chokes and regulator output impedance are required to make this possible.

The following example waveforms show the inrush current (Figure 4) and resultant drop in VDD levels (Figure 5) when the current spike occurs. The results were obtained from a non-optimized power supply design using TPS76801QD power regulator, 2.2-µF decoupling caps, and chokes as shown in Figure 3.

Figure 3. Non-Optimized Power Supply Design

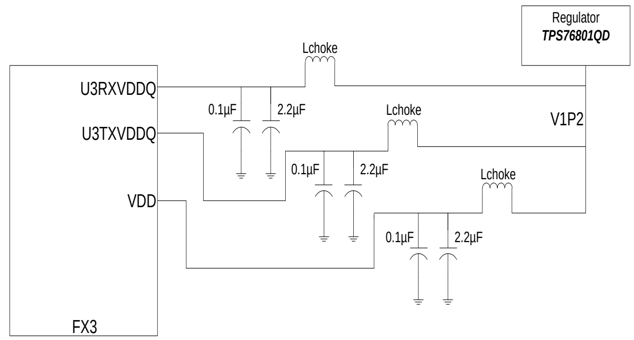


Figure 4. Inrush Current (80 mV/0.1 Ω = 800 mA)

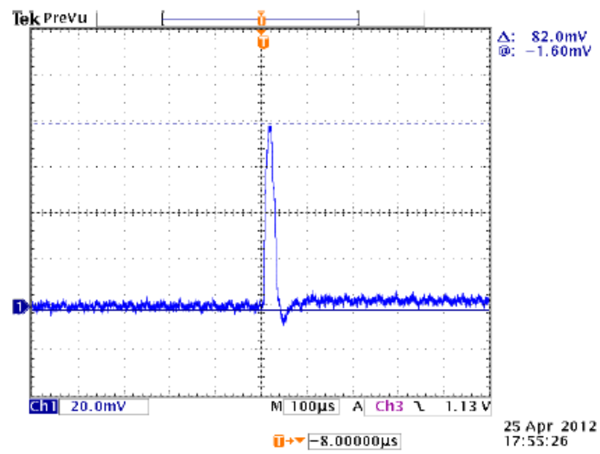
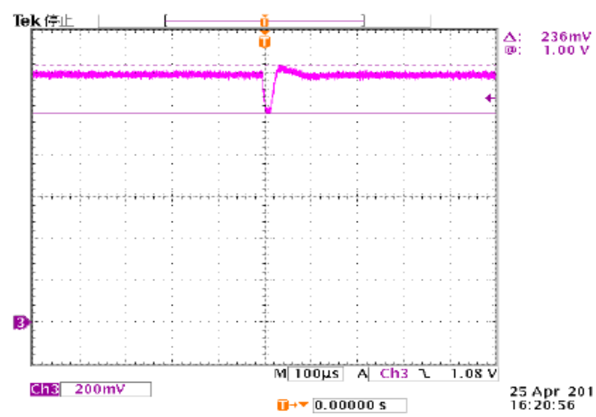


Figure 5. 1.2-V Power Domain Voltage Drop (200 mV)



In contrast, an optimized power design shown in Figure 6 below designed using the same regulator (TPS76801QD), with the modification of using a 22-µF decoupling capacitor and removing the choke from VDD supply, shows a reduction in the inrush (Figure 7) and an improvement in the power supply drop (Figure 8).

Figure 6. Optimized Power Supply Design

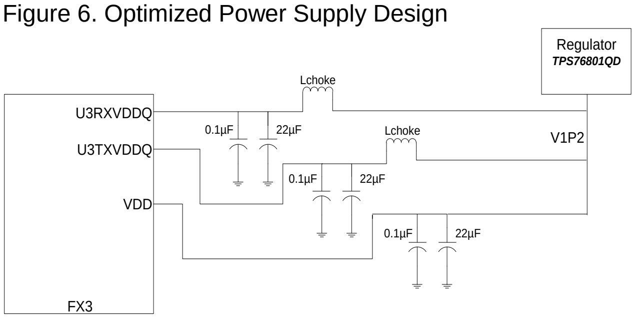


Figure 7. Inrush Current (320 mA)

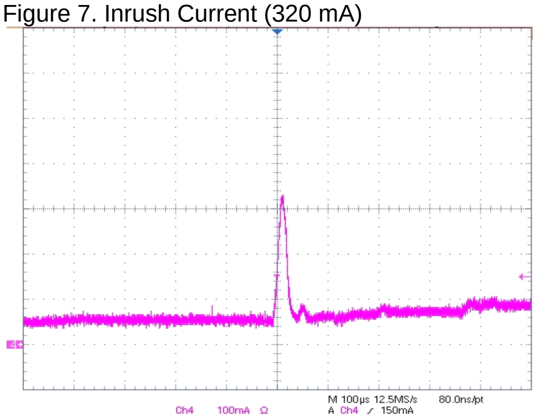
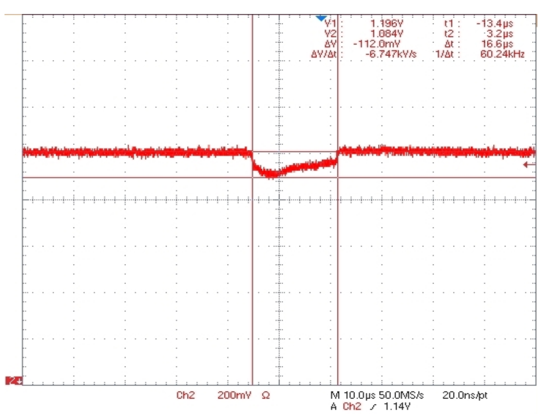


Figure 8. 1.2-V Power Domain Voltage Drop (112 mV)



Customers can choose any regulator with similar specifications.

It is always a good practice to isolate different power supplies from each other. If you are shorting IO power supplies (VIO1-5) to CVDDQ, it is always recommended to isolate CVDDQ using a choke (as shown in Figure 1). This will help in reducing the PHY errors. Also, operating VIO1 at lower voltages (1.8 V) helps in reducing the PHY errors.

Clocking

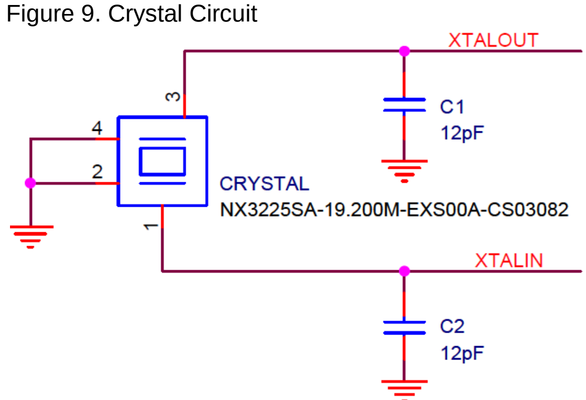
The EZ-USB FX3 device can use

1) either a 19.2-MHz crystal or
2) any of 19.2 MHz, 26 MHz 38.4 MHz, or 52 MHz clock as the clocking source.

Crystal

Figure 9 shows the connection of the crystal.

Figure 9. Crystal Circuit



The 19.2-MHz crystal requirements are listed in Table 4.

Table 4. Crystal Requirements

Parameter	Specification	Unit
Tolerance	±100	ppm
Temp Range	-40 to 85	°F
Drive level	Use Equation 1	mW

The power dissipation of the crystal depends on

1) the drive level of the XTALOUT pin (for FX3, this is 1.32 V),
2) the desired frequency (19.2 MHz), and
3) the equivalent resistance of the crystal.

Equation 1. Power dissipation of the crystal

$$P = I^2 R = \left(\frac{V_x}{|Z|}\right)^2 R$$
$$= 2[\pi f\,(C_0 + C_L)\,V_x]^2\,R$$

Where:

f is the crystal frequency,

C_0 is the shunt capacitance of the crystal obtained from the crystal data sheet,

C_L is the load capacitance, for C_L calculation, refer to the next section,

R is the crystal ESR obtained from the data sheet of the crystal,

V_x is the maximum voltage on XTALOUT pin - 1.32 V.

Use of a crystal with a drive level less than the crystal's power dissipation may result in accelerated aging or even burnout of the crystal.

Examples of compatible crystals are shown in Table 5. Note that only the NX3225SA was characterized with the EZ-USB FX3, and the rest for the crystals are provided as examples using Equation 1.

Table 5. Crystal Selection

Device	Max R1 (Ω) From Datasheet	CL eqv (pF)	C0 (pF) Estimate	Drive Level Using Equation 1 (uW)	Max Drive Level (Spec) uW
Epson FA-20H	80	11	nil	123	200
NX2520SA	60	12	nil	110	200
NX3225SA	80	9	1.26	107	200

Note Do not connect any series resistor to the XTALOUT and XTALIN pins of the crystal. Placing a series resistor will add resistance to the crystal ESR, resulting in increased crystal power dissipation and startup time.

Crystal Effective Load Capacitor Calculation

Load capacitance C_L plays a critical role in providing an accurate clock source to FX3. The capacitors C_1 and C_2 (as shown in Figure 9) must be chosen carefully based on the load capacitance value of the crystal.

The load capacitance is calculated using the following equation:

Equation 2. Load capacitance of a crystal

$$C_L = \frac{C_1 * C_2}{C_1 + C_2} + C_s$$

C_s is the stray capacitance of XTALOUT and XTALIN traces on the PCB. Usually the value of C_s is around 2-5 pF as long as you follow good layout practice and keep the trace from the crystal to the pins on the FX3 as short as possible.

For the crystal used in FX3 development kit, C_L = 9 pF. PCB C_s = 3 pF. From Equation 2, C_1 = C_2 = 12 pF.

Clock

Clock inputs to EZ-USB FX3 must meet the phase noise and jitter requirements specified in the following table.

Table 6. Clock Requirements

Parameter	Description	Specification		Units
		Min	Max	
Phase noise	100 Hz Offset	–	–75	dB
	1 kHz Offset	–	-104	dB
	10 kHz Offset.	–	-120	dB
	100 kHz Offset	–	-128	dB
	1 MHz Offset	–	-130	dB
Maximum frequency deviation		–	150	ppm
Duty cycle		30	70	%
Overshoot		–	3	%
Undershoot		–	-3	%
Rise time/fall time		–	3	ns

Based on the clocking option that is used, the frequency select, FSLC[2:0], lines can be tied to power, through a weak pull-up resistor, or to ground. Table 7 shows the values of FSLC[2:0] for the different clocking options.

Table 7. Frequency Select Configuration

FSLC[2]	FSLC[1]	FSLC[0]	Crystal/Clock Frequency
0	0	0	19.2 MHz crystal
1	0	0	19.2 MHz input clock
1	0	1	26 MHz input clock
1	1	0	38.4 MHz input clock
1	1	1	52 MHz input clock

CVDDQ supply is the supply associated with the clock input. It should be set to the same voltage level as the external clock input (if any).

If only external clock input is used, the XTALIN and XTALOUT pins can be left unconnected. If only crystal clocking is used, the CLKIN pin can be left unconnected.

Watchdog Timer

A 32.768-kHz clock input can be used for the watchdog timer operation during Standby mode. This may be optionally supplied by an external source.

Table 8. Wachdog Timer Requirements

Parameter	Min	Max	Unit
Duty Cycle	40	60	%
Frequency Deviation	-	±200	ppm

GPIF II Interface

EZ-USB FX3 offers a high-performance general programmable interface, GPIF II. This interface enables functionality similar to but more advanced than FX2LP's GPIF and Slave FIFO interfaces. Refer to the application notes AN75779 - Interfacing an Image Sensor to EZ-USB® FX3™ in a USB video class (UVC) Framework , for more details on the GPIF interface.

Following are some general design guidelines for the EZ-USB FX3's GPIF II interface.

- The maximum frequency of the GPIF II interface is 100 MHz. It is recommended that all lines on the GPIF II bus should be length matched within 500 mils. We also recommend using 22-Ω series termination resistors to avoid reflection on these lines.
- If the GPIF lines are to be routed for more than 5 inches or routed through a medium, which can cause impedance mismatch, we recommend doing signal integrity simulation using the EZ-USB FX3 IBIS model, available at CYUSB3KIT-001 EZ-USB® FX3™ and come up with a termination.
- GPIO[16] (PCLK) should be used as the GPIF II clock signal in all synchronous interfaces.
- GPIO[32:30] (PMODE[2:0]) signals should be configured appropriately at FX3 boot-up. After boot-up, these signals can be used as GPIOs.
- INT# signal cannot be used as a GPIO. This pin can be either left floating or pulled up to VIO1 if it is not used.

Note SPI interface lines are not available when GPIF II is configured in 32-bit mode. It is possible to use SPI interface for booting when GPIF II is configured in 32-bit mode.

I^2C Interface

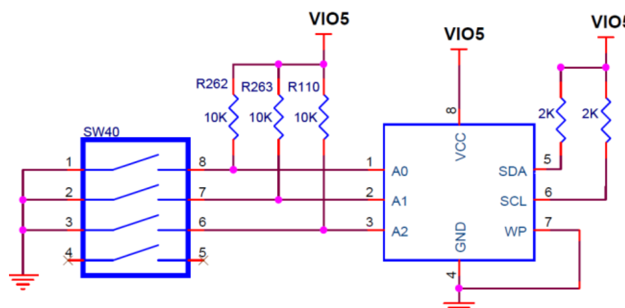
EZ-USB FX3 has an I^2C interface compatible with the I^2C Bus Specification Revision 3. EZ-USB FX3's I^2C interface is capable of operating as I^2C Master only. For example, EZ-USB FX3 may boot from an EEPROM connected to the I^2C interface, as a selectable boot option. EZ-USB FX3's I^2C Master Controller also supports the multi-master mode functionality.

The power supply for the I^2C interface is VIO5, which is a separate power domain from the other serial peripherals. This is to allow the I^2C interface the flexibility to operate at a different voltage than the other serial interfaces.

The bus frequencies supported by the I^2C controller are 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V; the operating frequencies supported are 400 kHz and 1 MHz.

If an external EEPROM is used on the I^2C bus for firmware image booting, 2-kΩ pull-up resistors should be placed on the SCL and SDA lines for proper operation as shown in the following figure.

Figure 10. I^2C Configuration



Note Address pins A0, A1 and A2 of the EEPROM should be connected per the recommendations in the EEPROM datasheet.

Low-Performance Peripherals (LPP)

JTAG

EZ-USB FX3 has a JTAG interface to provide a standard five-pin interface for connecting to a JTAG debugger. This feature enables the debugging of the firmware through the CPU core's on-chip debug circuitry.

There is no need for external pull up/down on the JTAG signals as the JTAG signals TDI, TMC, TRST# have fixed 50 kΩ internal pull-ups and the TCK signal has a fixed 10 kΩ pull-down resistor.

Please note that the FX3/FX3S does not support boundary scan. The JTAG interface available in these devices is for debugging purpose only.

I^{2}S

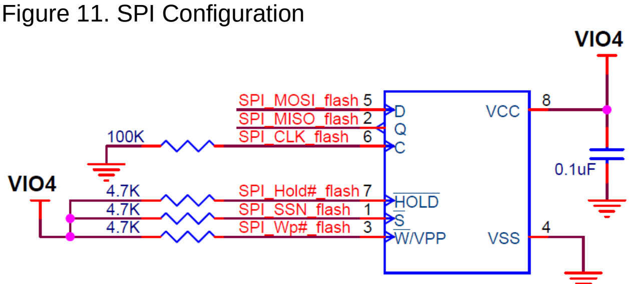
EZ-USB FX3 has an I^{2}S port to support external audio codec devices. EZ-USB FX3 functions as an I^{2}S master (**transmitter only**). EZ-USB FX3 can generate the system clock as an output on the I2S_MCLK line or accept an external system clock input on the same line.

SPI and UART

EZ-USB FX3 supports an SPI master interface on the serial peripherals port. The SPI GPIOs are shared with the UART GPIOs. There should be no pull-up or pull-down on MOSI and MISO signals.

Figure 11 shows the correct SPI signal connection using the M25P40-VMN6TPB SPI device.

Figure 11. SPI Configuration



Selection of SPI Flash

Use the following guidelines while selecting the SPI flash.

- Flash size: 1 Kbit to 32 Mbit in size are supported.
- Voltage: 1.7 V – 3.6 V are supported.
- Command set: SPI flash should support the following commands to support FX3 boot.
  - Read data: 03h with 3 byte addressing
  - Read Status register: 05h
  - Write Enable: 06h
  - Write data (Page Program): 02h
  - Sector Erase: D8h

An SPI flash can be used for FX3 boot as long as the read commands match. If there are any differences in the write commands, then programming of that SPI flash will not be successful with the provided CyBootProgrammer.img (located at *C:\Program Files (x86)\Cypress\Cypress USBSuite\application\c_sharp\ controlcenter*); it requires changing the SPI write commands used in the USBFlashProg example project of the FX3 SDK. The image file resulted after building the modified USBFlashProg project should replace the provided CyBootProgrammer.img (with the same name) for successful programming of the SPI flash.

Booting

EZ-USB FX3 can be either the main processor in a system or a co-processor to another main processor. The booting option you use depends on the specific system implementation. PMODE[2:0] configures the boot option and can be connected directly to the main processor or hardwired on the board depending on the booting option that will be used. The following table shows the levels of the PMODE[2:0] signals required for the different booting options.

Table 9. PMODE Signals Setting

PMODE[2:0]	Boot from
Z00	Sync ADMUX (16-bit)
Z01	Async ADMUX (16-bit)
Z11	USB boot
Z0Z	Async SRAM (16-bit)
Z1Z	I^{2}C, on failure, USB boot is enabled
1ZZ	I^{2}C only
0Z1	SPI, on failure, USB boot is enabled
000*	S0-port (eMMC). On failure, USB boot is enabled – FX3S only
100*	S0-port (eMMC) – FX3S only

Note Z = HI-Z, Open drain, No connect, *Applies to FX3S only

We recommend adding pull-up and pull-down options (using 10 KΩ) on the PMODE [2:0] signals and load the combination needed for preferred booting option. This will give the flexibility to debug the system during early development.

EMI and ESD Considerations

You must consider EMI and ESD on a case-by-case basis relative to the product enclosure, deployment environment, and regulatory statutes. This application note does not give specific recommendations regarding EMI, EZ-USB FX3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. EZ-USB FX3 can tolerate reasonable EMI, which is conducted by the aggressor, outlined by these specifications and continue to function as expected. However this application note gives general EMI and ESD considerations. Refer to Appendix A – PCB Layout Tips for general information on PCB layout techniques. You can also refer ‘Appendix A: PCB Layout Tips of AN61290 - PSoC® 3 and PSoC 5 Hardware Design Considerations’, which has a list of layout tips to improve EMI/EMC and also have reference books on this topic.

EZ-USB FX3 has built-in ESD protection on the D+, D-, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

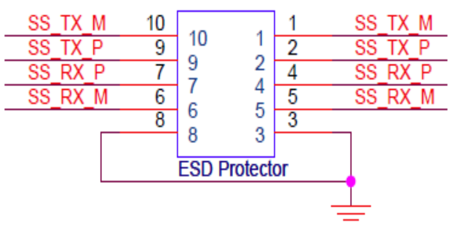
- ±2.2-kV human body model (HBM) based on ±6-kV Contact Discharge and ±8-kV Air Gap Discharge based on IEC61000-4-2 level 3A
- ±8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device will continue to function after ESD events up to the levels stated.

The SSRX+, SSRX-, SSTX+, SSTX- pins have only up to ±2.2-kV human body model (HBM) internal ESD protection.

You can include additional protection to these pins by using high performance, low capacitance external ESD devices (SP3010-04UTG), as shown in Figure 12. To prevent an effect on the performance of this bus, the added capacitance should not exceed 0.5 pF.

Figure 12. Low Capacitance External USB SuperSpeed (SS) ESD Protection



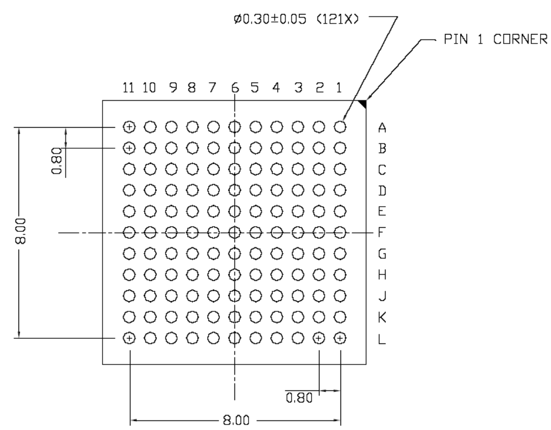
In terms of EMI, all signal and clock traces emit electromagnetic (EM) radiation when they switch from one level to another. To meet the various standards in different countries, these emissions must be minimized. You can use several techniques to lower EM emissions:

- Consider putting the power and ground planes as the outside layers with signal layers underneath.
- Always have solid copper fills beneath integrated circuits and clocks.
- Ensure an adequate ground return path for all signals.
- Minimize the trace length of high speed, high current traces.

FX3 Device Package Dimensions

EZ-USB FX3 is packaged on a 10 x 10 mm, 0.8 mm pitch ball grid array (BGA). The recommended pad size is 0.241 mm (9.5 mil).

Figure 13. EZ-USB FX3 Package Dimension



Electrical Design Consideration

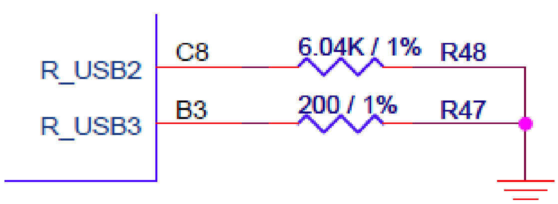
USB 3.0 protocol enhances USB speed up to 5 Gbps. By including SuperSpeed (SS) lines along with High Speed (HS) lines, it is backward compatible with the USB 2.0 specification. Both buses require a greater level of attention to electrical design. Careful attention to component selection, supply decoupling, signal line impedance, and noise are required when designing for SuperSpeed USB. These physical issues are mostly affected by the PCB design. Refer to Appendix A – PCB Layout Tips for general information on PCB layout techniques.

USB 3.0 SuperSpeed Design Guidelines

EZ-USB FX3 has SuperSpeed USB lines and High-Speed USB lines. Use the following best practices when designing with these busses:

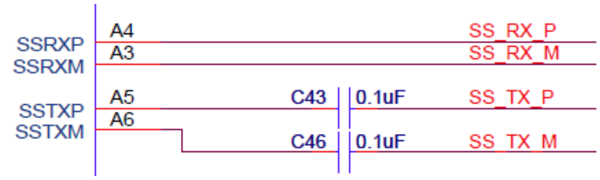
- Minimize the trace length of USB lines as much as possible (<3 inches). These should be routed first to make sure certain recommendations on this list are achievable. Long traces affect the transmitter quality and introduce intersymbol interference (ISI) on the receive side.
- The polarity can be swapped on the USB 3.0 differential pairs. Polarity detection is done automatically by the USB 3.0 PHY during link training, as define in the USB 3.0 specification section 6.4.2, and does not require any additional changes to device Firmware. Given the different USB connectors pin-out, the polarity inversion mechanism can be utilized to ensure that USB traces do not cross each other.
- Tie the R_USB2 pin to ground through a 1% 6.04-kΩ precision resistor. R_USB3 pin should be tied to ground through a 1% 200-Ω precision resistor.

Figure 14. USB2 and USB3 Reference Resistors



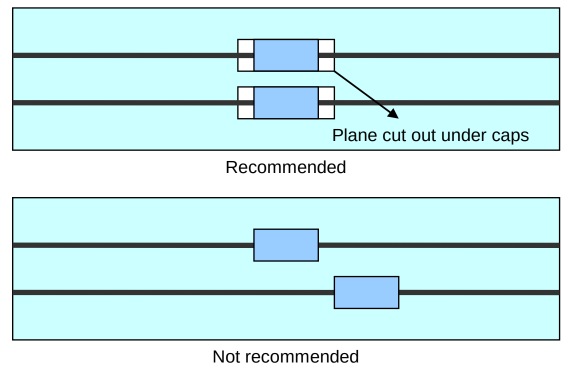
- USB 3.0 traces require additional AC coupling capacitors (0.1 µF) placed on the SS_TX lines. Place these capacitors symmetrically and close to the EZ-USB FX3 device.

Figure 15. SuperSpeed TX Line Decoupling Caps



- At least one immediate plane underneath these AC coupling capacitors should have a cut out in the shape of these capacitors to avoid extra capacitance on the lines because of the capacitor pads. Figure 16 shows the proper layout of the decoupling caps.

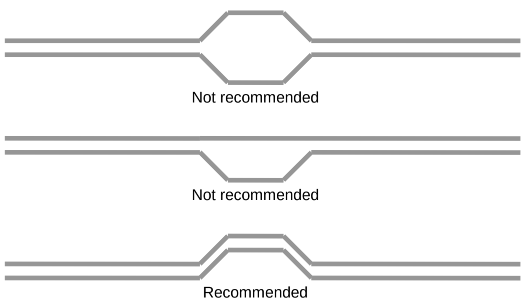
Figure 16. SuperSpeed TX decoupling Caps Layout



- Keep the USB signal line impedance at 90 Ω differential (±7%).
- Fill the space between the two differential pairs with ground. Maintain a minimum of $2W$ space between the ground and the differential pairs, where W = trace width.
- Keep the crystal trace as short as possible. Place the crystal within 2 cm from FX3.
- Do not place any Hi-Speed signal trace near to the crystal. If needed due to space constraints, fill the space with ground.
- Place the capacitor used in the RC reset circuitry as close as possible to the reset pin of FX3.
- Use split planes on the power layer for different power domains.
- Keep the power traces away from Hi-Speed data and clock lines.
- Power trace widths should be ≥25 mils to reduce inductance.
- Keep power traces as short as possible. Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.

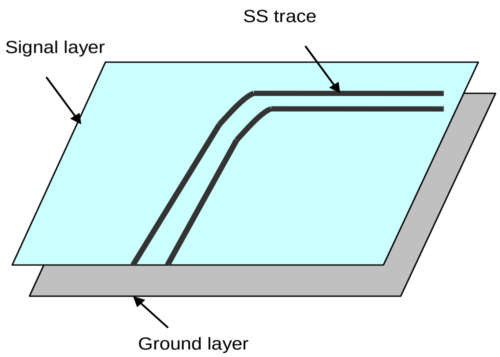
- Avoid any split in the immediate plane under the USB lines. The presence of split under the USB trace will result in variation of characteristic impedance at that point.
- Keep trace spacing between differential pairs consistent to avoid impedance mismatches as shown in the following figure.

Figure 17. Differential Pairs Impedance Matching Techniques



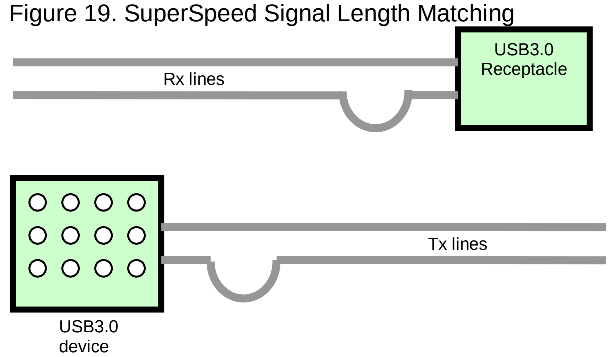
- All SS signal lines should be routed entirely over a solid ground plane on an adjacent layer. Splitting the ground plane underneath the SS signals increases loop inductance, introduces impedance mismatches and increases electrical emissions. Figure 18 shows a solid ground plain under the SuperSpeed signal.

Figure 18. Solid Ground Plain under the SuperSpeed Signal



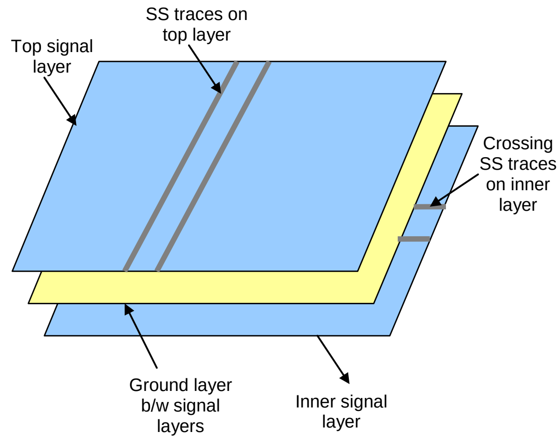
- Differential SS pair trace lengths should be matched within 0.12 mm (5 mils). The HS D+ and D– signal trace lengths should be matched within 1.25 mm (50 mils). Adjustment for HS signals should be made near the USB receptacle, if necessary. Adjustments for SS Rx signals should be made near the USB receptacle, while adjustments for SS Tx signals should be made near the device, if necessary. An example for length matching for the SuperSpeed signal is shown in Figure 19.

Figure 19. SuperSpeed Signal Length Matching



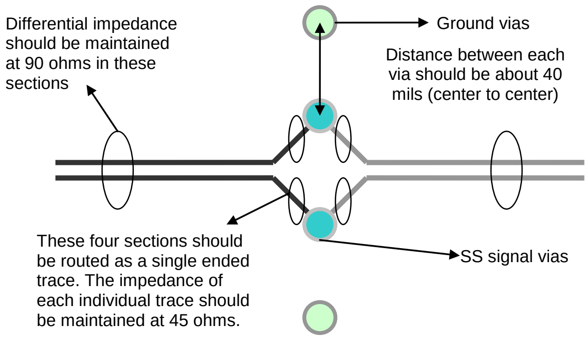
- The number of layers on the PCB should at least be four. To maintain 90 Ω differential impedance, use a solid reference power plane.
- Any time two pairs of USB traces cross each other in different layers, a ground layer should run all the way between the two USB signal layers as illustrated in Figure 20.

Figure 20. Ground Insertion



- If signal routing has to be changed to another layer, continuous grounding has to be maintained to ensure uniform impedance throughout. To achieve this, ground vias should be placed next to signal vias as shown in Figure 21. The distance between the signal and ground vias should be at least 40 mils.

Figure 21. Ground Vias



- Maintain constant trace width in differential pairs to avoid impedance mismatches as shown in following figure.

Figure 22. Differential Pairs Placements

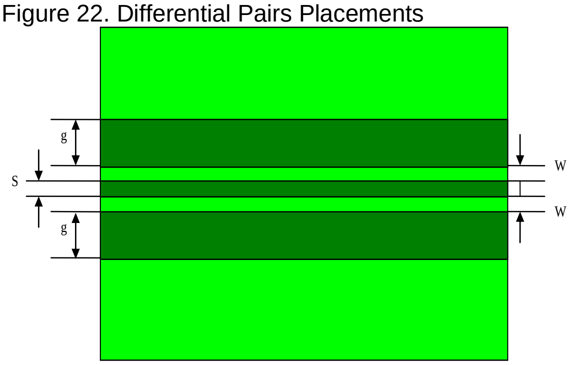


Table 10 defines the recommended parameters mentioned in the previous figure.

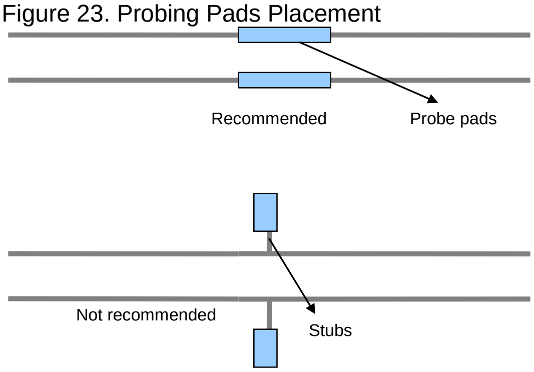
Table 10. USB Traces Specification

S	Intra pair spacing	8 mils
W	Trace width	11 mils
g	Minimum gap b/w trace and other planes	8 mils

However, variation in the above values could be ignored if the lines have a characteristic impedance of 90 Ω.

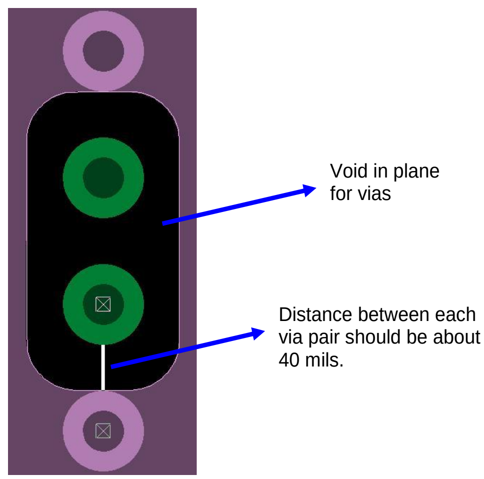
- Avoid stubs on all USB lines. If pads are needed on the lines for probing purposes, they should not extend out of the trace in the form of a stub. An illustration is shown in Figure 23.

Figure 23. Probing Pads Placement



- Void for vias on the SS signal lines should be common for the differential pair. Having a common void, as shown in figure, maintains better impedance matching in comparison to separate vias.

Figure 24. Void Vias Placement For SS Traces



- Because the Micro B receptacle is a surface mount receptacle, the USB signals can be routed entirely on the same layer as the EZ-USB FX3 device and the USB 3.0 Micro B receptacle, as shown in the Figure 25. In addition, the layout is shown in Figure 26.

Figure 25. Micro-B receptacle Placement

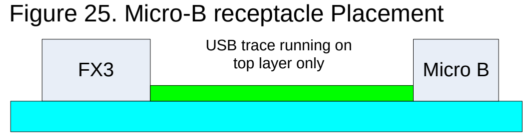
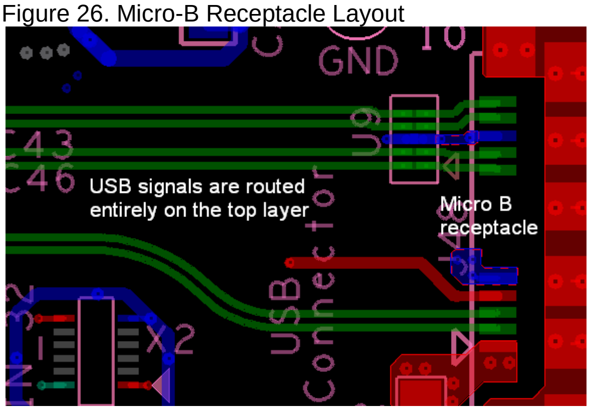


Figure 26. Micro-B Receptacle Layout



- It is highly recommended that, when using a standard B receptacle (through hole receptacle), the USB signal lines be connected to the receptacle pins on the opposite layer of where the receptacle is placed as shown in Figure 27and Figure 28. For example, if the standard B receptacle is placed on the top layer, the signal lines should connect to the receptacle pins on the bottom layer. This prevents the unnecessary stubs due to the USB receptacle pins. A diagram of the recommended layout versus the stub producing layout is illustrated in details in Figure 29 and Figure 30 respectively. To avoid introduction of vias, the EZ-USB FX3 device can be placed on the opposite layer of the standard B receptacle. In this case, the USB traces can be routed entirely on the same layer.

Figure 27. Standard-B Receptacle Placement

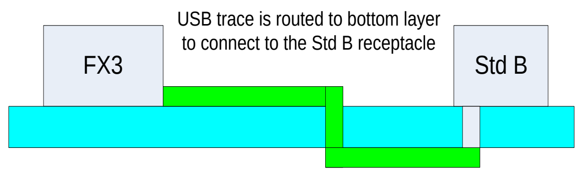
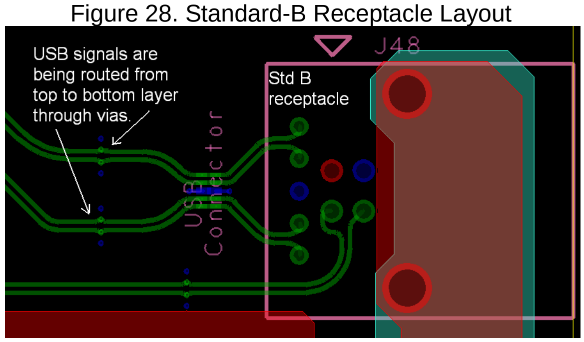


Figure 28. Standard-B Receptacle Layout



Both routing schemes mentioned earlier are tested to work at SS trace length of up to three inches.

Figure 29. USB Signals Connected on the Opposite Side of the Standard Type-B USB Receptacle

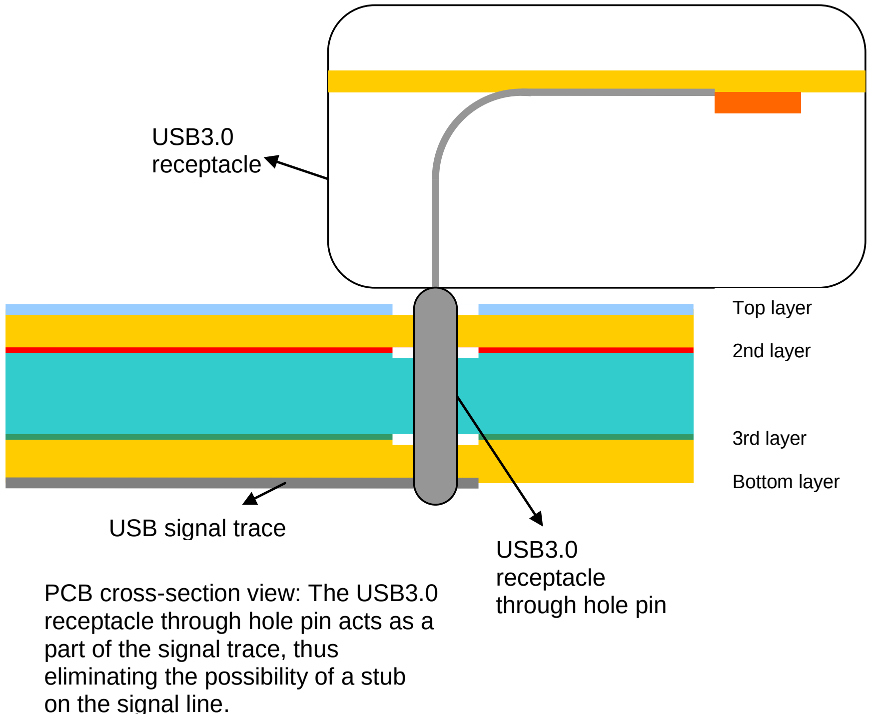
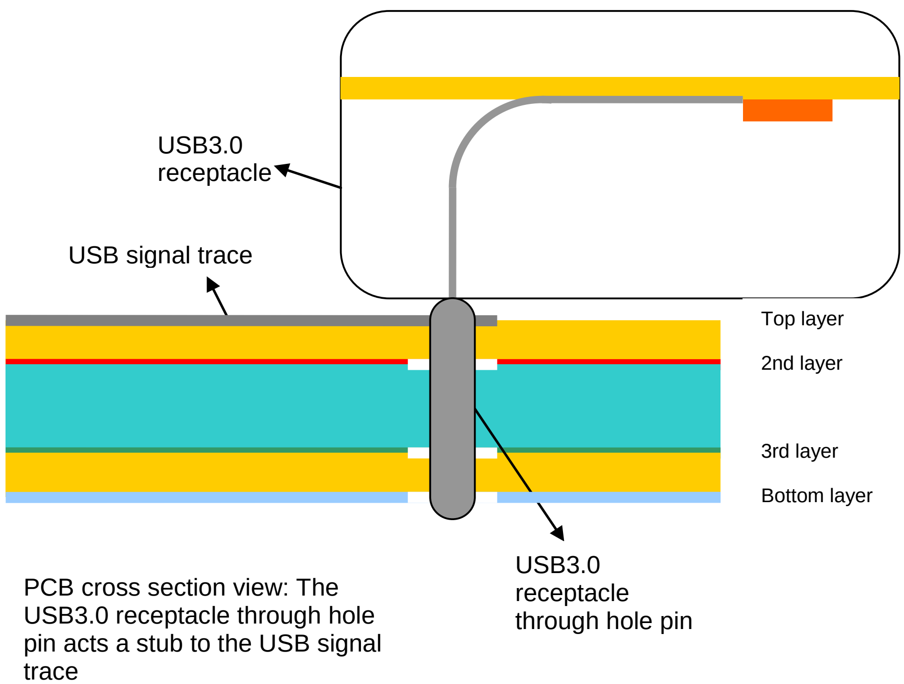
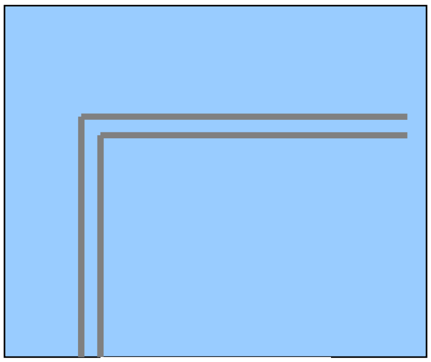


Figure 30. USB Signals Connected on the Same Side of the Standard Type-B USB Receptacle

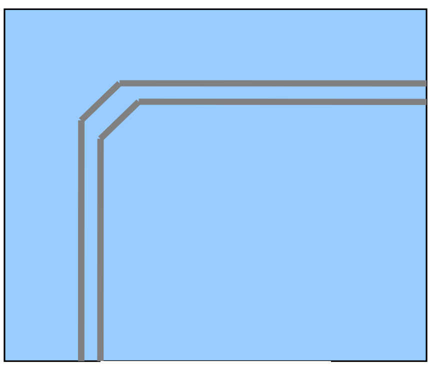


- Connect the "shield" pins on the USB 3.0 receptacle to ground through an LC circuit for AC isolation.
- On the USB signal lines, use as few bends as possible. Do not use a 90-degree bend. Use 45 degrees or rounded (curved) bends if necessary. An illustration is shown in Figure 31.

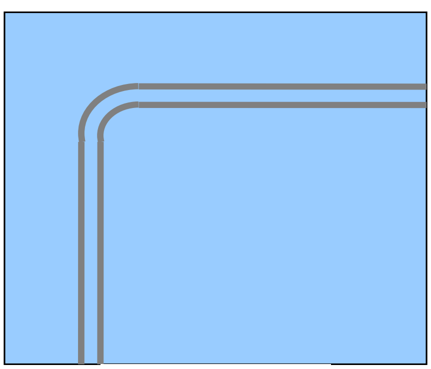
Figure 31. USB Signal Bends



Not recommended



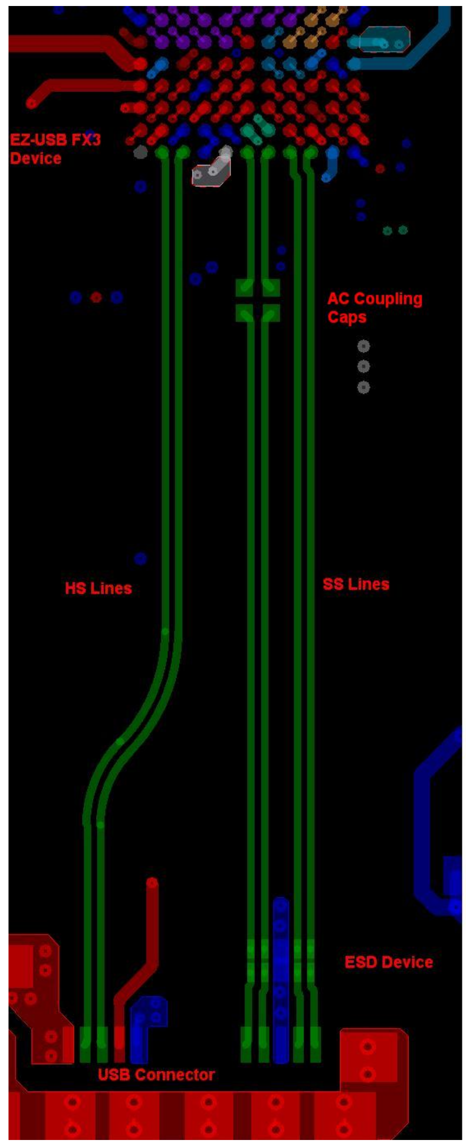
Recommended



Recommended

- To avoid cross talk, do not place the differential pairs close to other differential pairs, clock signals, or any other high-speed signals.
- Figure 32 shows an example of routing the USB signals from the EZ-USB FX3 device to the USB 3.0 Micro B receptacle. Each differential pair should be kept uniform throughout the trace. Place AC coupling caps as close to the device as possible. ESD devices should be placed as close to the receptacle as possible.

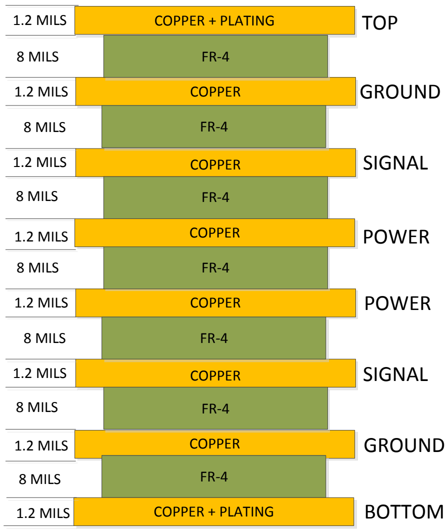
Figure 32. USB Signals Layout Example



8-Layer PCB Example

Figure 33 shows the layers present in the layout of FX3 development kit.

Figure 33. Stackup Details



FX3S Hardware Design Considerations

This section is specific only to EZ-USB FX3S. You need to consider the following guidelines in addition to the FX3 hardware design guidelines.

S-Port Interface

EZ-USB FX3S has two independent storage ports (S0-port and S1-port). Both storage ports support the following:

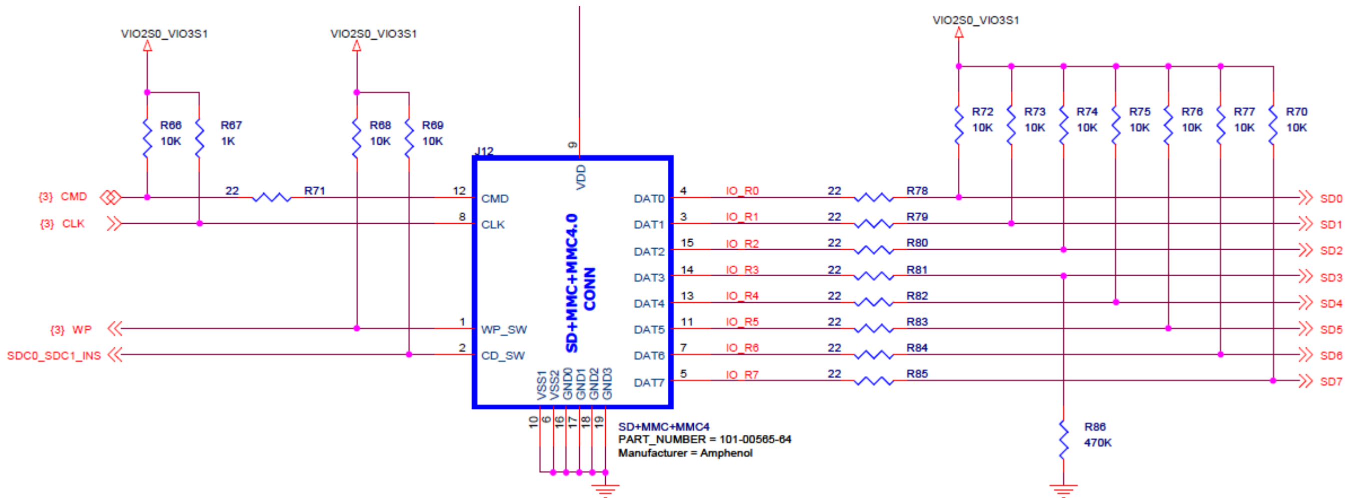
- MMC-system specification, MMCA Technical Committee, Version 4.4
- SD specification Version, 3.0
- SDIO host controller compliant with SDIO specification Version 2.00 (Jan 30, 2007)

To satisfy the requirements of these specifications, the following guidelines should be followed while designing the storage port circuitry on an EZ-USB FX3S system PCB.

- All data lines, command, and clock lines should be length-matched.
- The trace lengths should be at least 3.2 inches and not more than 5 inches. These numbers are calculated based on the worst-case timing parameters for SD cards, eMMC devices, and the EZ-USB FX3S device and should be taken only as a recommendation.
- In the case of SD card, the V_{DD} should be tied to 3.3 V regardless of the I/O voltage used on the other SD lines, as illustrated in Figure 34.
- In case of an eMMC device, VCC should be tied to 3.3 V and VCC should be tied to the port I/O voltage supply (VIO2 or VIO3). Figure 35 shows an eMMC device circuit.
- Add a 10-kΩ pull-up resistor to the SD data signals, except for SD_D3, which is used as one of the card insertion's detect mechanism. A 470 kΩ is used to pull down SD_DQ3. SD_CLK is pulled up using only a 1-kΩ resistor.
- SD card voltage supply (VIO2 or VIO3) should be changed to 1.8 V dynamically when UHS-I memory card is used.
- Card insertion and removal detection is provided using the following mechanisms:
  - SD-D3 data line: SD cards have an internal 10-kΩ pull-up resistor. When you insert or remove the card from the SD/MMC connector, the voltage level at the SD_D3 pin changes and triggers an interrupt to the CPU. Note that older generations of MMC cards do not support this card detection mechanism.
  - S0/S1_INS pin: Some SD/MMC connectors facilitate a micro switch for card insertion and removal detection. This micro switch can be connected to S0/S1_INS. When you insert or remove the card from the SD/MMC connector, it turns the micro switch on and off. This changes the voltage level at the pin that triggers the interrupt to the CPU. Note that this S0/S1_INS pin is shared between the two S-Ports. Register configuration determines which port gets to use this pin. This pin is mapped to the VIO3 power domain; if VIO2 and VIO3 are at different voltage levels, this pin cannot be used as S1_INS. The insertion/removal detection mechanism is not used for eMMC devices because the devices are usually soldered on the board and do not involve insertion/removal detection.

The following figures show different implementation of the SD/MMC cards and eMMC devices.

Figure 34. SD/MMC Card Circuit

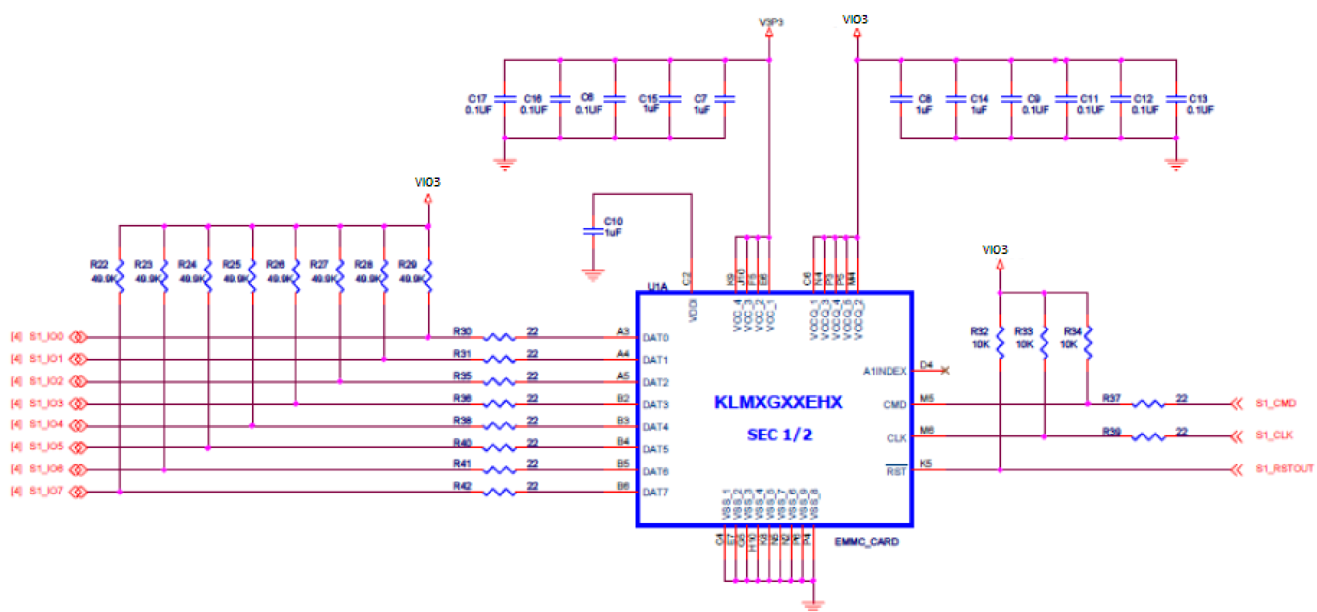


Note

1. VIO2S0_VIO3S1 – VIO2S0 or VIO3S1

   This voltage supply can be either VIO2 or VIO3 based on the place where you connect the storage daughter card. It will be VIO2 if you are connecting the storage daughter card to S0 port, VIO3 if you are connecting the storage daughter card to S1 port.
2. When SD card is connected to S1 port then some of the serial interfaces are not available. Refer to pin description section in FXS datasheet for details.

Figure 35. eMMC Device



Schematics and Layout Review Checklist

Table 11 is a checklist for all the important guidelines. Provide an answer to each checklist item to find out the extent to which your hardware design meets these guidelines.

Table 11. Schematics and Layout Review Checklist

Sl. No	Schematic checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors connected as per Table 3?	
2	Does the crystal meet the specification in this application note?	
3	Are the ferrite beads connected on AVDD, U3TXVDD, U3RXVDD, and CVDD?	
4	Do the Power-on-Reset RC components meet the minimum reset time (1 ms)?	
5	Do the USB precision resistors have 1% tolerance?	
6	Are the I^2C lines provided with pull-up resistors to the VIO5 domain?	
7	Does the USB port shield terminated properly?	
8	Do the SuperSpeed USB lines have ESD device connected?	
9	Do the GPIF lines have 22-Ω series resistor connected?	
10	Are the PMODE lines connected per Table 9?	
11	Does the SPI flash meet the specification in this application note?	
12	Did you make sure that the JTAG lines don't have pull up resistors?	
Sl. No	**Layout Checklist**	**Answer (Yes/No/NA)**
1	Is the crystal placed close to the chip (less than 2 cm)?	
2	Are the decoupling capacitors and bulk capacitors placed close to the FX3 power pins?	
3	Are the clock traces routed away from the high speed data lines and the power lines?	
4	Are the power traces routed away from the high speed data lines and the clock lines?	
5	Is the capacitor in the RC reset circuitry placed close to the reset pin of FX3?	
6	Are the USB SS and HS signal lines have 90ohm differential impedance?	
7	Are the USB SS and HS signal lines matched in length?	
8	Are the USB data lines provided with solid ground plane underneath?	
9	Are the SS traces provided with the guard traces along the USB data trace with stitching vias?	
10	Are the SS traces provided with the AC decoupling capacitors (0.1 µF) on the TX lines?	
11	Are the USB traces kept as short as possible?	
12	Is it ensured that there are no stubs on all the USB traces?	
13	Is it ensured that there are no vias on the SS traces?	
14	Do the USB traces have few bends and no 90-degree bends?	
15	Do the two planes underneath the AC coupling capacitors have cut in shape of the capacitor?	
16	Is it ensured that SS and HS USB traces are routed with consistent trace spacing?	

Appendix A – PCB Layout Tips

There are many classic techniques for designing PCBs for low noise and EMC. Some of these techniques include:

- **Multiple layers:** Although they are more expensive, it is best to use a multi-layer PCB with separate layers dedicated to the V_{SS} and V_{DD} supplies. This gives good decoupling and shielding effects. Separate fills on these layers should be provided for V_{SSA}, V_{SSD}, V_{DDA}, and V_{DDD}.

  To reduce cost, a 2-layer or even a single-layer PCB can be used. In that case you must have a good layout for all V_{SS} and V_{DD}.

- **Component Position:** You should separate the different circuits on the PCB according to their electromagnetic interference (EMI) contribution. This will help reduce cross-coupling on the PCB. For example, you should separate noisy high current circuits, low voltage circuits, and digital components.

- **Ground and Power Supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using 2-layer or single-layer PCBs.

  The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI.

- **Decoupling:** The standard decoupler for external power is a 100 µF capacitor. Supplementary 0.1 µF capacitors should be placed as close as possible to the V_{SS} and V_{DD} pins of the device, to reduce high frequency power supply ripple.

  Generally, you should decouple all sensitive or noisy signals to improve electromagnetic compatibility (EMC) performance. Decoupling can be both capacitive and inductive.

- **Signal Routing:** When designing an application, the following areas should be closely studied to improve EMC performance:
  - Noisy signals, for example signals with fast edge times
  - Sensitive and high impedance signals
  - Signals that capture events, such as interrupts and strobe signals

To increase EMC performance, keep the trace lengths as short as possible and isolate the traces with V_{SS} traces. To avoid crosstalk, do not route them near to or parallel to other noisy and sensitive traces.

References

For more information, several references are available:

- The Circuit Designer's Companion, Second Edition, (EDN Series for Design Engineers) by Tim Williams
- PCB Design for Real-World EMI Control (The Springer International Series in Engineering and Computer Science), by Bruce R. Archambeault and James Drewniak
- Printed Circuits Handbook (McGraw Hill Handbooks), by Clyde Coombs
- Emc and the Printed Circuit Board: Design, Theory, and Layout Made Simple, by Mark I. Montrose
- Signal Integrity Issues and Printed Circuit Board Design, by Douglas Brooks

Document History

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Document Number: 001-70707

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3312933	HFO	07/14/2011	New application note.
*A	3381402	MRKA	09/23/2011	Updated trace adjustment diagram. Updated via void diagram. Updated AC coupling capacitors diagram.
*B	3490652	MRKA	01/11/2011	Added 'Schematic design checklist' before the recommendations Added GPIF II Interface section Updated decoupling capacitor recommendation table Changed heading of the package detail section to 'FX3 Package Dimensions' Updated USB signal routing schemes using standard and micro B receptacles
*C	3729135	ROSM	09/18/2012	Replaced the "F" symbol in the Booting section with High-Z Added Crystal and Clock specification and added a list of compatible crystals Added Inrush Consideration and Power Supply Design section Added decoupling cap placement sample Added values for termination resistors Added ESD part number and placement example Updated the loading capacitance requirements for the external USB 3.0 ESD Added Links to schematic and IBIS model Added the location of USB3.0 Polarity Inversion section in the USB 3.0 Spec Added GPIF example Application Notes numbers Added I2C, SPI/UART, I2S Consideration Added Images and tables numbers Added table of Content section Changed the VBUS min to 4.0 V Changed to standby mode support for the 32.768 kHz clock input Added Appendix A
*D	3765036	OSG	10/03/2012	Updated Figure 21 Title
*E	3824291	ROSM	11/28/2012	Updated cap value column in Table 2 Updated VBUS/VBATT description
*F	3889052	RSKV	1/28/2013	Modified to cover details of FX3S Changed title to include FX3S Added Table 1 Figure 12 is modified Added FX3S hardware design considerations section
*G	4320320	RSKV	04/11/2014	Figure 1 is modified to show the decoupling capacitors connected to each pin Table 3 is modified Crystal section is modified Section for selecting SPI flash for FX3 boot is added Figure 33 is added to show the stackup details of FX3 DVK Schematics and Layout Review Checklist is added

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