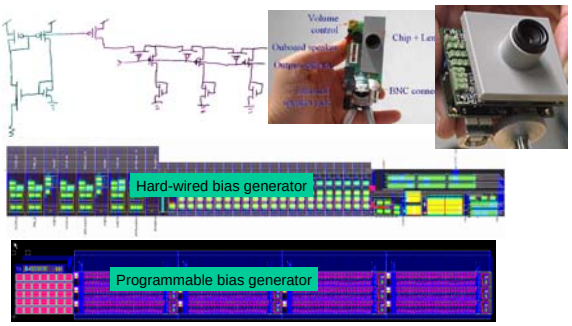
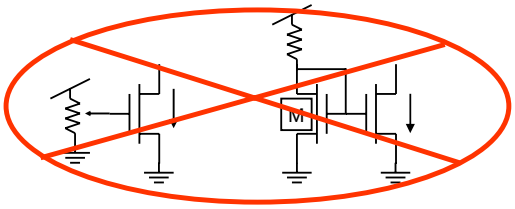
ABC's of Bias Generators



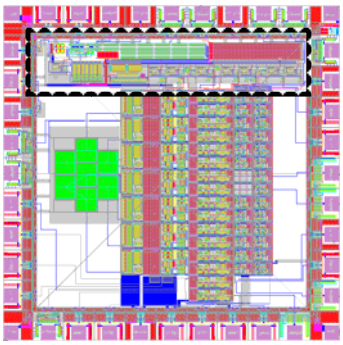
jaer.wiki.sourceforge.net/biasgen

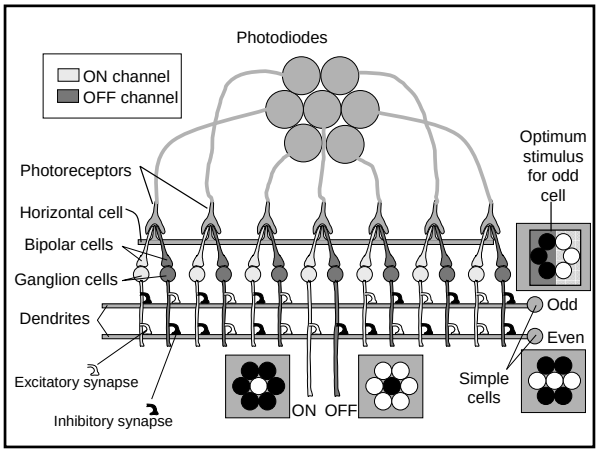
Neuromorphic chips often use a very wide range of dynamics (6+ decades), spanning mA to pA (V/ns to V/s). Historically, the required bias currents in experimental chips have been specified by schemes like these:



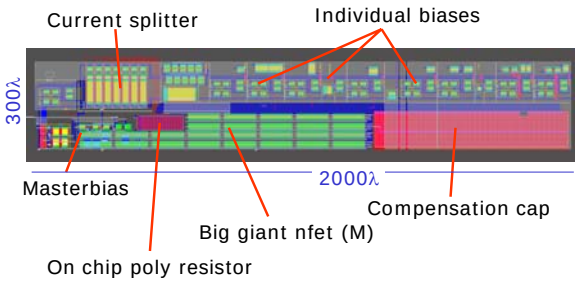
These methods are NOT manufacturable. Each chip needs custom adjustment. You don't know that your chip can actually be built in quantity. Users are hard to support. BAD!

Chip with bias generator

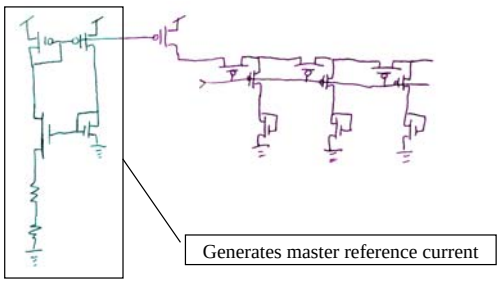




Layout



The basic idea

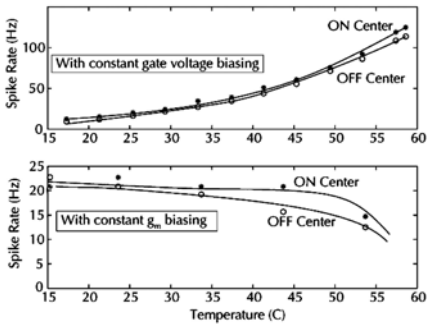


Historical development of masterbias

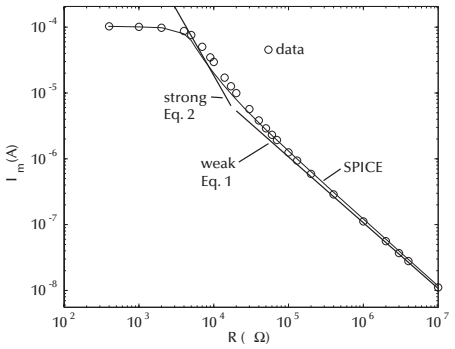
- Bob Widlar, 1960's, bipolar bootstrapped current reference

1977, LM10 opamp

Temperature effects with and without bias generator

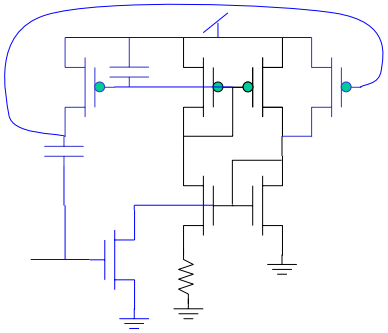


Masterbias current vs. R

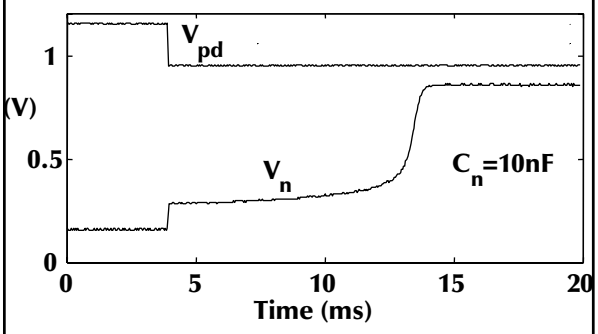


Startup circuit

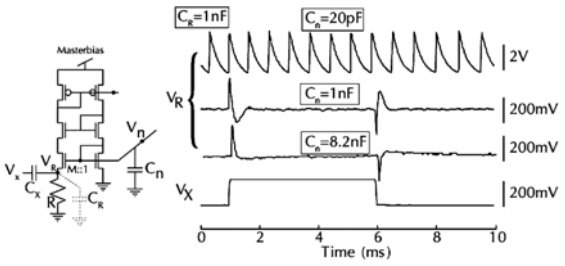
Used on commercial product (>200 million chips)



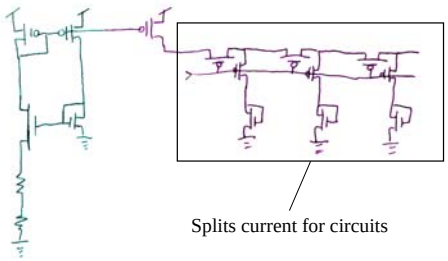
Masterbias startup

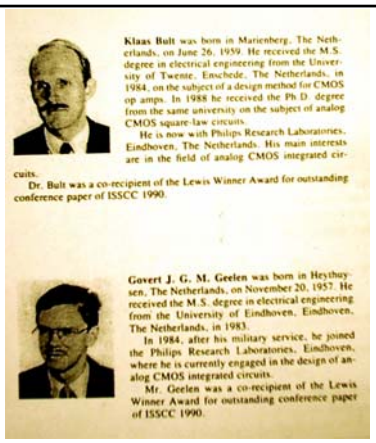


Masterbias stability



The basic idea





Klaas Bult was born in Marienberg, The Netherlands, on June 26, 1959. He received the M.S. degree in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1984, on the subject of a design method for CMOS op amps. In 1988 he received the Ph.D. degree from the same university on the subject of analog CMOS square-law circuits.

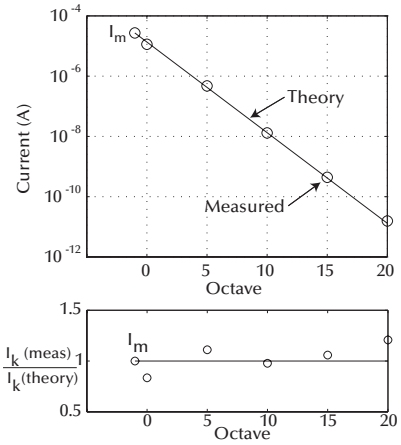
He is now with Philips Research Laboratories, Eindhoven, The Netherlands. His main interests are in the field of analog CMOS integrated circuits.

Dr. Bult was a co-recipient of the Lewis Winner Award for outstanding conference paper of ISSCC 1990.

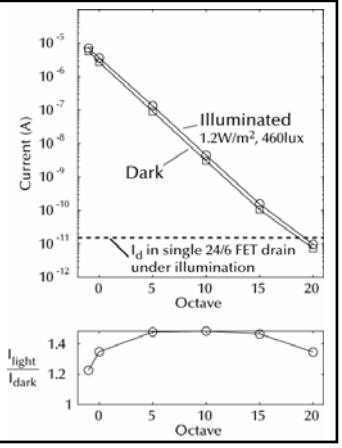
Govert J. G. M. Geelen was born in Heythuysen, The Netherlands, on November 20, 1957. He received the M.S. degree in electrical engineering from the University of Eindhoven, Eindhoven, The Netherlands, in 1983.

In 1984, after his military service, he joined the Philips Research Laboratories, Eindhoven, where he is currently engaged in the design of analog CMOS integrated circuits.

Mr. Geelen was a co-recipient of the Lewis Winner Award for outstanding conference paper of ISSCC 1990.

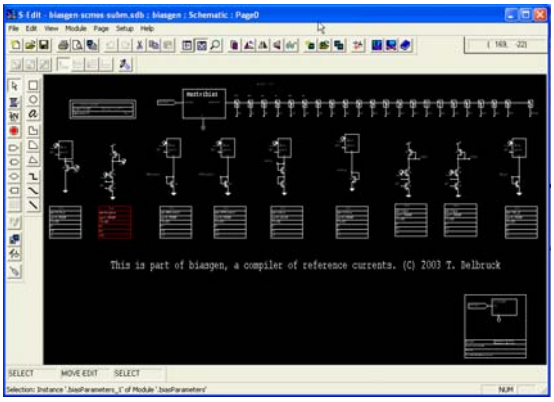


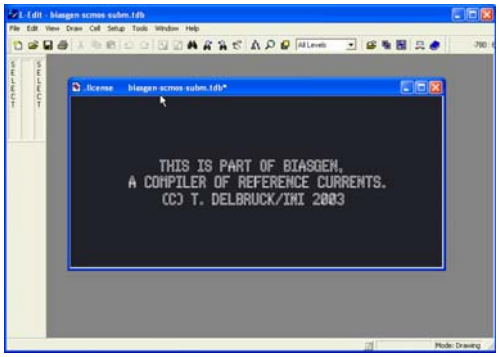
The generated currents are protected from effects of illumination

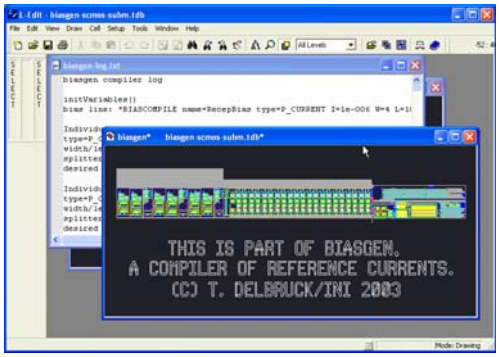


Bias current generator design kit

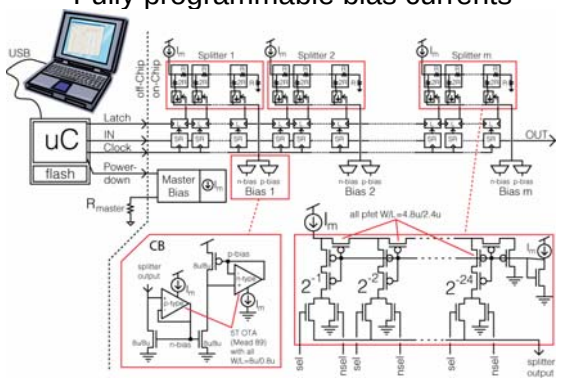
- Compiles layout for a bias generator
- For Tanner tools (L-Edit, S-Edit, L-Comp) v.10+
- Layout uses MOSIS SCMOS scalable rules
- 2 metal, single poly
- Shielded from light and minority carrier diffusion



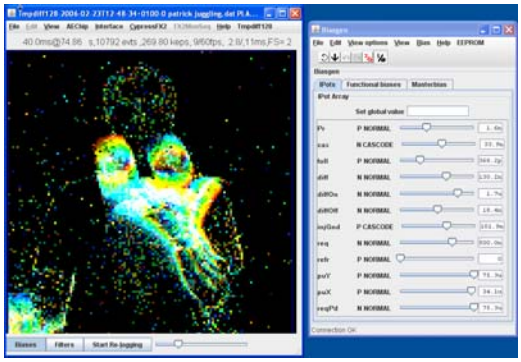




Fully programmable bias currents



As used on silicon retina



Programmable biases allow feedback control

Retina chip

Event rate measurement

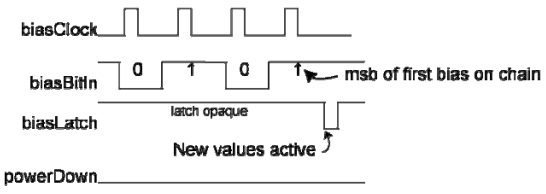
Threshold control policy

Rate low: Decrease threshold		Rate high: Increase threshold

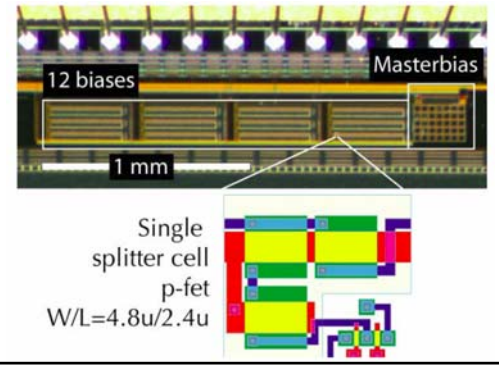
rate

Programming interface

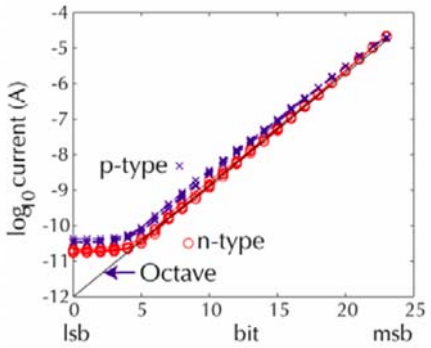
- uController loads N biases, each 24 bits, over 3-wire interface.



Each bias occupies 65% of bond pad in 0.35u process



Biases can be programmed over about 6 decades



Making chip biases

1. Gather all required biasing information for chip
2. Develop core level SPICE simulation running using bias *currents* (i.e. all gate bias voltages are generated by driving currents into diode connected transistors)
3. Build biasgen schematic from design kit, simulate chip level with biasgen
4. Run biasgen compiler to build biasgen layout from schematic
5. Integrate with core and padframe