CYUSB301X

EZ-USB® FX3 SuperSpeed USB Controller

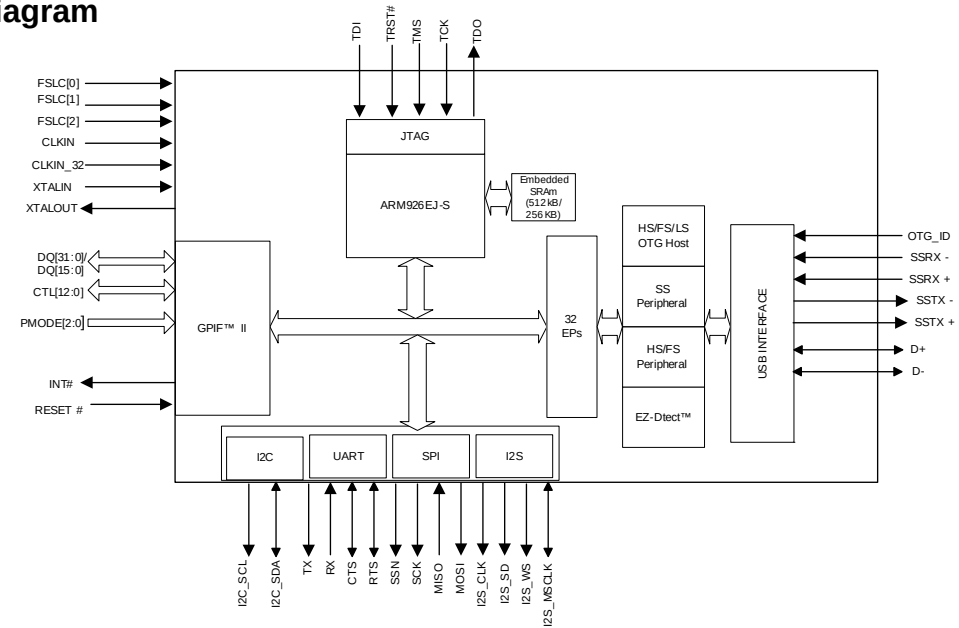
Features

- Universal serial bus (USB) integration
  - USB 3.0 and USB 2.0 peripherals compliant with USB 3.0 specification 1.0
  - 5-Gbps USB 3.0 PHY compliant with PIPE 3.0
  - High-speed On-The-Go (HS-OTG) host and peripheral compliant with OTG Supplement Version 2.0
  - Thirty-two physical endpoints
  - Support for battery charging Spec 1.1 and accessory charger adaptor (ACA) detection
- General Programmable Interface (GPIF™ II)
  - Programmable 100-MHz GPIF II enables connectivity to a wide range of external devices
  - 8-, 16-, and 32-bit data bus
  - As many as16 configurable control signals
- Fully accessible 32-bit CPU
  - ARM926EJ core with 200-MHz operation
  - 512-KB or 256-KB embedded SRAM
- Additional connectivity to the following peripherals
  - I^2C master controller at 1 MHz
  - I^2S master (transmitter only) at sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz
  - UART support of up to 4 Mbps
  - SPI master at 33 MHz
- Selectable clock input frequencies
  - 19.2, 26, 38.4, and 52 MHz
  - 19.2-MHz crystal input support
- Ultra low-power in core power-down mode
  - Less than 60 µA with V_{BATT} on and 20 µA with V_{BATT} off
- Independent power domains for core and I/O
  - Core operation at 1.2 V
  - I^2S, UART, and SPI operation at 1.8 to 3.3 V
  - I^2C operation at 1.2 V
- 10- × 10-mm, 0.8-mm pitch Pb-free ball grid array (BGA) package
- EZ-USB® software and development kit (DVK) for easy code development

Applications

- Digital video camcorders
- Digital still cameras
- Printers
- Scanners
- Video capture cards
- Test and measurement equipment
- Surveillance cameras
- Personal navigation devices
- Medical imaging devices
- Video IP phones
- Portable media players
- Industrial cameras

Logic Block Diagram



Contents

Functional Overview

Cypress's EZ-USB FX3 is the next-generation USB 3.0 peripheral controller, providing integrated and flexible features.

FX3 has a fully configurable, parallel, general programmable interface called GPIF II, which can connect to any processor, ASIC, or FPGA. GPIF II is an enhanced version of the GPIF in FX2LP, Cypress's flagship USB 2.0 product. It provides easy and glueless connectivity to popular interfaces, such as asynchronous SRAM, asynchronous and synchronous address data multiplexed interfaces, and parallel ATA.

FX3 has integrated the USB 3.0 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications. It implements an architecture that enables 375-MBps data transfer from GPIF II to the USB interface.

An integrated USB 2.0 OTG controller enables applications in which FX3 may serve dual roles; for example, EZ-USB FX3 may function as an OTG Host to MSC as well as HID-class devices.

FX3 contains 512 KB or 256 KB of on-chip SRAM (see Ordering Information on page 36) for code and data. EZ-USB FX3 also provides interfaces to connect to serial peripherals such as UART, SPI, I^2C, and I^2S.

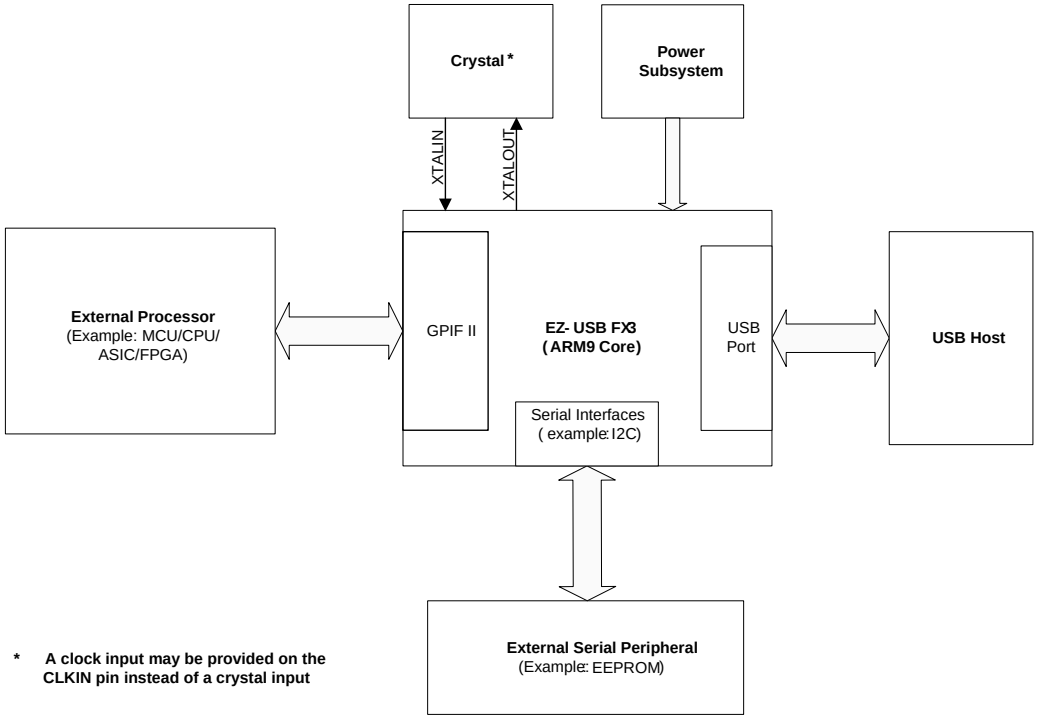
FX3 comes with application development tools. The software development kit comes with application examples for accelerating time to market.

FX3 complies with the USB 3.0 v1.0 specification and is also backward compatible with USB 2.0. It also complies with the Battery Charging Specification v1.1 and USB 2.0 OTG Specification v2.0.

Application Examples

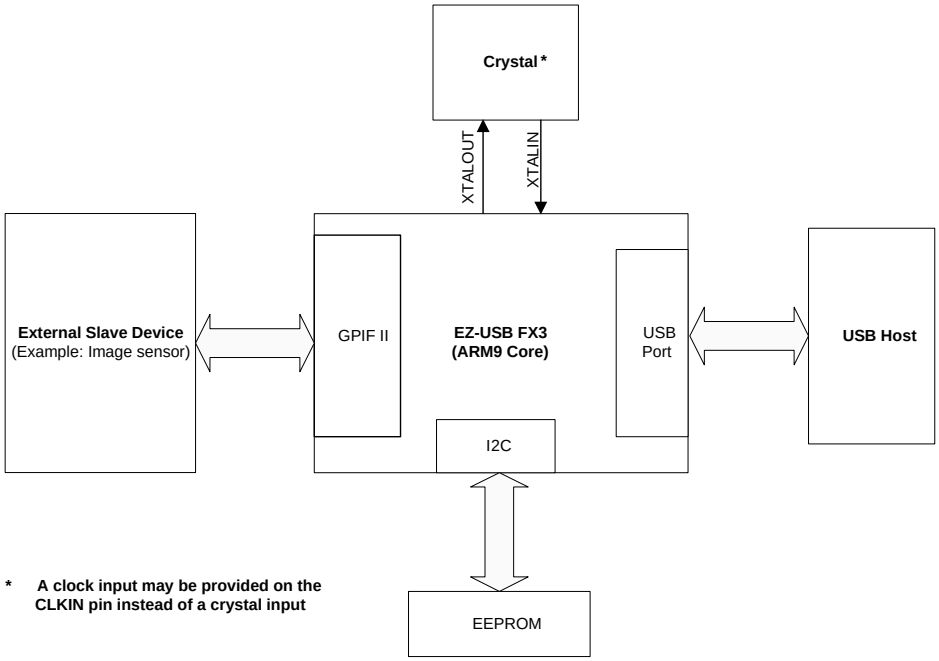
In a typical application (see Figure 1), FX3 functions as a coprocessor and connects to an external processor, which manages system-level functions. Figure 2 shows a typical application diagram when FX3 functions as the main processor.

Figure 1. EZ-USB FX3 as a Coprocessor



Note
1. Assuming that GPIF II is configured for a 32-bit data bus (available with certain part numbers; see Ordering Information on page 36), synchronous interface operating at 100 MHz. This number also includes protocol overheads.

Figure 2. EZ-USB FX3 as Main Processor



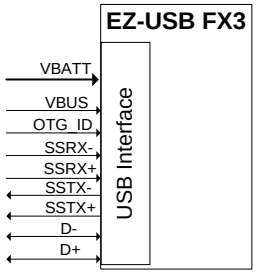
USB Interface

FX3 complies with the following specifications and supports the following features:

- Supports USB peripheral functionality compliant with USB 3.0 Specification Revision 1.0 and is also backward compatible with the USB 2.0 Specification.
- Complies with OTG Supplement Revision 2.0. It supports High-Speed, Full-Speed, and Low-Speed OTG dual-role device capability. As a peripheral, FX3 is capable of SuperSpeed, High-Speed, and Full-Speed. As a host, it is capable of High-Speed, Full-Speed, and Low-Speed.
- Supports Carkit Pass-Through UART functionality on USB D+/D– lines based on the CEA-936A specification.
- Supports up to 16 IN and 16 OUT endpoints.
- Supports the USB 3.0 Streams feature. It also supports USB Attached SCSI (UAS) device-class to optimize mass-storage access performance.
- As a USB peripheral, FX3 supports UAS, USB Video Class (UVC), Mass Storage Class (MSC), and Media Transfer Protocol (MTP) USB peripheral classes. As a USB peripheral, all other device classes are supported only in pass-through mode when handled entirely by a host processor external to the device.
- As an OTG host, FX3 supports MSC and HID device classes.

Note When the USB port is not in use, disable the PHY and transceiver to save power.

Figure 3. USB Interface Signals



OTG

FX3 is compliant with the OTG Specification Revision 2.0. In OTG mode, FX3 supports both A and B device modes and supports Control, Interrupt, Bulk, and Isochronous data transfers.

FX3 requires an external charge pump (either standalone or integrated into a PMIC) to power VBUS in the OTG A-device mode.

The Target Peripheral List for OTG host implementation consists of MSC- and HID-class devices.

FX3 does not support Attach Detection Protocol (ADP).

OTG Connectivity

In OTG mode, FX3 can be configured to be an A, B, or dual-role device. It can connect to the following:

- ACA device
- Targeted USB peripheral
- SRP-capable USB peripheral
- HNP-capable USB peripheral
- OTG host
- HNP-capable host
- OTG device

ReNumeration

Because of FX3's soft configuration, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, FX3 enumerates automatically with the Cypress Vendor ID (0x04B4) and downloads firmware and USB descriptors over the USB interface. The downloaded firmware executes an electrical disconnect and connect. FX3 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called ReNumeration, happens instantly when the device is plugged in.

EZ-Dtect

FX3 supports USB Charger and accessory detection (EZ-Dtect). The charger detection mechanism complies with the Battery Charging Specification Revision 1.1. In addition to supporting this version of the specification, FX3 also provides hardware support to detect the resistance values on the ID pin.

FX3 can detect the following resistance ranges:

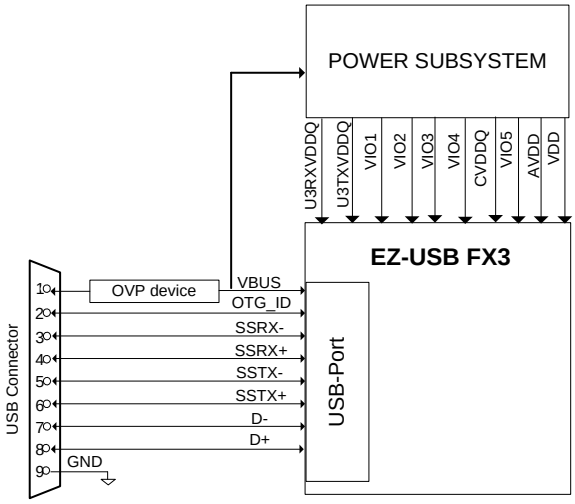
- Less than 10 Ω
- Less than 1 kΩ
- 65 kΩ to 72 kΩ
- 35 kΩ to 39 kΩ
- 99.96 kΩ to 104.4 kΩ (102 kΩ ± 2%)
- 119 kΩ to 132 kΩ
- Higher than 220 kΩ
- 431.2 kΩ to 448.8 kΩ (440 kΩ ± 2%)

FX3's charger detects a dedicated wall charger, Host/Hub charger, and Host/Hub.

VBUS Overvoltage Protection

The maximum input voltage on FX3's VBUS pin is 6 V. A charger can supply up to 9 V on VBUS. In this case, an external overvoltage protection (OVP) device is required to protect FX3 from damage on VBUS. Figure 4 shows the system application diagram with an OVP device connected on VBUS. Refer to Table 7 for the operating range of VBUS and VBATT.

Figure 4. System Diagram with OVP Device For VBUS



Carkit UART Mode

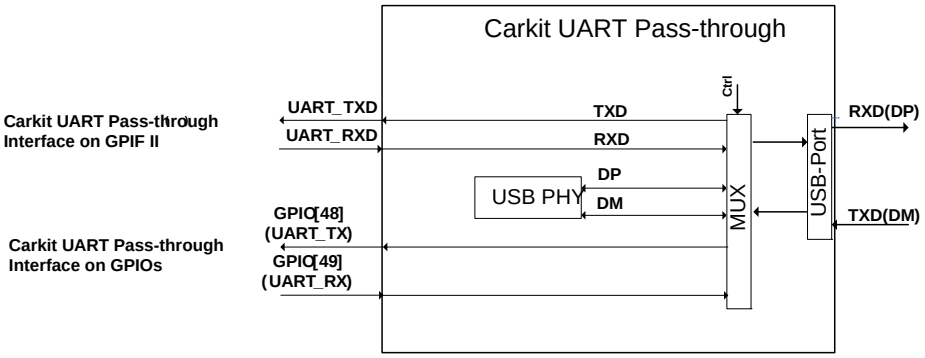
The USB interface supports the Carkit UART mode (UART over D+/D–) for non-USB serial data transfer. This mode is based on the CEA-936A specification.

In the Carkit UART mode, the output signaling voltage is 3.3 V. When configured for the Carkit UART mode, TXD of UART (output) is mapped to the D– line, and RXD of UART (input) is mapped to the D+ line.

In the Carkit UART mode, FX3 disables the USB transceiver and D+ and D– pins serve as pass-through pins to connect to the UART of the host processor. The Carkit UART signals may be routed to the GPIF II interface or to GPIO[48] and GPIO[49], as shown in Figure 5 on page 6.

In this mode, FX3 supports a rate of up to 9600 bps.

Figure 5. Carkit UART Pass-through Block Diagram



GPIF II

The high-performance GPIF II interface enables functionality similar to, but more advanced than, FX2LP's GPIF and Slave FIFO interfaces.

The GPIF II is a programmable state machine that enables a flexible interface that may function either as a master or slave in industry-standard or proprietary interfaces. Both parallel and serial interfaces may be implemented with GPIF II.

Here are a list of GPIF II features:

- Functions as master or slave
- Provides 256 firmware programmable states
- Supports 8-bit, 16-bit, and 32-bit parallel data bus
- Enables interface frequencies up to 100 MHz
- Supports 14 configurable control pins when a 32- bit data bus is used. All control pins can be either input/output or bidirectional.
- Supports 16 configurable control pins when a 16/8 data bus is used. All control pins can be either input/output or bi-directional.

GPIF II state transitions are based on control input signals. The control output signals are driven as a result of the GPIF II state transitions. The INT# output signal can be controlled by GPIF II. Refer to the GPIFII Designer tool. The GPIF II state machine's behavior is defined by a GPIF II descriptor. The GPIF II descriptor is designed such that the required interface specifications are met. 8 kB of memory (separate from the 512 kB of embedded SRAM) is dedicated to the GPIF II waveform where the GPIF II descriptor is stored in a specific format.

Cypress's GPIFII Designer Tool enables fast development of GPIF II descriptors and includes examples for common interfaces.

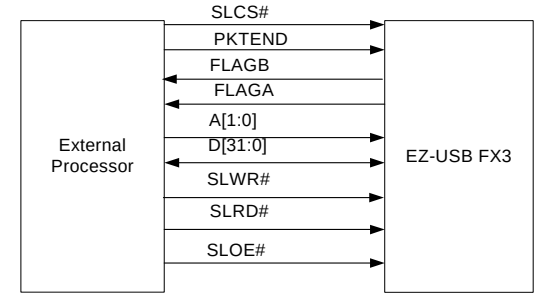
Example implementations of GPIF II are the asynchronous slave FIFO and synchronous slave FIFO interfaces.

Slave FIFO interface

The Slave FIFO interface signals are shown in Figure 6. This interface allows an external processor to directly access up to four buffers internal to FX3. Further details of the Slave FIFO interface are described on page 24.

Note Access to all 32 buffers is also supported over the slave FIFO interface. For details, contact Cypress Applications Support.

Figure 6. Slave FIFO Interface



Note: Multiple Flags may be configured.

CPU

FX3 has an on-chip 32-bit, 200-MHz ARM926EJ-S core CPU. The core has direct access to 16 kB of Instruction Tightly Coupled Memory (TCM) and 8 kB of Data TCM. The ARM926EJ-S core provides a JTAG interface for firmware debugging.

FX3 offers the following advantages:

- Integrates 512 KB of embedded SRAM for code and data and 8 kB of Instruction cache and Data cache.
- Implements efficient and flexible DMA connectivity between the various peripherals (such as, USB, GPIF II, I^2S, SPI, UART), requiring firmware only to configure data accesses between peripherals, which are then managed by the DMA fabric.
- Allows easy application development on industry-standard development tools for ARM926EJ-S.

Examples of the FX3 firmware are available with the Cypress EZ-USB FX3 Development Kit. Software APIs that can be ported to an external processor are available with the Cypress EZ-USB FX3 Software Development Kit.

JTAG Interface

FX3's JTAG interface has a standard five-pin interface to connect to a JTAG debugger in order to debug firmware through the CPU-core's on-chip-debug circuitry.

Industry-standard debugging tools for the ARM926EJ-S core can be used for the FX3 application development.

Other Interfaces

FX3 supports the following serial peripherals:

- UART
- I^2C
- I^2S
- SPI

The SPI, UART, and I^2S interfaces are multiplexed on the serial peripheral port.

The CYUSB3012 and CYUSB3014 Pin List (GPIF II with 32-bit Data Bus Width) on page 13 shows details of how these interfaces are multiplexed. Note that when GPIF II is configured for a 32-bit data bus width (CYUSB3012 and CYUSB3014), only the UART interface is available on GPIO[53] to GPIO[56].

UART Interface

The UART interface of FX3 supports full-duplex communication. It includes the signals noted in Table 1.

Table 1. UART Interface Signals

Signal	Description
TX	Output signal
RX	Input signal
CTS	Flow control
RTS	Flow control

The UART is capable of generating a range of baud rates, from 300 bps to 4608 Kbps, selectable by the firmware. If flow control is enabled, then FX3's UART only transmits data when the CTS input is asserted. In addition to this, FX3's UART asserts the RTS output signal, when it is ready to receive data.

I^2C Interface

FX3's I^2C interface is compatible with the I^2C Bus Specification Revision 3. This I^2C interface is capable of operating only as I^2C master; therefore, it may be used to communicate with other I^2C slave devices. For example, FX3 may boot from an EEPROM connected to the I^2C interface, as a selectable boot option.

FX3's I^2C Master Controller also supports multi-master mode functionality.

The power supply for the I^2C interface is VIO5, which is a separate power domain from the other serial peripherals. This gives the I^2C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I^2C controller supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I^2C controller supports the clock-stretching feature to enable slower devices to exercise flow control.

The I^2C interface's SCL and SDA signals require external pull-up resistors. The pull-up resistors must be connected to VIO5.

I^2S Interface

FX3 has an I^2S port to support external audio codec devices. FX3 functions as I^2S Master as transmitter only. The I^2S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). FX3 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the I^2S interface are 32 kHz, 44.1 kHz, and 48 kHz.

SPI Interface

FX3 supports an SPI Master interface on the Serial Peripherals port. The maximum operation frequency is 33 MHz.

The SPI controller supports four modes of SPI communication (see SPI Timing Specification on page 32 for details on the modes) with the Start-Stop clock. This controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from 4 bits to 32 bits.

Boot Options

FX3 can load boot images from various sources, selected by the configuration of the PMODE pins. Following are the FX3 boot options:

- Boot from USB
- Boot from I^2C
- Boot from SPI (SPI devices supported are M25P16 (16 Mbit), M25P80 (8 Mbit), and M25P40 (4 Mbit)) or their equivalents
- Boot from GPIF II ASync ADMux mode
- Boot from GPIF II Sync ADMux mode
- Boot from GPIF II ASync SRAM mode

Table 2. FX3 Booting Options

PMODE[2:0][2]	Boot From
F00	Sync ADMux (16-bit)
F01	Async ADMux (16-bit)
F11	USB boot
F0F	Async SRAM (16-bit)
F1F	I^2C, On Failure, USB Boot is Enabled
1FF	I^2C only
0F1	SPI, On Failure, USB Boot is Enabled

Reset

Hard Reset

A hard reset is initiated by asserting the Reset# pin on FX3. The specific reset sequence and timing requirements are detailed in Figure 18 on page 34 and Table 17 on page 33. All I/Os are tristated during a hard reset.

Soft Reset

In a soft reset, the processor sets the appropriate bits in the PP_INIT control register. There are two types of Soft Reset:

- CPU Reset – The CPU Program Counter is reset. Firmware does not need to be reloaded following a CPU Reset.
- Whole Device Reset – This reset is identical to Hard Reset.
- The firmware must be reloaded following a Whole Device Reset.

Clocking

FX3 allows either a crystal to be connected between the XTALIN and XTALOUT pins or an external clock to be connected at the CLKIN pin. The XTALIN, XTALOUT, CLKIN, and CLKIN_32 pins can be left unconnected if they are not used.

Crystal frequency supported is 19.2 MHz, while the external clock frequencies supported are 19.2, 26, 38.4, and 52 MHz.

FX3 has an on-chip oscillator circuit that uses an external 19.2-MHz (±100 ppm) crystal (when the crystal option is used). An appropriate load capacitance is required with a crystal. Refer to the specification of the crystal used to determine the appropriate load capacitance. The FSLC[2:0] pins must be configured appropriately to select the crystal- or clock-frequency option. The configuration options are shown in Table 3.

Clock inputs to FX3 must meet the phase noise and jitter requirements specified in Table 4 on page 9.

The input clock frequency is independent of the clock and data rate of the FX3 core or any of the device interfaces (including P-Port and S-Port). The internal PLL applies the appropriate clock multiply option depending on the input frequency.

Table 3. Crystal/Clock Frequency Selection

FSLC[2]	FSLC[1]	FSLC[0]	Crystal/Clock Frequency
0	0	0	19.2-MHz crystal
1	0	0	19.2-MHz input CLK
1	0	1	26-MHz input CLK
1	1	0	38.4-MHz input CLK
1	1	1	52-MHz input CLK

Note
2. F indicates Floating.

Table 4. FX3 Input Clock Specifications

Parameter	Description	Specification		Units
		Min	Max	
Phase noise	100-Hz offset	–	–75	dB
	1- kHz offset	–	–104	dB
	10-kHz offset	–	–120	dB
	100-kHz offset	–	–128	dB
	1-MHz offset	–	–130	dB
Maximum frequency deviation		–	150	ppm
Duty cycle		30	70	%
Overshoot		–	3	%
Undershoot		–	–3	%
Rise time/fall time		–	3	ns

32-kHz Watchdog Timer Clock Input

FX3 includes a watchdog timer. The watchdog timer can be used to interrupt the ARM926EJ-S core, automatically wake up the FX3 in Standby mode, and reset the ARM926EJ-S core. The watchdog timer runs a 32-kHz clock, which may be optionally supplied from an external source on a dedicated FX3 pin.

The firmware can disable the watchdog timer.

Requirements for the optional 32-kHz clock input are listed in Table 5.

Table 5. 32-kHz Clock Input Requirements

Parameter	Min	Max	Units
Duty cycle	40	60	%
Frequency deviation	–	±200	ppm
Rise time/fall time	–	200	ns

Power

FX3 has the following power supply domains:

- **IO_VDDQ**: This is a group of independent supply domains for digital I/Os. The voltage level on these supplies is 1.8 V to 3.3 V. FX3 provides six independent supply domains for digital I/Os listed as follows (see Table 7 for details on each of the power domain signals):
  - VIO1: GPIF II I/O
  - VIO2: IO2
  - VIO3: IO3
  - VIO4: UART-/SPI/I^2S
  - VIO5: I^2C and JTAG (supports 1.2 V to 3.3 V)
  - CVDDQ: Clock
  - **V_{DD}**: This is the supply voltage for the logic core. The nominal supply-voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for the following:
    - AVDD: This is the 1.2-V supply for the PLL, crystal oscillator, and other core analog circuits
    - **U3TXVDDQ/U3RXVDDQ**: These are the 1.2-V supply voltages for the USB 3.0 interface.
- **VBATT/VBUS**: This is the 3.2-V to 6-V battery power supply for the USB I/O and analog circuits. This supply powers the USB transceiver through FX3's internal voltage regulator. VBATT is internally regulated to 3.3 V.

Power Modes

FX3 supports the following power modes:

- Normal mode: This is the full-functional operating mode. The internal CPU clock and the internal PLLs are enabled in this mode.
  - Normal operating power consumption does not exceed the sum of I_{CC} Core max and I_{CC} USB max (see Table 7 for current consumption specifications).
  - The I/O power supplies VIO2, VIO3, VIO4, and VIO5 can be turned off when the corresponding interface is not in use. VIO1 cannot be turned off at any time if the GPIF II interface is used in the application.
- Low-power modes (see Table 6 on page 10):
  - Suspend mode with USB 3.0 PHY enabled (L1)
  - Suspend mode with USB 3.0 PHY disabled (L2)
  - Standby mode (L3)
  - Core power-down mode (L4)

Table 6. Entry and Exit Methods for Low-Power Modes

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend Mode with USB 3.0 PHY Enabled (L1)	■ The power consumption in this mode does not exceed ISB_1 ■ USB 3.0 PHY is enabled and is in U3 mode (one of the suspend modes defined by the USB 3.0 specification). This one block alone is operational with its internal clock while all other clocks are shut down ■ All I/Os maintain their previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory, and all internal RAM are maintained ■ All transactions must be completed before FX3 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on ARM926EJ-S core can put FX3 into suspend mode. For example, on USB suspend condition, firmware may decide to put FX3 into suspend mode ■ External Processor, through the use of mailbox registers, can put FX3 into suspend mode	■ D+ transitioning to low or high ■ D- transitioning to low or high ■ Impedance change on OTG_ID pin ■ Resume condition on SSRX± ■ Detection of VBUS ■ Level detect on UART_CTS (programmable polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#
Suspend Mode with USB 3.0 PHY Disabled (L2)	■ The power consumption in this mode does not exceed ISB_2 ■ USB 3.0 PHY is disabled and the USB interface is in suspend mode ■ The clocks are shut off. The PLLs are disabled ■ All I/Os maintain their previous state ■ USB interface maintains the previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory and all internal RAM are maintained ■ All transactions must be completed before FX3 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on ARM926EJ-S core can put FX3 into suspend mode. For example, on USB suspend condition, firmware may decide to put FX3 into suspend mode ■ External Processor, through the use of mailbox registers can put FX3 into suspend mode	■ D+ transitioning to low or high ■ D- transitioning to low or high ■ Impedance change on OTG_ID pin ■ Resume condition on SSRX± ■ Detection of VBUS ■ Level detect on UART_CTS (programmable polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Standby Mode (L3)	■ The power consumption in this mode does not exceed ISB3 ■ All configuration register settings and program/data RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed. Therefore, the external processor should take care that the data needed is read before putting FX3 into this Standby Mode ■ The program counter is reset after waking up from Standby ■ GPIO pins maintain their configuration ■ Crystal oscillator is turned off ■ Internal PLL is turned off ■ USB transceiver is turned off ■ ARM926EJ-S core is powered down. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually	■ Firmware executing on ARM926EJ-S core or external processor configures the appropriate register	■ Detection of VBUS ■ Level detect on UART_CTS (Programmable Polarity) ■ GPIF II interface assertion of CTL[0] ■ Assertion of RESET#
Core Power Down Mode (L4)	■ The power consumption in this mode does not exceed ISB_4 ■ Core power is turned off ■ All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware ■ In this mode, all other power domains can be turned on/off individually	■ Turn off V_{DD}	■ Reapply VDD ■ Assertion of RESET#

Configuration Options

Configuration options are available for specific usage models. Contact Cypress Applications or Marketing for details.

Digital I/Os

FX3 has internal firmware-controlled pull-up or pull-down resistors on all digital I/O pins. An internal 50-kΩ resistor pulls the pins high, while an internal 10-kΩ resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 kΩ)
- Pull-down (via internal 10 kΩ)
- Hold (I/O hold its value) when in low-power modes
- The JTAG TDI, TMC, and TRST# signals have fixed 50-kΩ internal pull-ups, and the TCK signal has a fixed 10-kΩ pull-down resistor.

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

GPIOs

EZ-USB enables a flexible pin configuration both on the GPIF II and the serial peripheral interfaces. Any unused control pins (except CTL[15]) on the GPIF II interface can be used as GPIOs. Similarly, any unused pins on the serial peripheral interfaces may be configured as GPIOs. See the on page 16 for pin configuration options.

All GPIF II and GPIO pins support an external load of up to 16 pF for every pin.

EMI

FX3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. FX3 can tolerate reasonable EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

System-level ESD

FX3 has built-in ESD protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-KV human body model (HBM) based on JESD22-A114 Specification
- ±6-KV contact discharge and ±8-KV air gap discharge based on IEC61000-4-2 level 3A
- ± 8-KV Contact Discharge and ±15-KV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated in this section.

The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ±2.2-KV HBM internal ESD protection.

Figure 7. FX3 Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	**AVDD**	VSS	DP	DM	NC
B	VIO4	FSLC[0]	R_USB3	FSLC[1]	U3TXVDDQ	CVDDQ	**AVSS**	**VSS**	VSS	**VDD**	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	**VBATT**	**VBUS**
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Pin Description

Table 7. CYUSB3012 and CYUSB3014 Pin List (GPIF II with 32-bit Data Bus Width)

Pin		I/O	Name	Description	
				GPIF II (VIO1 Power Domain)	
				GPIF II Interface	Slave FIFO Interface
F10	VIO1	I/O	GPIO[0]	DQ[0]	DQ[0]
F9	VIO1	I/O	GPIO[1]	DQ[1]	DQ[1]
F7	VIO1	I/O	GPIO[2]	DQ[2]	DQ[2]
G10	VIO1	I/O	GPIO[3]	DQ[3]	DQ[3]
G9	VIO1	I/O	GPIO[4]	DQ[4]	DQ[4]
F8	VIO1	I/O	GPIO[5]	DQ[5]	DQ[5]
H10	VIO1	I/O	GPIO[6]	DQ[6]	DQ[6]
H9	VIO1	I/O	GPIO[7]	DQ[7]	DQ[7]
J10	VIO1	I/O	GPIO[8]	DQ[8]	DQ[8]
J9	VIO1	I/O	GPIO[9]	DQ[9]	DQ[9]
K11	VIO1	I/O	GPIO[10]	DQ[10]	DQ[10]
L10	VIO1	I/O	GPIO[11]	DQ[11]	DQ[11]
K10	VIO1	I/O	GPIO[12]	DQ[12]	DQ[12]
K9	VIO1	I/O	GPIO[13]	DQ[13]	DQ[13]
J8	VIO1	I/O	GPIO[14]	DQ[14]	DQ[14]
G8	VIO1	I/O	GPIO[15]	DQ[15]	DQ[15]
J6	VIO1	I/O	GPIO[16]	PCLK	CLK
K8	VIO1	I/O	GPIO[17]	CTL[0]	SLCS#
K7	VIO1	I/O	GPIO[18]	CTL[1]	SLWR#
J7	VIO1	I/O	GPIO[19]	CTL[2]	SLOE#
H7	VIO1	I/O	GPIO[20]	CTL[3]	SLRD#
G7	VIO1	I/O	GPIO[21]	CTL[4]	FLAGA
G6	VIO1	I/O	GPIO[22]	CTL[5]	FLAGB
K6	VIO1	I/O	GPIO[23]	CTL[6]	GPIO
H8	VIO1	I/O	GPIO[24]	CTL[7]	PKTEND#
G5	VIO1	I/O	GPIO[25]	CTL[8]	GPIO
H6	VIO1	I/O	GPIO[26]	CTL[9]	GPIO
K5	VIO1	I/O	GPIO[27]	CTL[10]	GPIO
J5	VIO1	I/O	GPIO[28]	CTL[11]	A1
H5	VIO1	I/O	GPIO[29]	CTL[12]	A0
G4	VIO1	I/O	GPIO[30]	PMODE[0]	PMODE[0]
H4	VIO1	I/O	GPIO[31]	PMODE[1]	PMODE[1]
L4	VIO1	I/O	GPIO[32]	PMODE[2]	PMODE[2]
L8	VIO1	I/O	INT#	INT#/CTL[15]	CTL[15]
C5	CVDDQ	I	RESET#	RESET#	RESET#
				IO2 (VIO2 Power Domain)	
				GPIF II (32-bit data mode)	
K2	VIO2	I/O	GPIO[33]	DQ[16]	GPIO
J4	VIO2	I/O	GPIO[34]	DQ[17]	GPIO
K1	VIO2	I/O	GPIO[35]	DQ[18]	GPIO
J2	VIO2	I/O	GPIO[36]	DQ[19]	GPIO
J3	VIO2	I/O	GPIO[37]	DQ[20]	GPIO
J1	VIO2	I/O	GPIO[38]	DQ[21]	GPIO
H2	VIO2	I/O	GPIO[39]	DQ[22]	GPIO

Table 7. CYUSB3012 and CYUSB3014 Pin List (GPIF II with 32-bit Data Bus Width) (continued)

Pin		I/O	Name	Description					
H3	VIO2	I/O	GPIO[40]	DQ[23]				GPIO	
F4	VIO2	I/O	GPIO[41]	DQ[24]				GPIO	
G2	VIO2	I/O	GPIO[42]	DQ[25]				GPIO	
G3	VIO2	I/O	GPIO[43]	DQ[26]				GPIO	
F3	VIO2	I/O	GPIO[44]	DQ[27]				GPIO	
F2	VIO2	I/O	GPIO[45]	GPIO					
				IO3 (VIO3 Power Domain)					
				GPIO + SPI	GPIO + UART	GPIO only	GPIF II - 32b + I2S + UART[3]	GPIO + I2S	UART + SPI + I2S
F5	VIO3	I/O	GPIO[46]	GPIO	GPIO	GPIO	DQ[28]	GPIO	UART_RTS
E1	VIO3	I/O	GPIO[47]	GPIO	GPIO	GPIO	DQ[29]	GPIO	UART_CTS
E5	VIO3	I/O	GPIO[48]	GPIO	GPIO	GPIO	DQ[30]	GPIO	UART_TX
E4	VIO3	I/O	GPIO[49]	GPIO	GPIO	GPIO	DQ[31]	GPIO	UART_RX
D1	VIO3	I/O	GPIO[50]	GPIO	GPIO	GPIO	I2S_CLK	GPIO	I2S_CLK
D2	VIO3	I/O	GPIO[51]	GPIO	GPIO	GPIO	I2S_SD	GPIO	I2S_SD
D3	VIO3	I/O	GPIO[52]	GPIO	GPIO	GPIO	I2S_WS	GPIO	I2S_WS
				IO4 (VIO4) Power Domain					
D4	VIO4	I/O	GPIO[53]	SPI_SCK	UART_RTS	GPIO	UART_RTS	GPIO	SPI_SCK
C1	VIO4	I/O	GPIO[54]	SPI_SSN	UART_CTS	GPIO	UART_CTS	I2S_CLK	SPI_SSN
C2	VIO4	I/O	GPIO[55]	SPI_MISO	UART_TX	GPIO	UART_TX	I2S_SD	SPI_MISO
D5	VIO4	I/O	GPIO[56]	SPI_MOSI	UART_RX	GPIO	UART_RX	I2S_WS	SPI_MOSI
C4	VIO4	I/O	GPIO[57]	GPIO	GPIO	GPIO	I2S_MCLK	I2S_MCLK	I2S_MCLK
				USB Port (VBATT/VBUS Power Domain)					
C9	VBUS/ VBATT	I	OTG_ID	OTG_ID					
				USB Port (U3TXVDDQ/U3RXVDDQ Power Domain)					
A3	U3RXVDDQ	I	SSRXM	SSRX-					
A4	U3RXVDDQ	I	SSRXP	SSRX+					
A6	U3TXVDDQ	O	SSTXM	SSTX-					
A5	U3TXVDDQ	O	SSTXP	SSTX+					
				USB Port (VBATT/VBUS Power Domain)					
A9	VBUS/VBATT	I/O	DP	D+					
A10	VBUS/VBATT	I/O	DM	D–					
A11			NC	No connect					
				Crystal/Clocks (CVDDQ Power Domain)					
B2	CVDDQ	I	FSLC[0]	FSLC[0]					
C6	AVDD	I/O	XTALIN	XTALIN					
C7	AVDD	I/O	XTALOUT	XTALOUT					
B4	CVDDQ	I	FSLC[1]	FSLC[1]					
E6	CVDDQ	I	FSLC[2]	FSLC[2]					
D7	CVDDQ	I	CLKIN	CLKIN					
D6	CVDDQ	I	CLKIN_32	CLKIN_32					
				I2C and JTAG (VIO5 Power Domain)					
D9	VIO5	I/O	I2C_GPIO[58]	I^2C_SCL					
D10	VIO5	I/O	I2C_GPIO[59]	I^2C_SDA					

Note
3. When GPIF II is configured for the 32-bit data bus width, GPIO[50]-GPIO[52] may be configured as GPIOs or I2S, and GPIO[53] to GPIO[56] may be configured as GPIOs or UART interface only.

Table 7. CYUSB3012 and CYUSB3014 Pin List (GPIF II with 32-bit Data Bus Width) (continued)

Pin		I/O	Name	Description
E7	VIO5	I	TDI	TDI
C10	VIO5	O	TDO	TDO
B11	VIO5	I	TRST#	TRST#
E8	VIO5	I	TMS	TMS
F6	VIO5	I	TCK	TCK
D11	VIO5	O	O[60]	Charger detect output
				Power
E10		PWR	VBATT	
B10		PWR	VDD	
A1		PWR	U3VSSQ	
E11		PWR	VBUS	
D8		PWR	VSS	
H11		PWR	VIO1	
E2		PWR	VSS	
L9		PWR	VIO1	
G1		PWR	VSS	
F1		PWR	VIO2	
G11		PWR	VSS	
E3		PWR	VIO3	
L1		PWR	VSS	
B1		PWR	VIO4	
L6		PWR	VSS	
B6		PWR	CVDDQ	
B5		PWR	U3TXVDDQ	
A2		PWR	U3RXVDDQ	
C11		PWR	VIO5	
L11		PWR	VSS	
A7		PWR	AVDD	
B7		PWR	AVSS	
C3		PWR	VDD	
B8		PWR	VSS	
E9		PWR	VDD	
B9		PWR	VSS	
F11		PWR	VDD	
H1		PWR	VDD	
L7		PWR	VDD	
J11		PWR	VDD	
L5		PWR	VDD	
K4		PWR	VSS	
L3		PWR	VSS	
K3		PWR	VSS	
L2		PWR	VSS	
A8		PWR	VSS	
				Precision Resistors
C8	VBUS/VBATT	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 kΩ ±1% resistor between this pin and GND)
B3	U3TXVDDQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 Ω ±1% resistor between this pin and GND)

Table 8. CYUSB3011 and CYUSB3013 Pin List (GPIF II with 16-bit Data Bus Width)

Pin		I/O	Name	Description	
				GPIF II (VIO1 Power Domain)	
				GPIF II Interface	Slave FIFO Interface
F10	VIO1	I/O	GPIO[0]	DQ[0]	DQ[0]
F9	VIO1	I/O	GPIO[1]	DQ[1]	DQ[1]
F7	VIO1	I/O	GPIO[2]	DQ[2]	DQ[2]
G10	VIO1	I/O	GPIO[3]	DQ[3]	DQ[3]
G9	VIO1	I/O	GPIO[4]	DQ[4]	DQ[4]
F8	VIO1	I/O	GPIO[5]	DQ[5]	DQ[5]
H10	VIO1	I/O	GPIO[6]	DQ[6]	DQ[6]
H9	VIO1	I/O	GPIO[7]	DQ[7]	DQ[7]
J10	VIO1	I/O	GPIO[8]	DQ[8]	DQ[8]
J9	VIO1	I/O	GPIO[9]	DQ[9]	DQ[9]
K11	VIO1	I/O	GPIO[10]	DQ[10]	DQ[10]
L10	VIO1	I/O	GPIO[11]	DQ[11]	DQ[11]
K10	VIO1	I/O	GPIO[12]	DQ[12]	DQ[12]
K9	VIO1	I/O	GPIO[13]	DQ[13]	DQ[13]
J8	VIO1	I/O	GPIO[14]	DQ[14]	DQ[14]
G8	VIO1	I/O	GPIO[15]	DQ[15]	DQ[15]
J6	VIO1	I/O	GPIO[16]	PCLK	CLK
K8	VIO1	I/O	GPIO[17]	CTL[0]	SLCS#
K7	VIO1	I/O	GPIO[18]	CTL[1]	SLWR#
J7	VIO1	I/O	GPIO[19]	CTL[2]	SLOE#
H7	VIO1	I/O	GPIO[20]	CTL[3]	SLRD#
G7	VIO1	I/O	GPIO[21]	CTL[4]	FLAGA
G6	VIO1	I/O	GPIO[22]	CTL[5]	FLAGB
K6	VIO1	I/O	GPIO[23]	CTL[6]	GPIO
H8	VIO1	I/O	GPIO[24]	CTL[7]	PKTEND#
G5	VIO1	I/O	GPIO[25]	CTL[8]	GPIO
H6	VIO1	I/O	GPIO[26]	CTL[9]	GPIO
K5	VIO1	I/O	GPIO[27]	CTL[10]	GPIO
J5	VIO1	I/O	GPIO[28]	CTL[11]	A1
H5	VIO1	I/O	GPIO[29]	CTL[12]	A0
G4	VIO1	I/O	GPIO[30]	PMODE[0]	PMODE[0]
H4	VIO1	I/O	GPIO[31]	PMODE[1]	PMODE[1]
L4	VIO1	I/O	GPIO[32]	PMODE[2]	PMODE[2]
L8	VIO1	I/O	INT#	INT#/CTL[15]	CTL[15]
C5	CVDDQ	I	RESET#	RESET#	RESET#
				IO2 (VIO2 Power Domain)	
K2	VIO2	I/O	GPIO[33]	GPIO	
J4	VIO2	I/O	GPIO[34]	GPIO	
K1	VIO2	I/O	GPIO[35]	GPIO	
J2	VIO2	I/O	GPIO[36]	GPIO	
J3	VIO2	I/O	GPIO[37]	GPIO	
J1	VIO2	I/O	GPIO[38]	GPIO	
H2	VIO2	I/O	GPIO[39]	GPIO	

Table 8. CYUSB3011 and CYUSB3013 Pin List (GPIF II with 16-bit Data Bus Width) (continued)

Pin		I/O	Name	Description					
H3	VIO2	I/O	GPIO[40]	GPIO					
F4	VIO2	I/O	GPIO[41]	GPIO					
G2	VIO2	I/O	GPIO[42]	GPIO					
G3	VIO2	I/O	GPIO[43]	GPIO					
F3	VIO2	I/O	GPIO[44]	GPIO					
F2	VIO2	I/O	GPIO[45]	GPIO					
				IO3 (VIO3 Power Domain)					
F5	VIO3	I/O	GPIO[46]	GPIO					
E1	VIO3	I/O	GPIO[47]	GPIO					
E5	VIO3	I/O	GPIO[48]	GPIO					
E4	VIO3	I/O	GPIO[49]	GPIO					
D1	VIO3	I/O	GPIO[50]	GPIO	GPIO	GPIO	I2S_CLK	GPIO	I2S_CLK
D2	VIO3	I/O	GPIO[51]	GPIO	GPIO	GPIO	I2S_SD	GPIO	I2S_SD
D3	VIO3	I/O	GPIO[52]	GPIO	GPIO	GPIO	I2S_WS	GPIO	I2S_WS
				IO4 (VIO4) Power Domain					
D4	VIO4	I/O	GPIO[53]	SPI_SCK	UART_RTS	GPIO	UART_RTS	GPIO	SPI_SCK
C1	VIO4	I/O	GPIO[54]	SPI_SSN	UART_CTS	GPIO	UART_CTS	I2S_CLK	SPI_SSN
C2	VIO4	I/O	GPIO[55]	SPI_MISO	UART_TX	GPIO	UART_TX	UART_TX	SPI_MISO
D5	VIO4	I/O	GPIO[56]	SPI_MOSI	UART_RX	GPIO	UART_RX	UART_RX	SPI_MOSI
C4	VIO4	I/O	GPIO[57]	GPIO	GPIO	GPIO	I2S_MCLK	I2S_MCLK	I2S_MCLK
				USB Port (VBATT/VBUS Power Domain)					
C9	VBUS/ VBATT	I	OTG_ID	OTG_ID					
				USB Port (U3TXVDDQ/U3RXVDDQ Power Domain)					
A3	U3RXVDDQ	I	SSRXM	SSRX-					
A4	U3RXVDDQ	I	SSRXP	SSRX+					
A6	U3TXVDDQ	O	SSTXM	SSTX-					
A5	U3TXVDDQ	O	SSTXP	SSTX+					
				USB Port (VBATT/VBUS Power Domain)					
A9	VBUS/VBATT	I/O	DP	D+					
A10	VBUS/VBATT	I/O	DM	D–					
A11			NC	No connect					
				Crystal/Clocks (CVDDQ Power Domain)					
B2	CVDDQ	I	FSLC[0]	FSLC[0]					
C6	AVDD	I/O	XTALIN	XTALIN					
C7	AVDD	I/O	XTALOUT	XTALOUT					
B4	CVDDQ	I	FSLC[1]	FSLC[1]					
E6	CVDDQ	I	FSLC[2]	FSLC[2]					
D7	CVDDQ	I	CLKIN	CLKIN					
D6	CVDDQ	I	CLKIN_32	CLKIN_32					
				I2C and JTAG (VIO5 Power Domain)					
D9	VIO5	I/O	I2C_GPIO[58]	I^2C_SCL					
D10	VIO5	I/O	I2C_GPIO[59]	I^2C_SDA					
E7	VIO5	I	TDI	TDI					
C10	VIO5	O	TDO	TDO					
B11	VIO5	I	TRST#	TRST#					

Table 8. CYUSB3011 and CYUSB3013 Pin List (GPIF II with 16-bit Data Bus Width) (continued)

Pin		I/O	Name	Description
E8	VIO5	I	TMS	TMS
F6	VIO5	I	TCK	TCK
D11	VIO5	O	O[60]	Charger detect output
				Power
E10		PWR	VBATT	
B10		PWR	VDD	
A1		PWR	U3VSSQ	
E11		PWR	VBUS	
D8		PWR	VSS	
H11		PWR	VIO1	
E2		PWR	VSS	
L9		PWR	VIO1	
G1		PWR	VSS	
F1		PWR	VIO2	
G11		PWR	VSS	
E3		PWR	VIO3	
L1		PWR	VSS	
B1		PWR	VIO4	
L6		PWR	VSS	
B6		PWR	CVDDQ	
B5		PWR	U3TXVDDQ	
A2		PWR	U3RXVDDQ	
C11		PWR	VIO5	
L11		PWR	VSS	
A7		PWR	AVDD	
B7		PWR	AVSS	
C3		PWR	VDD	
B8		PWR	VSS	
E9		PWR	VDD	
B9		PWR	VSS	
F11		PWR	VDD	
H1		PWR	VDD	
L7		PWR	VDD	
J11		PWR	VDD	
L5		PWR	VDD	
K4		PWR	VSS	
L3		PWR	VSS	
K3		PWR	VSS	
L2		PWR	VSS	
A8		PWR	VSS	
				Precision Resistors
C8	VBUS/VBATT	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 kΩ ±1% resistor between this pin and GND)
B3	U3TXVDDQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 Ω ±1% resistor between this pin and GND)

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature..... –65 °C to +150 °C

Ambient temperature with power supplied (Industrial)..... –40 °C to +85 °C

Supply voltage to ground potential

V_{DD}, A_{VDDQ} .....1.25 V

V_{IO1},V_{IO2}, V_{IO3}, V_{IO4}, V_{IO5}.....3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$.....1.25 V

DC input voltage to any input pin.....VCC+0.3

DC voltage applied to outputs in high Z state.....VCC+0.3

(VCC is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ± 2.2-KV HBM based on JESD22-A114
- Additional ESD protection levels on D+, D–, and GND pins, and serial peripheral pins
- ± 6-KV contact discharge, ± 8-KV air gap discharge based on IEC61000-4-2 level 3A, ± 8-KV contact discharge, and ± 15-KV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current..... .....> 200 mA

Maximum output short-circuit current for all I/O configurations. (Vout = 0V)..... ..... –100 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial..... –40 °C to +85 °C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$

Supply voltage.....1.15 V to 1.25 V

V_{BATT} supply voltage.....3.2 V to 6 V

V_{IO1}, V_{IO2}, V_{IO3}, V_{IO4}, C_{VDDQ}

Supply voltage.....1.7 V to 3.6 V

V_{IO5} supply voltage..... 1.15 V to 3.6 V

Table 9. DC Specifications

Parameter	Description	Min	Max	Units	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
V_{IO1}	GPIF II I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO2}	IO2 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO3}	IO3 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO4}	UART/SPI/I2S power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply.
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply.
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IO5}	I^2C and JTAG voltage supply	1.15	3.6	V	1.2-, 1.8-, 2.5-, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	0.625 × VCC	VCC + 0.3	V	For 2.0 V ≤ V_{CC} ≤ 3.6 V (except USB port).VCC is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	VCC – 0.4	VCC + 0.3	V	For 1.7 V ≤ V_{CC} ≤ 2.0 V (except USB port).VCC is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	–0.3	0.25 × VCC	V	VCC is the corresponding I/O voltage supply.

Table 9. DC Specifications (continued)

Parameter	Description	Min	Max	Units	Notes
V_{OH}	Output HIGH voltage	0.9 × VCC	–	V	I_{OH} (max) = –100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply.
V_{OL}	Output LOW voltage	–	0.1 × VCC	V	I_{OL} (min) = +100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply.
I_{IX}	Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ} (For I/Os with a pull-up or pull-down resistor connected, the leakage current increases by V_{DDQ}/R_{pu} or V_{DDQ}/R_{PD}
I_{OZ}	Output High-Z leakage current for all pins except SSTXP/ SSXM/ SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ}
I_{CC} Core	Core and analog voltage operating current	–	200	mA	Total current through A_{VDD}, V_{DD}
I_{CC} USB	USB voltage supply operating current	–	60	mA	
I_{SB1}	Total suspend current during suspend mode with USB 3.0 PHY enabled (L1)	–	–	mA	Core current: 1.5 mA I/O current: 20 µA USB current: 2 mA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB2}	Total suspend current during suspend mode with USB 3.0 PHY disabled (L2)	–	–	mA	Core current: 250 µA I/O current: 20 µA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB3}	Total standby current during standby mode (L3)	–	–	µA	Core current: 60 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB4}	Total standby current during core power-down mode (L4)	–	–	µA	Core current: 0 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25 °C.)
V_{RAMP}	Voltage ramp rate on core and I/O supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise level permitted on V_{DD} and I/O supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise level permitted on A_{VDD} supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

AC Timing Parameters

GPIF II Timing

Figure 8. GPIF II Timing in Synchronous Mode

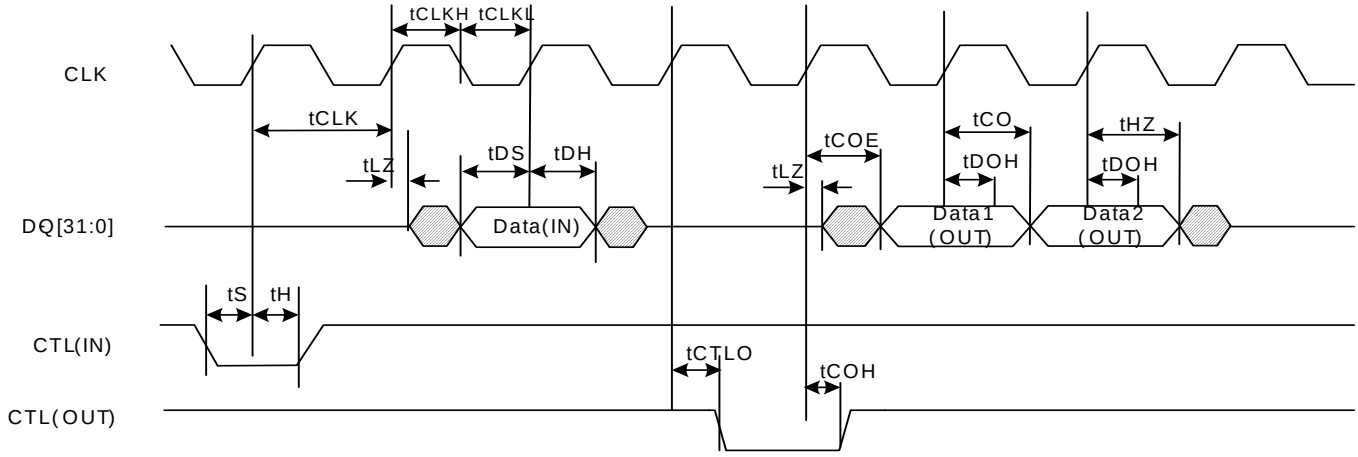


Table 10. GPIF II Timing Parameters in Synchronous Mode[4]

Parameter	Description	Min	Max	Units
Frequency	Interface clock frequency	–	100	MHz
tCLK	Interface clock period	10	–	ns
tCLKH	Clock high time	4	–	ns
tCLKL	Clock low time	4	–	ns
tS	CTL input to clock setup time (Sync speed = 1)	2	–	ns
tH	CTL input to clock hold time (Sync speed = 1)	0.5	–	ns
tDS	Data in to clock setup time (Sync speed = 1)	2	–	ns
tDH	Data in to clock hold time (Sync speed = 1)	0.5	–	ns
tCO	Clock to data out propagation delay when DQ bus is already in output direction (Sync speed = 1)	–	8	ns
tCOE	Clock to data out propagation delay when DQ lines change to output from tristate and valid data is available on the DQ bus (Sync speed = 1)	-	9	
tCTLO	Clock to CTL out propagation delay (Sync speed = 1)	–	8	ns
tDOH	Clock to data out hold	2	–	ns
tCOH	Clock to CTL out hold	0	–	ns
tHZ	Clock to high-Z	–	8	ns
tLZ	Clock to low-Z (Sync speed = 1)	0	–	ns
tS_ss0	CTL input/data input to clock setup time (Sync speed = 0)	5	–	ns
tH_ss0	CTL input/data input to clock hold time (Sync speed = 0)	2.5	–	ns
tCO_ss0	Clock to data out / CTL out propagation delay (sync speed = 0)	–	15	ns
tLZ_ss0	Clock to low-Z (sync speed = 0)	2	–	ns

Note
4. All parameters guaranteed by design and validated through characterization.

Figure 9. GPIF II Timing in Asynchronous Mode

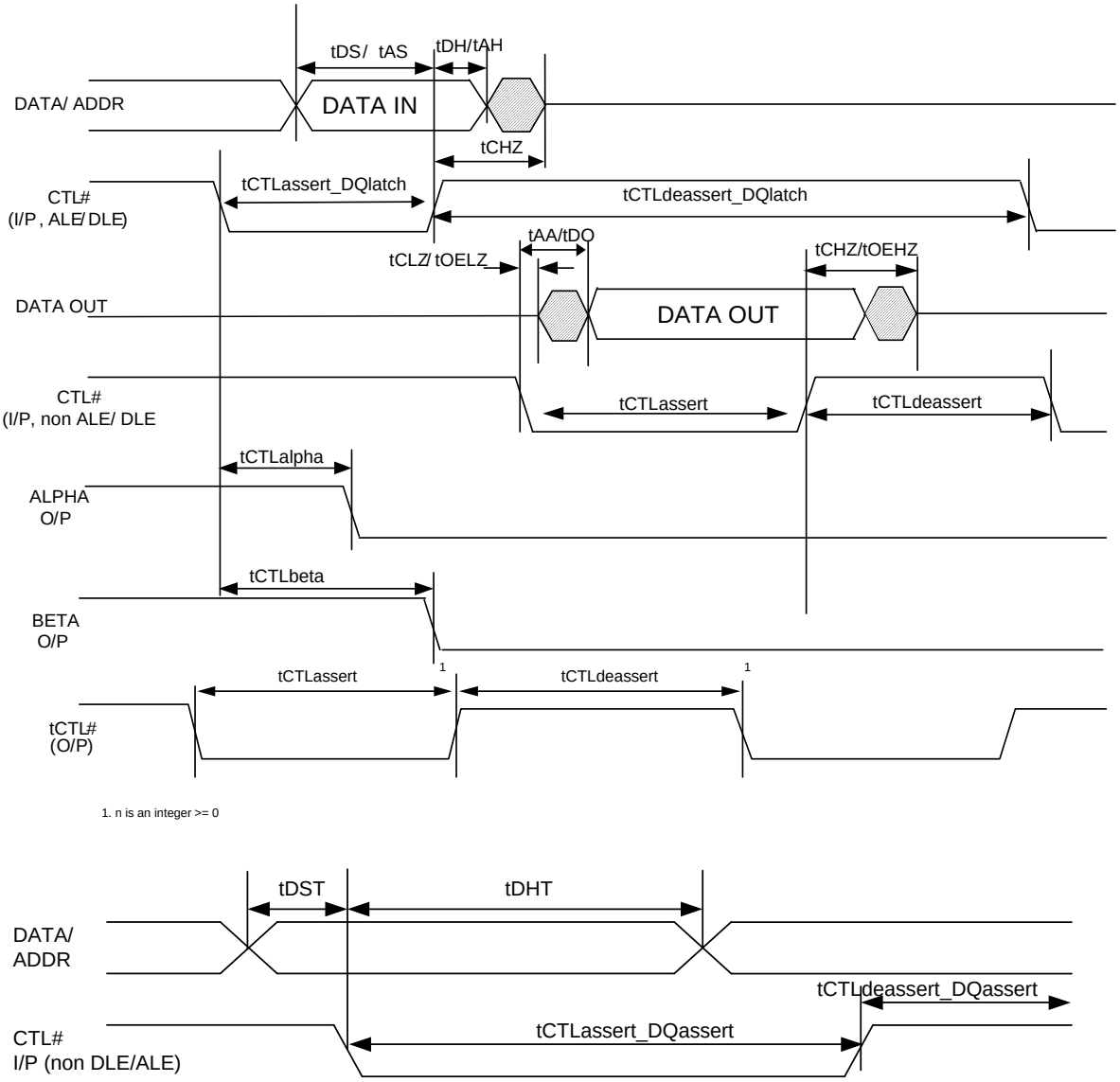


Figure 10. GPIF II Timing in Asynchronous DDR Mode

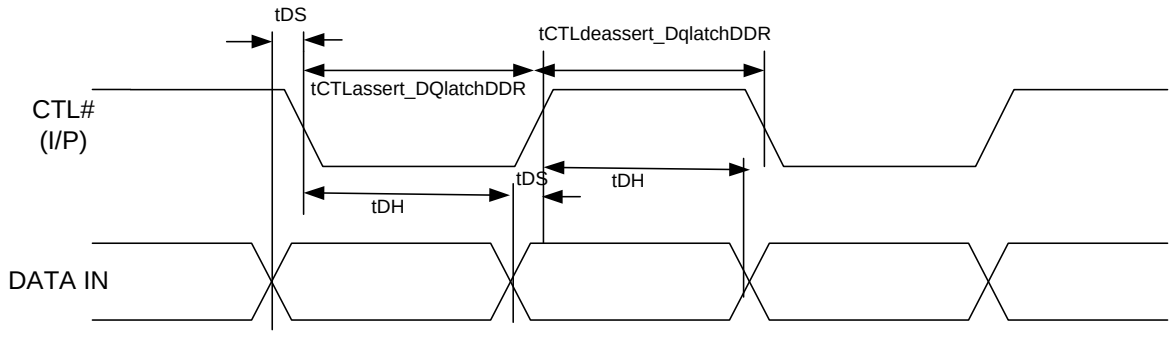


Table 11. GPIF II Timing in Asynchronous Mode[5]

Note The following parameters assume one state transition

Parameter	Description	Min	Max	Units
tDS	Data In to DLE setup time. Valid in DDR async mode.	2.3	–	ns
tDH	Data In to DLE hold time. Valid in DDR async mode.	2	–	ns
tAS	Address In to ALE setup time	2.3	–	ns
tAH	Address In to ALE hold time	2	–	ns
tCTLassert	CTL I/O asserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLdeassert	CTL I/O deasserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLassert_DQassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLdeassert_DQassert	CTL deasserted pulse width for CTL inputs that signify DQ input valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLassert_DQdeassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLdeassert_DQdeassert	CTL deasserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLassert_DQlatch	CTL asserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches are always close at the deasserting edge.	7	–	ns
tCTLdeassert_DQlatch	CTL deasserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches always close at the deasserting edge.	10	–	ns
tCTLassert_DQlatchDDR	CTL asserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tCTLdeassert_DQlatchDDR	CTL deasserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tAA	DQ/CTL input to DQ output time when DQ change or CTL change needs to be detected and affects internal updates of input and output DQ lines.	–	30	ns
tDO	CTL to data out when the CTL change merely enables the output flop update whose data was already established.	–	25	ns
tOELZ	CTL designated as OE to low-Z. Time when external devices should stop driving data.	0	–	ns
tOEHZ	CTL designated as OE to high-Z	8	8	ns
tCLZ	CTL (non-OE) to low-Z. Time when external devices should stop driving data.	0	–	ns
tCHZ	CTL (non-OE) to high-Z	30	30	ns
tCTLalpha	CTL to alpha change at output	–	25	ns
tCTLbeta	CTL to beta change at output	–	30	ns
tDST	Addr/data setup when DLE/ALE not used	2	–	ns
tDHT	Addr/data hold when DLE/ALE not used	20	–	ns

Note
5. All parameters guaranteed by design and validated through characterization.

Slave FIFO Interface

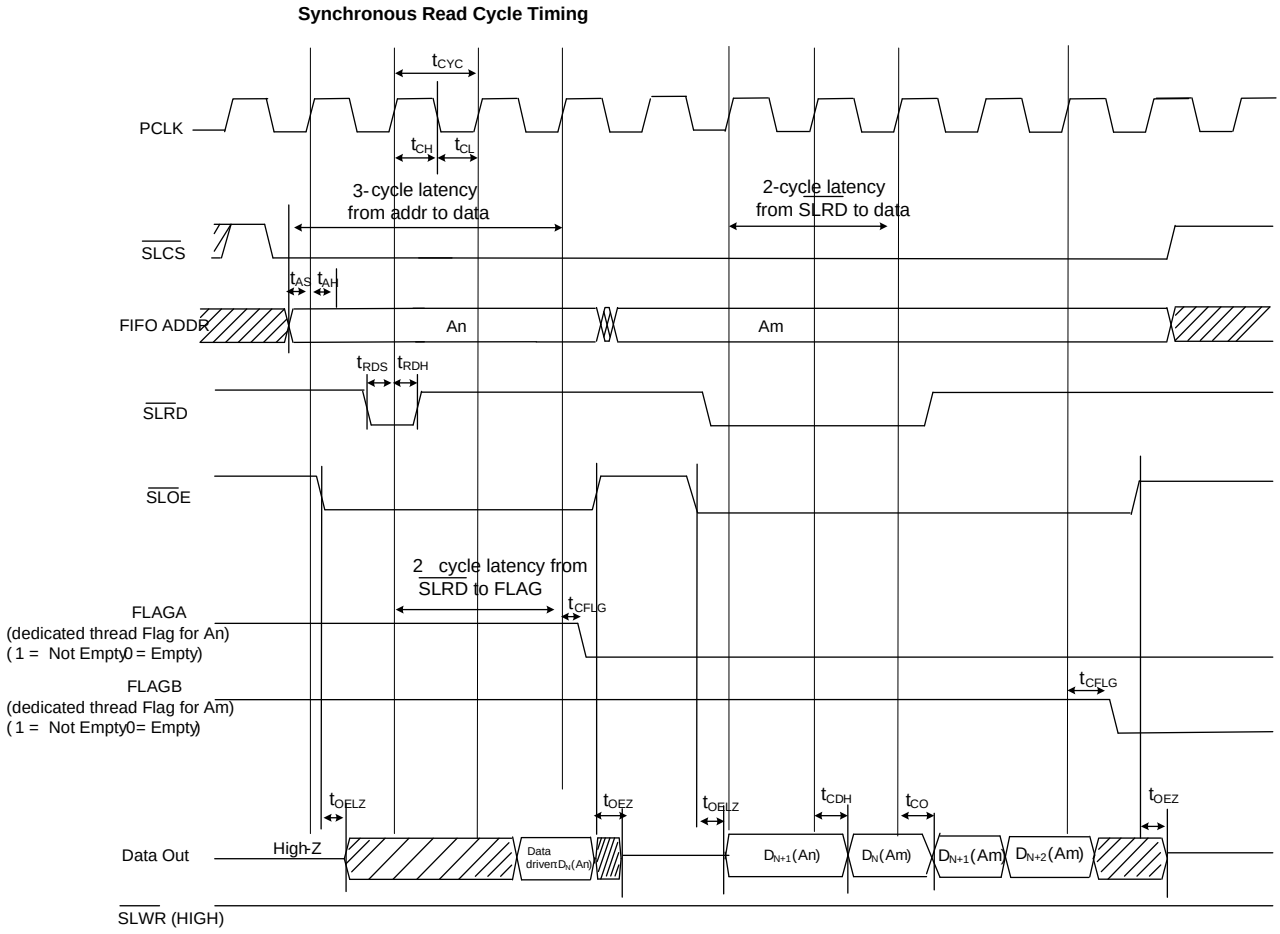
Synchronous Slave FIFO Sequence Description

- FIFO address is stable and SLCS is asserted
- SLOE is asserted. SLOE is an output-enable only, whose sole function is to drive the data bus.
- SLRD is asserted
- The FIFO pointer is updated on the rising edge of the PCLK, while the SLRD is asserted. This starts the propagation of data from the newly addressed location to the data bus. After a propagation delay of tco (measured from the rising edge of PCLK), the new data value is present. N is the first data value read from the FIFO. To have data on the FIFO data bus, SLOE must also be asserted.

The same sequence of events is shown for a burst read.

Note For burst mode, the SLRD# and SLOE# are asserted during the entire duration of the read. When SLOE# is asserted, the data bus is driven (with data from the previously addressed FIFO). For each subsequent rising edge of PCLK, while the SLRD# is asserted, the FIFO pointer is incremented and the next data value is placed on the data bus.

Figure 11. Synchronous Slave FIFO Read Mode



Synchronous Slave FIFO Write Sequence Description

- FIFO address is stable and the signal SLCS# is asserted
- External master or peripheral outputs the data to the data bus
- SLWR# is asserted
- While the SLWR# is asserted, data is written to the FIFO and on the rising edge of the PCLK, the FIFO pointer is incremented
- The FIFO flag is updated after a delay of t_{WFLG} from the rising edge of the clock

The same sequence of events is also shown for burst write

Note For the burst mode, SLWR# and SLCS# are asserted for the entire duration, during which all the required data values are written. In this burst write mode, after the SLWR# is asserted, the data on the FIFO data bus is written to the FIFO on every rising edge of PCLK. The FIFO pointer is updated on each rising edge of PCLK.

Short Packet: A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

Zero-Length Packet: The external device or processor can signal a Zero-Length Packet (ZLP) to FX3 simply by asserting PKTEND#, without asserting SLWR#. SLCS# and address must be driven as shown in Figure 12 on page 25.

FLAG Usage: The FLAG signals are monitored for flow control by the external processor. FLAG signals are outputs from FX3 that may be configured to show empty, full, or partial status for a dedicated thread or the current thread that is addressed.

Figure 12. Synchronous Slave FIFO Write Mode

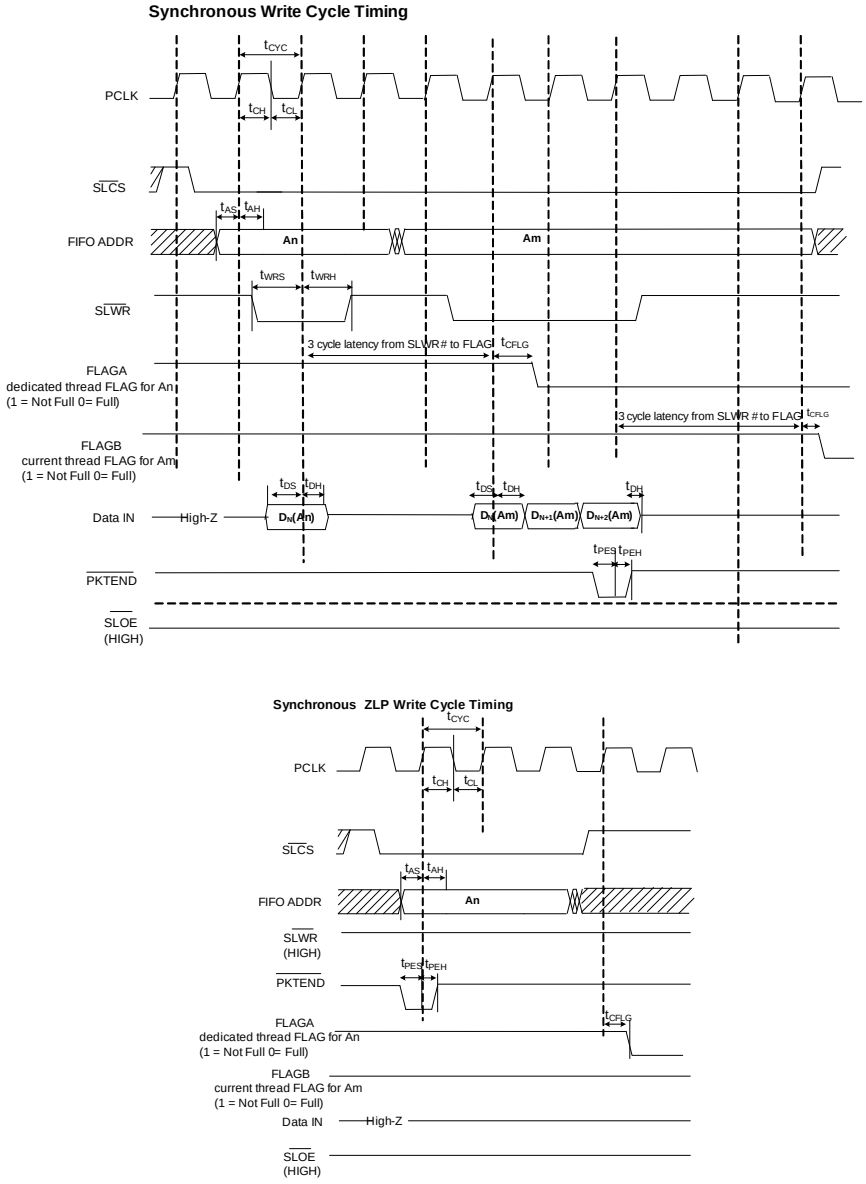


Table 12. Synchronous Slave FIFO Parameters[6]

Parameter	Description	Min	Max	Units
FREQ	Interface clock frequency	–	100	MHz
tCYC	Clock period	10	–	ns
tCH	Clock high time	4	–	ns
tCL	Clock low time	4	–	ns
tRDS	SLRD# to CLK setup time	2	–	ns
tRDH	SLRD# to CLK hold time	0.5	–	ns
tWRS	SLWR# to CLK setup time	2	–	ns
tWRH	SLWR# to CLK hold time	0.5	–	ns
tCO	Clock to valid data	–	8	ns
tDS	Data input setup time	2	–	ns
tDH	CLK to data input hold	0.5	–	ns
tAS	Address to CLK setup time	2	–	ns
tAH	CLK to address hold time	0.5	–	ns
tOELZ	SLOE# to data low-Z	0	–	ns
tCFLG	CLK to flag output propagation delay	–	8	ns
tOEZ	SLOE# deassert to Data Hi Z	–	8	ns
tPES	PKTEND# to CLK setup	2	–	ns
tPEH	CLK to PKTEND# hold	0.5	–	
tCDH	CLK to data output hold	2	–	ns
Note Three-cycle latency from ADDR to DATA/FLAGS				

.

Asynchronous Slave FIFO Read Sequence Description

- FIFO address is stable and the SLCS# signal is asserted.
- SLOE# is asserted. This results in driving the data bus.
- SLRD # is asserted.
- Data from the FIFO is driven after assertion of SLRD#. This data is valid after a propagation delay of tRDO from the falling edge of SLRD#.
- FIFO pointer is incremented on deassertion of SLRD#

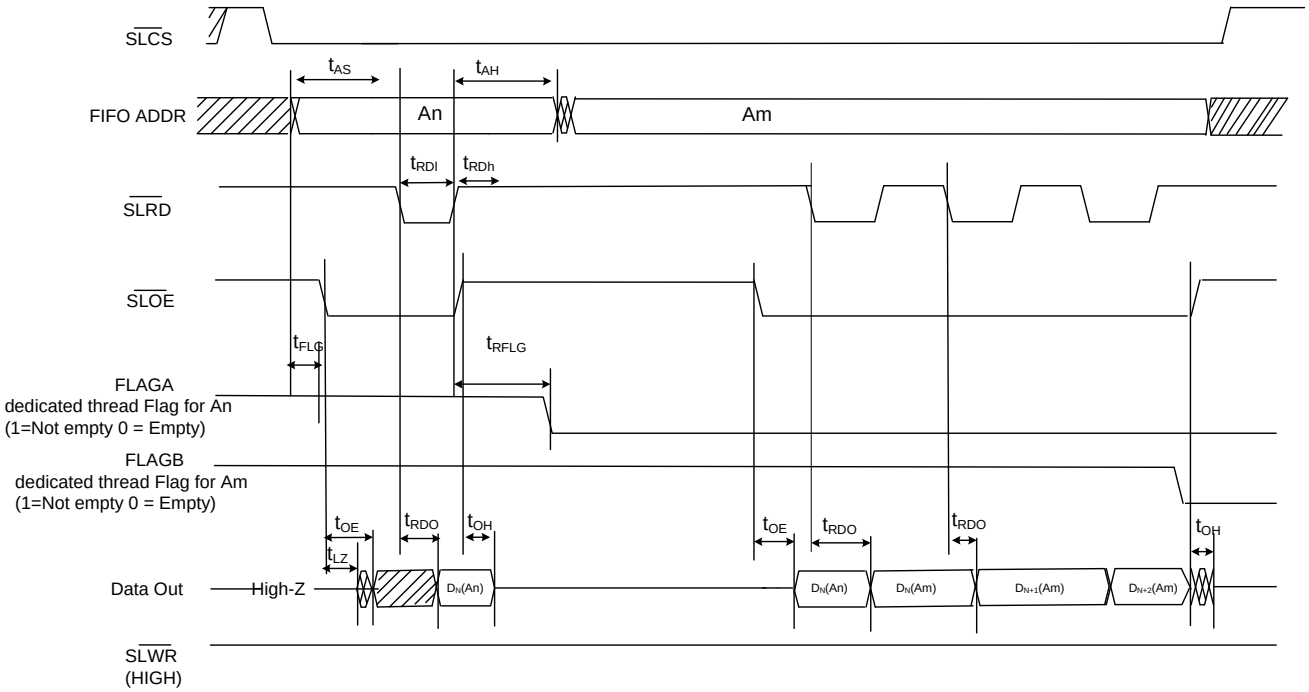
In Figure 13, data N is the first valid data read from the FIFO. For data to appear on the data bus during the read cycle, SLOE# must be in an asserted state. SLRD# and SLOE# can also be tied.

The same sequence of events is also shown for a burst read.

Note In the burst read mode, during SLOE# assertion, the data bus is in a driven state (data is driven from a previously addressed FIFO). After assertion of SLRD# data from the FIFO is driven on the data bus (SLOE# must also be asserted). The FIFO pointer is incremented after deassertion of SLRD#.

Note
6. All parameters guaranteed by design and validated through characterization.

Figure 13. Asynchronous Slave FIFO Read Mode



Asynchronous Slave FIFO Write Sequence Description

- FIFO address is driven and SLCS# is asserted
- SLWR# is asserted. SLCS# must be asserted with SLWR# or before SLWR# is asserted
- Data must be present on the tWRS bus before the deasserting edge of SLWR#
- Deassertion of SLWR# causes the data to be written from the data bus to the FIFO, and then the FIFO pointer is incremented
- The FIFO flag is updated after the tWFLG from the deasserting edge of SLWR.

The same sequence of events is shown for a burst write.

Note that in the burst write mode, after SLWR# deassertion, the data is written to the FIFO, and then the FIFO pointer is incremented.

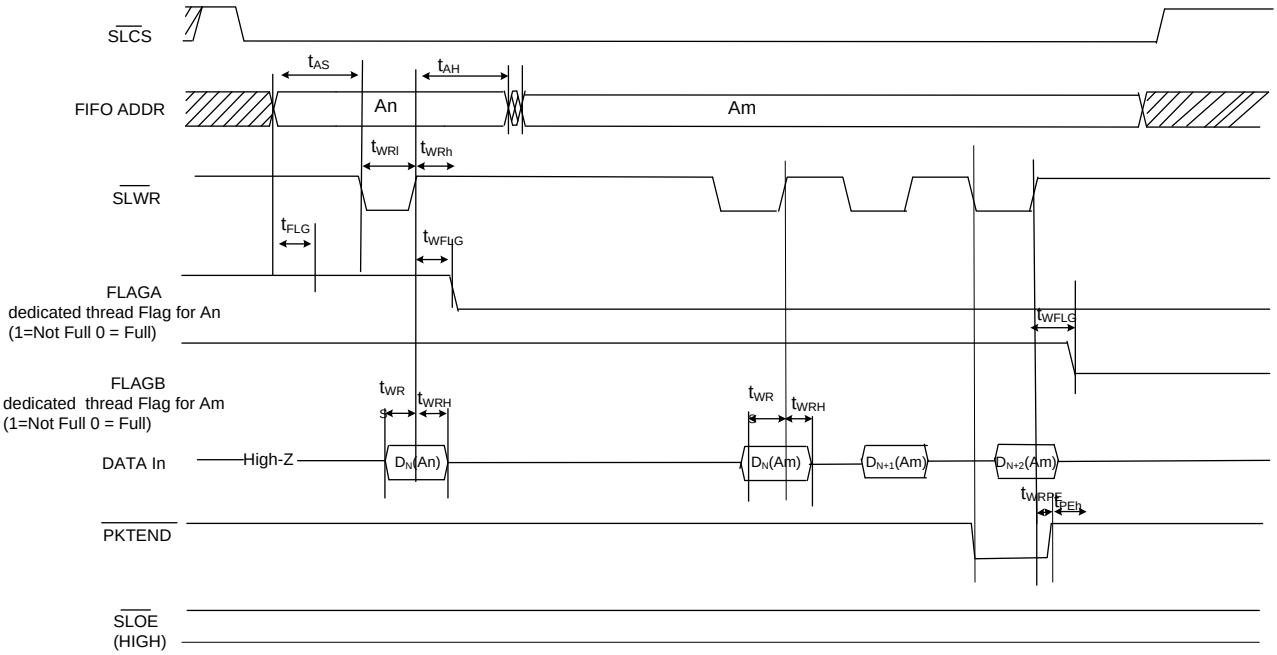
Short Packet: A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

Zero-Length Packet: The external device or processor can signal a zero-length packet (ZLP) to FX3 simply by asserting PKTEND#, without asserting SLWR#. SLCS# and the address must be driven as shown in Figure 14 on page 28.

FLAG Usage: The FLAG signals are monitored by the external processor for flow control. FLAG signals are FX3 outputs that can be configured to show empty, full, and partial status for a dedicated address or the current address.

Figure 14. Asynchronous Slave FIFO Write Mode

Asynchronous Write Cycle Timing



tWRPE: SLWR# de-assert to PKTEND deassert = 2ns min (This means that PKTEND should not be be deasserted before SLWR#)
Note: PKTEND must be asserted at the same time as SLWR#.

Asynchronous ZLP Write Cycle Timing

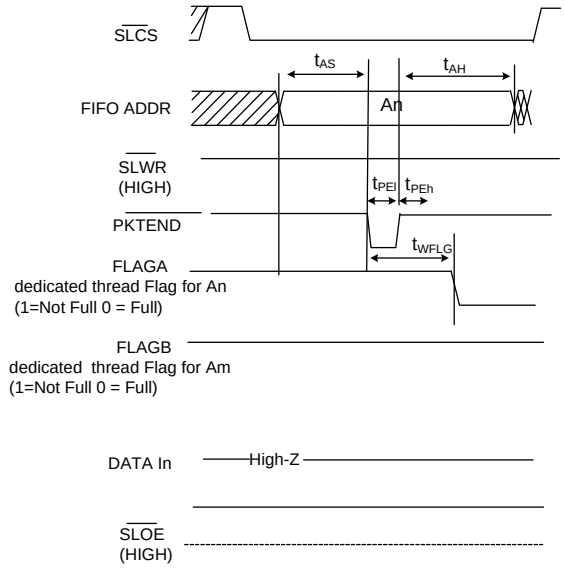


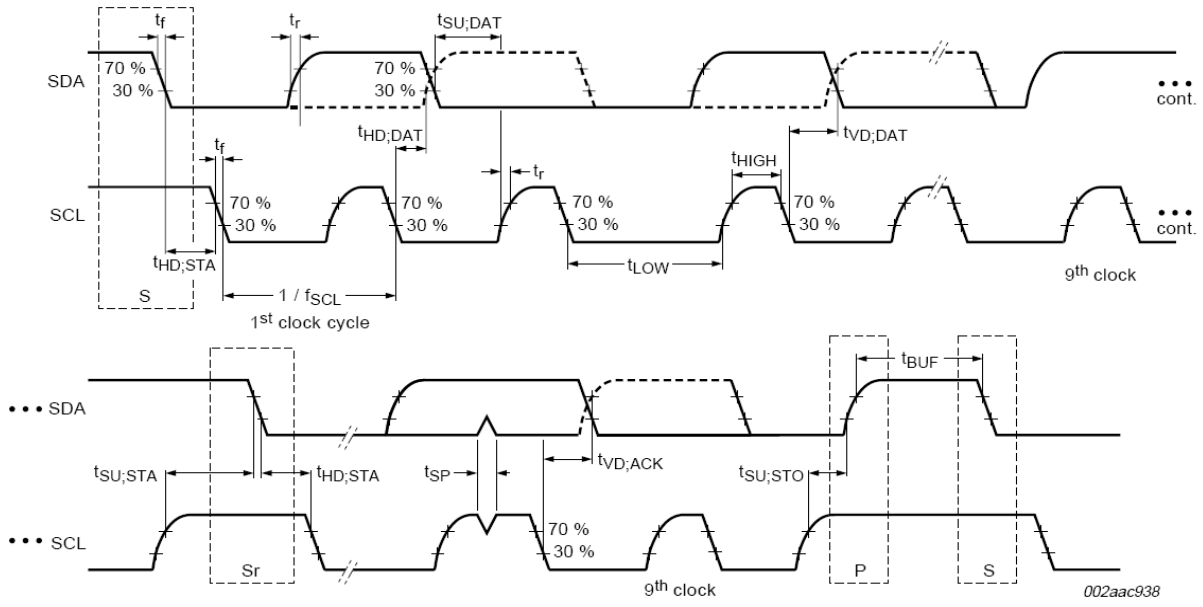
Table 13. Asynchronous Slave FIFO Parameters[7]

Parameter	Description	Min	Max	Units
tRDI	SLRD# low	20	–	ns
tRDh	SLRD# high	10	–	ns
tAS	Address to SLRD#/SLWR# setup time	7	–	ns
tAH	SLRD#/SLWR#/PKTEND to address hold time	2	–	ns
tRFLG	SLRD# to FLAGS output propagation delay	–	35	ns
tFLG	ADDR to FLAGS output propagation delay		22.5	
tRDO	SLRD# to data valid	–	25	ns
tOE	OE# low to data valid	–	25	ns
tLZ	OE# low to data low-Z	0	–	ns
tOH	SLOE# deassert data output hold	–	22.5	ns
tWRI	SLWR# low	20	–	ns
tWRh	SLWR# high	10	–	ns
tWRS	Data to SLWR# setup time	7	–	ns
tWRH	SLWR# to Data Hold time	2	–	ns
tWFLG	SLWR#/PKTEND to Flags output propagation delay	–	35	ns
tPEI	PKTEND low	20	–	ns
tPEh	PKTEND high	7.5	–	ns
tWRPE	SLWR# deassert to PKTEND deassert	2	–	

Serial Peripherals Timing

I^2C Timing

Figure 15. I^2C Timing Definition



Note
7. All parameters guaranteed by design and validated through characterization.

Table 14. I²C Timing Parameters[8]

Parameter	Description	Min	Max	Units
I²C Standard Mode Parameters				
fSCL	SCL clock frequency	0	100	kHz
tHD:STA	Hold time START condition	4	–	µs
tLOW	LOW period of the SCL	4.7	–	µs
tHIGH	HIGH period of the SCL	4	–	µs
tSU:STA	Setup time for a repeated START condition	4.7	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	250	–	ns
tr	Rise time of both SDA and SCL signals	–	1000	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	4	–	µs
tBUF	Bus free time between a STOP and START condition	4.7	–	µs
tVD:DAT	Data valid time	–	3.45	µs
tVD:ACK	Data valid ACK	–	3.45	µs
tSP	Pulse width of spikes that must be suppressed by input filter	n/a	n/a	
I²C Fast Mode Parameters				
fSCL	SCL clock frequency	0	400	kHz
tHD:STA	Hold time START condition	0.6	–	µs
tLOW	LOW period of the SCL	1.3	–	µs
tHIGH	HIGH period of the SCL	0.6	–	µs
tSU:STA	Setup time for a repeated START condition	0.6	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	100	–	ns
tr	Rise time of both SDA and SCL signals	–	300	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	0.6	–	µs
tBUF	Bus free time between a STOP and START condition	1.3	–	µs
tVD:DAT	Data valid time	–	0.9	µs
tVD:ACK	Data valid ACK	–	0.9	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns
I²C Fast Mode Plus Parameters (Not supported at I2C_VDDQ=1.2 V)				
fSCL	SCL clock frequency	0	1000	kHz
tHD:STA	Hold time START condition	0.26	–	µs
tLOW	LOW period of the SCL	0.5	–	µs
tHIGH	HIGH period of the SCL	0.26	–	µs
tSU:STA	Setup time for a repeated START condition	0.26	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	50	–	ns

Note
8. All parameters guaranteed by design and validated through characterization.

Table 14. I²C Timing Parameters[8] (continued)

Parameter	Description	Min	Max	Units
tr	Rise time of both SDA and SCL signals	–	120	ns
tf	Fall time of both SDA and SCL signals	–	120	ns
tSU:STO	Setup time for STOP condition	0.26	–	µs
tBUF	Bus-free time between a STOP and START condition	0.5	–	µs
tVD:DAT	Data valid time	–	0.45	µs
tVD:ACK	Data valid ACK	–	0.55	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns

I²S Timing Diagram

Figure 16. I²S Transmit Cycle

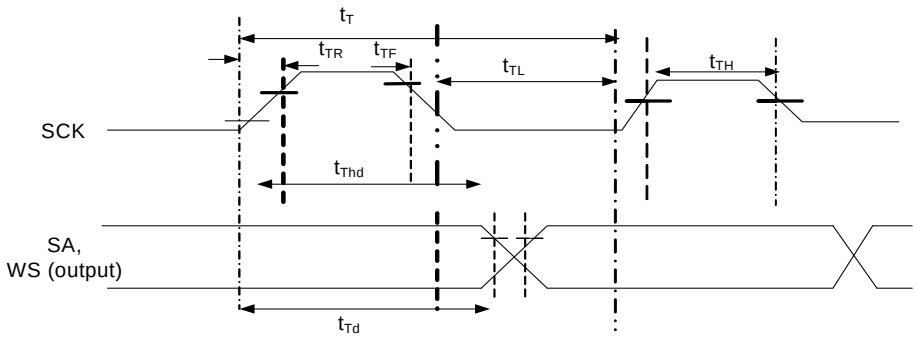


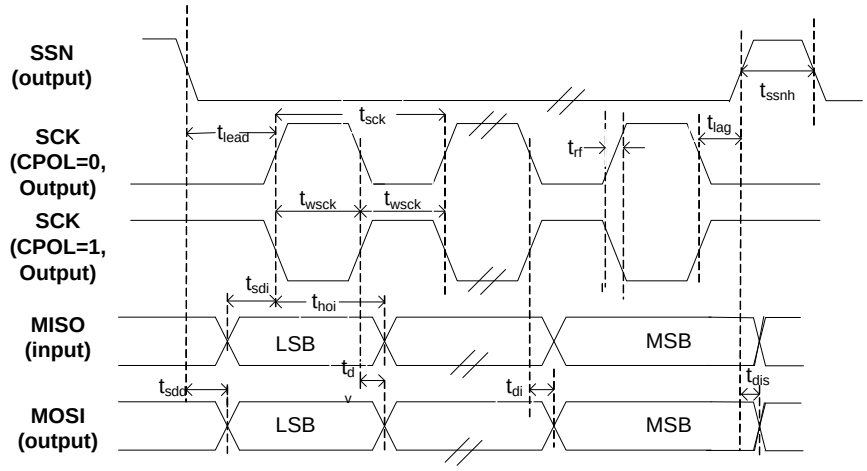
Table 15. I²S Timing Parameters[9]

Parameter	Description	Min	Max	Units
tT	I²S transmitter clock cycle	Ttr	–	ns
tTL	I²S transmitter cycle LOW period	0.35 Ttr	–	ns
tTH	I²S transmitter cycle HIGH period	0.35 Ttr	–	ns
tTR	I²S transmitter rise time	–	0.15 Ttr	ns
tTF	I²S transmitter fall time	–	0.15 Ttr	ns
tThd	I²S transmitter data hold time	0	–	ns
tTd	I²S transmitter delay time	–	0.8tT	ns
Note tT is selectable through clock gears. Max Ttr is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz).				

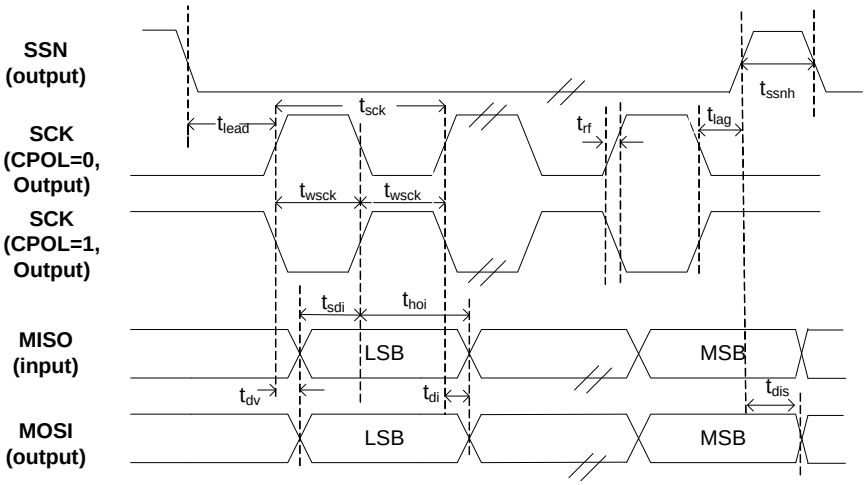
Note
9. All parameters guaranteed by design and validated through characterization.

SPI Timing Specification

Figure 17. SPI Timing



SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

Table 16. SPI Timing Parameters[10]

Parameter	Description	Min	Max	Units
fop	Operating frequency	0	33	MHz
tsck	Cycle time	30	–	ns
twsck	Clock high/low time	13.5	–	ns
tlead	SSN-SCK lead time	1/2 tsck[11]-5	1.5 tsck[11]+ 5	ns
tlag	Enable lag time	0.5	1.5 tsck[11]+5	ns
trf	Rise/fall time	–	8	ns
tsdd	Output SSN to valid data delay time	–	5	ns
tdv	Output data valid time	–	5	ns
tdi	Output data invalid	0	–	ns
tssnh	Minimum SSN high time	10	–	ns
tsdi	Data setup time input	8	–	ns
thoi	Data hold time input	0	–	ns
tdis	Disable data output on SSN high	0	–	ns

Reset Sequence

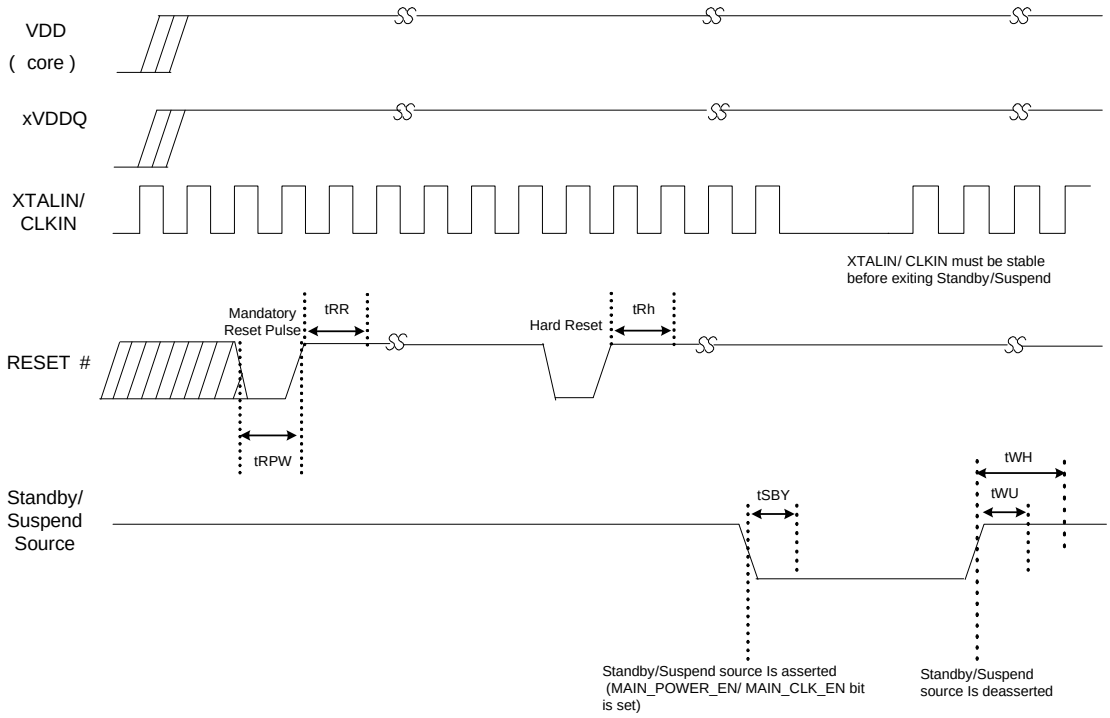
FX3's hard reset sequence requirements are specified in this section.

Table 17. Reset and Standby Timing Parameters

Parameter	Definition	Conditions	Min (ms)	Max (ms)
tRPW	Minimum RESET# pulse width	Clock Input	1	–
		Crystal Input	1	–
tRH	Minimum high on RESET#	–	5	–
tRR	Reset recovery time (after which Boot loader begins firmware download)	Clock Input	1	–
		Crystal Input	5	
tSBY	Time to enter standby/suspend (from the time MAIN_CLOCK_EN/ MAIN_POWER_EN bit is set)	–	–	1
tWU	Time to wakeup from standby	Clock Input	1	–
		Crystal Input	5	–
tWH	Minimum time before Standby/Suspend source may be reasserted	–	5	–

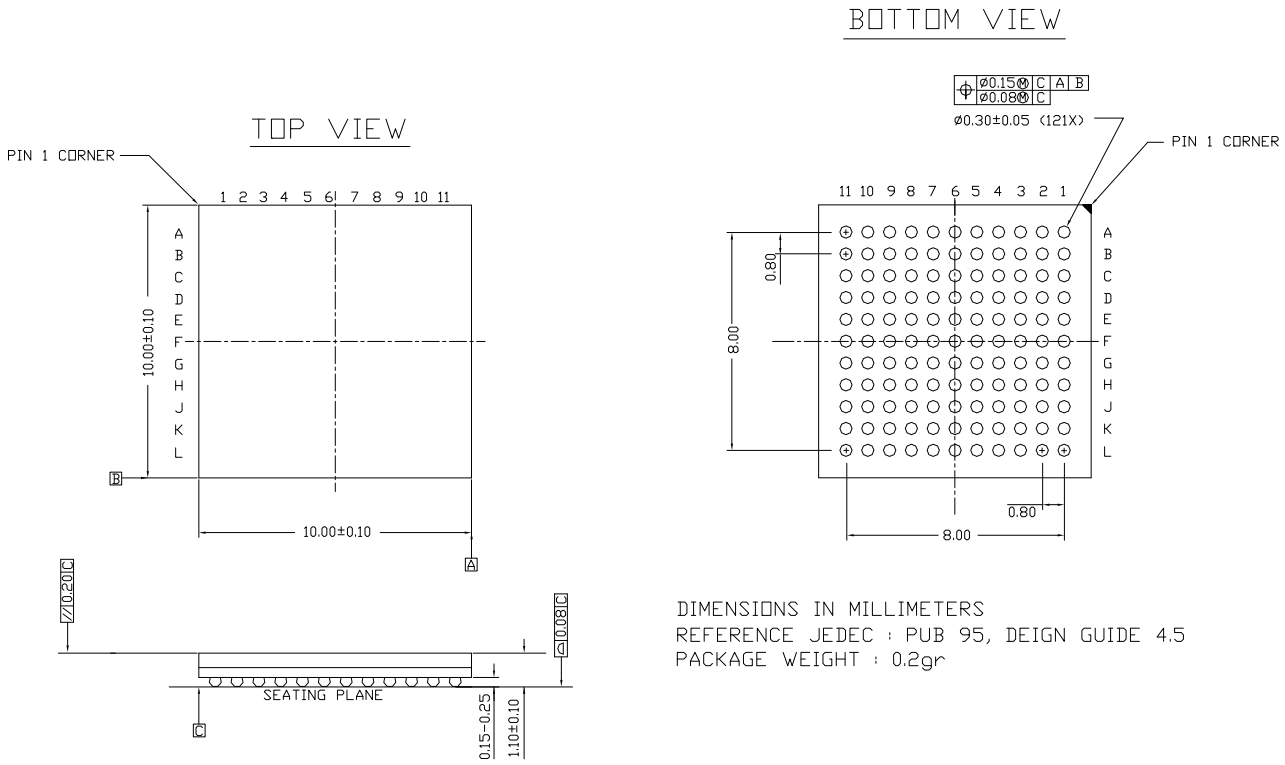
Notes
10. All parameters guaranteed by design and validated through characterization.
11. Depends on LAG and LEAD setting in the SPI_CONFIG register.

Figure 18. Reset Sequence



Package Diagram

Figure 19. 121-Ball FBGA 10 × 10 × 1.2 Diagram



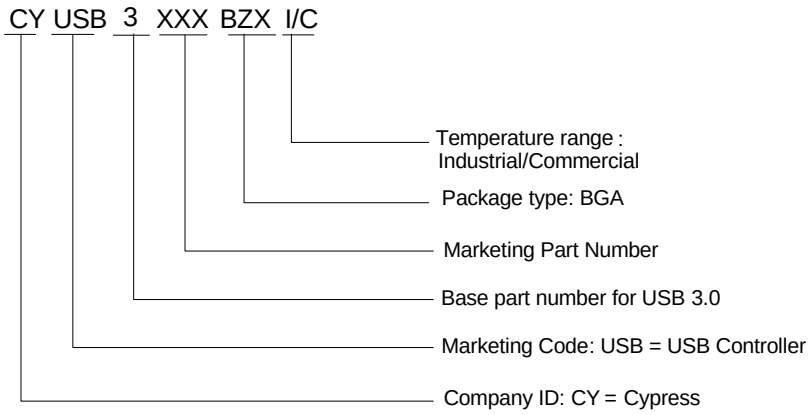
001-54471 *C

Ordering Information

Table 18. Ordering Information

Ordering Code	SRAM (kB)	GPIF II Data Bus Width	Package Type
CYUSB3011-BZXC	256	16-bit	121-ball BGA
CYUSB3012-BZXC	256	32-bit	121-ball BGA
CYUSB3013-BZXC	512	16-bit	121-ball BGA
CYUSB3014-BZXC	512	32-bit	121-ball BGA
CYUSB3014-BZXI	512	32-bit	121-ball BGA

Ordering Code Definition



Acronyms

Acronym	Description
DMA	direct memory access
HNP	host negotiation protocol
MMC	multimedia card
MTP	media transfer protocol
PLL	phase locked loop
PMIC	power management IC
SD	secure digital
SD	secure digital
SDIO	secure digital input / output
SLC	single-level cell
SLCS	Slave Chip Select
SLOE	Slave Output Enable
SLRD	Slave Read
SLWR	Slave Write
SPI	serial peripheral interface
SRP	session request protocol
USB	universal serial bus
WLCSP	wafer level chip scale package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microamperes
µs	microseconds
mA	milliamperes
Mbps	Megabits per second
MBps	Megabytes per second
MHz	mega hertz
ms	milliseconds
ns	nanoseconds
Ω	ohms
pF	pico Farad
V	volts

Document History Page

Document Title: CYUSB301X EZ-USB® FX3 SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2669761	VSO/PYRS	03/06/09	New Datasheet
*A	2758370	VSO	09/01/09	Updated the part# from CYX01XXBB to CYUSB3011-BZXI Changed the title from “ADVANCE” to “ADVANCE INFORMATION” In page 1, the second bullet (Flexible Host Interface), add “32-bit, 100 MHz” to first sub bullet. In page 1, changed the second bullet “Flexible Host Interface” to General Programmable Interface”. In page 1, the second bullet (Flexible Host Interface), removed "DMA Slave Support” and "MMC Slave support with Pass through Boot" sub bullets. In page 1, third bullet, changed "50 µA with Core Power" to "60 µA with Core Power" In page 1, fifth bullet, added "at 1 MHz" In page 1, seventh bullet, added "up to 4MHz" to UART In page 1, Applications Section, move “Digital Still Cameras” to second line. In page 1, Applications Section, added “Machine Vision” and Industrial Cameras” Added ™ to GPIF and FX3. In page 1, updated Logic Block Diagram. In page 2, section of “Functional Overview”, updated the whole section. In page 2, removed the section of “Product Interface” In page 2, removed the section of “Processor Interface (P-Port)” In page 2, removed the section of “USB Interface (U-Port)” In page 2, removed the section of “Other Interfaces” In page 2, added a section of "GPIF II" In page 2, added a section of "CPU" In page 2, added a section of "JTAG Interface" In page 2, added a section of "Boot Options" In page 2, added a section of "ReNumeration" In page 2, added a section of "Power" In the section of “Package”, replaced “West Bridge USB 3.0 Platform” by FX3. In the section of “Package”, added 0.8 mm pitch in front of BGA. Added Pin List (Table 1)
*B	2779196	VSO/PYRS	09/29/09	Features: Added the thrid bullet “Fully accessible 32-bit ARM9 core with 512kB of embedded SRAM” Added the thrid line “EZ USB™ Software and DVK for easy code development” Table 1: Pin 74, corrected to NC - No Connect. Changed title to EZ-USB™ FX3: SuperSpeed USB Controller
*C	2823531	OSG	12/08/09	Added data sheet to the USB 3.0 EROS spec 001-51884. No technical updates.
*D	3080927	OSG	11/08/2010	Changed status from Advance to Preliminary Changed part number from CYUSB3011 to CYUSB3014 Added the following sections: Power, Configuration Options, Digital I/Os, System-level ESD, Absolute Maximum Ratings, AC Timing Parameters, Reset Sequence, Package Diagram Added DC Specifications table Updated feature list Updated Pin List Added support for selectable clock input frequencies. Updated block diagram Updated part number Updated package diagram

Document Title: CYUSB301X EZ-USB® FX3 SuperSpeed USB Controller Document Number: 001-52136				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E	3204393	OSG	03/24/2011	Updated Slave FIFO protocol and added ZLP signaling protocol Changed GPIFII asynchronous tDO parameter Changed Async Slave FIFO tOE parameter Changed Async Slave FIFO tRDO parameter Added tCOE parameter to GPIFII Sync mode timing parameters Renamed GPIFII Sync mode tDO to tCO and tDO_ss0 to tCO_ss0 Modified description of GPIFII Sync tCO (previously tDO) parameter Changed tAH(address hold time) parameter in Async Slave FIFO modes to be with respect to rising edge of SLWR#/SLRD# instead of falling edge. Correspondingly, changed the tAH number. Removed 24 bit data bus support for GPIFII.
*F	3219493	OSG	04/07/2011	Minor ECN - Release to web. No content changes.
*G	3235250	GSZ	04/20/2011	Minor updates in Features.
*H	3217917	OSG	04/06/2011	Updated GPIFII Synchronous Timing diagram. Added SPI Boot option. Corrected values of R_USB2 and R_USB3. Corrected TCK and TRST# pull-up/pull-down configuration. Minor updates to block diagrams. Corrected Synchronous Slave FIFO tDH parameter.
*I	3305568	DSG	07/07/2011	Minor ECN - Correct ECN number in revision *F. No content changes.
*J	3369042	OSG	12/06/2011	Changed tWRPE parameter to 2ns Updated tRR and tRPW for crystal input Added clarification regarding I_{OZ} and I_{IX} Updated Sync SLave FIFO Read timing diagram Updated SPI timing diagram Removed tGRANULARITY parameter Updated I2S Timing diagram and tTd parameter Updated 121-ball FBGA package diagram. Added clarification regarding VCC in DC Specifications table In Power Modes description, stated that VIO1 cannot be turned off at any time if the GPIFII is used in the application Updated Absolute Maximum Ratings Added requirement for by-pass capacitor on $U3RX_{VDDQ}$ and $U3TX_{VDDQ}$ Updated tPEI parameter in Async Slave FIFO timing table Updated Sync Slave FIFO write and read timing diagrams Updated I2C interface tVD:ACK parameter for 1MHz operation Clarified that CTL[15] is not usable as a GPIO Changed datasheet status from Preliminary to Final.
*K	3534275	OSG	02/24/2012	Corrected typo in the block diagram.
*L	3649782	OSG	08/16/2012	Changed part number to CYUSB301X. Added 256 KB range for embedded SRAM. Updated Functional Overview, Other Interfaces, and Clocking sections. Added Pin List for CYUSB3011 and CYUSB3013 parts. Updated Ordering Information with new part numbers.

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