CS311: Computer Architecture Lab

Assignment 5 - Report

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The aim was to implement MemoryLatency delays during Instruction Fetch and Memory Access while developing a pipelined processor Simulator for ToyRISC.

Statistics -

Sl No.	***Program***	***No. of Instructions executed***	***No. of cycles taken***	***Instructions per cycle (IPC)***
1.	*descending.asm*	*277*	*11481*	*0.024127*
2.	*even-odd.asm*	*6*	*249*	*0.024096*
3.	*fibonacci.asm*	*78*	*3175*	*0.024567*
4.	*palindrome.asm*	*49*	*1979*	*0.024760*
5.	*prime.asm*	*29*	*1188*	*0.024411*

Table: *Statistics of Processor performance on Test Programs*

(provided in the assignment)