CS311: Computer Architecture Lab

Assignment 3 - Report

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The aim was to develop a single-cycle processor Simulator for ToyRISC.

Implementation Details

The elements introduced for storage in the latch after each stage is listed below:-

- ➔ *IF_OF Latch*
  - ◆ *Instruction*
- ➔ *OF_EX Latch*
  - ◆ *Immx*
  - ◆ *branchTarget*
  - ◆ *Op1*
  - ◆ *Op2*
- ➔ *EX_IF Latch*
  - ◆ *isBranchTaken*
  - ◆ *branchPC*
- ➔ *EX_MA Latch*
  - ◆ *aluResult*
  - ◆ *Op2*
- ➔ *MA_RW Latch*
  - ◆ *ldResult*

*Additional classes created and instantiated in **class Processor** include-*

- ★ ***Class ControlUnit:*** *It stores opCode in integer and string format. It is initialized by passing the instruction to its instance in the Instruction Fetch stage..*
- ★ ***Class ArithmeticLogicUnit:*** *It stores two operands A and B and also has a reference to the processor's Control Unit to retrieve control flags. The getALUResult() method is used to fetch the ALU result.*

Results -

Sl No.	***Program***	***No. of Instructions executed***	***No. of cycles taken***
1.	*descending.asm*	*277*	*277*
2.	*even-odd.asm*	*6*	*6*
3.	*fibonacci.asm*	*78*	*78*
4.	*palindrome.asm*	*49*	*49*
5.	*prime.asm*	*29*	*29*

Table: *Statistics of Processor performance on Test Programs*

(provided in the assignment)