





OPTIONAL TO DO: inversion of pin order of JST HX connectors for SIO A and SIO B (currently order is backwards from the one inherited from Simple80 - which is my prefered pinout now) (:(but this requires re-routing the board) workaround so far is to install the JST HX connectors backwards to maintain the pin compatiblity with my other SIO boards) VCC Q U-SIO1 SIO1-DIP-40
D0 > RXDA 12
D1 + RXCA 13 DO 40 DO D1 1 D1 RxA_CLK RXCA 13 D2 39 D2 TXDA 15 D3 2 D3 TXCA 14 TxA_CLK SIOA_CLK_HEADER BX CK3 D4 38 D4 RxB_CLK SYNCA 11 D5 3 D5 D[0..7] → CK4 W/RDYA 10 D6 37 D6 D7 4 D7 J-SIO-A1 RTSA ₹×B2CLK SIOA_Conn_01x06 18 SIOCE D-CTSA SIOB_CLK_HEADER_3x2 16 DTRA RESETD 21 RESET DCDA 19 8 M1 M₁D 28 RXDB 36 IORQ VCC TORQ D RXTXCB 27 32 RD RDD-TXDB 25 TxCB 26 CLK 20 CK2D-J-SIO-B1 29 **SYNCB** 30 TNT CI W/RDYB 6 IEI IEID-7 IEO RTSB JP_SIO_IEI0 SIO IEI SIOB_Conn_01x06 23 CTSB A1 34 B/A IEO 🗗 A1 34 A0 33 C/D 5 DCDB 22 SIO IEO JP-SIO-IEOO A[0..7]D GND Channel B SIO 0/1/2 jumpers GND SIO 0 1 JP-T1 -- 1-2 JP-T2 2-3 1-2 JP-T3 1-2 1-2 what to do with unused SIO pins that can be used for general IO T1, 2, 3 configure SIO port B
T1 — Rx and Tx clock source
T2 — Tx pin assignment SI00: GND - RxTx clock on pin 27 - Tx clock on pin 26 - Tx clock on pin 27 T3 — Rx pin assignment - Rx clock on pin 27 - TxDB on pin 25 - Rx clock on pin 28 - TxDB on pin 26 - TxDB on pin 26 - RxDB on pin 28 - RxDB on pin 28 - RxDB on pin 29 S.V.Pantazi (svpantazi@gmail.com) Sheet: /Serial IO (SIO 0,1,2)/ File: serial_IO.sch Title: Cobra 2 (Turbo Spectrum) 10 decoding with GAL22V10 Size: A4 Rev: v5 UPDATE KiCad E.D.A. kicad 4.0.6 ld: 4/5

