

8-Bit CPU Results

Shauryavardhan Shah

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1 RTL Netlist

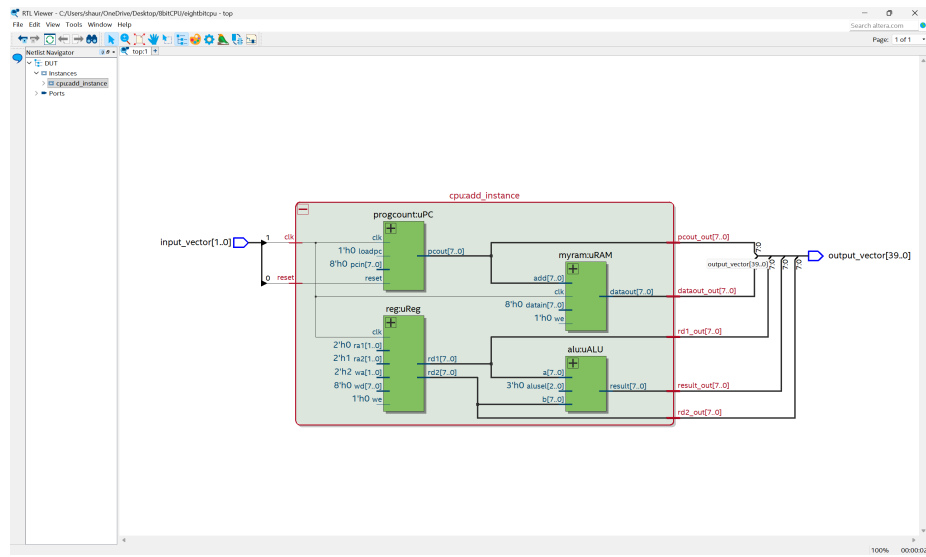


Figure 1: Modular Netlist

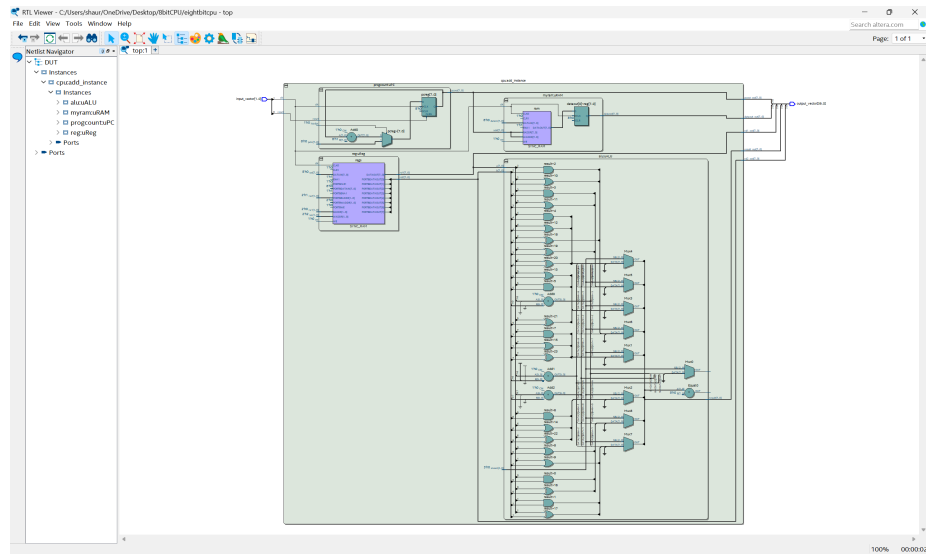


Figure 2: Expanded Netlist

2 Modelsim Screenshots

```

Q: Testbench
File Edit View Bookmarks Window Help
FileView
--
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Loading package std_logic_1164_pkg
-- Compiling entity qpu
-- Compiling architecture structure of qpu
-- Loading entity reg
-- Loading entity mux
-- Loading entity progcount
-- Loading entity sumbit
End time 00:14:15 on Oct 03, 2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

vcom -93 -work work C:/Users/shauro/Desktop/Drive/Desktop/HsicQpu/Testbench.vhdl
Model: Testbench: ModelSim - Intel FPGA Edition vcom 10.5b Compiler 2014.10 Oct 3 2014
Start time 00:14:15 on Oct 03, 2025
Work - testbench: 100 - 0 - work work C:/Users/shauro/Desktop/Drive/Desktop/HsicQpu/Testbench.vhdl
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Compiling entity Testbench
-- Compiling architecture behavior of Testbench
End time 00:14:15 on Oct 03, 2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

vsim -93 -lps -l altera -l ipm -l ngate -l altera_mf -l altera_inas -l fiftyfivem -l rti_work -l work -mupdate="acc" Testbench
vcom -93 -work work C:/Users/shauro/Desktop/Drive/Desktop/HsicQpu/Testbench.vhdl
Start time 00:14:17 on Oct 03, 2025
Loading ipm
Loading std_textio(body)
Loading work.std_logic_1164(body)
Loading work.testbench(behave)
Loading work.dot(behave)
Loading work.numeric_std(body)
Loading work.testbench
Loading work.reg(acc2)
Loading work.alteracc1
Loading work.progcount(acc3)
Loading work.symbit(acc4)

add wave *
view structure
  show pane.structure.interior.csb.body.struct
view signals
  show pane.signals.interior.csb.body.time
run -all
** WARNING: SINGRDC_FTD_*: parameter detected, returning FALSE
Time: 0 ps Iteration: 0 Instance: /testbench/dot_instance/add_instance/AUT
** Note: SUCCESS: all waves named.
Time: 139 ns Iteration: 0 Instance: /testbench
[PSM >]

```

