8-Bit CPU Results

Shauryavardhan Shah

July 2025

1 RTL Netlist

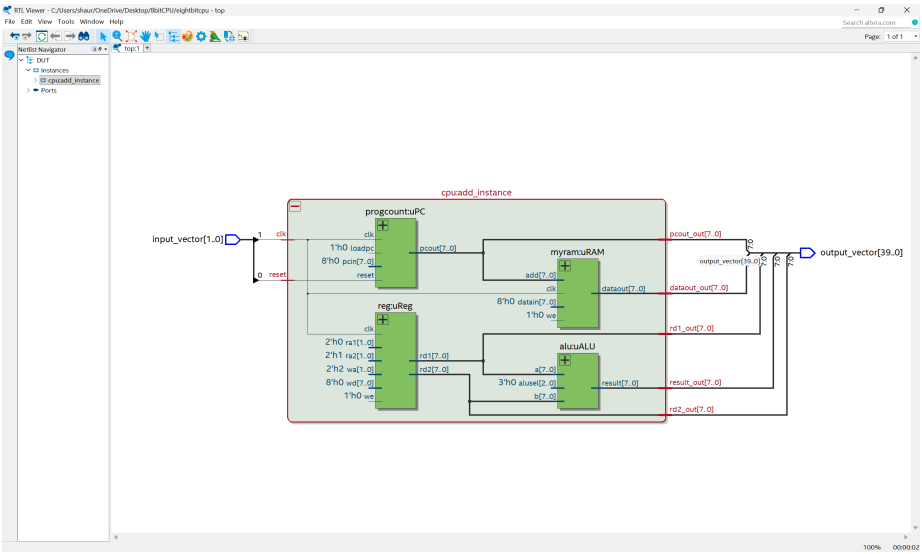

Figure 1: Modular Netlist

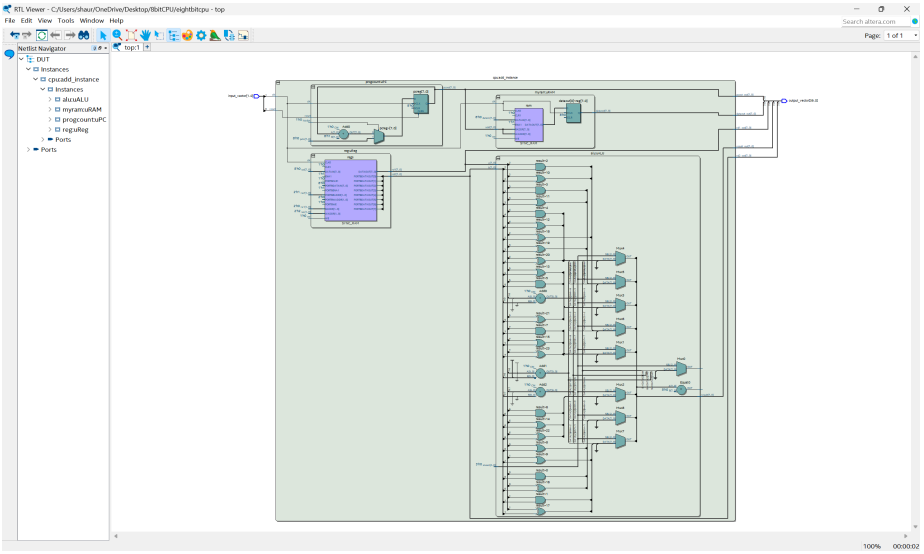

Figure 2: Expanded Netlist

2 Modelsim Screenshots

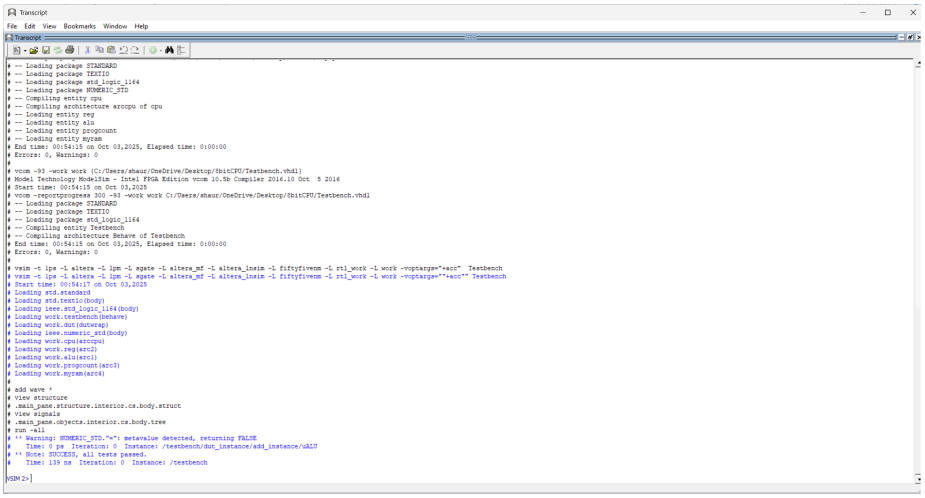

Figure 3: Transcript

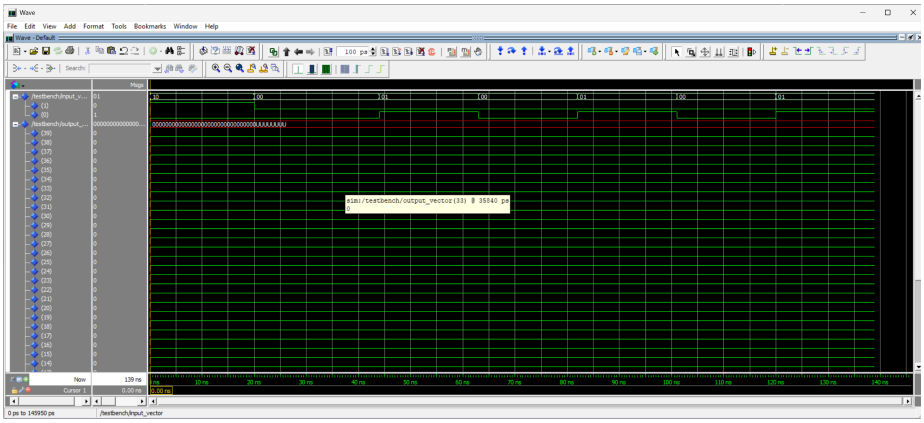

Figure 4: Waveform

Note: The red wavefrom in the Modelsim Window is due to an initial undefined value in VHDL, the test cases pass nonetheless.