

CS 161 Lab 6
TA: Jose Rodriguez

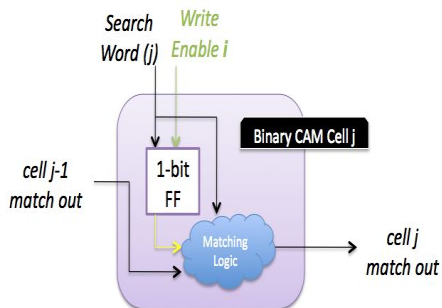
Team Leader: Selik Samai

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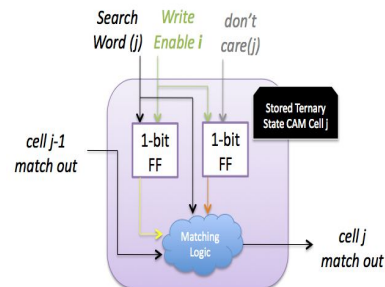
Remarks:

First, we created the binary CAM cell, Stored Ternary State CAM cell, Ternary at Input CAM cell

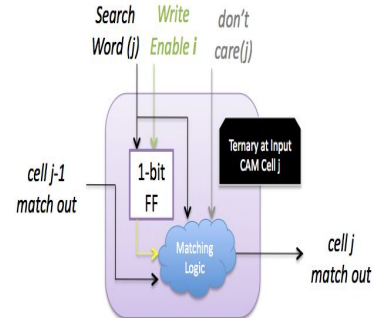
BCAM



SCAM



TCAM



For each CAM, we created the entity with clk, rst, we, search_bit, dont_care_bit and match_bit_in all as input and a match_bit_out as output. In our TB, we wait for clock_period * 2 when loading the addresses

For the STCAM, we used the following code for the don't care bit.

```
else
    if (cell_search_bit = curr_bit or dont_care = '1') and cell_match_bit_in = '1' then
        cell_match_bit_out <= '1';
    else
        cell_match_bit_out <= '0';
    end if;
```

We implemented tests to verify results but were unclear on whether or not our implementation of the STCAM was correct based off the given specs.