1 | JFET CONCEPTS

The concept of the field-effect phenomenon was the basis for the first proposed solid-state transistor. Patents filed in the 1920s and 1930s conceived and investigated the transistor shown in Figure 13.1. A voltage applied to the metal plate modulated the conductance of the semiconductor under the metal and controlled the current be- tween the ohmic contacts. Good semiconductor materials and processing technology were not available at that time, so the device was not seriously considered again until the 1950s.

The phenomenon of modulating the conductance of a semiconductor by an elec- tric field applied perpendicular to the surface of a semiconductor is called field effect. This type of transistor has also been called the unipolar transistor, to emphasize that only one type of carrier, the majority carrier, is involved in the operation.

1.1 Basic PN JFET Construction

The first type of field-effect transistor is the pn junction field-effect transistor, or pn JFET. A simplified cross section of a symmetrical device is shown in Figure 13.2. The n region between the two p regions is known as the channel and, in this n-channel device, majority carrier electrons flow between the source and drain terminals. The source is the terminal from which carriers enter the channel from the external circuit, the drain is the terminal where carriers leave, or are drained from, the device, and the gate is the control terminal. The two gate terminals shown in Figure 13.2 are tied to- gether to form a single gate connection. Since majority carrier electrons are primarily involved in the conduction in this n-channel transistor, the JFET is a majority-carrier device.

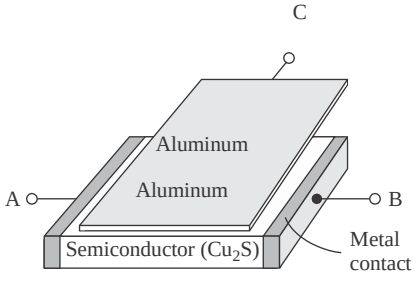

Figure 13.1 | Idealization of the Lilienfeld transistor. *(From Pierret [10].)*

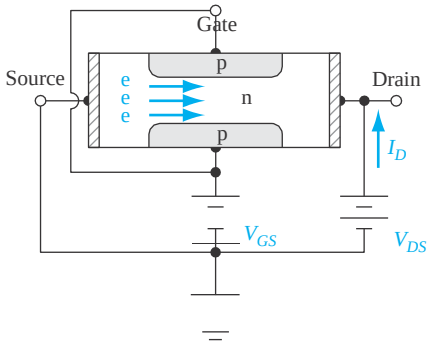

Figure 13.2 | Cross section of a symmetrical n-channel pn junction FET.

1.2. PN JFET Operation.

Operation-1

V_{GS} Changes, and V_{ds} Constant.

Case 1 V_{GS}=0

Figure 13.3a shows an n-channel pn JFET with zero volts applied to the gate. If the source is at ground potential, and if a small positive drain voltage is applied, a drain current I_D is produced between the source and drain terminals. The n channel is essentially a resistance so the I_D versus V_{DS} characteristic, for small V_{DS} values, is approximately linear, as shown in the figure.

Case 2 V_{GS}=-V1

When we apply a voltage to the gate of a pn JFET with respect to the source and drain, we alter the channel conductance. If a negative voltage is applied to the gate of the n-channel pn JFET shown in Figure 13.3, the gate-to-channel pn junction becomes reverse biased. The space charge region now widens so the channel region becomes narrower and the resistance of the n channel increases. The slope of the I_D versus V_{DS} curve, for small V_{DS}, decreases. These effects are shown in Figure 13.3b.

Case 3 V_{GS}=-V3

If a larger negative gate voltage is applied, the condition shown in Figure 13.3c can be achieved. The reverse-biased gate-to-channel space charge region has completely filled the channel region. This condition is known as ***pinchoff*.** The drain current at pinchoff is essentially zero, since the depletion region isolates the source and drain terminals. Figure 13.3c shows the I_D versus V_{DS} curve for this case, as well as the other two cases.

The current in the channel is controlled by the gate voltage. The control of the current in one part of the device by a voltage in another part of the device is the basic transistor action. This device is a normally on or *depletion mode* device, which means that a voltage must be applied to the gate terminal to turn the device off.

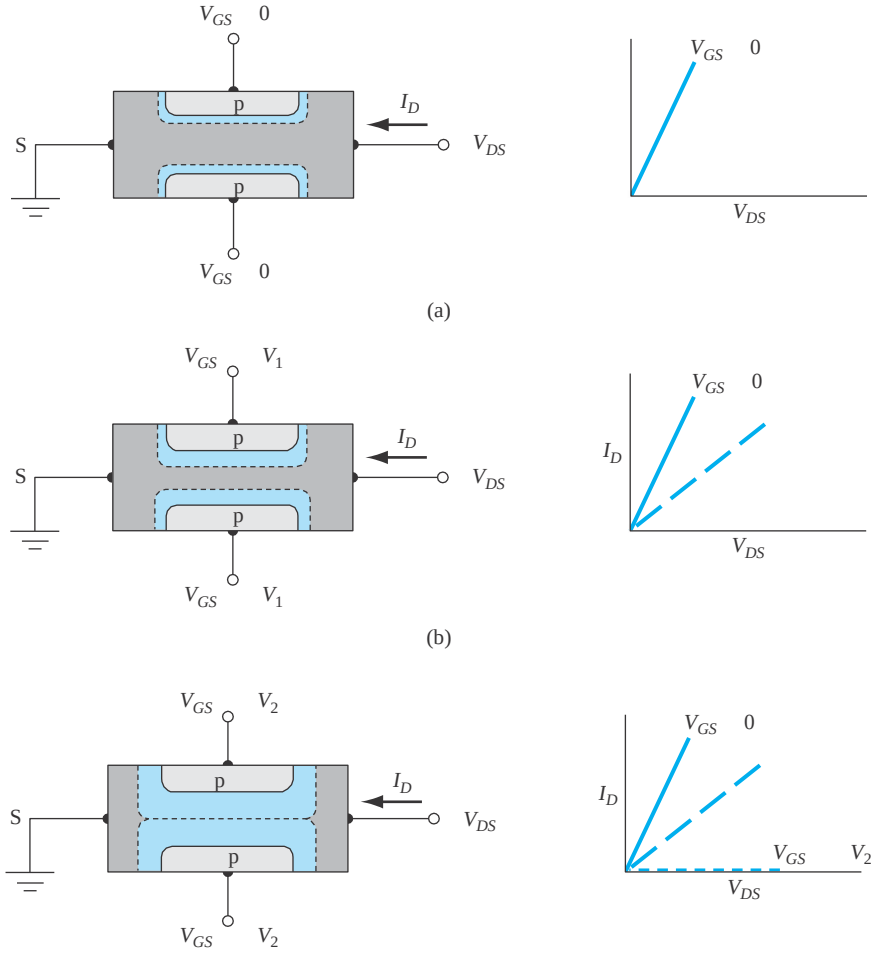

Figure 13.3 | Gate-to-channel space charge regions and *I–V* characteristics for small V_{DS} values and for (a) zero gate voltage, (b) small reverse-biased gate voltage, and (c) a gate voltage to achieve pinchoff.

Operation-2
V_{GS} =0, and V_{ds} Changes
Case 1 V_{DS}=+

Now consider the situation in which the gate voltage is held at zero volts, V_{GS} 0, and the drain voltage changes. Figure 13.4a is a replica of Figure 13.3a for zero gate voltage and a small drain voltage. As the drain voltage increases (positive), the gate-to-channel pn junction becomes reverse biased near the drain terminal so that the space charge region extends further into the channel.

Case 2 V_{DS}=++

The channel is essentially a resistor, and the effective channel resistance increases as the space charge region widens; therefore, the slope of the I_D versus V_{DS} characteristic decreases as shown in Figure 13.4b.

Case 3 V_{DS}=+++

The effective channel resistance now varies along the channel length and, since the channel current must be constant, the voltage drop through the channel becomes dependent on position

If the drain voltage increases further, the condition shown in Figure 13.4c can result. The channel has been pinched off at the drain terminal. Any further increase in drain voltage will not cause an increase in drain current. The *I–V* characteristic for this condition is also shown in this figure.

The drain voltage at pinchoff is referred to as V_{DS}(sat). For V_{DS} V_{DS}(sat), the transistor is said to be in the saturation region and the drain current, for this ideal case, is independent of V_{DS}. At first glance, we might expect the drain current to go to zero when the channel becomes pinched off at the drain terminal, but we will show why this does not happen.

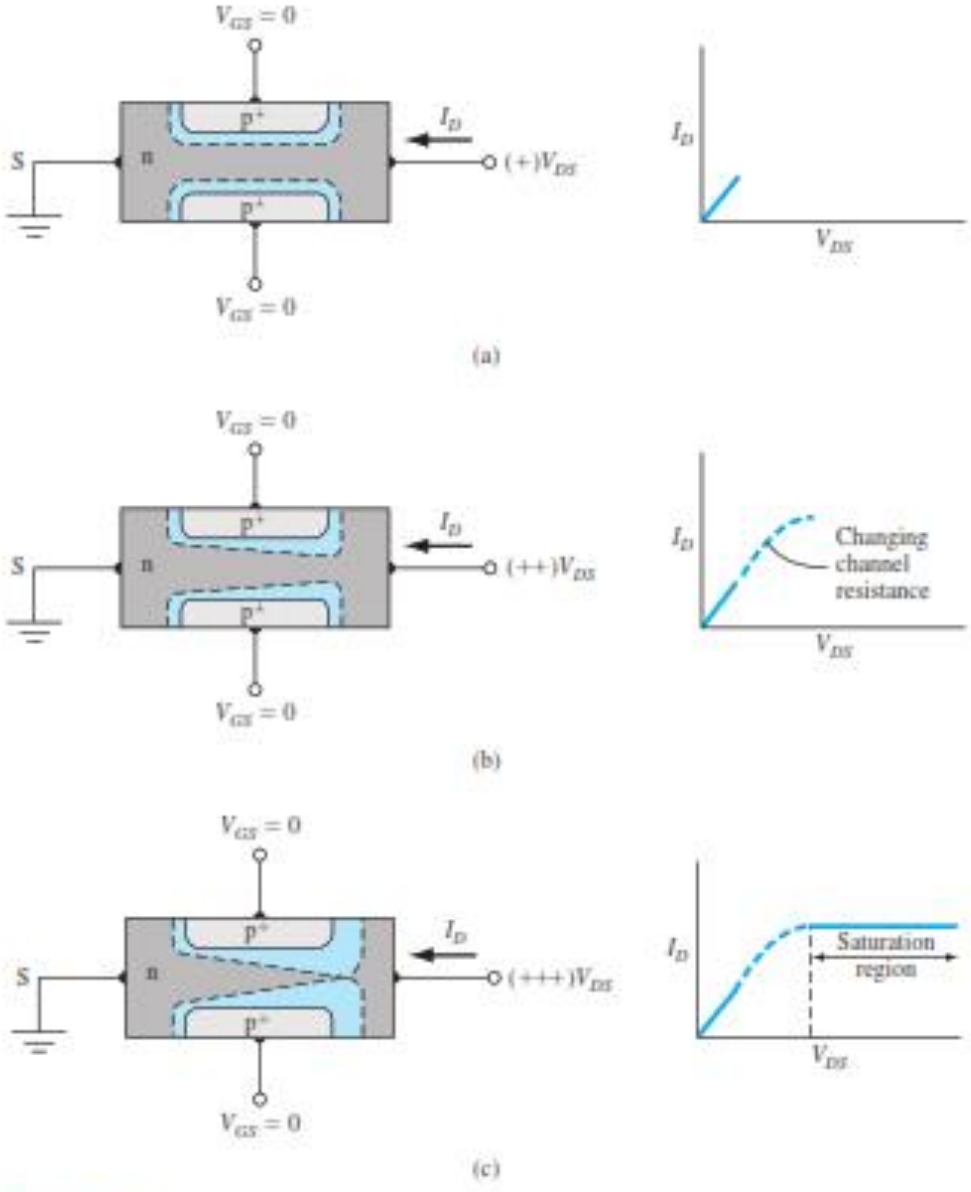

Figure 13.4 | Gate-to-channel space charge regions and I–V characteristics for zero gate voltage and for (a) a small drain voltage, (b) a larger drain voltage, and (c) a drain voltage to achieve pinchoff at the drain terminal.