DIGITAL VOLTMETERS

(source: www.eeeguide.com)

RAMP technique :

- Here unknown voltage is converted into a time interval.
- Principle is based on the measure of time taken by a linear RAMP to reach ground level from the given input voltage level under measurement OR vice versa.
- The time interval is measured using an electronic counter & the count is displayed as a measured value.

fig

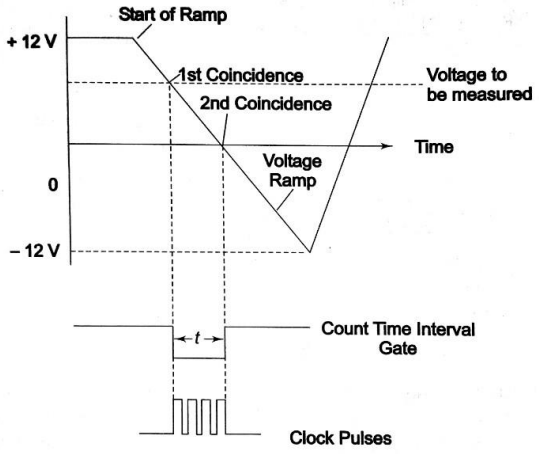


Fig. 5.1 Voltage to time conversion

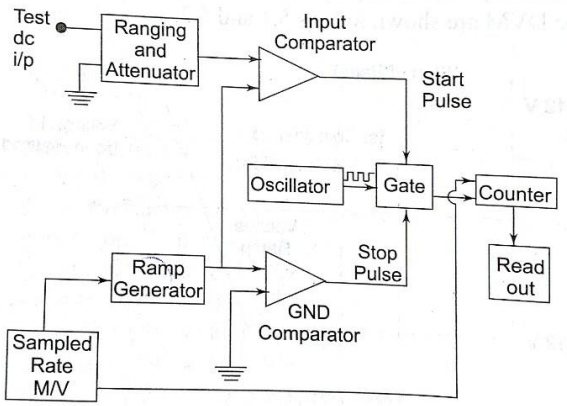


Fig. 5.2 Block diagram of ramp type DVM

at the start,

- Sample rate generator generates a pulse which starts the RAMP generator and reset the counter.
- When the RAMP voltage is same as the input test voltage, then the Input comparator generates a pulse to start the counter.
- When the RAMP voltage reaches ground level, the Ground comparator generates a pulse to stop the counter.
- The counter output is displayed on a display unit which is the measure of the input test voltage.

Dual slope integrating type DVM

Principle :

- The input voltage e_i to be measured is integrated for a fixed time interval t_1 .
- The slope of the positive RAMP generated by integrator is proportional to the input voltage e_i.

- After interval t_1 , the input of the integrator is disconnected from 'e_i' and connected to a negative fixed reference voltage '$–e_r$' . Hence, integrator now produces negative RAMP voltage (since capacitor starts charging towards –ve voltage $–e_i$).

The slope of the –ve RAMP is fixed as $-e_r$ is a fixed value.

- The time 't_2' taken by –ve RAMP to reach ground level voltage is directly proportional to the input voltage e_i , which is converted into the appropriate reading measuring e_i .

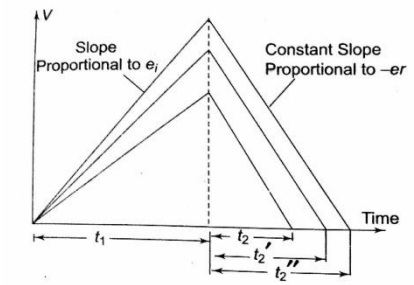


Fig. 5.3 Basic principle of dual slope type DVM

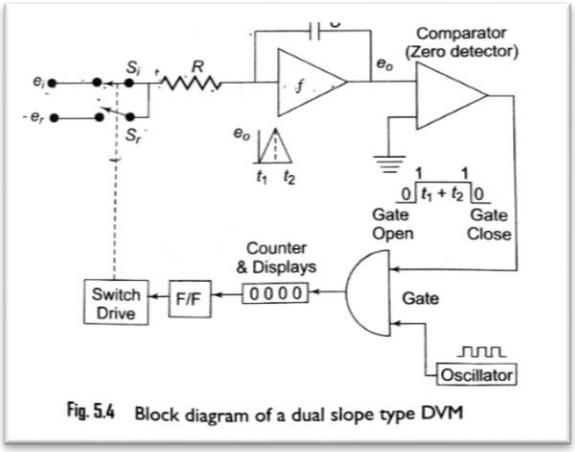


Fig. 5.4 Block diagram of a dual slope type DVM

At the start, Flip flop is triggered to generate output logic '0' which closes switch s_i and opens switch s_r .

As the input voltage e_i is connected to the integrator, the capacitor starts charging towards e_i . Once it exceeds zero voltage, comparator opens the gate allowing the pulses to counter and counter starts counting . When it reaches a fixed count say 9999, on the next pulse it is reset to 0000. This event triggers the flip flop to produce output logic '1', which closes s_r and opens s_i. Now the integrator capacitor starts charging towards charging negative voltage $–e_r$, and counter continuous counting from zero.

When it reaches ground level, again comparator (o/p-0) triggers the gate to close it and pulses are not allowed to counter.

- The final count in the counter is proportional to e_i as shown below.

- during +ve RAMP, when the counter reaches fixed count, output voltage of RAMP is e_o, it is produced in time period t_1.

$$e_o = -\frac{1}{RC}\int_0^t e_i\,dt = -\frac{e_i\,t_1}{RC}$$

- when the –ve RAMP is generated, the capacitor discharges from e_o and reaches voltage in the time t_2 .

During discharging

$$e_o = \frac{1}{RC}\int_0^{t_2} -e_r\,dt = -\frac{e_r\,t_2}{RC} \qquad (5.2)$$

Subtracting Eqs 5.2 from 5.1 we have

$$e_o - e_o = \frac{-e_r\,t_2}{RC} - \left(\frac{-e_i\,t_1}{RC}\right)$$

$$0 = \frac{-e_r\,t_2}{RC} - \left(\frac{-e_i\,t_1}{RC}\right)$$

$$\Rightarrow \quad \frac{e_r\,t_2}{RC} = \frac{e_i\,t_1}{RC}$$

$$\therefore \quad e_i = e_r\,\frac{t_2}{t_1} \qquad (5.3)$$

If the oscillator period equals T and the digital counter indicates n_1 and n_2 counts respectively,

$$e_i = \frac{n_2\,T}{n_1\,T}e_r \quad \text{i.e.} \quad e_i = \frac{n_2}{n_1}e_r$$

$\therefore$

Now, n_1 and e_r are constants. Let $K_1 = \frac{e_r}{n_1}$. Then $e_i = K_1\,n_2$ (5.4)

SRK

Advantages:

1) The reading accuracy is independent of RC time constant and as well the frequency of the oscillator.
2) Any spurious noise gets averaged out during integration. Hence, it has good noise rejection capability.
3) Accuracy upto ± 0.05 %.

ADC principles :

1) Direct compensation or Counter Type:

An internal voltage is produced which increases from zero in steps. This is compared with the unknown input voltage. When both are same, the number of steps generated to reach the full compensation is taken as the digital equivalent value of analog input voltage.

Staircase RAMP :

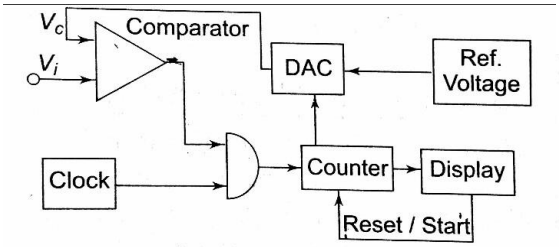


Fig. 5.8 Block diagram of a staircase ramp type

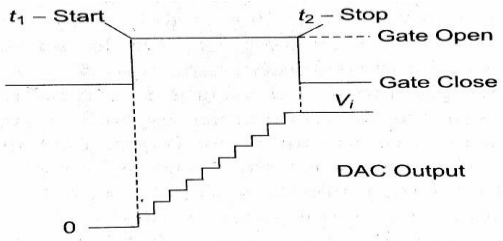


Fig. 5.9 Staircase waveform

- At start, a reset makes counter to reset to '0', say at 't_1'.
- When V_c is just greater than zero, comparator output opens gate. The counter starts counting from t_1.
- When V_c reaches V_i, comparator output closes gate at (full compensation) t_2 (say).
- The counts counted and its value in binary is the digital equivalent value of input V_i.

Advantages:

1) Has high input impedance when the compensation is reached
2) Simple hardware
3) Clock has no effect on accuracy.

Disadvantage:

1) The system measures the input voltage value at the instant of reaching the compensation, but not the value at the start of measuring.
2) Until the full compensation is reached, the input impedance is low, which can influence the accuracy.

Successive approximation type ADC :

- Uses DAC like direct compensation type ADC.
- Here DAC input do not start from all binary input 0000, but starts from the binary input which is equivalent to half of its full binary input.
  Ex : for 4 digit binary 1000 – as input. (MSB as 1)
- Again output of DAC is compared with input voltage V_i .

(1) If the DAC output is higher than the input voltage V_i, then the present MSB is made zero and next MSB is set.

(2) If the DAC output is less than the input voltage V_i, then the present MSB is retained as it is and next MSB is set.

This process is continued till last bit i.e LSB is reached.

- This is the process of generating approximate output in each iteration and to reach the required level of input voltage, which happens always in 'N' steps only, where N is the number of binary bits of DAC like 4,8,10, …

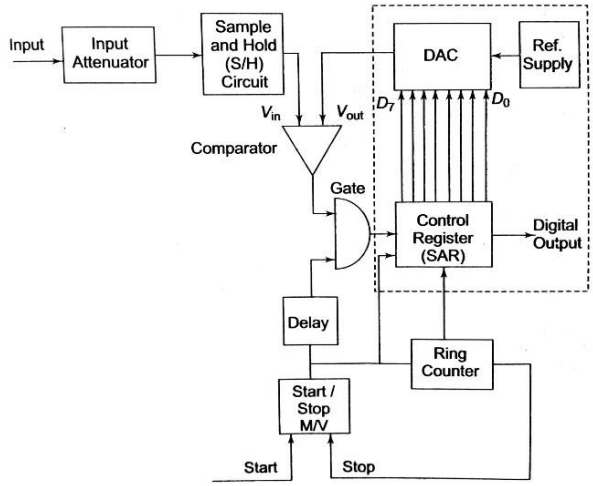


Fig. 5.10 Successive approximation DVM

- Sample and hold circuit is used to maintain constant input voltage for the input of comparator from the instant of start of measurement till the end instant of measurement.

- A start pulse is applied to the start-stop multivibrator, which sets a 1 in MSB of the control register (SAR).
- This makes DAC to develop half of full voltage (reference voltage).
- The convertor output is compared with input voltage by the comparator.
- If the DAC output is less than input voltage, the comparator produce an output which makes SAR to retain the present MSB as logic 1.
- If the DAC output is greater than the input voltage, then comparator output makes the SAR to reset the present MSB.
- Next, ring counter advances one count shifting a '1' in next MSB of SAR. The output of DAC is compared with the input voltage and the present MSB is retained or reset as above.
- The above cycle of setting/resetting present MSB bit and ring counter counting continuous till the 'N' number of cycles corresponding to N bit of SAR, after which the count and measurement cycle stops.
- The setting of SAR after the last cycle is the ADC output for given input voltage.
- In the N^{th} cycle the DAC output is approximately equal to input voltage.

Example:

Let a 4 bit DAC is used ($D_3D_2D_1D_0$) with 4V reference voltage. That is, it gives 4V output (V_{DAC}) for digital input 1111. Let the applied input voltage V_{in} is 1.3V. Following table gives the iterations of measurement.

Step No	SAR setting	DAC output	Compare V_{DAC} with V_{in}	Action
1	1000	2V	$V_{DAC} > V_{in}$	Reset present MSB D_3 and set next MSB D_2
2	0100	1V	$V_{DAC} < V_{in}$	Retain present MSB D_2 and set next MSB D_1
3	0110	1.5V	$V_{DAC} > V_{in}$	Reset present MSB D_1 and set next MSB D_0
4	0101	1.25V	$V_{DAC} < V_{in}$	Retain present MSB D_0; ***hence output is 0101***

Hence, digital output corresponding to 1.3V is 0101, which corresponds to 1.25V of DAC.

If the applied input is 1.2V, then in the last step, 1.25V > 1.2V.
Hence, D_0 bit is reset and the output is 0100, which corresponds to 1V of DAC.

DIGITAL INSTRUMENTS

•The parameters that are normally measured in a laboratory environment using digital instruments are (1) voltage (2) current (3) power (4) frequency and (5) digital logic outputs. These input parameters are analog in nature. They are converted to equivalent digital value using Analog to Digital Converters (ADCs).

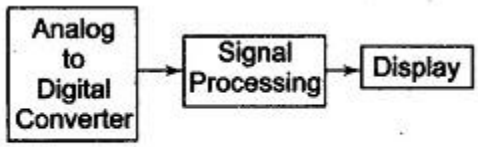


Fig. 6.1 Building Block of a Digital Instrument

In the above setup, display can be analog or digital. If analog, then DAC is required.

DIGITAL MULTIMETERS

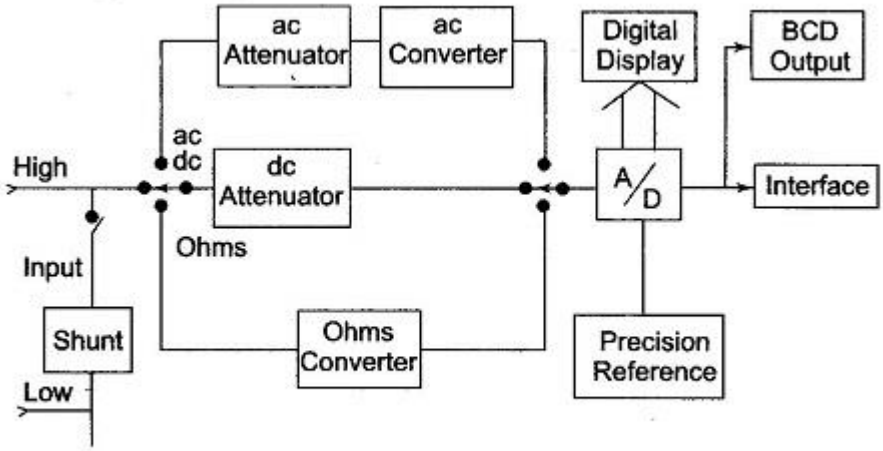


Fig. 6.2 (a) Digital Multimeter

Digital Multimeters are used to measure ac/dc voltages, dc currents and resistance.
Output is a digital display.
Ac voltage is converted into dc voltage using rectifiers.
A constant current is passed through the resistance under measurement to produce a proportional dc voltage.

Analog Meters V/S Digital Meters

Analog Meters:

- **A**nalog meters donot require power supply to operate and give a better indication of changes of output and suffers less from electric noise and isolation problems.
- They are simple and inexpensive.

Digital Meters:

- They have high accuracy, high input impedance, small in size (portable)
- Gives unambiguous reading even from a greater viewing distances

- In addition to the output reading, other forms of the output for further processing is available.
- Three categories of digital meters are,

1 Panel meters

2 Bench meters

3 System meters

- Panel meters are usually placed/fixed at one location.
- Bench and System meters are portable and are often multimeters, which can be used to measure voltage, currents, resistance over several ranges.

Panel Meters

- Available in varieties of functions.
- Display: basic 3 digit (±0.1%) to 4½ digits/4 ¾ digits with accuracy of ±0.005%.
- Can accept DC voltage from few microvolts to 20 volts, ac voltage (true RMS measurements), line voltage, strain gauge bridges of many types (meter provides bridge excitation), RTDs (meter provides sensor excitation), thermocouples of many type (meter provides cold junction compensation and linearization) and frequency inputs (example- pulses from tachometer).

Bench Meters

- They are hand held type meters, inexpensive, 3 ½ digit to 5 ½ digits with 1 microvolt resolution.
- Digital nano voltmeters and pico ammeters are available

System Type Meters

They are designed to provide the basic analog conversion function in DVMs or DMMs assembled with other interfacing peripherals like data acquisition systems. A microprocessor can be used to provide several mathematical functions in addition to managing the meter operations. AC and DC voltages and resistance modes are available. They are usually costlier.

Computation of scientific expressions are possible.

Mathematical functions usually include,

1. null
2. first reading and difference can be subtracted from each successive reading and difference can be displayed.
3. function STAT accumulates reading and calculates mean and variance.
4. with dBm(R), the user enters the resistance value R and all the readings are displayed as power dissipated in R, in decimals.
5. with THMS°F, the temperature of a thermistor probe is displayed in degree Fahrenheit or degree centigrade.
6. function (X-Z)/Y provides offsetting and scaling with user entered Z and Y constants. X is reading.
7. function ((X-Z)/Y)*100 provides percentage deviation.
8. 20log(X/Y), displays X in decibels relative to value Y.

Block Diagram of Digital Multimeter

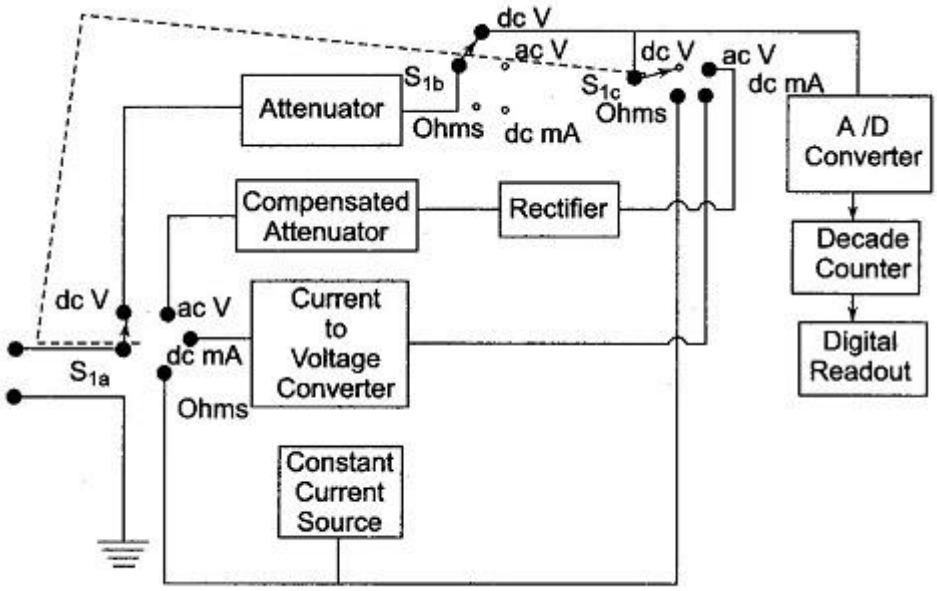


Fig. 6.2 (b) Block Diagram of a Basic Digital Multimeter

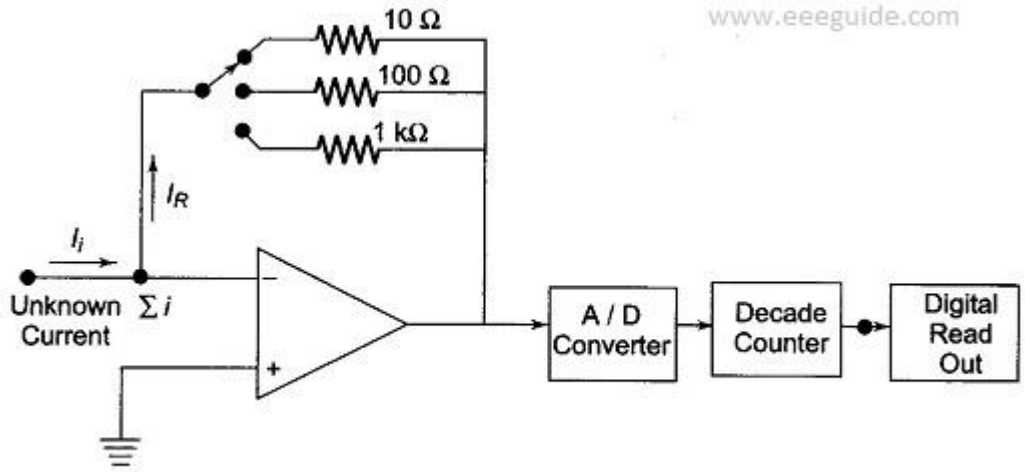


Fig. 6.2 (c) Current to Voltage Converter

(1) AC voltage is converted into dc voltage using rectifiers and filters.

(2) Current is converted into voltage by passing the current through precision low shunt resistance. In the above circuit, the input current is applied to op-amp at the summing junction. The current I_R is same as current I_i, since the terminal of junction acts as virtual ground. The voltage drop across feedback resistor is measured.

(3) Resistance is measured by passing low current generated from a constant current source. Voltage drop across the resistor is measured.

The dc analog voltage for the (i) dc input voltage or (ii) corresponding ac input voltage or (iii) corresponding resistance, is applied to an A/D converter. Output of A/D converter is a measure of the input parameter, which is displayed on the digital display.

DIGITAL FREQUENCY METER

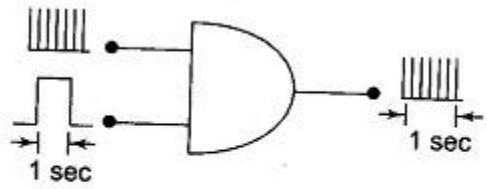


Fig. 6.4 Principle of Digital Frequency Measurement

- The signal whose frequency is to be measured is converted into train of pulses and the number of pulses in 1 second are counted with the help of a gate and counter.

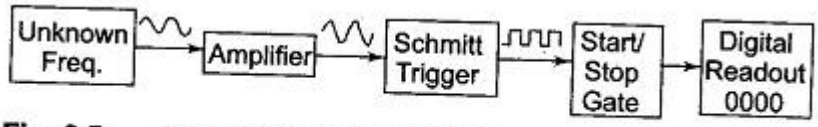


Fig. 6.5 Basic Circuit of a Digital Frequency Meter

- Signal is amplified, if necessary.
- Schmitt trigger converts the input signal into rectangular pulses, which are differentiated and clipped.
- Start/Stop Gate is operated to open the gate for a known time interval.

Basic Circuit for Frequency Measurement:

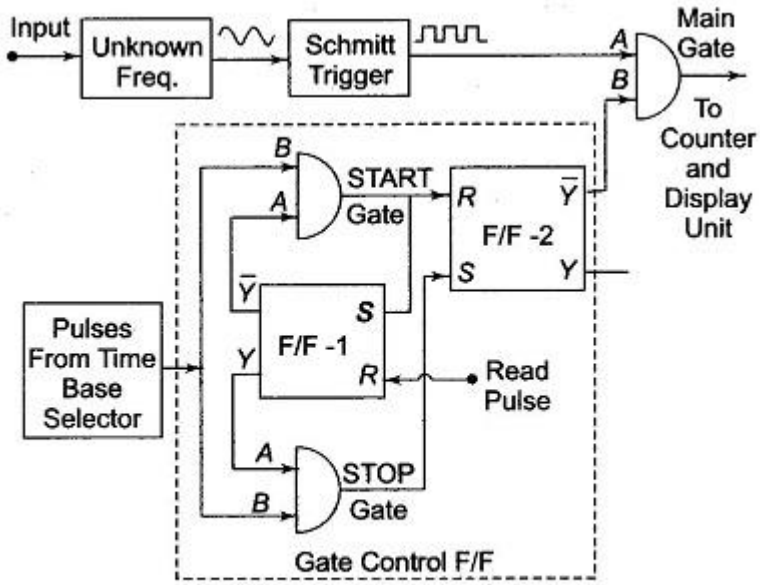


Fig. 6.6 Basic Circuit for Measurement of Frequency Showing Gate Control F/F

- Initially flip flop-1 is set so that Y=1 and compliment of Y is 0. This enables STOP gate and disables START gate.

- As STOP gate is enabled, the pulses from time base generator sets flip flop -2 and disables main gate.
- When a Start pulse/read pulse is applied, flip flop-1 is reset which enables START gate and disables STOP gate. Same read pulse is applied to counter to reset it.
- When a pulse, say no.1 from Time base generator enters START gate, it comes out and resets flip flop-2. This enables main gate and counter starts counting. Same pulse sets the flip flop-1 as it is connected to Set input, thereby disabling START and enabling STOP gate.
- When the next pulse say no.2 as in figure, arrives from the Time base generator, it passes through the STOP gate and sets flip flop-2, thereby disabling the main gate (as compliment of Y =0).
- Counter stops counting and the unknown frequency is measured directly in terms of hertz (Hz) if the timing between two successive pulses of Time base generator is 1 second.

The above control with two flip flops and two gates is called 'Gate Control Flip flop'.
The block diagram of a digital frequency meter employing a Gate control F/F is as shown below.

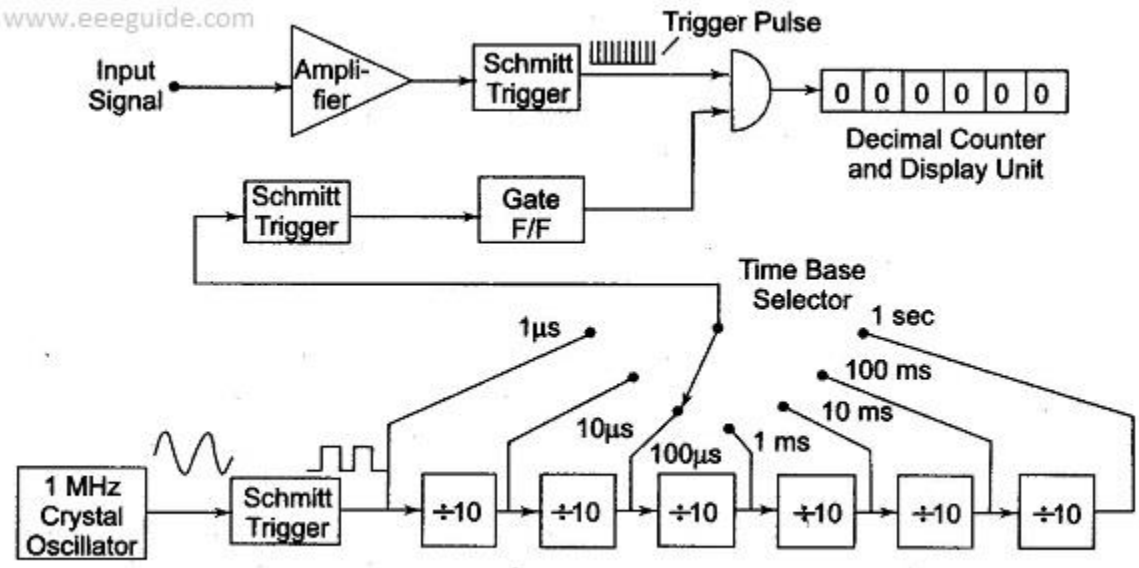


Fig. 6.7 Block Diagram of a Digital Frequency Meter

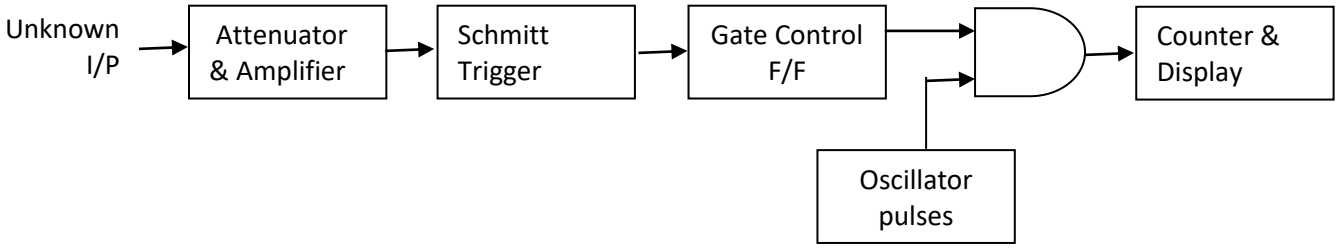
The input signal is amplified and converted to a square wave by a Schmitt trigger circuit. In this diagram, the square wave is differentiated and clipped to produce a train of pulses, each pulse separated by the period of the input signal.
To obtain highly accurate time base of 1 sec duration, it is derived by chain of decade dividers from a 1 MHz crystal oscillator. The time base is also similarly converted into positive pulses using Schmitt trigger.
The first pulse activates the gate control F/F. This gate control F/F provides an enable signal to the AND gate. The trigger pulses of the input signal are allowed to pass through the gate for a selected time period and counted. The second pulse from the decade frequency

divider changes the state of the control F/F and removes the enable signal from the AND gate, thereby closing it. The decimal counter and display unit output corresponds to the number of input pulses received during a precise time interval; hence the counter display corresponds to the frequency.

Digital Measurement of Time

Principle :

Convert the input signal into a train of pulses using *Schmitt* trigger. A high frequency train of pulses are counted for one time period of input signal.



- Gate Control Flip-flop is operated to open in the beginning of the time period of the unknown signal and to close at the end of the time period.

- The number of oscillator pulses counted for one period of the input signal is the measure of the time period.

Time Base Selector:

Time base generator is used to generate the timing pulses which are counted for the given one period of the input signal whose time period is to be measured.

The time base consist of a fixed frequency crystal oscillator, called a clock oscillator, which has to be very accurate. In order to ensure its accuracy, the crystal is enclosed in a constant temperature oven.

The output of this constant frequency oscillator is fed to a Schmitt trigger, which converts the input sine wave to an output consisting of a train of pulses at a rate equal to the frequency of the clock oscillator.

The train of pulses then passes through a series of frequency divider decade assemblies connected in cascade. Each decade divider consists of a decade counter and divides the frequency by ten. Outputs are taken from each decade frequency divider by means of a selector switch; any output may be selected.

The circuit of Fig. 6.8 consists of a clock oscillator having a 1 MHz frequency. The output of the Schmitt trigger is 106 pulses per second and this point corresponds to a time of 1 microsecond. Hence by using a 6 decade frequency divider, a time base with a range of 1 µs — 10 µs — 100 µs — 1 ms —10 ms — 100 ms — 1 s can be selected using a selector switch.

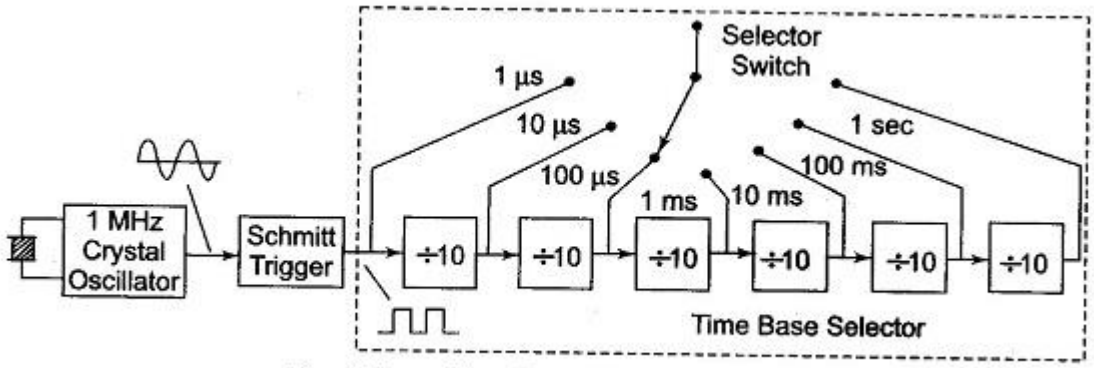


Fig. 6.8 Time Base Selector

Measurement of Time Period:

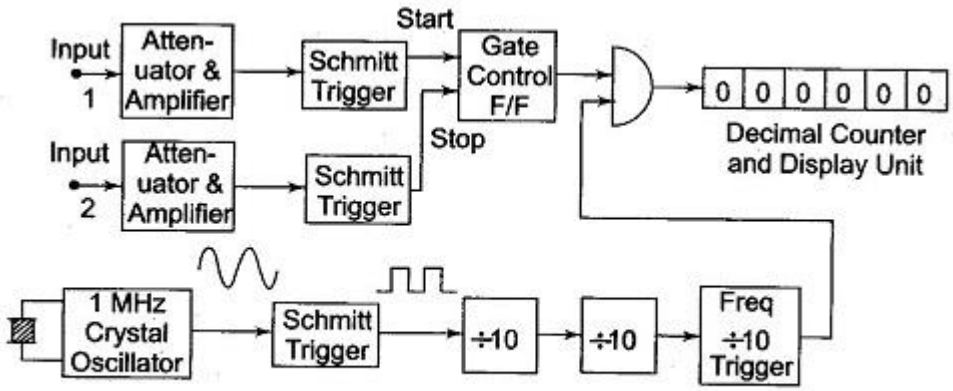


Fig. 6.9 Basic Block Diagram of Time Measurement

Above circuit can be used to measure time period of a signal, by opening the Main gate to count the Time base generator pulses for one period of the input signal.

Input 2, is derived from Input 1.

During the raising edge of the pulse of a cycle of Input 1 signal which is derived from the Schmitt trigger, triggers the control F/F which in turn enables the Main gate and the pulses

from the Time base generator passes through the Main gate. Counter starts counting the pulses of Time bases generator.

During the second pulse of the next cycle of Input 1 cycle, a pulse is generated from Input 2 signal to Gate control F/F which in turn disables the Main gate. This stops counter. The counts counted by the counter are a measure of the Time period of the input signal in terms of the Time bases generator pulses. If the Time base generator time period is 1 ms, then the counts give the time period of input signal in terms of milli seconds. Ex: If counts are 120, then the time period is 120 ms.

The accuracy of time period measurements can be increased by opening the Main gate for more than one period of input signal, like for 10 or 100 or more cycles. This is achieved by dividing the input signal frequency by decade divider circuits DDAs (Decade Divider Assemblies). In such cases, the counts counted should be divided by 10 or 100 .. accordingly to get the actual time period.
Figure 6.10 show the multiple average mode of operation. In this circuit, five more decade dividing assemblies are added so that the gate is now enabled for a much longer interval of time than it was with single DDA.

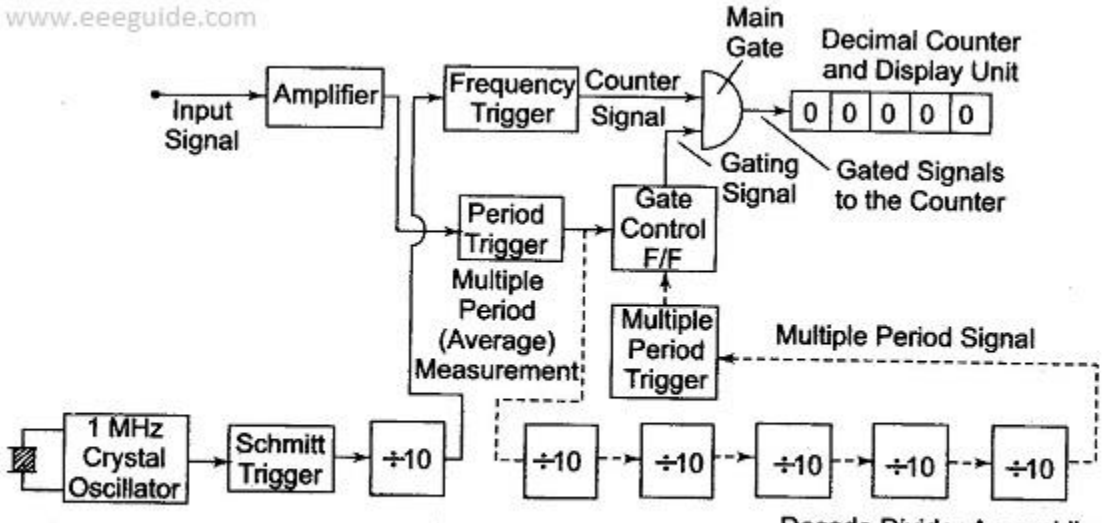


Fig. 6.10 Block Diagram of a Single and Multiple Period (Average) Measurement