

29/08/19.

classmate

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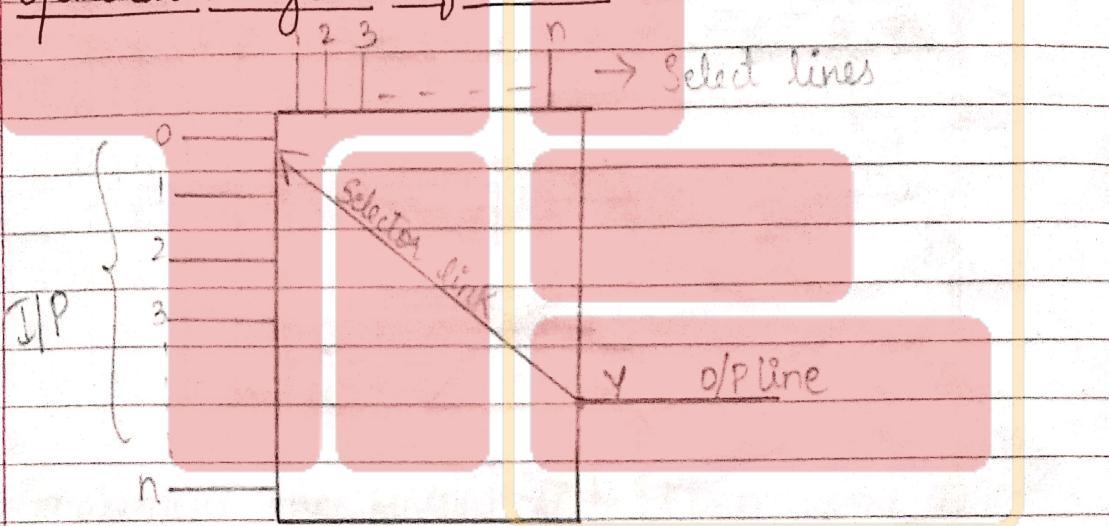
MODULE: 03MULTIPLEXER

A multiplexer is a device which has multiple input and single output.

Designing a multiplexer requires 3 objectives:

1. Input line.
2. Select line / Select input.
3. Output line.

General diagram of MUX

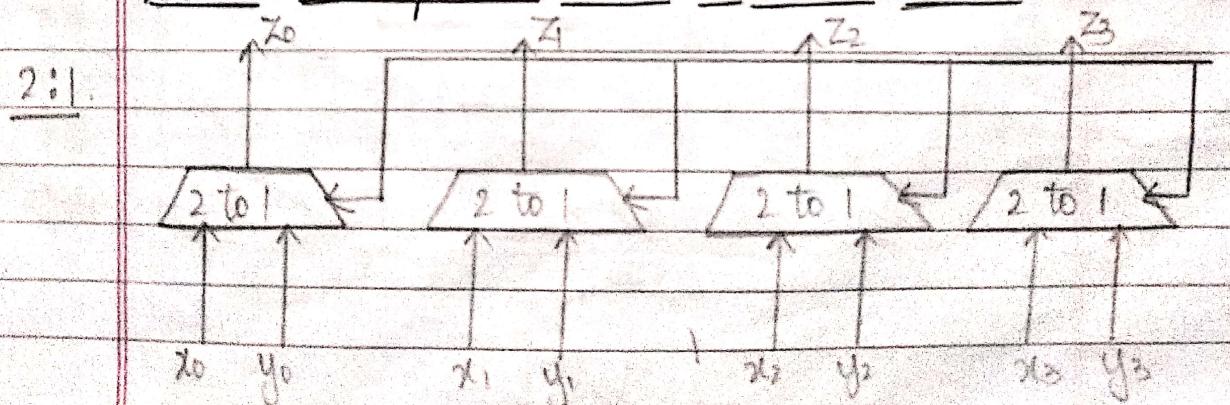


Note: The output line selects the proper input line based on the selector link.

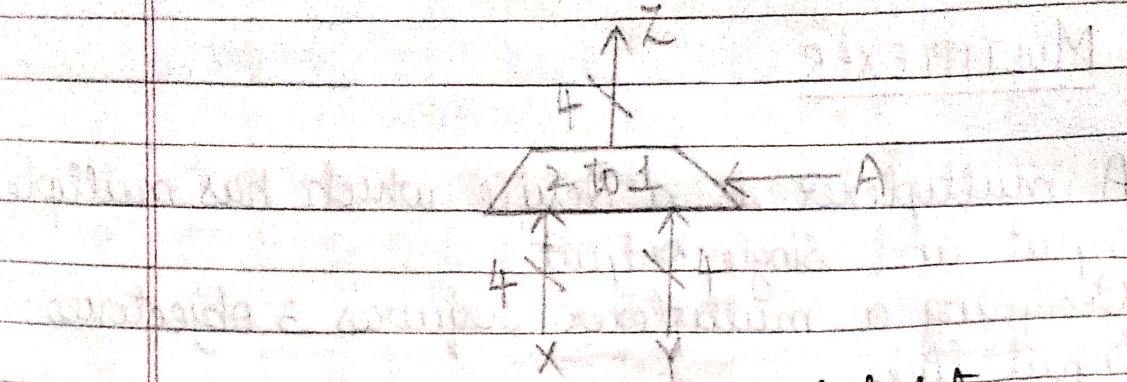
There are 5 different types of MUX:

2:1, 4:1, 8:1, 16:1, 32:1.

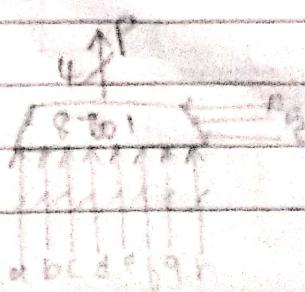
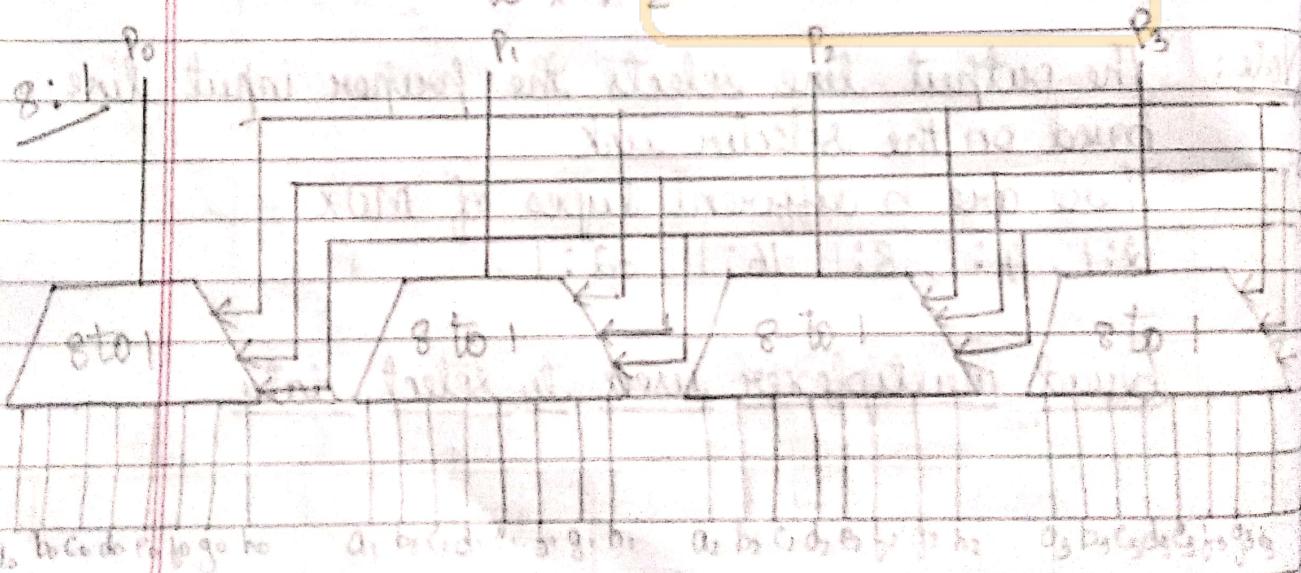
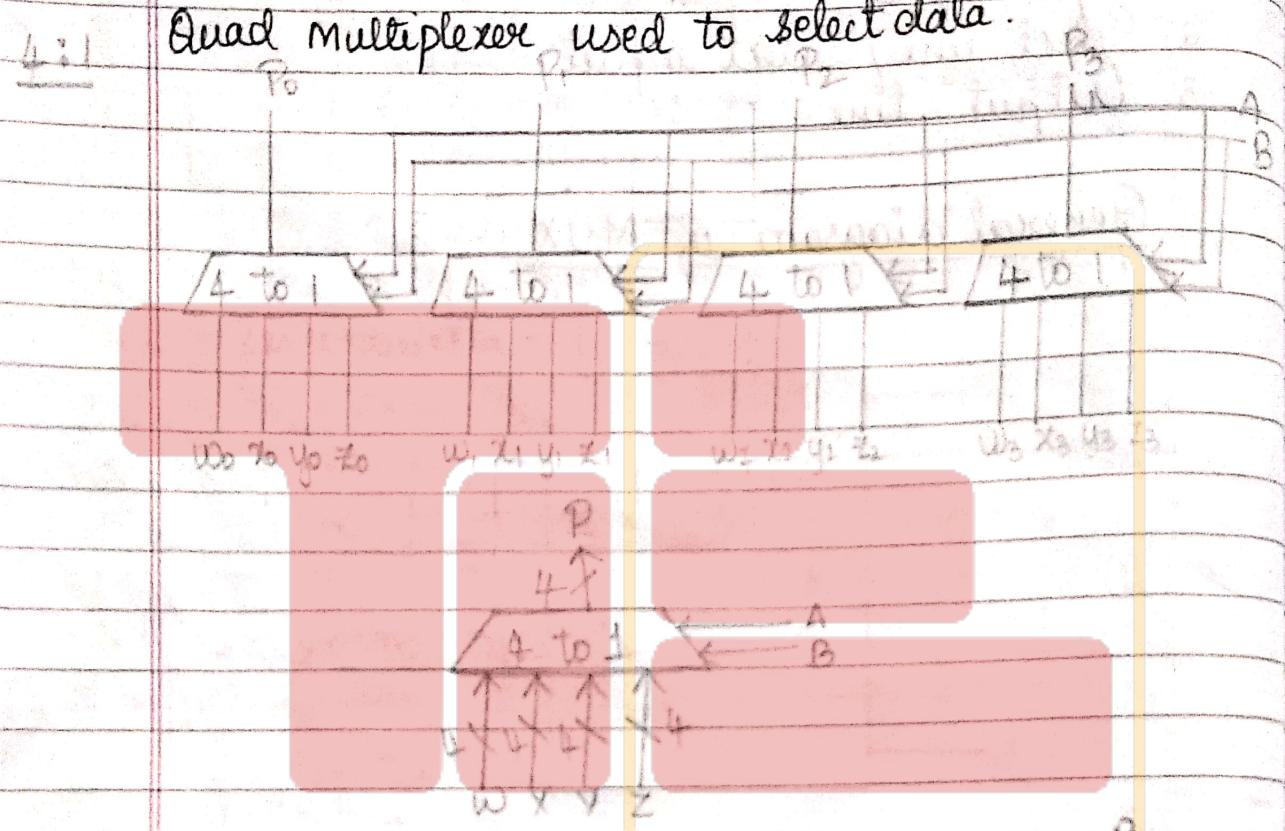
Quad multiplexer used to select data



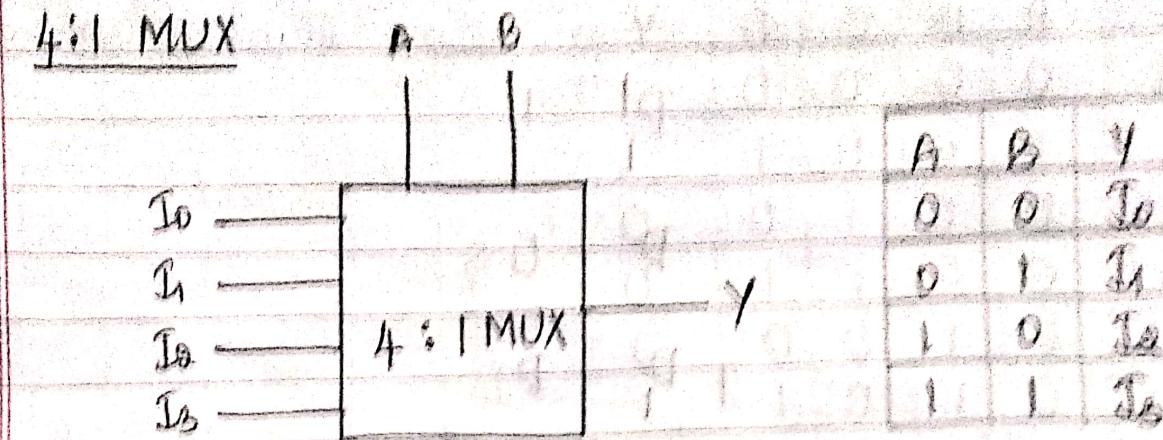
# Quad multiplexer with bus input & output



Quad multiplexer used to select data.

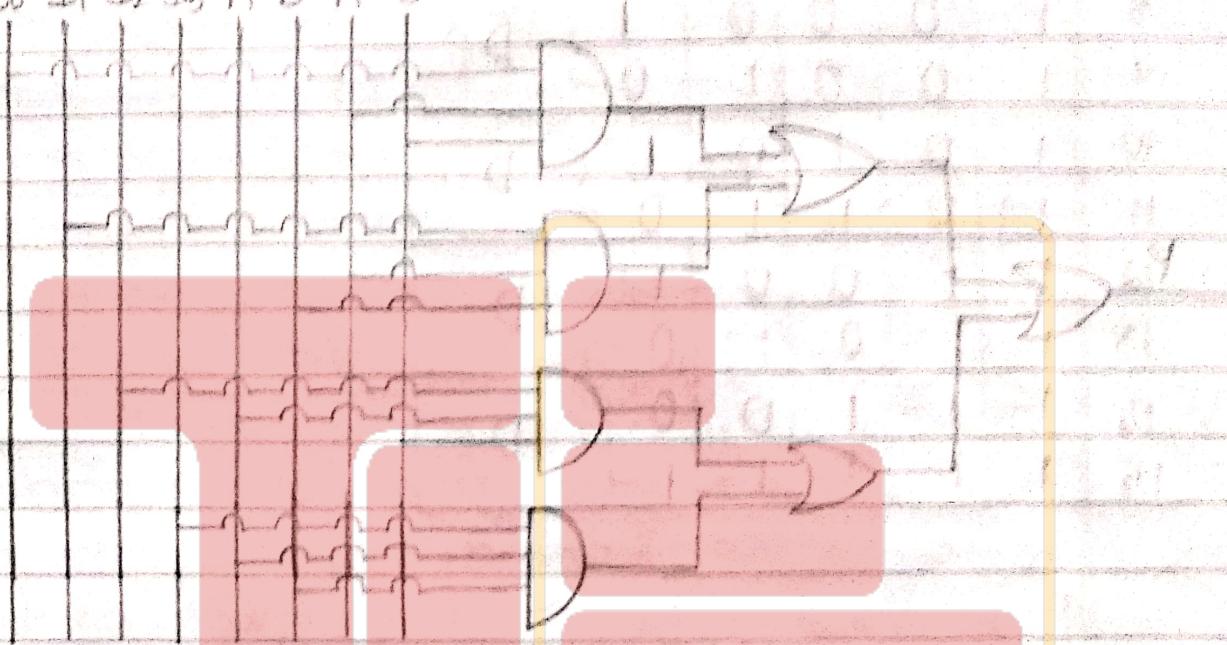


4:1 MUX



$$I_0 \bar{A} \bar{B} + I_1 \bar{A} B + I_2 A \bar{B} + I_3 A B$$

$$I_0 \bar{A} \bar{B} + I_1 \bar{A} B + I_2 A \bar{B} + I_3 A B$$

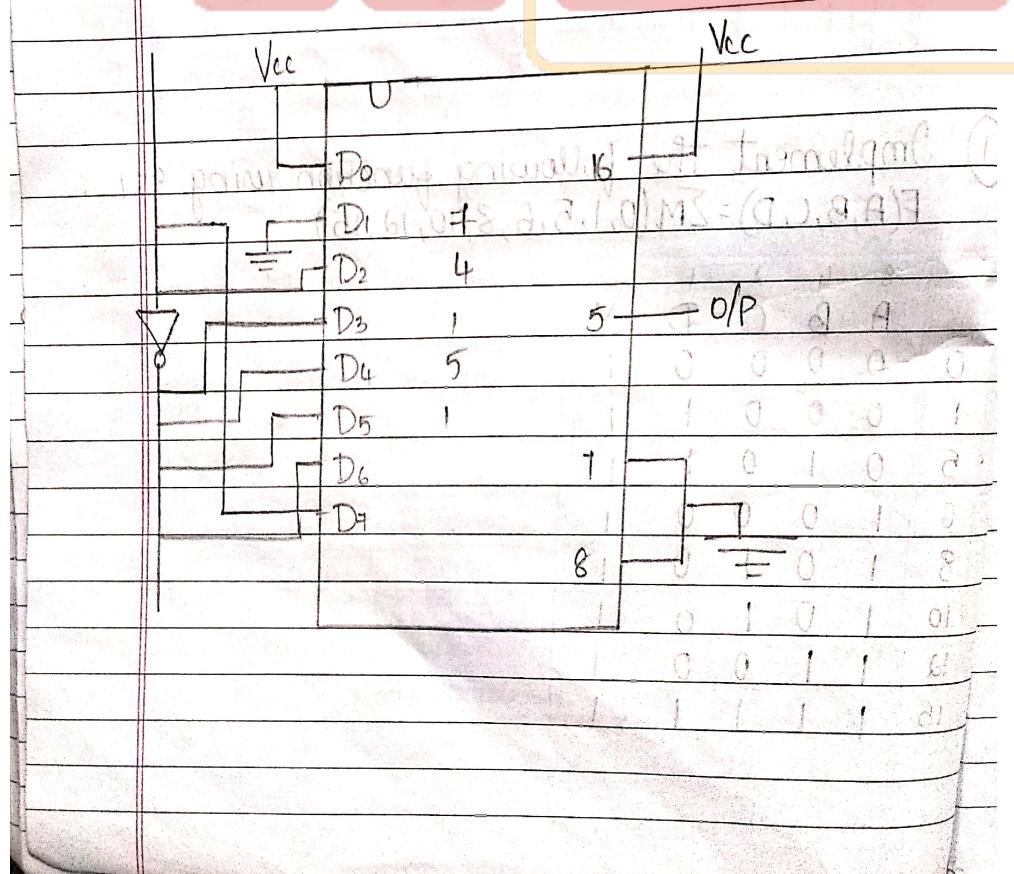


①

Implement the following function using 8:1  
 $F(A, B, C, D) = \sum m(0, 1, 5, 6, 8, 10, 12, 15)$ .

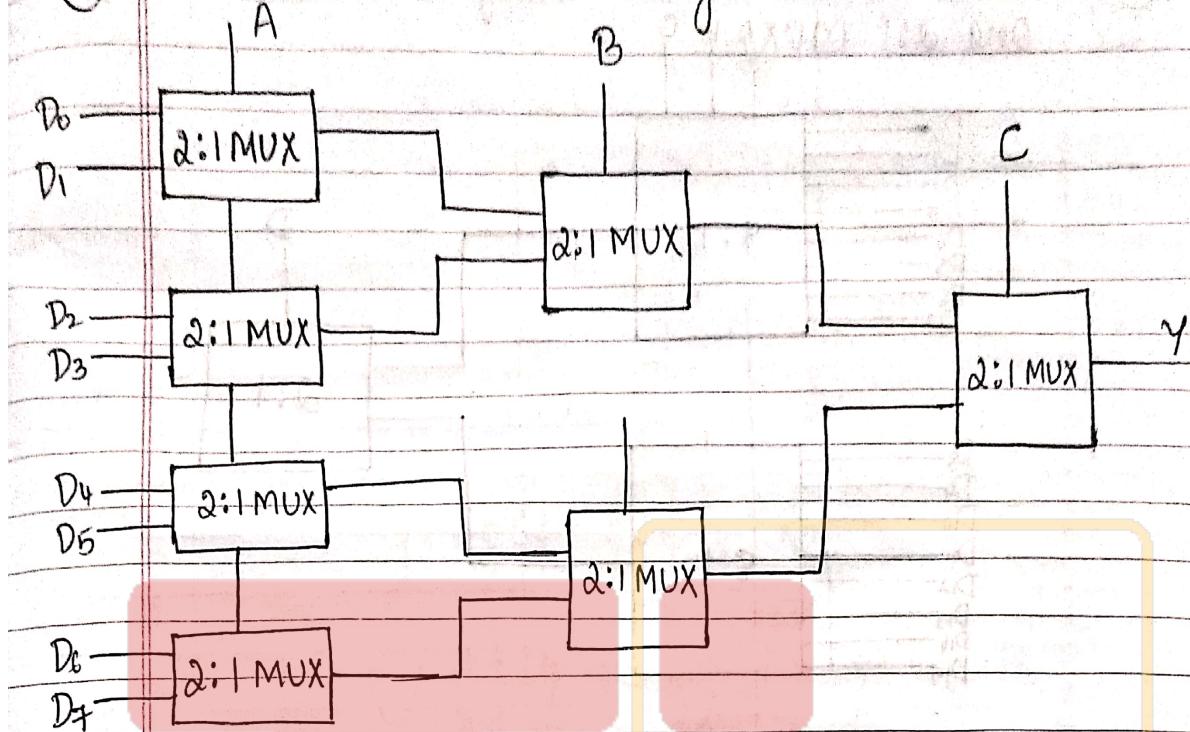
X	8	4	2	1	A	B	C	D	Y
0	0	0	0	0	1				
1	0	0	0	1	1				
5	0	1	0	1	1				
6	1	0	0	0	1				
8	1	0	1	0	1				
10	1	0	1	0	1				
12	1	1	0	0	1				
15	1	1	1	1	1				

	8	4	2	1	Y.	
	A	B	C	D		
0	0	0	0	0	1	
1	0	0	0	1	0	
2	0	0	1	0	0	
3	0	0	1	1	0	
4	0	1	0	0	0	$D_2$
5	0	1	0	1		
6	0	1	1	0	1	$\bar{D}_3$
7	0	1	1	1	0	
8	1	0	0	0	1	$\bar{D}_4$
9	1	0	0	1	0	
10	1	0	1	0	1	$\bar{D}_5$
11	1	0	1	1	0	
12	1	1	0	0	1	$\bar{D}_6$
13	1	1	0	1	0	
14	1	1	1	0	0	$D_1$
15	1	1	1	1	1	



(2)

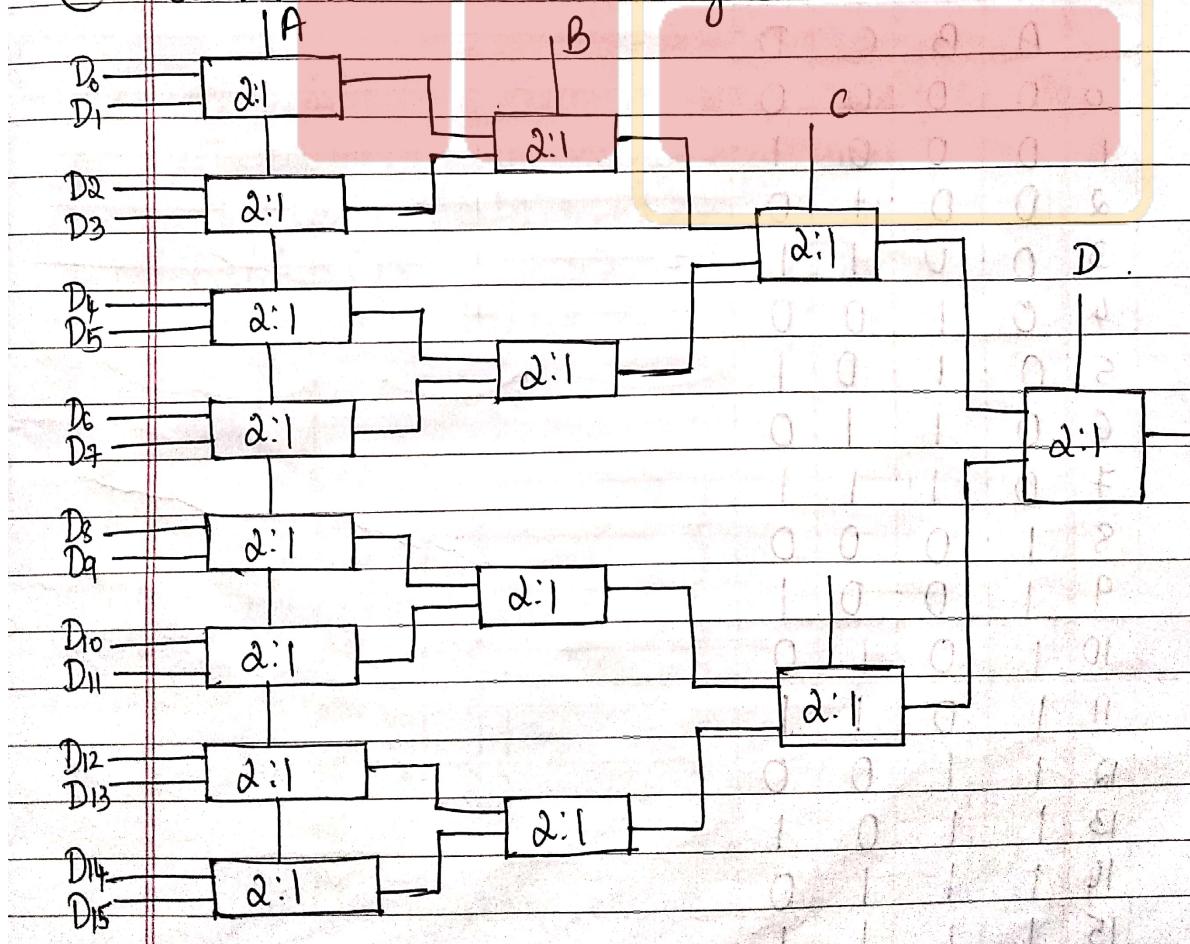
Construct 8:1 MUX using 2:1 MUX.



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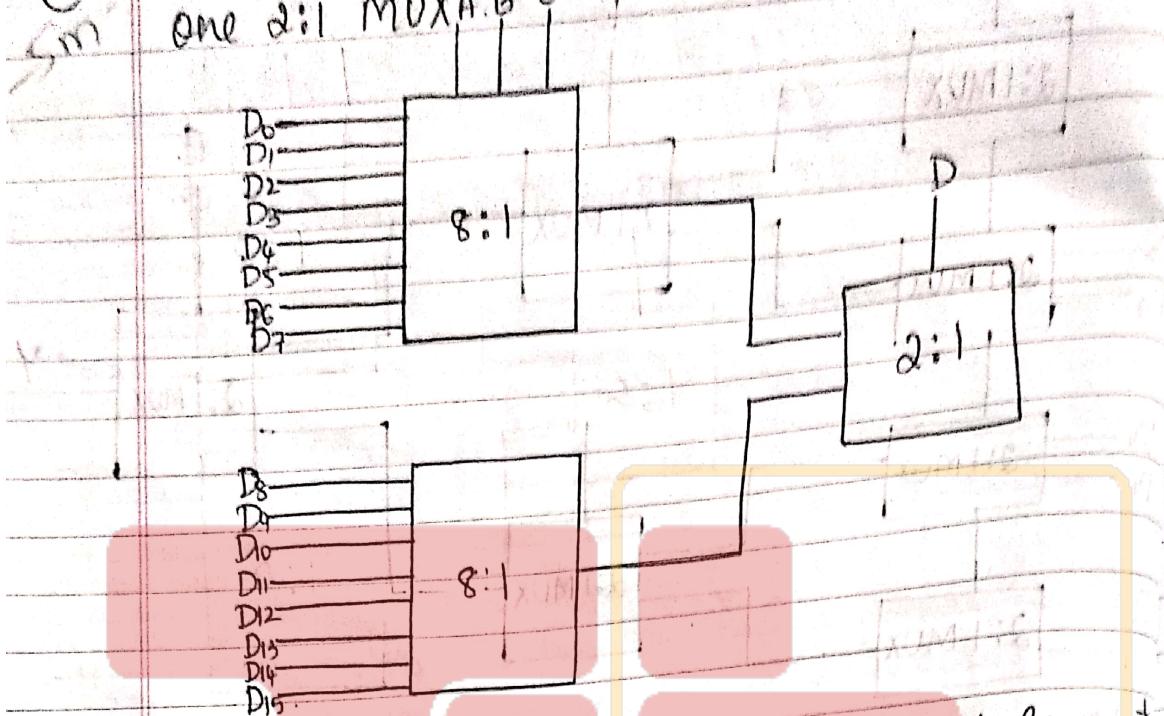
(3)

Construct 16:1 MUX using 2:1 MUX.



(4)

Construct 16:1 MUX using two 8:1 MUX &  
one 2:1 MUX A, B, C

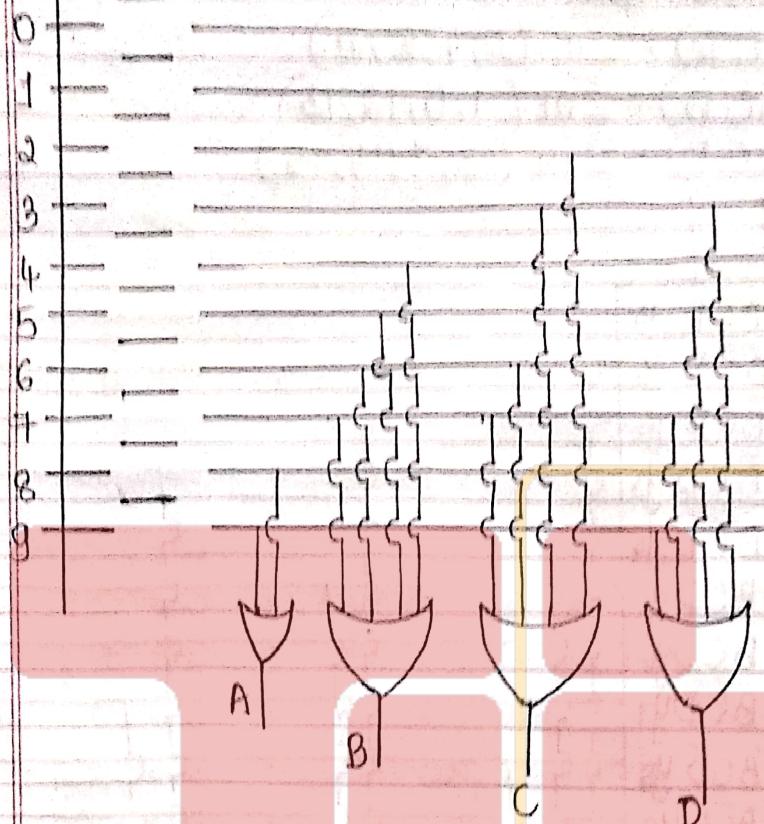


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4-bit encoder and decoder using 7 segment  
display. (16:1 encoder)

	8	4	2	1	A	B	C	D	7 Segment Display
0	0	0	0	0	0	0	0	0	a b c d
1	0	0	0	1	1	0	0	0	b
2	0	0	1	0	0	1	0	0	c
3	0	0	1	1	0	1	0	0	d
4	0	1	0	0	0	0	1	0	e
5	0	1	0	1	1	0	0	0	f
6	0	1	1	0	0	0	1	0	g
7	0	1	1	1	0	0	0	0	h
8	1	0	0	0	0	0	0	1	i
9	1	0	0	1	0	0	0	1	j
10	1	0	1	0	0	1	0	1	k
11	1	0	1	1	1	0	0	1	l
12	1	1	0	0	0	1	0	0	m
13	1	1	0	1	0	1	0	0	n
14	1	1	1	0	0	0	1	0	o
15	1	1	1	1	0	0	0	0	p

15V  
Vec



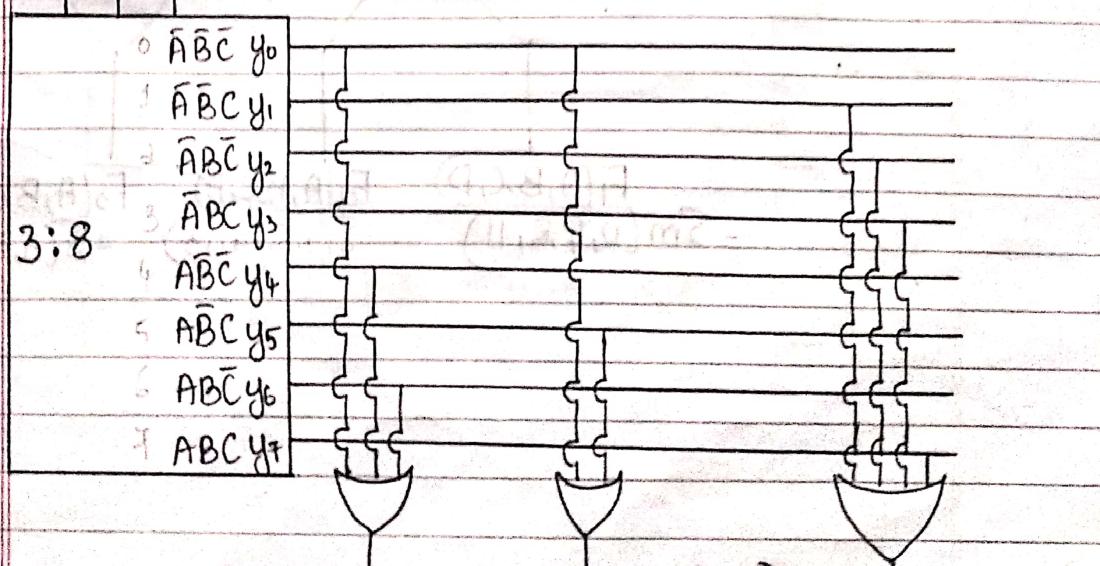
Q →

Show that 3:8 decoder and multiple input OR gate is the following boolean expression:-

$$F_1(A, B, C) = \sum m(0, 4, 6)$$

$$F_2(A, B, C) = \sum m(0, 5)$$

$$F_3(A, B, C) = \sum m(1, 2, 3, 7)$$



$$F_1(A, B, C) = \sum m(0, 4, 6) \quad F_2(A, B, C) = \sum m(0, 5) \quad F_3(A, B, C) = \sum m(1, 2, 3)$$

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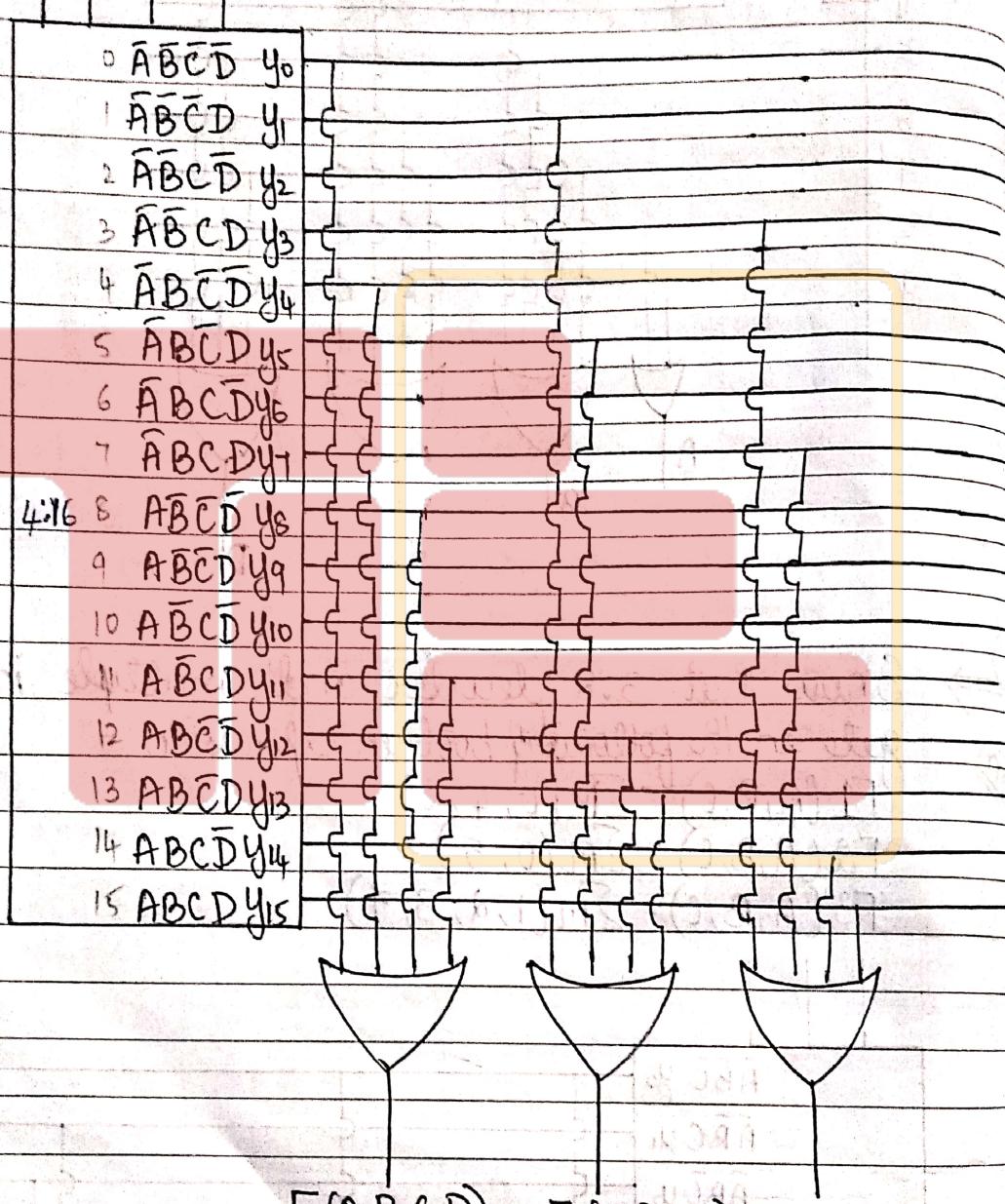
(2)

Show that 4:16 decoder & multiple input OR gate

$$F_1(A, B, C, D) = \sum m(0, 4, 8, 11)$$

$$F_2(A, B, C, D) = \sum m(1, 5, 12, 13)$$

$$F_3(A, B, C, D) = \sum m(3, 7, 14, 15)$$



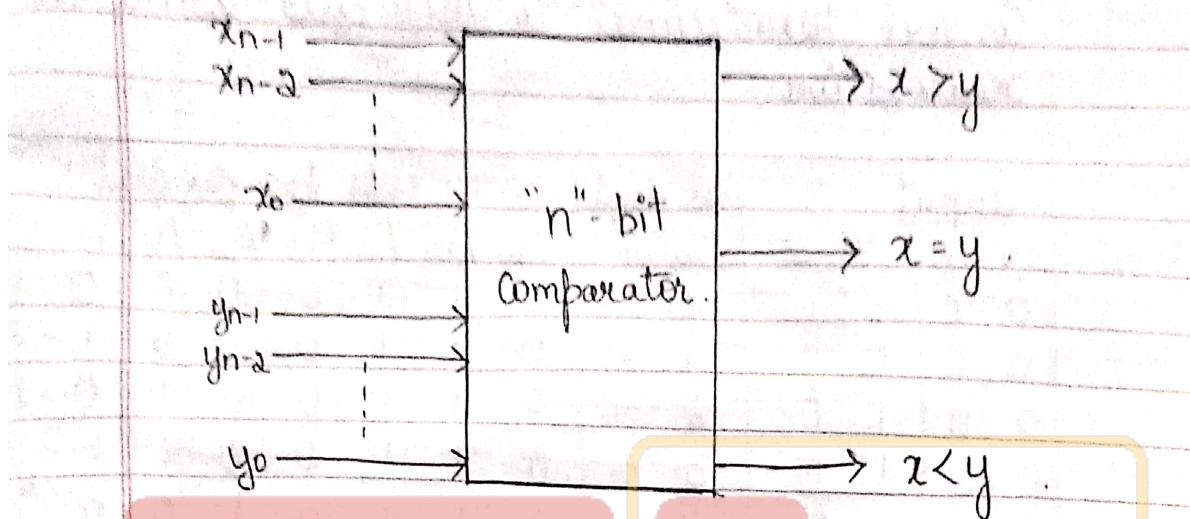
$$F_1(A, B, C, D) \\ = \sum m(0, 4, 8, 11)$$

$$F_2(A, B, C, D) \\ = \sum m(1, 5, 12, 13)$$

$$F_3(A, B, C, D) \\ = \sum m(3, 7, 14, 15)$$

2nd  
PM

## Magnitude comparator



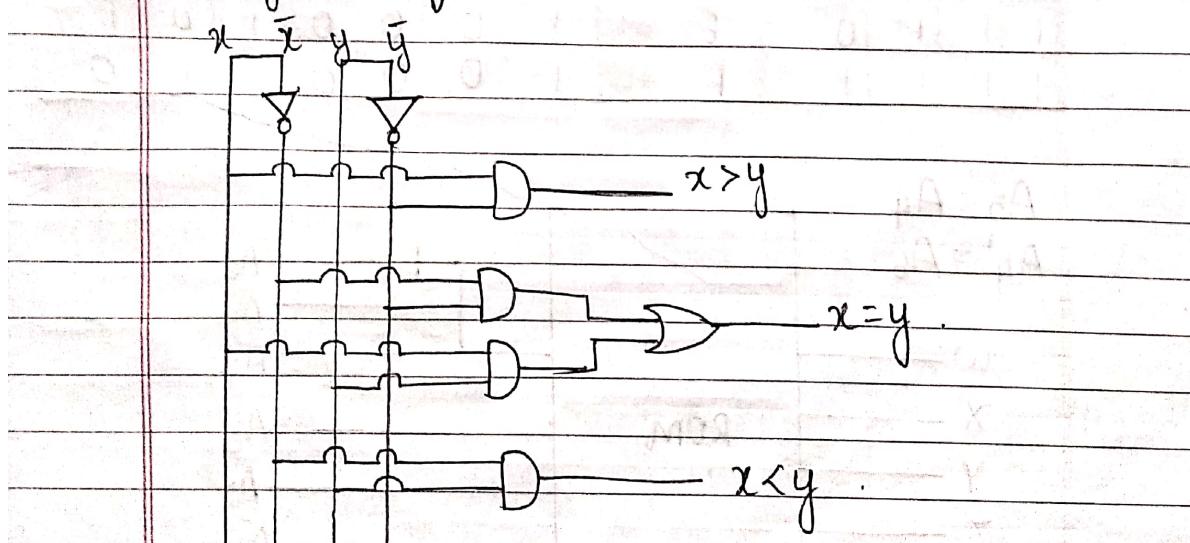
$x$	$y$	$x > y$	$x = y$	$x < y$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

I  
II  
III

$$x > y \Rightarrow x\bar{y}$$

$$x = y \Rightarrow \bar{x}\bar{y} + xy$$

$$x < y \Rightarrow \bar{x}y$$



## Read Only Memory

Convert hexadecimal to ASCII code using ROM realization

Input	W	X	Y	Z	Hex digit	ASCII code for Hex digit						
						A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	
	0	0	0	0	0	48	0	1	1	0	0	0
	0	0	0	1	1	49	0	1	1	0	0	0
	0	0	1	0	2	50	0	1	1	0	0	1
	0	0	1	1	3	51	0	1	1	0	0	1
	0	1	0	0	4	52	0	1	1	0	1	0
	0	1	0	1	5	53	0	1	1	0	1	0
	0	1	1	0	6	54	0	1	1	0	1	1
	0	1	1	1	7	55	0	1	1	0	1	1
	1	0	0	0	8	56	0	1	1	1	0	0
	1	0	0	1	9	57	0	1	1	1	0	1
	1	0	1	0	A	65	1	0	0	0	0	1
	1	0	1	1	B	66	1	0	0	0	0	0
	1	1	0	0	C	67	1	0	0	0	0	1
	1	1	0	1	D	68	1	0	0	0	1	0
	1	1	1	0	E	69	1	0	0	0	1	0
	1	1	1	1	F	70	1	0	0	0	1	0

$$A_5 = A_4$$

$$A_4' = A_6$$

W

X

Y

Z

ROM



A<sub>6</sub>

A<sub>5</sub>

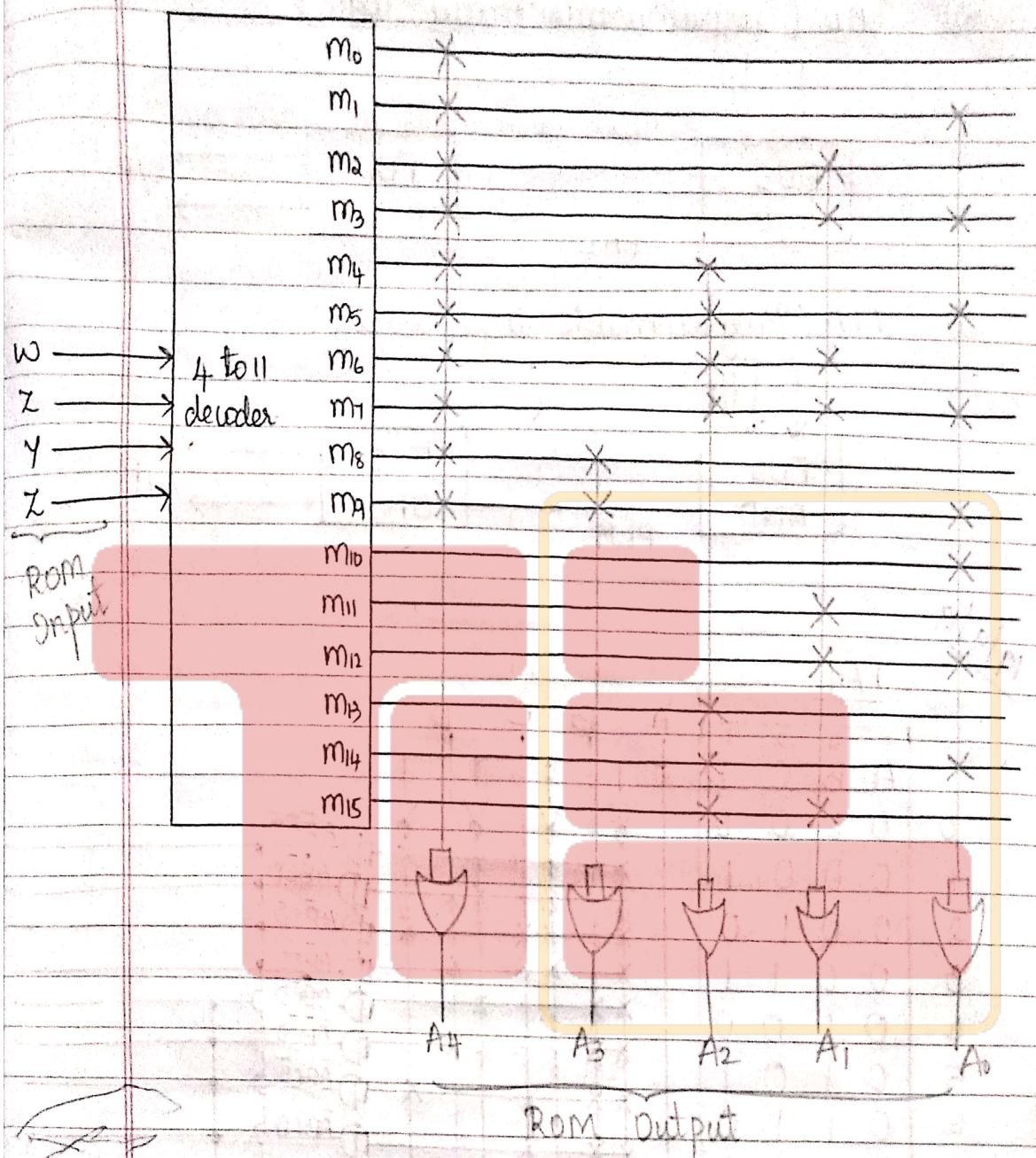
A<sub>4</sub>

A<sub>3</sub>

A<sub>2</sub>

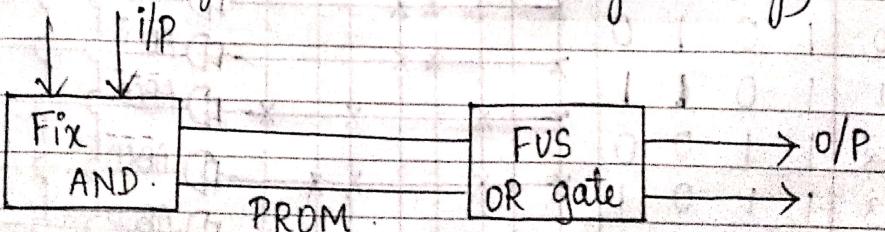
A<sub>1</sub>

A<sub>0</sub>

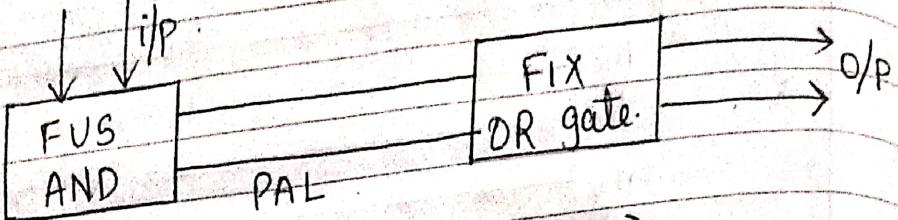


~~Out of 3  
Any 2/3 Imp~~

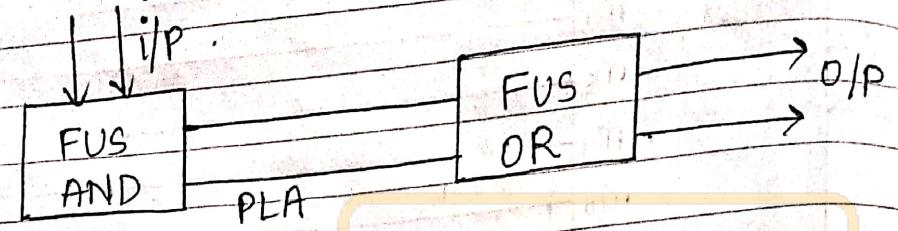
### 1) PROM (Programmable Read only memory.)



2) PAL (Programmable Array logic)

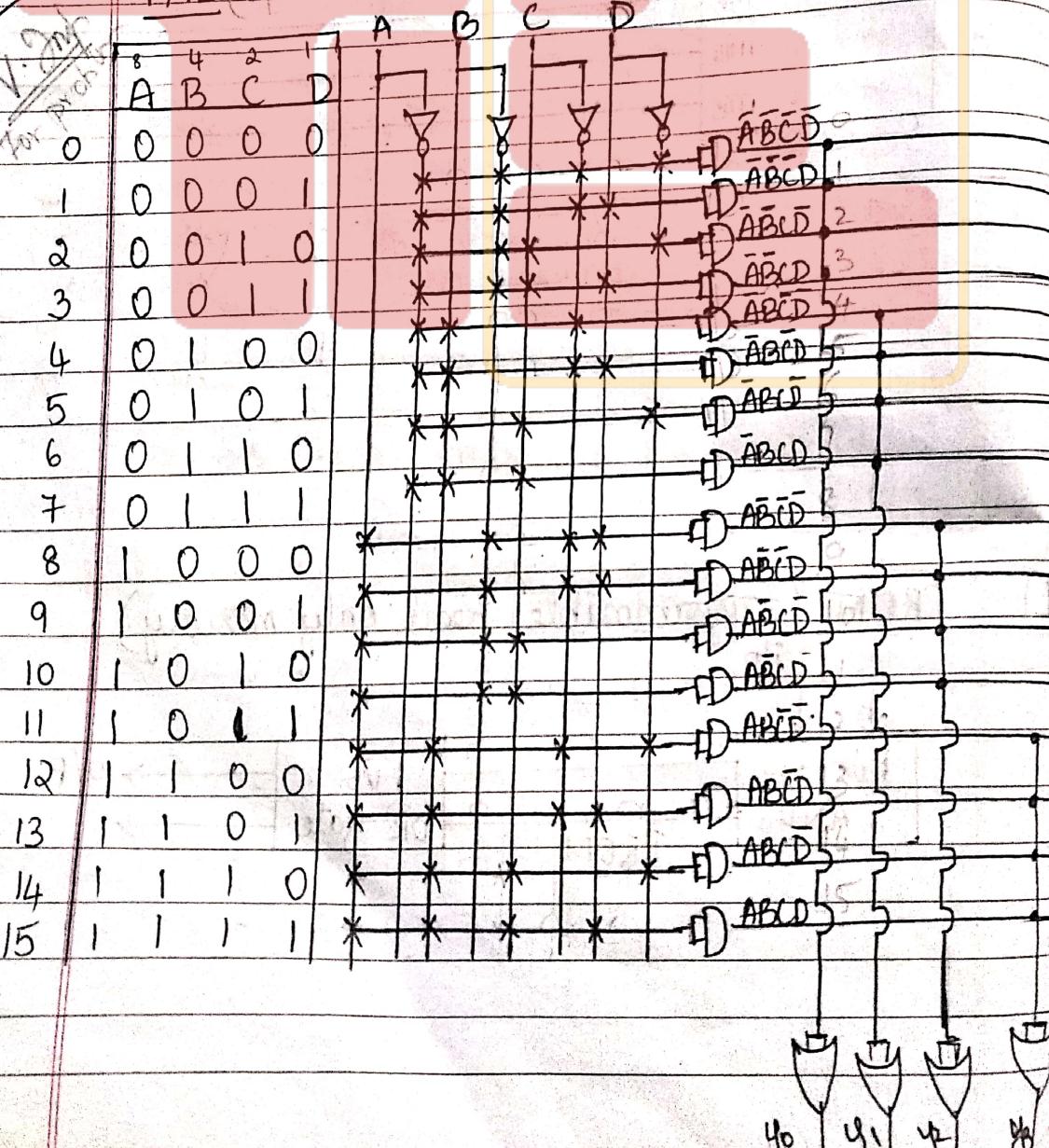


3) PLA (Programmable logic array)



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PAL (General structure.)



## Problem:

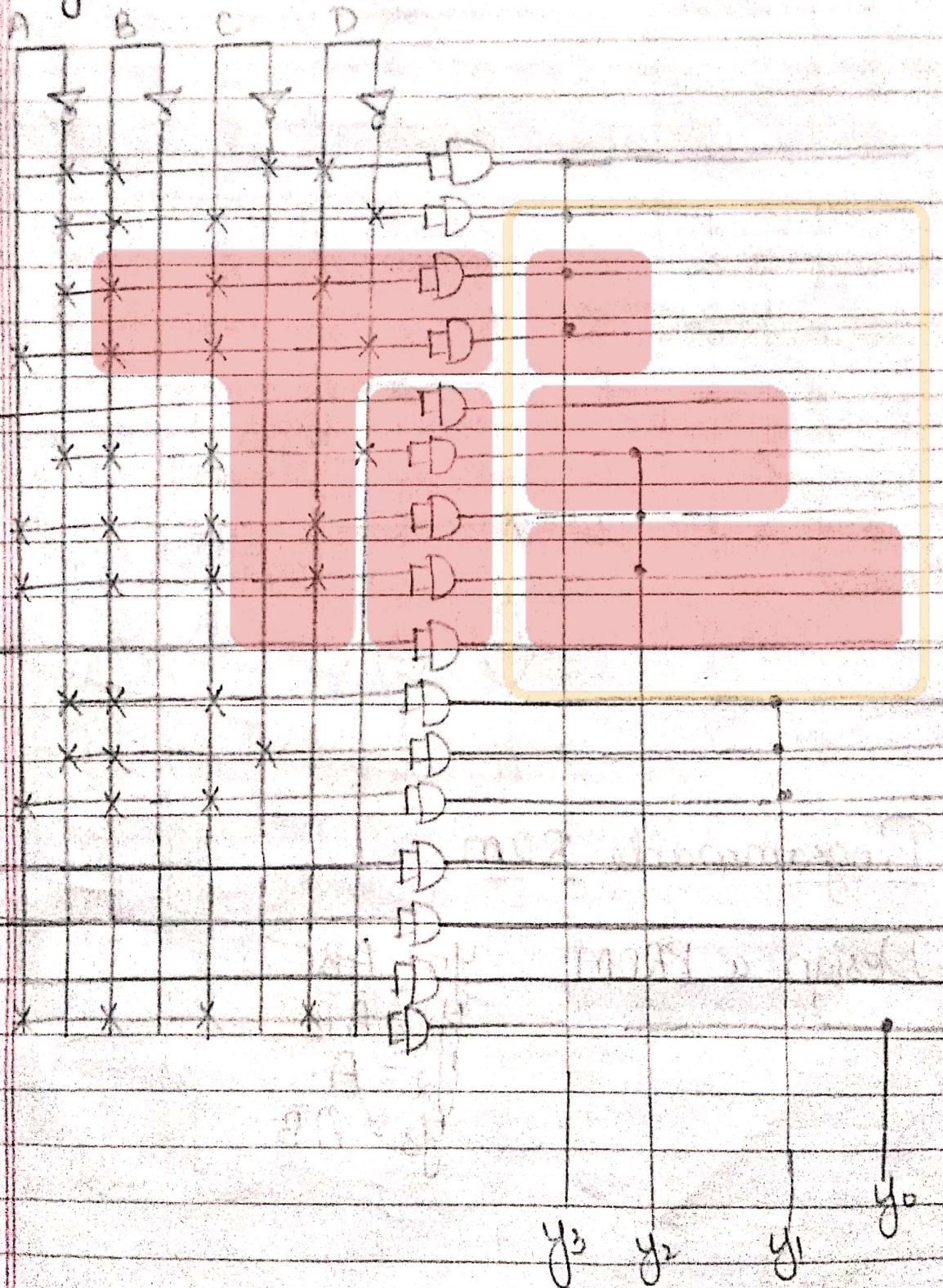
Generate the following boolean function using PAL.

$$y_3 = \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}B\bar{C}D + A\bar{B}CD$$

$$y_2 = \bar{A}\bar{B}\bar{C}\bar{D} + ABCD + A\bar{B}CD$$

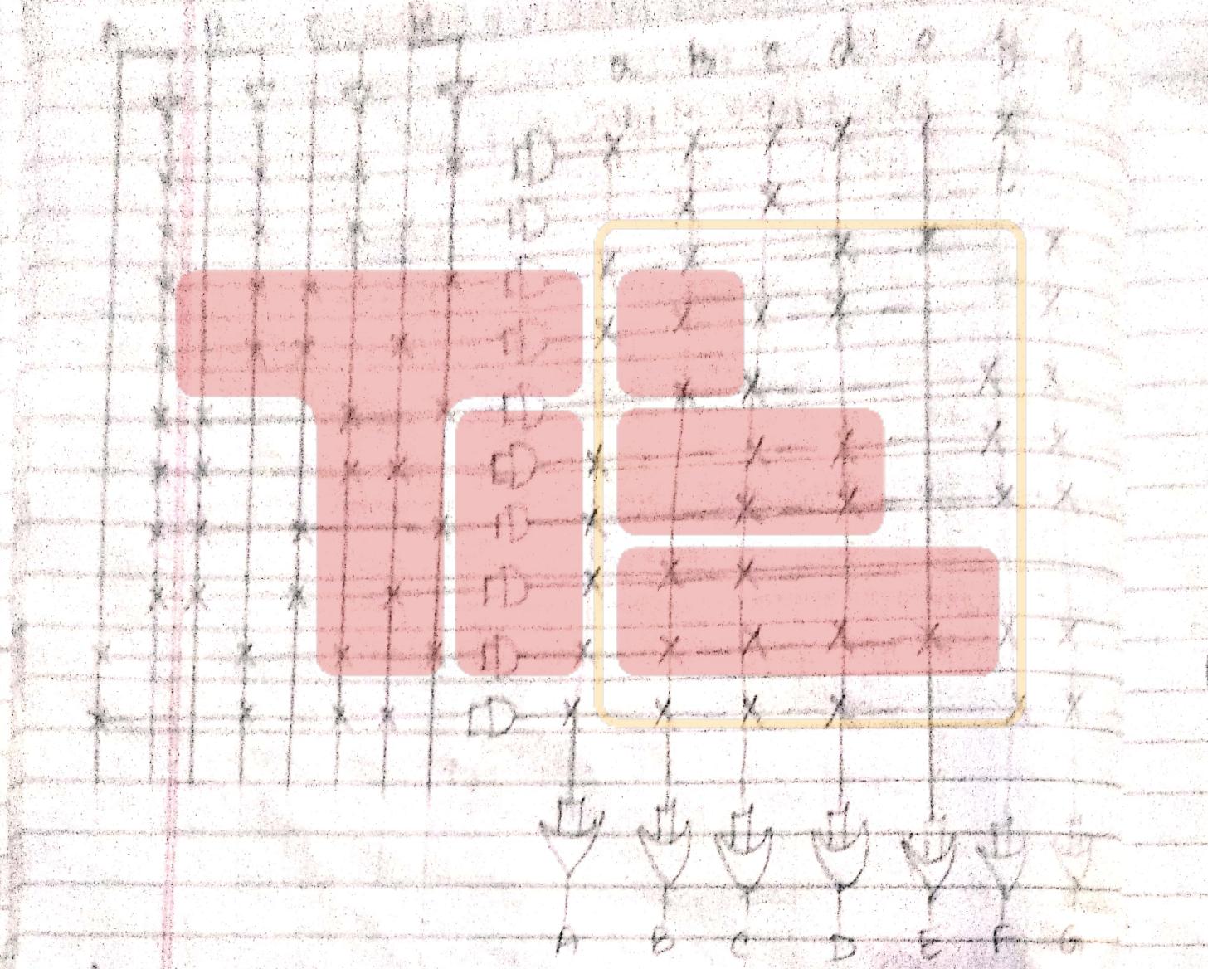
$$y_1 = \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C}$$

$$y_0 = ABCD$$



## Programmable Logic Array

Design a PLA using 1 segment display



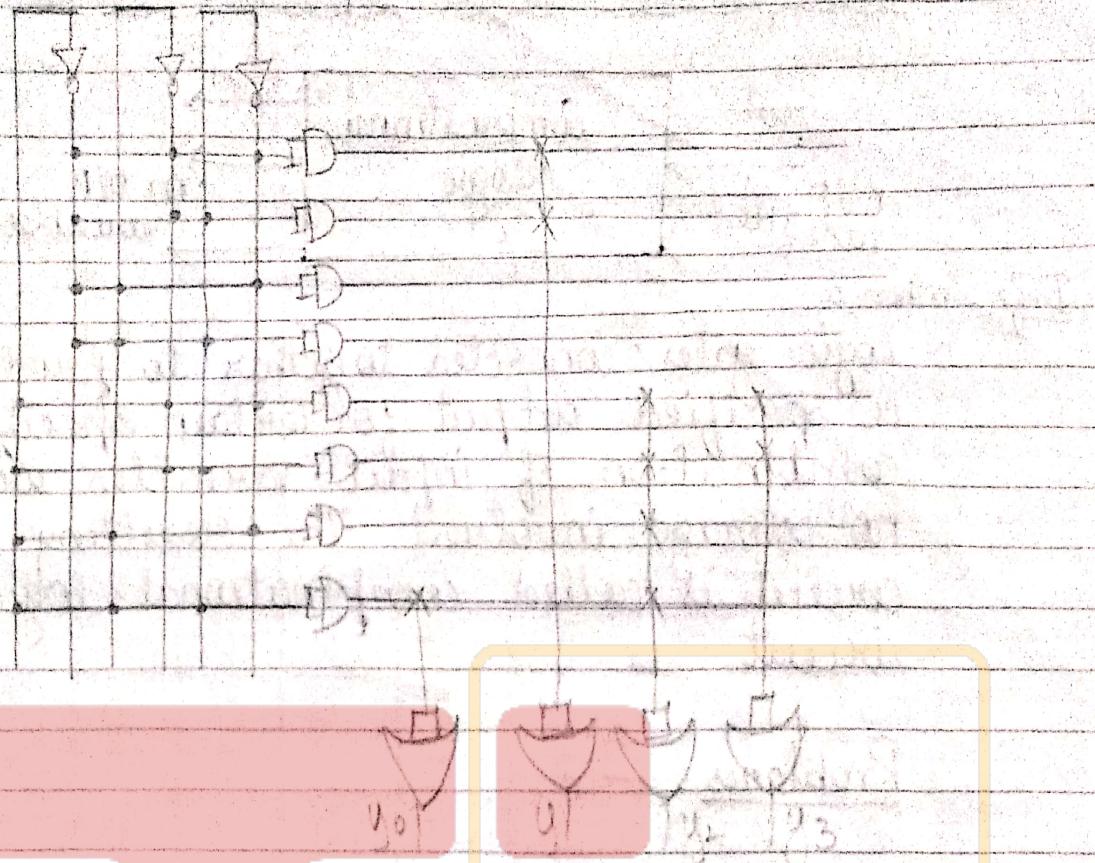
## Programmable ROM

- ① Design a PROM ,  $y_0 = ABC$ .

$$y_1 = \bar{A}\bar{B}$$

$$y_2 = A.$$

$$y_3 = A\bar{B}.$$

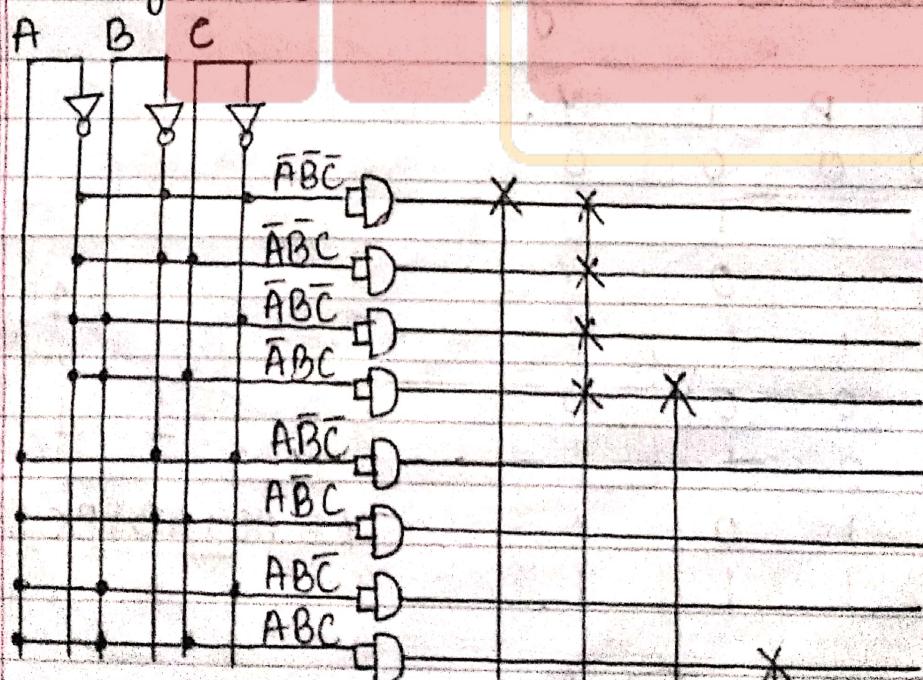


② Design a PROM

$$Y_0 = \bar{A}\bar{B}\bar{C}$$

$$Y_1 = \bar{A}$$

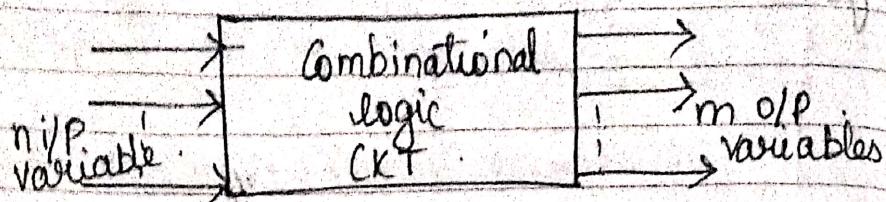
$$Y_2 = \bar{A}BC$$



$Y_0$   $Y_1$   $Y_2$   $Y_3$

## Chapter: 02

### Combinational Logic circuit design (Block diagram)



Defn: when a

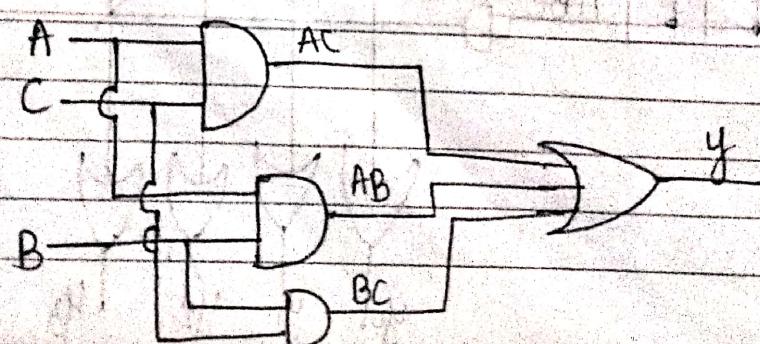
Logic gates <sup>are</sup> connected together to produce a specified output for certain specified combination of input variables with no storage involved. The resulting circuit is called **combinational logic circuit**.

#### Problems:

- Design a combinational logic circuit with 3 input variables that will produce a logic 1 output when more than 1 input variables are logic 1.

A	B	C	Y						
0	0	0	0						
0	0	1	0	A	BC	BC	BC	BC	
0	1	0	0		A				
0	1	1	1			0	1	1	1
1	0	0	0	A					
1	0	1	1		1	1	1	1	1
1	1	0	1						
1	1	1	1						

$Y = AC + AB + BC$



# BCD: Binary Coded Decimal

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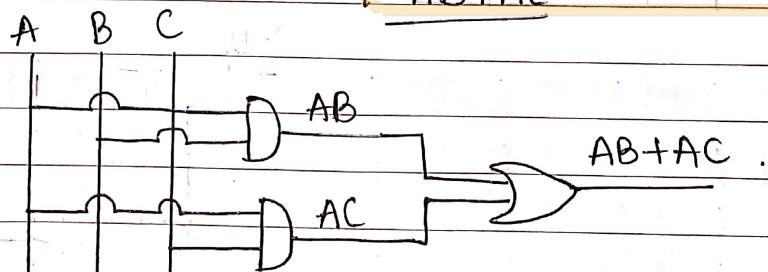
(a)

Design a circuit to detect invalid BCD no & implement using NAND gate only.

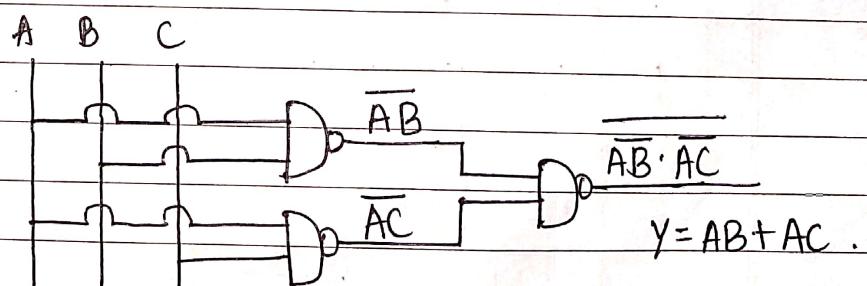
b <sub>3</sub>	b <sub>2</sub>	b <sub>1</sub>	b <sub>0</sub>	A	B	C	D	y
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	1	0	0	1
3	0	0	1	1	0	0	0	1
4	0	1	0	0	0	0	0	0
5	0	1	0	1	0	0	0	0
6	0	1	1	0	0	1	0	0
7	0	1	1	1	0	0	0	0
8	1	0	0	0	0	0	0	0
9	1	0	0	1	0	0	1	0
10	1	0	1	0	1	0	0	0
11	1	0	1	1	1	1	1	1
12	1	1	0	0	0	1	0	1
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	1	1
15	1	1	1	1	1	1	1	1

$$Y = AB + AC$$

Basic gates



NAND gates:

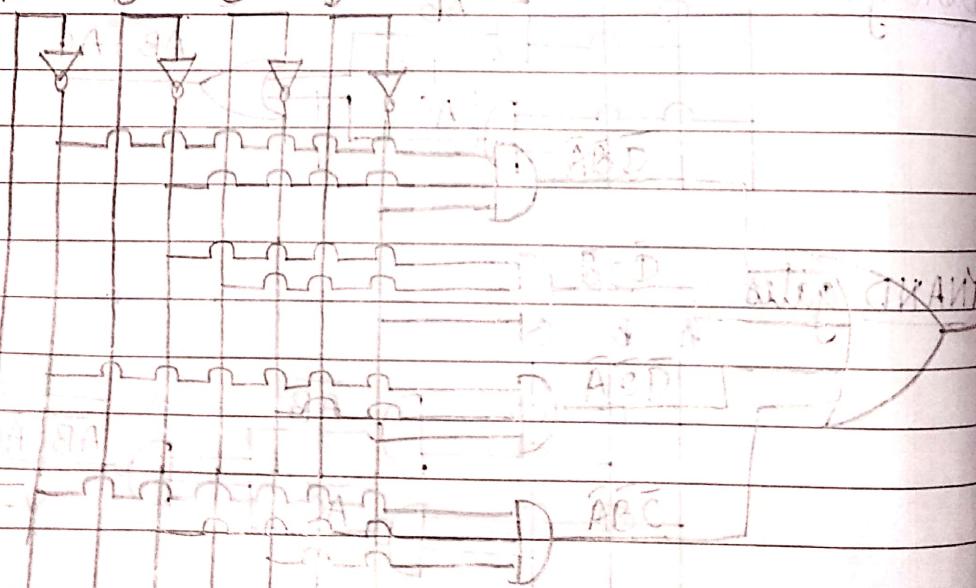


- ③ Design a combinational logic circuit  
Output is high only when majority of inputs A B C D are low.

	8	4	2	1	V	Q	3	9	?
A	0	0	0	0	Y	0	0	0	1
B	0	0	0	1		0	1	1	0
C	0	0	1	0		0	0	1	1
D	0	0	1	0		0	1	0	0
	0	0	1	1	0		0	1	2
	0	1	0	0	1	AB	00	01	11
	0	1	0	1	0		00	01	10
	0	1	1	0	0		00	01	11
	0	1	1	1	0		00	01	10
	1	0	0	0	1	CD	00	01	11
	1	0	0	1	0		00	01	10
	1	0	1	0	0		00	01	11
	1	0	1	1	0		00	01	10
	1	1	0	0	0		00	01	11
	1	1	0	1	0		00	01	10
	1	1	1	0	0		00	01	11
	1	1	1	1	0		00	01	10
	1	1	1	1	0		00	01	11
	1	1	1	1	0		00	01	11
	1	1	1	1	0		00	01	11
	1	1	1	1	0		00	01	11

$$Y = \overline{ABD} + \overline{BCD} + \overline{ACD} + \overline{ABC}$$

A B C D



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## Design of circuit with limited gate Fan-in.

In a practical combination ckt, the maximum no of input on each gate is limited, i.e fan-in is limited. Depending on the type of gate used, this limits may be 2, 3, 4 or 8.

### Problems:

- (1) Minimize the given SOP equation and implement it using 3 input NOR gate.

$$F(A, B, C, D) = \sum m(0, 3, 4, 5, 8, 9, 10, 14, 15)$$

$$F(A, B, C, D) = \prod m(1, 2, 6, 7, 11, 12, 13)$$

Solu:

AB	CD	$\bar{A}\bar{B}$	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	$CD$
		0	0	3	0	2
		4	5	0	0	6
AB		0	0	12	13	15
		12	13	15	14	11
AB				0		
		8	9	11	10	

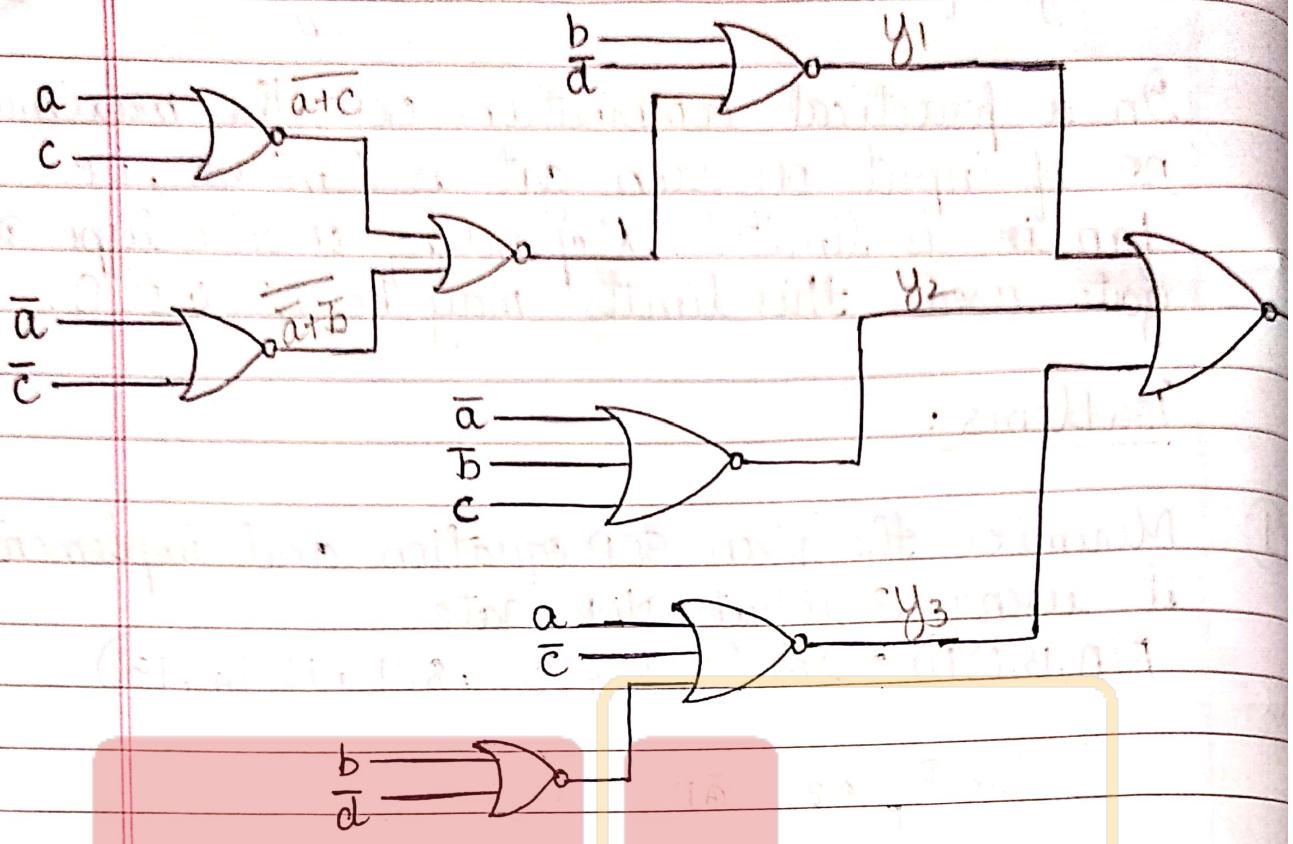
$$F = \bar{A}\bar{B}\bar{C}D + A\bar{B}CD + \bar{A}C\bar{D} + \bar{A}BC + ABC$$

$$F = (A+B+C+\bar{D})(\bar{A}+B+\bar{C}+\bar{D})(A+\bar{C}+D)(A+\bar{B}+\bar{C}) \\ (\bar{A}+\bar{B}+C)$$

$$\bar{F} = \bar{a}\bar{b}\bar{c}d + a\bar{b}cd + ab\bar{c} + \bar{a}bc + \bar{a}c\bar{d}$$

$$F = \bar{b}d[(\bar{a}\bar{c}) + (ac)] + ab\bar{c} + \bar{a}c[(b+d)]$$

$$= [(b+d) + (a+c)(\bar{a}+\bar{c})][\bar{a}+\bar{b}+c][(\bar{a}+\bar{c})+(b+d)] \\ = [b+\bar{d} + (a+c)(\bar{a}+\bar{c})][\bar{a}+\bar{b}+c][\bar{a}+\bar{c}+b+\bar{d}]$$



(2) Minimize the following function & implement only  $\bar{a}$  inputs NAND gate & invertors.

$$F_1 = \sum m(0, 3, 4, 5, 2)$$

$$F_2 = \sum m(0, 2, 3, 4, 7)$$

$$F_3 = \sum m(1, 2, 6, 7)$$

$A \quad BC \quad \bar{B}\bar{C} \quad \bar{B}C \quad BC \quad B\bar{C}$

$\bar{A}$	1 <sub>0</sub>	1	1 <sub>3</sub>	1 <sub>2</sub>
$A$	1 <sub>4</sub>	1 <sub>5</sub>	1 <sub>7</sub>	1 <sub>6</sub>

$$F_1 = \bar{B}A + \bar{B}\bar{C} + B\bar{A}$$

$$F_1 = \bar{B}(a+\bar{c}) + \bar{a}b$$

$A \quad BC \quad \bar{B}\bar{C} \quad \bar{B}C \quad BC \quad B\bar{C}$

$\bar{A}$	1 <sub>0</sub>	1	1 <sub>3</sub>	1 <sub>2</sub>
$A$	1 <sub>4</sub>	1 <sub>5</sub>	1 <sub>7</sub>	1 <sub>6</sub>

$$F_2 = \bar{B}\bar{C} + BC + \bar{A}B$$

$$F_2 = \bar{B}\bar{C} + b(\bar{a}+c) \quad \text{OR}$$

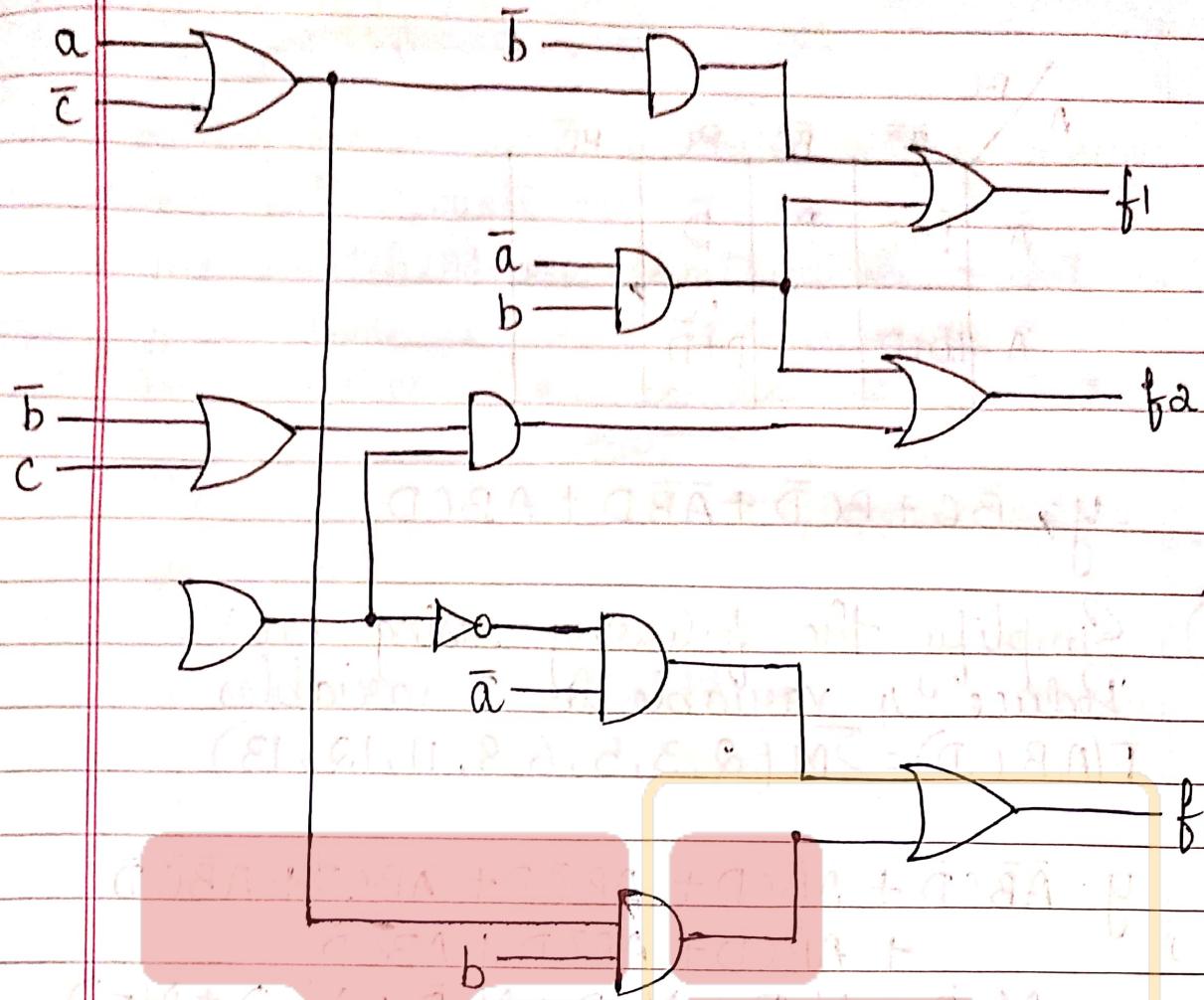
$$(B+C)(B+\bar{C}) + \bar{a}b$$

$A \quad BC \quad \bar{B}\bar{C} \quad \bar{B}C \quad BC \quad B\bar{C}$

$\bar{A}$	0	1 <sub>1</sub>	2	1 <sub>2</sub>
$A$	4	5	1 <sub>7</sub>	1 <sub>6</sub>

$$F_3 = \bar{A}\bar{B}C + AB + B\bar{C}$$

$$F_3 = \bar{a}\bar{b}c + b(a+\bar{c})$$



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Map : Entered Variable

① Simplify the following using VEM or MEV

$$y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D \\ A\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + ABCD.$$

$$y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD + A\bar{B}C\bar{D} \\ + ABC\bar{D}$$

$$= M_0\bar{D} + M_0D + M_4\bar{D} + M_4D + M_1D + M_3\bar{D} + M_2\bar{D} \\ + M_2\bar{D}.$$

$$= M_0\bar{D} + M_0D + M_1D + M_3\bar{D} + M_4D + M_4\bar{D} + M_7D + M_7\bar{D}$$

$$= M_0(D + \bar{D}) + M_1D + M_3\bar{D} + M_4(D + \bar{D}) + M_7(D + \bar{D})$$

	$A$	$\bar{A}$	$B\bar{C}$	$\bar{B}C$	$BC$	$B\bar{C}$	
$G_{11}$			$\bar{D}+D$	$D$	$\bar{D}$		$G_{12}$
	$A$		$\bar{D}+D$		$D+\bar{D}$		$G_{14}$

$$y = \bar{B}\bar{C} + BC\bar{D} + \bar{A}\bar{B}D + ABD.$$

(2) Simplify the following using MEV.

Reduce 4 variable to 3 variables

$$F(A, B, C, D) = \sum m(2, 3, 5, 6, 8, 11, 12, 13)$$

Sol:

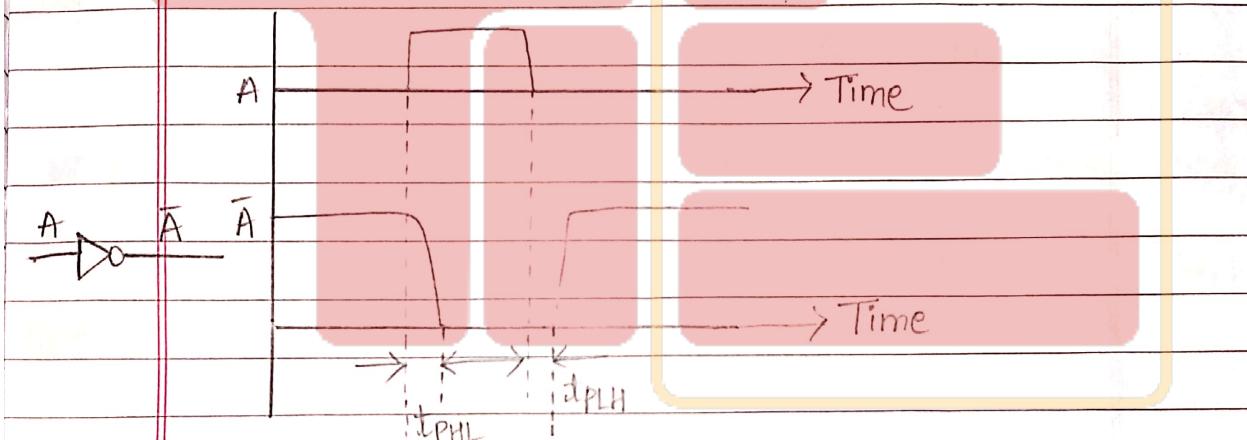
$$\begin{aligned}
 y &= \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{ABC}\bar{D} + \bar{ABC}\bar{D} + A\bar{B}\bar{C}\bar{D} \\
 &\quad + A\bar{B}CD + AB\bar{C}\bar{D} + ABC\bar{D} \\
 &= M_1\bar{D} + M_1D + M_2D + M_3\bar{D} + M_4\bar{D} + M_5D \\
 &\quad + M_6\bar{D} + M_6D \\
 &= M_1(D + \bar{D}) + M_2D + M_3\bar{D} + M_4\bar{D} + M_5D + \\
 &\quad M_6(D + \bar{D})
 \end{aligned}$$

	$A$	$\bar{A}$	$B\bar{C}$	$\bar{B}C$	$BC$	$B\bar{C}$	
$G_{11}$			$\bar{D}+\bar{D}$	$\bar{D}$	$D$	$\bar{D}$	$G_{12}$
	$A$		$\bar{D}$	$D$	$M_1$	$D+\bar{D}$	$G_{14}$

$$y = B\bar{C}D + \bar{A}\bar{C}\bar{D} + \bar{B}CD + A\bar{C}\bar{D}.$$

## Gate delays and Timing diagrams:

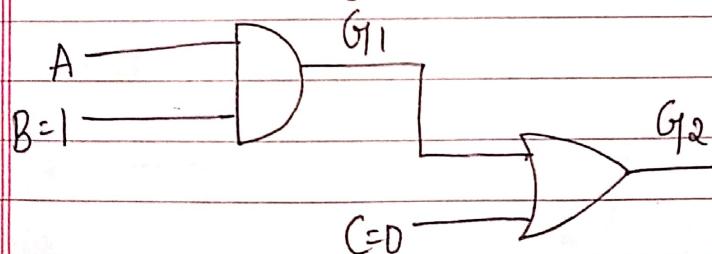
- When the input to a logic gate is changed, the output will not change immediately.
- The switching elements within a gate take a finite time to react to change in input.
- As a result change in the gate output is delayed with respect to input change. Such delay is called propagation delay of logic gate.
- The propagation delay for 0 to 1 output change ( $t_{PLH}$ ) may be different than the delay for a 1 to 0 change ( $t_{PHL}$ ).



Propagation Delay in an inverter.

①

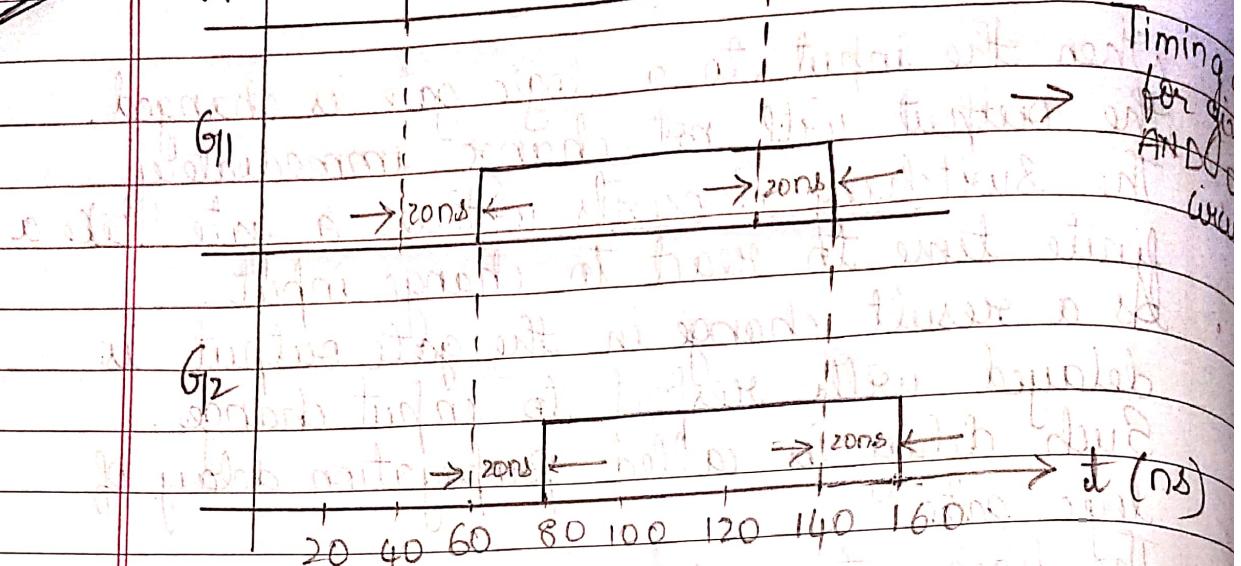
Draw the timing diagram for the circuit shown in figure assuming that each gate has a Propagation delay of 20 ns.



Solu:

A

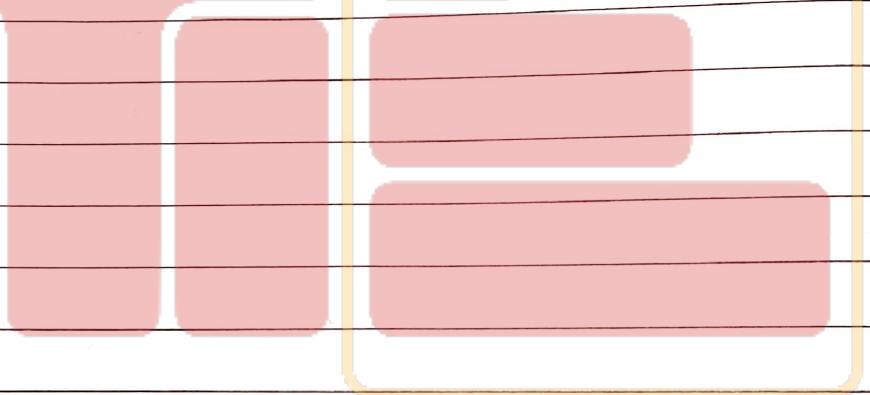
INTERFACIAL ZONE



Second division (daughter cell) starts at 120ns and ends at 160ns.

Daughter cell 1 starts at 120ns and ends at 160ns.

Daughter cell 2 starts at 120ns and ends at 160ns.



metaphase in the second division

the other cell has completed division and moved along the division line. Both daughter cells are in interphase, do not yet contain centrosomes. A and

