Module- 5

Fabrication of pn junction

The main fabrication processes are:

1) Thermal oxidation

2) Diffusion

3)Rapid thermal Processing

4) Ion implantation

5) Chemical Vapor deposition

6)Photolithography

7)Etching

8) Metallization

Thermal oxidation :

- Many fabrication steps involve heating up the wafer in order to enhance a chemical process. An important example of this is thermal oxidation of Si to form $Si0_2$.
- This involves placing a batch of wafers in a clean silica (quartz) tube which can be heated to very high temperatures (~800-1000°C) using heating coils in a furnace with ceramic brick insulating liners.
- An oxygen containing gas such as dry 0_2 or H_20 is flowed into the tube at atmospheric pressure, and flowed out at the other end.
- Traditionally, horizontal furnaces were used More recently, it has become common to employ vertical furnaces.
- A batch of Si wafers is placed in the silica wafer holders, each facing down to minimize particulate contamination.
- The wafers are then moved into the furnace. The gases flow in from the top and flow out at the bottom, providing more uniform flow than in conventional horizontal furnaces.
- The overall reactions that occur during oxidation are:

- $Si + 0_2$ —> SiO_2 (dry oxidation)
- $Si + 2H_20$ -» $Si0_2$+ $2H_2$ (wet oxidation)

Fabrication of P-N Junction

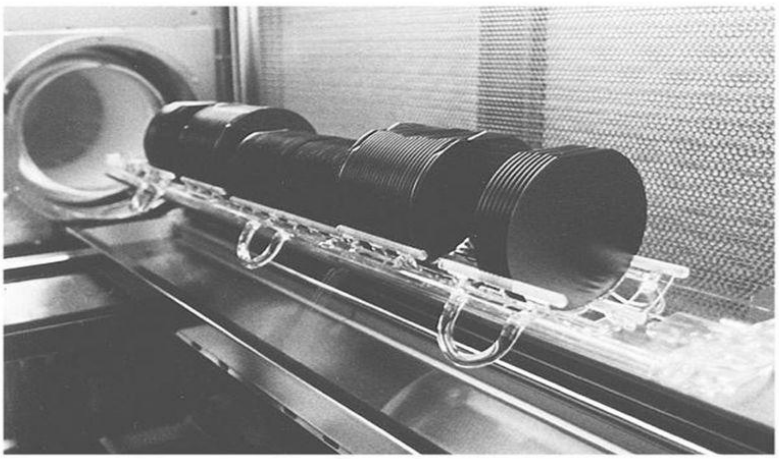


Figure 5—1a
Silicon wafers being loaded into a furnace. For 8-inch and larger wafers, this type of **horizontal loading** is often replaced by a **vertical furnace**.

Diffusion:

- The wafers are first oxidized and windows are opened in the oxide using the photolithography and etching .
- Dopants such as B, P, or As are introduced into these patterned wafers in a high temperature (-800-1100°C) diffusion furnace, generally using a gas or vapor source.
- Trie dopants are gradually transported from the high concentration region near the surface into the substrate through diffusion on temperature, *T.* It is given by $D = D_O \exp-(E_A/kT)$, where D_0 is a constant depending on the material and the dopant, and *EA* is the activation energy. The average distance the dopants diffuse is related to the diffusion length.

Fabrication of P-N Junction

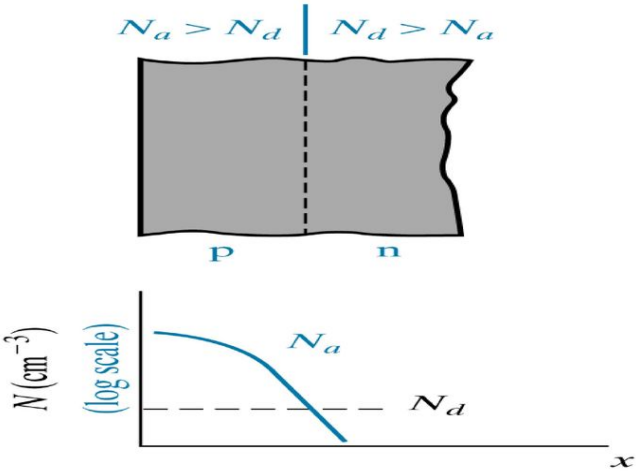
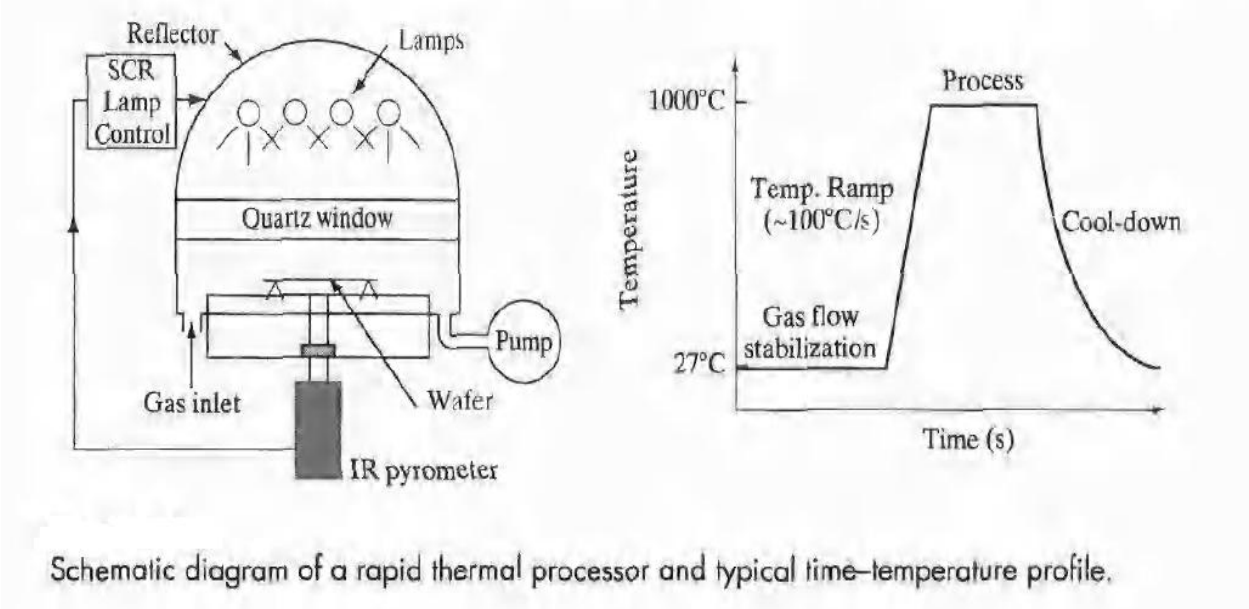


Figure 5—2
Impurity concentration profile for fabricating a p-n junction by diffusion.

Rapid Thermal Processing:



Schematic diagram of a rapid thermal processor and typical time–temperature profile.

- Rapid thermal processing (RTP) includes rapid thermal oxidation, annealing of ion implantation, and chemical vapor deposition.
- A simple RTP system is shown in Fig1 Instead of having a large batch of wafers in a conventional furnace where the temperature cannot be changed rapidly,a single wafer is

held on low-thermal mass quartz pins, surrounded by a bank of high-intensity (tens of kW) tungsten-halogen infrared lamps, with gold-plated reflectors around them.

- By turning on the lamps, the high intensity infrared radiation shines through the quartz chamber and is absorbed by the wafer, causing its temperatur to rise very rapidly (~50-100°C/s).
- The processing temperature can be reached quickly, after the gas flows have been stabilized in the chamber.
- At the end of the process, the lamps are turned off, allowing the wafer temperature to drop rapidly as compared to a furnace.
- In RTP, therefore, temperature is essentially used as a "switch" to start or quench the reaction.

Two critical aspects of RTP are:

- ensuring temperature uniformity across large wafers.
- accurate temperature measurement, for example with thermocouples or pyrometers.

Ion Implantation:

- A useful alternative to high-temperature diffusion is the direct implantation of energetic ions into the semiconductor.
- In this process a beam of impurity ions is accelerated to kinetic energies ranging from several keV to several MeV and is directed onto the surface of the semiconductor.
- As the impurity atoms enter the crystal, they give up their energy to the lattice in collisions and finally come to rest at some average penetration depth, called the *projected range*.
- Depending on the impurity and its implantation energy, *the* range in a given semiconductor may vary from a few hundred angstroms to about 1 um. For most implantations the ions come to rest distributed almost evenly about the projected range *Rp*.

Fabrication of P-N Junction

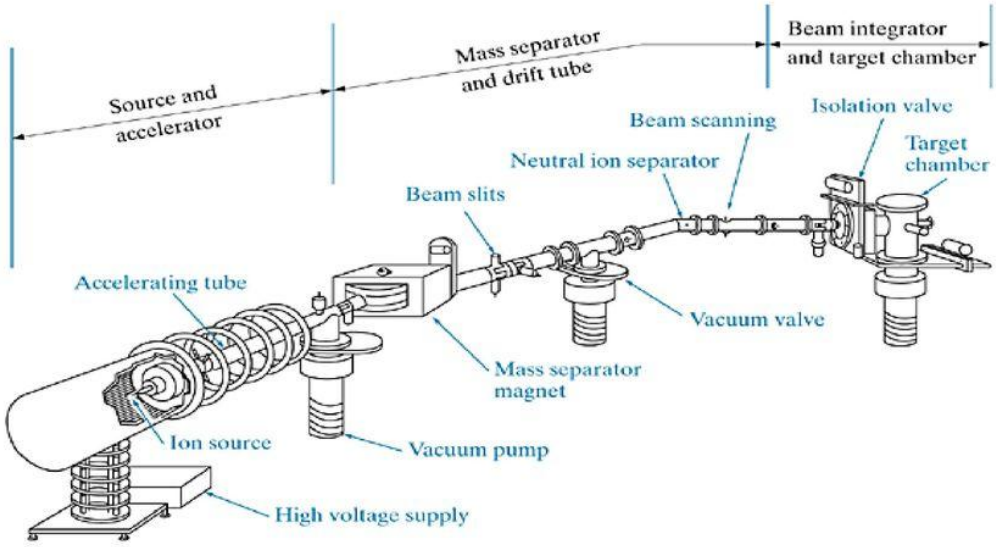


Figure 5—5
Schematic diagram of an ion implantation system.

- An obvious advantage of implantation is that it can be done at relatively low temperatures; this means that doping layers can be implanted without disturbing previously diffused regions.
- One of the major advantages of implantation is the precise control of doping concentration it provides.

Chemical Vapor Deposition(CVD)

- $Si0_2$ films can also be formed by *low pressure (-100* mTorr) chemical vapor deposition (LPCVD) (Fig. 5-6) or plasma-enhanced CVD (PECVD).
- The key differences are that thermal oxidation consumes Si from the substrate, and very high temperatures are required, whereas CVD of $Si0_2$ does not consume Si from the substrate and can be done at much lower temperatures.

- The CVD process reacts a Si-containing gas such as SiH_4 with an oxygen-containing precursor, causing a chemical reaction, leading to the deposition of $Si0_2$ on the substrate. the Si substrate may not be available for reaction, or there may be metallization on the wafer that cannot withstand very high temperatures ,In such cases, CVD is a necessary alternative.

Fabrication of P-N Junction

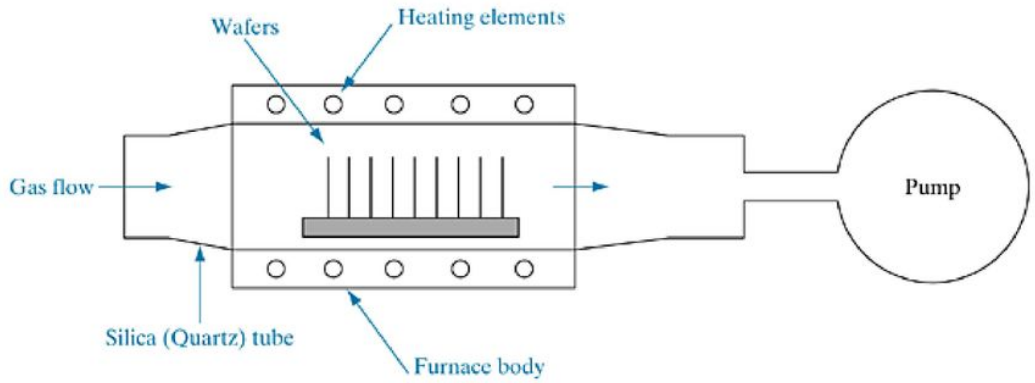


Figure 5—6
Low pressure chemical vapor deposition (LPCVD) reactor.

Photolithography

- Patterns corresponding to complex circuitry are formed on a wafer using *photolithography*.
- This involves first generating a reticle which is a transparent silica (quartz) plate containing the pattern.

Fabrication of P-N Junction

Figure 5—7a
A **photolithographic reticle** used for one step in the processing of a **16 Mb dynamic random access memory (DRAM).** In a "stepper" projection exposure system, ultraviolet light shines through the glass plate and the image **is projected onto** the wafer to **expose photoresist** for one die in the array of circuits, then steps to the next. (Photograph courtesy of IBM Corp.)

- Opaque regions on the mask are made up of an ultraviolet light-absorbing layer, such as iron oxide.
- The reticle typically contains the patterns corresponding to a single *chip rather than the entire wafer (in which case it would be called a mask).*
- *It* is usually created by a computer controlled electron beam driven by the circuit layout data, using pattern generation software.
- A thin layer of electron beam sensitive material called electron beam resist is placed on the iron oxide-covered quartz plate, and the resist is exposed by the electron beam.
- A resist is a thin organic polymer layer that undergoes chemical changes if it is exposed to energetic particles such as electrons or photons.
- The resist is exposed selectively, corresponding to the patterns that are required.
- After exposure, the resist is developed in a chemical solution. There are two types of resist. The developer is either used to remove the exposed (positive resist) or unexposed (negative resist) material.
- The iron oxide layer is then selectively etched off in a plasma to generate the appropriate patterns.
- The reticle can be used repeatedly to pattern Si wafers.

Etching:

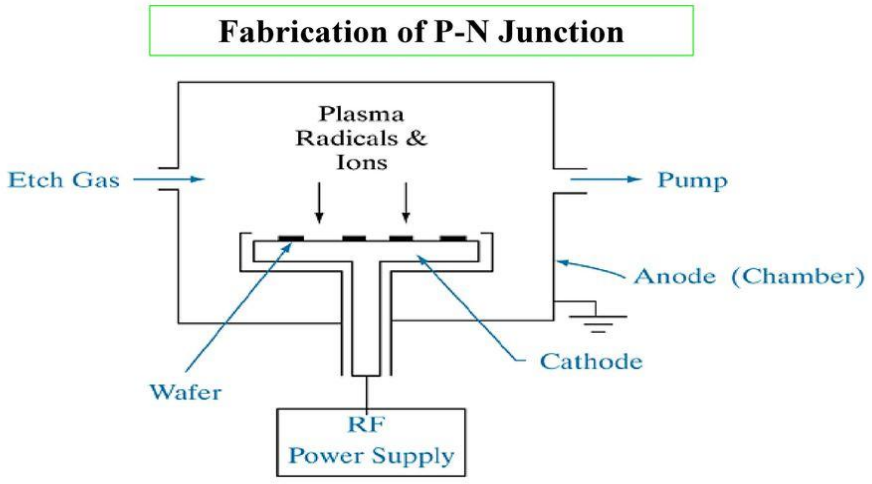


Figure 5—8
Reactive ion etcher. Single or multiple wafers are placed on the rf powered cathode to maximize the ion bombardment. Shown in the figure is a simple *diode* etcher in which we have just two electrodes. We can also use a third electrode to supply rf power separately to the etch gases in a *triode* etcher. **The most commonly used rf frequency is 13.56 MHz**, **which is a frequency dedicated to industrial use so that there is minimal interference with radio communications**.

- After the photoresist pattern is formed, it can be used as a mask to etch the material underneath. In the early days of Si technology, etching was done using wet chemicals.(Wet etching).
- For example, dilute HF can be used to etch Si02 layers grown on a Si substrate with excellent *selectivity.*
- The most popular type of plasma based etching is known as *reactive ion etching (RIE).*
- In a typical process, appropriate etch gases such as chlorofluorocarbons (CFCs) flow into the chamber at reduced pressure (-1-100 mTorr)(Dry Etching).
- A plasma is struck by applying an rf voltage across a cathode and an anode. The rf voltage accelerates the light electrons in the system to much higher kinetic energies (-10 eV) than the heavier ions. The high energy electrons collide with neutral atoms and molecules to create ions and molecular fragments called radicals.

- The wafers are held on the rf powered cathode, while the grounded chamber walls act as the anode.

Metallization:

- After the semiconductor devices are made they have to be connected to each other, and ultimately to the IC package, by metallization process.
- Metal films are generally deposited by a physical vapor deposition technique such as evaporation (e.g., Au on GaAs) or sputtering (e.g., Al on Si).

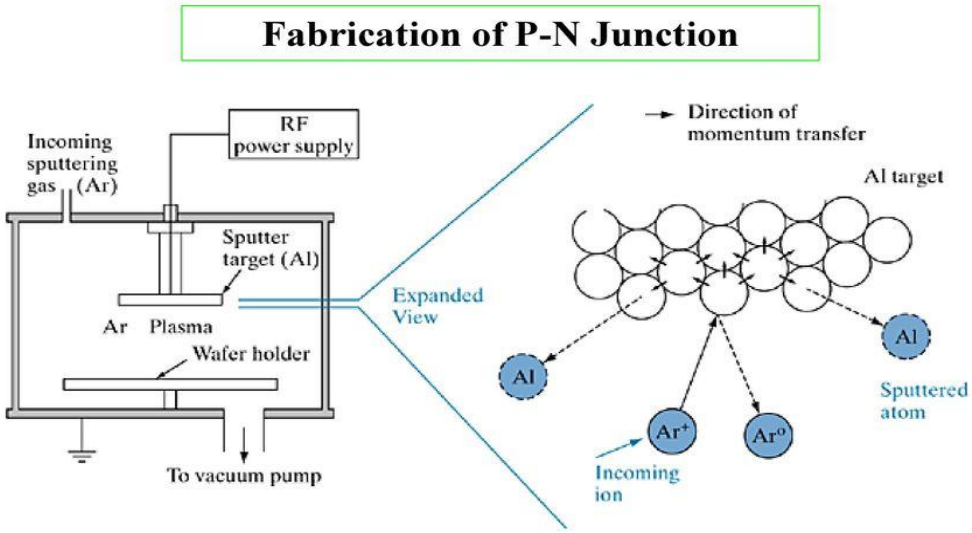


Figure 5—9
Aluminum sputtering by Ar^+ ions. The Ar^+ ions with energies of ~1–3 keV physically dislodge Al atoms which end up depositing on the Si wafers held in close proximity. The chamber pressures are kept low such that the mean free path of the ejected Al atoms is long compared to the target-to-wafer separation.

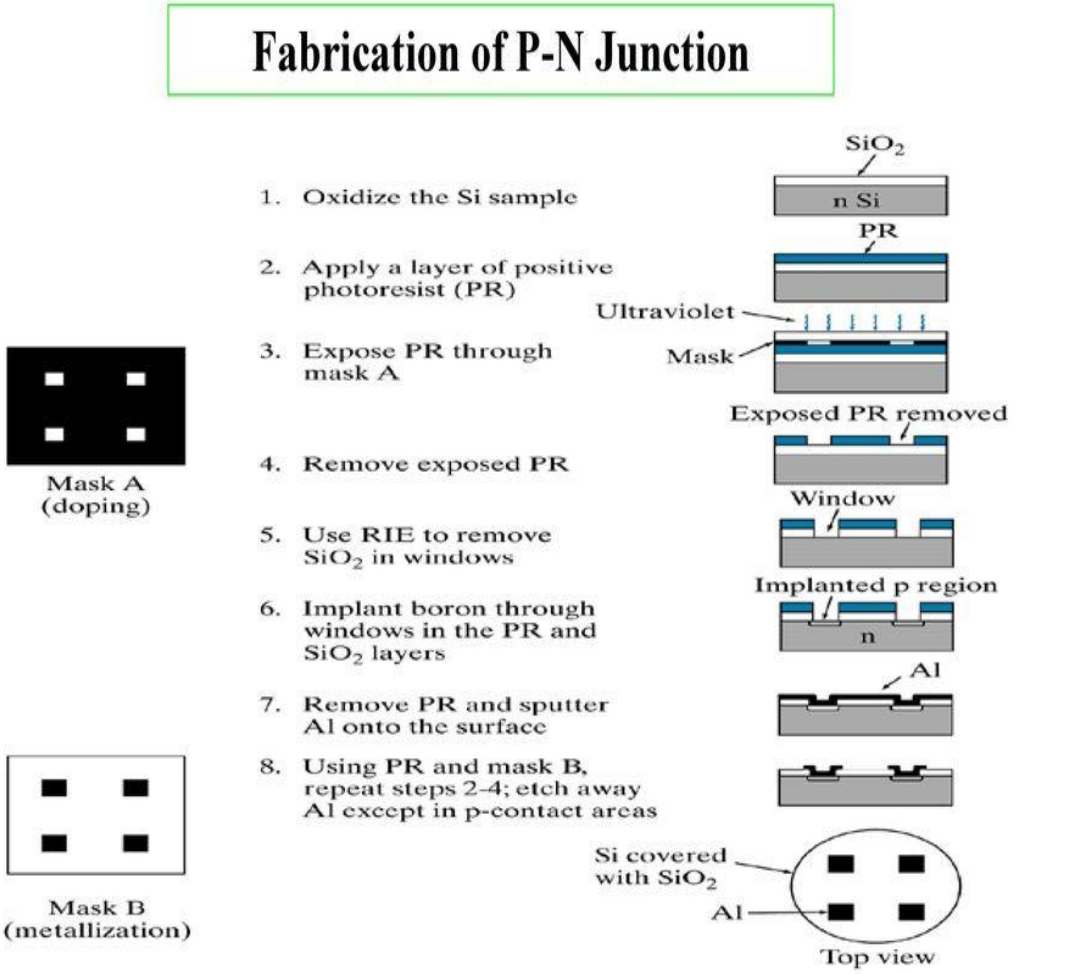


Figure 5—10
Simplified description of steps in the fabrication of p-n junctions. For simplicity, only four diodes per wafer are shown, and the relative thicknesses of the oxide, PR, and the Al layers are exaggerated.

Advantages of Integration:

- Many identical circuits can be built simultaneously on a single Si wafer this process is called **batch fabrication**.
- Although the processing steps for the wafer are complex and expensive, the large number of resulting integrated circuits makes the ultimate cost of each fairly low.
- The processing steps are essentially the same for a circuit containing millions of transistors as for a simpler circuit.

- Helps to build increasingly complex circuits and systems on each chip, and use larger Si wafers as a result, the number of components in each circuit increases without a proportional increase in the ultimate cost of the system.
- Extra components can be added on, without increasing the cost.
- Results in flexibility of design.
- Reliability is also improved since all devices and interconnections are made on a single rigid substrate,greatly minimizing failures due to the soldered interconnections of discrete component circuits

Advantages of Miniaturization:

- Many circuit functions can be packed into a small space, complex electronic equipment can be employed in many applications where weight and space are critical, such as in aircraft or space vehicles.
- Size of complex units are reduced and maintenance becomes easy.
- Response time and the speed of signal transfer between circuits is reduced in case of high frequency circuits.
- Reducing the size of each device greatly increases the chance for a given device to be free of defects(lattice defects).
- Integration(reduced sizing) can reduce parasitic capacitance and inductance between circuits.

The IC was invented in February 1959 by Jack Kilby of Texas instruments. The planar version of the IC was developed independently by Robert Noyce at Fairchild in July 1959.

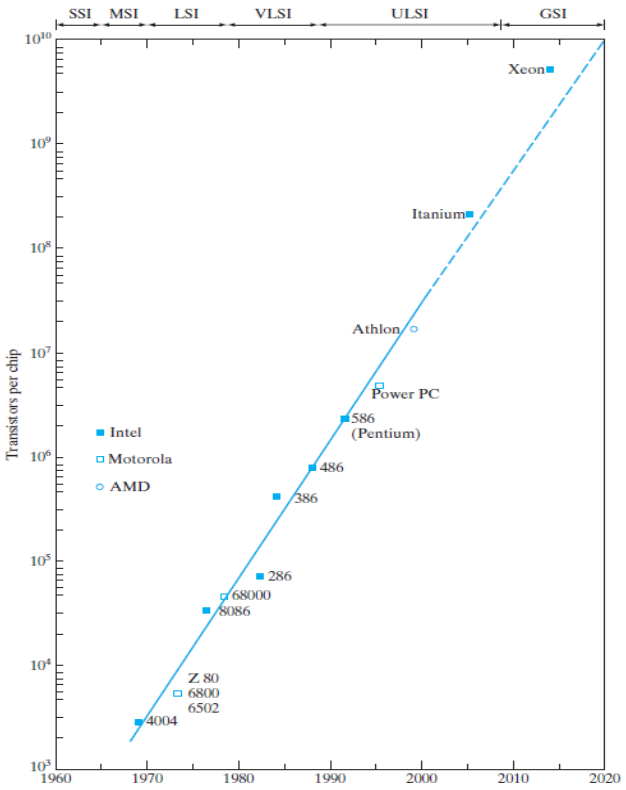


Figure: showing Moore's law for integrated circuits: Exponential increase in transistor count as a function of time for different generations of microprocessors.

The dashed line indicates projections based on the International Technology Roadmap for Semiconductors (ITRS) (constraints: economics & power dissipation)

Evolution of ICs :

- **Moore's Law** refers to Moore's perception that the number of transistors on a microchip doubles every two years, though the cost of computers is halved. Moore's Law states that we can expect the speed and capability of our computers to increase every couple of years, and we will pay less for them.

The history of ICs can be described in terms of different eras, depending on the component count.

- Small- scale integration(SSI) refers to the integration of 1-102 devices.
- medium- scale integration(MSI) to the integration of 102-103 devices.

- LSI to the integration of 103-105 devices.
- very large- scale integration(VLSI)to the integration of 105-106 devices.
- ultra large-scale integration(ULSI) to the integration of 106-109 devices.

Why there is scaling of devices?

- The main factor that has enabled this increase in complexity is the ability to shrink or scale devices.
- Scaling also has other advantages in terms of faster ICs which consume less power.
- The challenges for scaling lie in lithography and etching.
- Since scaling of horizontal dimensions also requires scaling of vertical geometries, there are also tremendous challenges in terms of doping, gate dielectrics, and metallization.
- In addition, small features and large chips require device fabrication in extremely clean environments.
- Particles that may not have caused yield problems in a 1μm IC technology can have catastrophic effects for a 22 nm process, which requires purer chemicals.
- About 90 % of the IC market is MOS based and about 8% BJT based.
- Optoelectronic devices based on compound semiconductors are still a relatively small component of the semiconductor market (about 4%), but are expected to grow in the future.
- Of the MOS Ics,the bulk are digital ICs.
- Of the entire semiconductor industry, only about 14% are analog ICs.
- Semiconductor memories such as DRAMs, SRAMs, and nonvolatile flash memories make up approximately 25% of the market.
- Microprocessors about 25% and other application-specific ICs (ASICs) about 20%.

CMOS Integration:

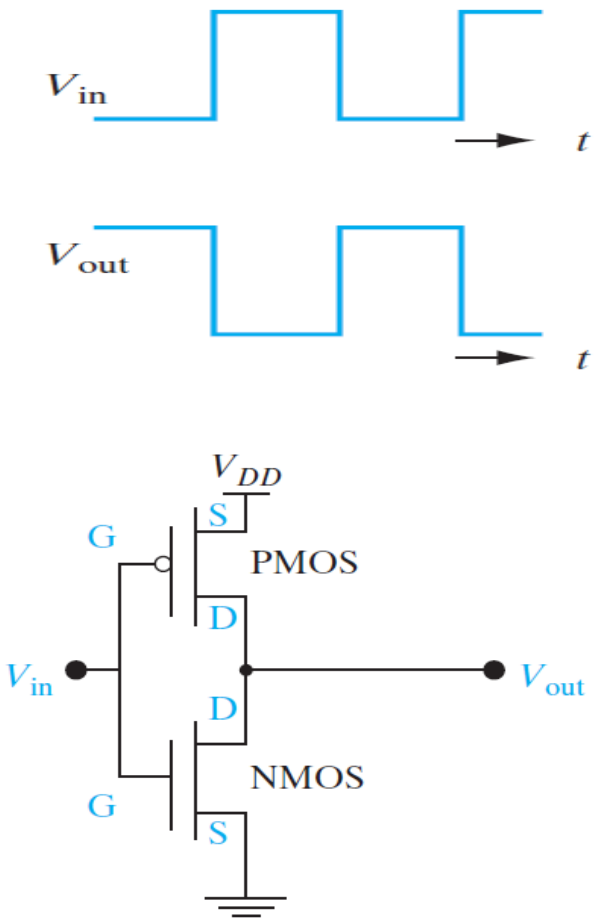


Fig1 CMOS inverter

Formation of p-channel & n-channel devices together:

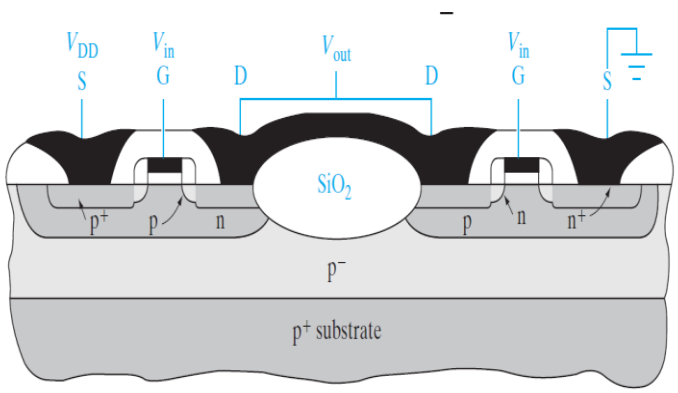


Fig 2: PMOS and NMOS together

- In the circuit (Fig 1) the drains of the two transistors are connected together and form the output.
- The input terminal is the common connection to the transistor gates.
- The p- channel device has a negative threshold voltage, and the n- channel transistor has a positive threshold voltage.

Working :

- A zero voltage input (*Vin = 0)* gives zero gate voltage for the n- channel device, but the voltage between the gate and source of the p-channel device is -*VDD.*
- Thus the p- channel device is ON, the n- channel device is OFF, and the full voltage *VDD is measured* at *Vout (i.e., VDD appears across the nonconducting n*- channel transistor).
- A +ve voltage input a positive value of *Vin turns the n*- channel transistor on, and the p-
- channel off. The output voltage measured across the "on" n- channel device is essentially zero.
- Note: The beauty of this circuit is that one of the devices is turned off for either condition. Since the devices are connected in series, no drain current flows, except for a small charging current during the switching process from one state to the other. **Since the CMOS inverter uses ultra little power, it is used in low power applications.**

Technology for CMOS devices:

- Matching of n and p type transistors is done by ion implantation (for identical threshold voltages)(done by use of tubs and wells)
- Proximity b/w n- channel and p-channel devices can lead to parasitic bipolar stuctures, leading to **latchup problems(large currents).** The solution to this would be to use **trench isolation (separate wells)** which allows independent control of threshold voltages of p & n type of transistor.

Integration of other circuit elements

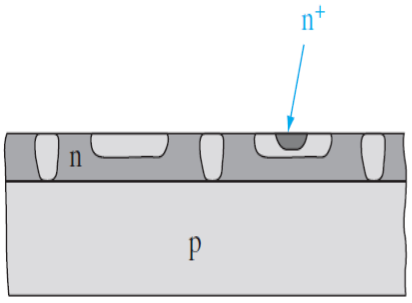
Other circuit elements like resistor, capacitor can also be formed in an integrated circuit.

Diodes.

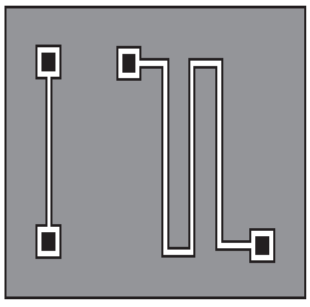
- It is simple to build p- n junction diodes in a monolithic circuit.
- It is also common practice to use transistors to perform diode functions.
- The most common method is to use the emitter junction as the diode, with the collector and base shorted.

Resistors :

- Diffused or implanted resistors can be obtained in monolithic circuits by using the shallow junctions used in forming the transistor regions.
- if the resistor is a p- type channel obtained during the base implant, **the surrounding n material can be connected to the most positive potential in the circuit to provide reverse- bias junction isolation.**
- The resistance of the channel depends on its length, width, depth of the implant, and resistivity of the implanted material.



(a)

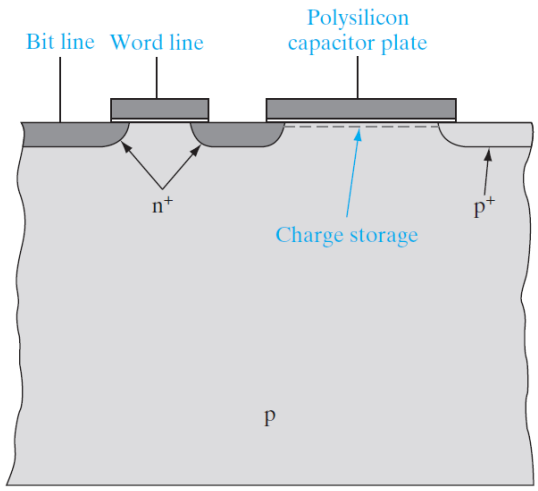


(b)

Monolithic resistors: (a) cross section showing use of base and emitter diffusions for resistors; (b) top view of two resistor patterns.

Capacitors.

- Capacitors are used in case of memory circuits, where charge is stored in a capacitor for each bit of information.



The top plate of the capacitor is polysilicon, and the bottom plate is an inversion charge contacted by an n+ region of the transistor. The terms *bit line and word line* refer to the row and column organization of the memory.

Contacts and Interconnections

- During the metallization step, the various regions of each circuit element are contacted and proper interconnection of the circuit elements is made.
- Aluminum is commonly used for the top metallization, since it adheres well to Si and to SiO2 if the temperature is raised briefly to about 550°C after deposition.
- Gold is used on GaAs devices.

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