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FF is a bistable electronic circuit that has 2 stable states and which stores 1 bit memory cell.

MODULE: 05

Registers and Counters

Registers:

- Flip flop stores 1 bit memory cells at a time
- Register is defined as group of flip flops or collection of flip flops together and it stores n bit flip flops in different types of registers.
- Classification of Registers:

* Shift Register.
* Storage Register

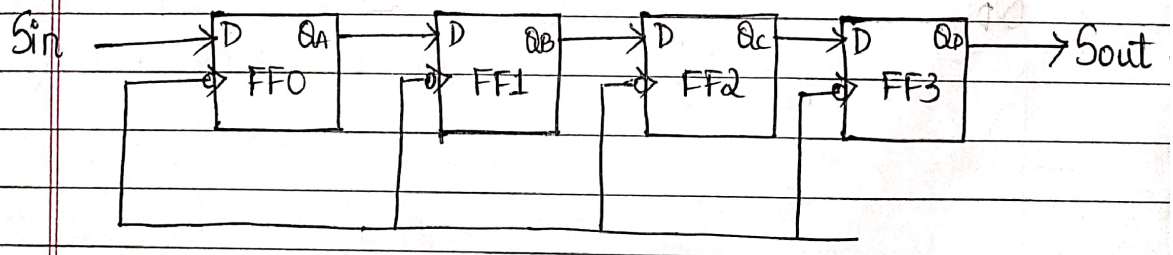
→ In Shift Registers, the input will be shifted one after the other & output is also as same as the input.

→ In Storage Register, whatever the input given, that will store in the current flip flop and immediately it will produce results.

Types of Registers:

1. Serial-In-Serial-Out (SISO) } Shift register.
2. Serial-In-Parallel-Out (SIPO) }
3. Parallel-In-Serial-Out (PISO) }
4. Parallel-In-Parallel-Out (PIPO) } Storage register.

SISO

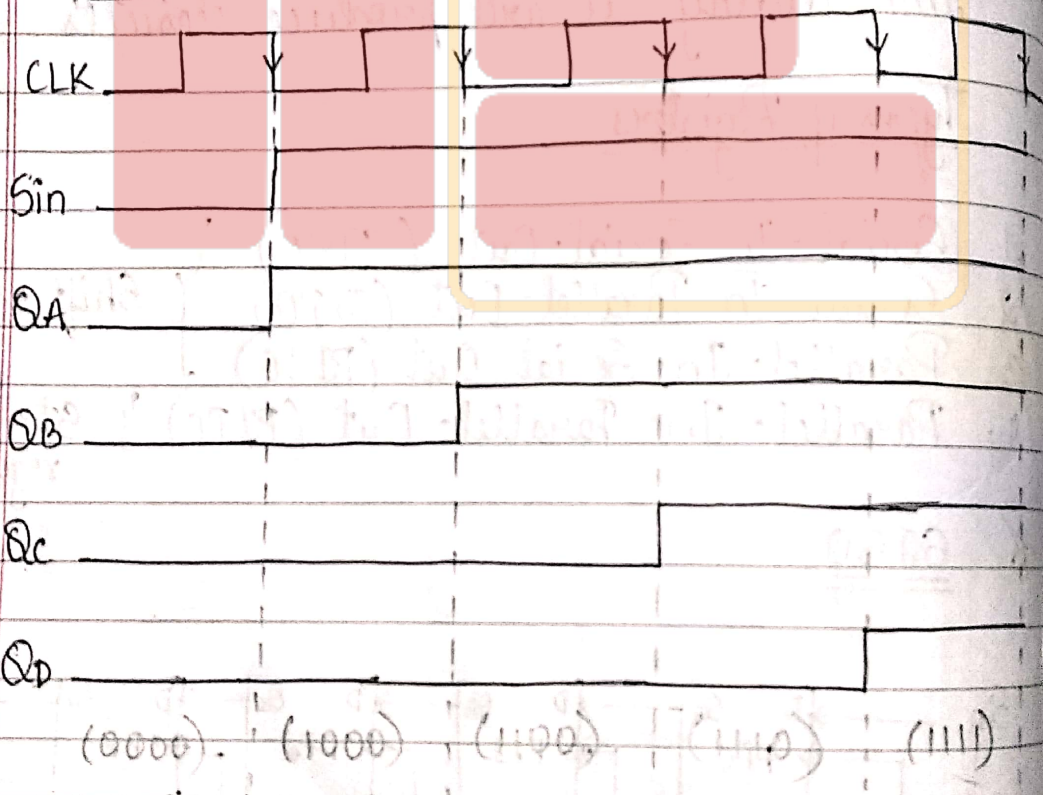


Sin	Q_A	Q_B	Q_C	Q_D
Initial	0	0	0	0
↓	1	0	0	0
↓	1	1	0	0
↓	1	1	1	0
↓	1	1	1	1

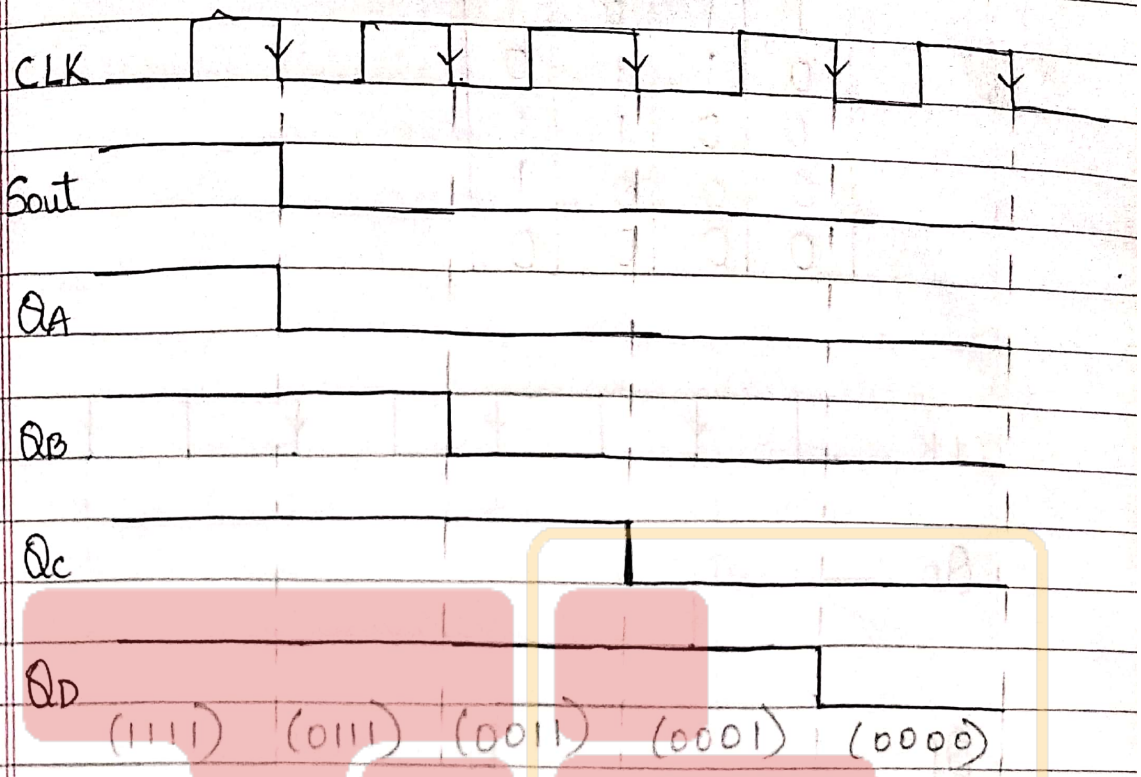
Sout	Q_A	Q_B	Q_C	Q_D
Initial	1	1	1	1
↓	0	1	1	1
↓	0	0	1	1
↓	0	0	0	1
↓	0	0	0	0

→ Timing diagram

A Sin



✱ Sout



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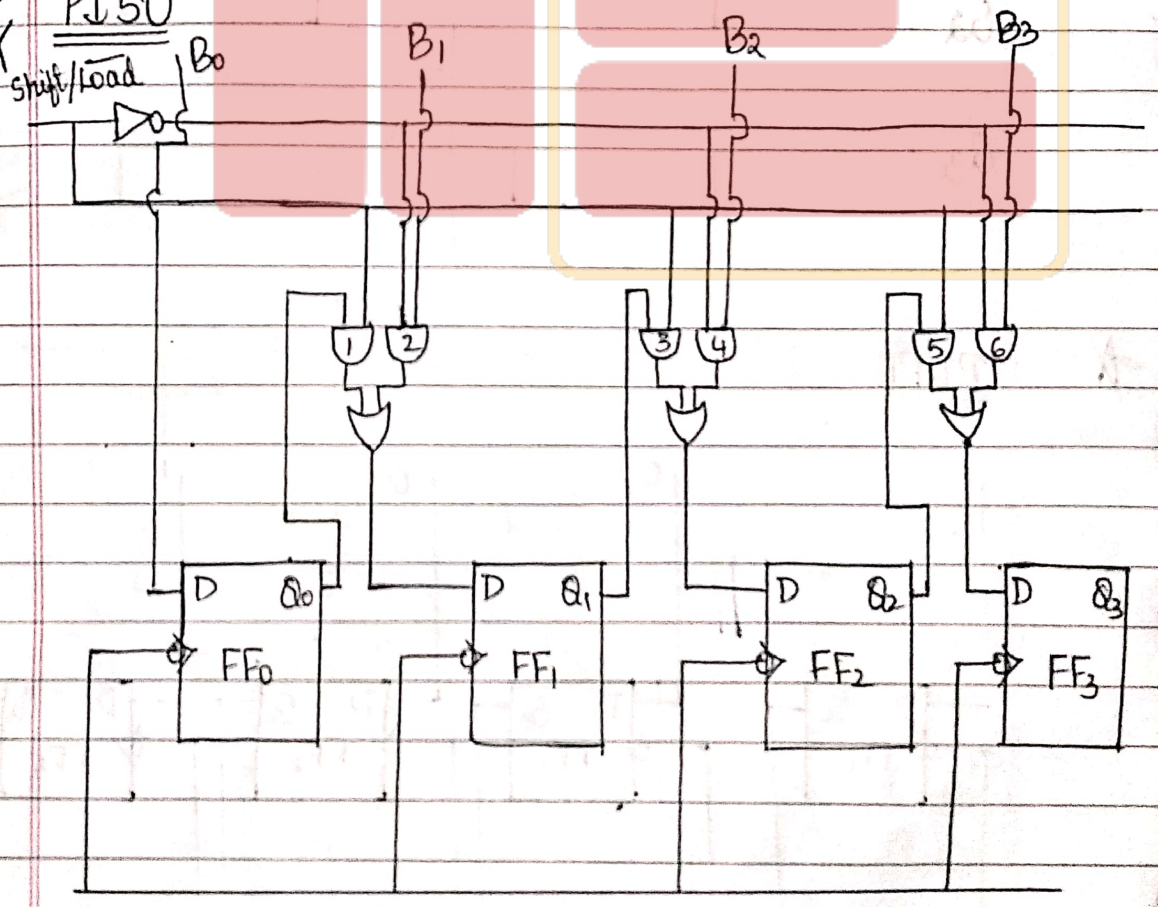
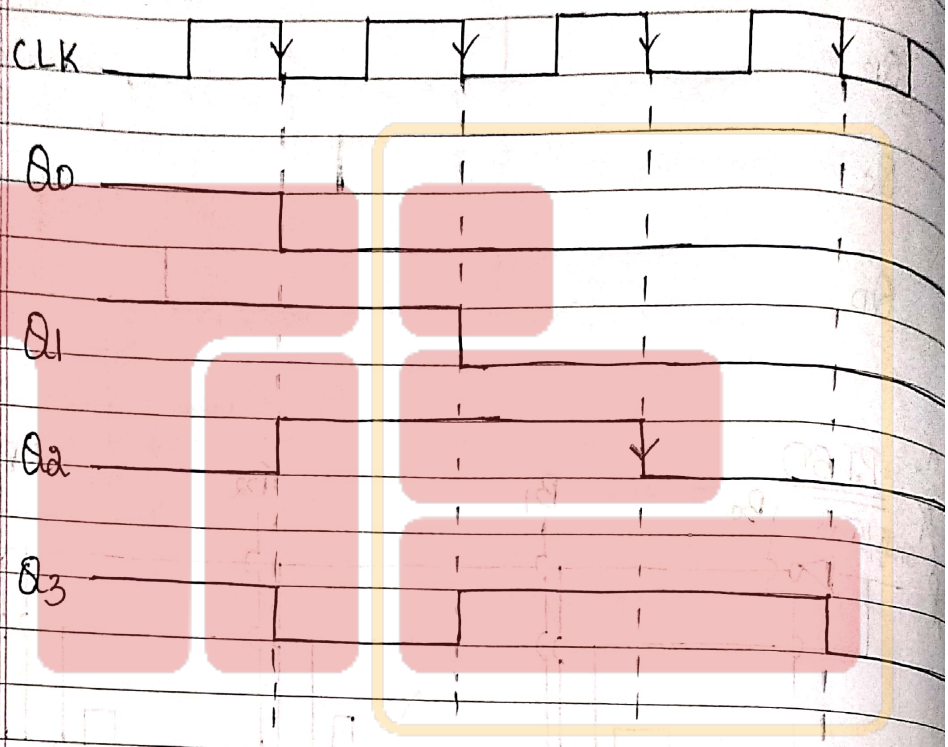
✱ PISO

Inp

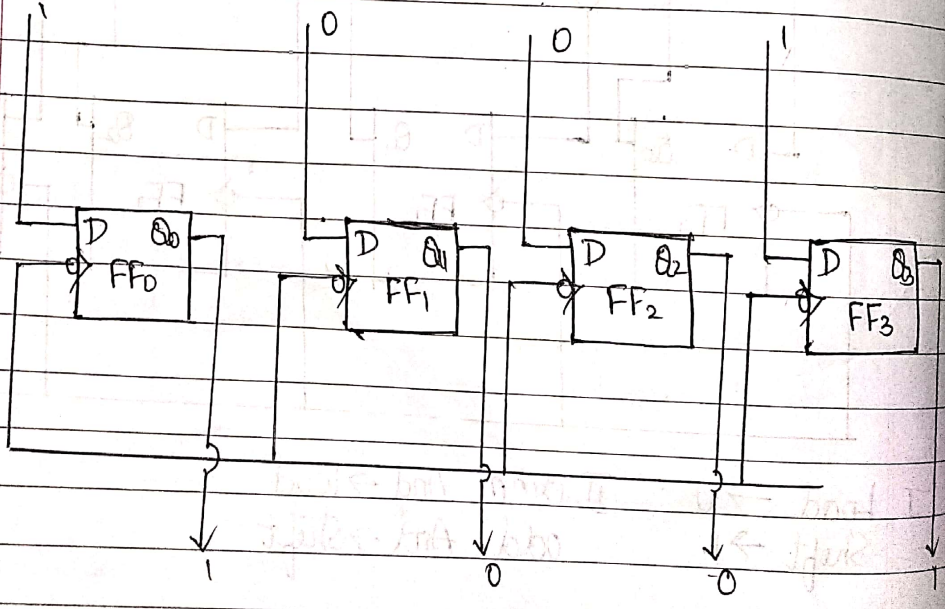


I Load → 0 II Even And → load
Shift → 1 odd And → Shift

Q_0	Q_1	Q_2	Q_3
1	1	0	1
0	1	1	0
0	0	1	1
0	0	0	1
0	0	0	0

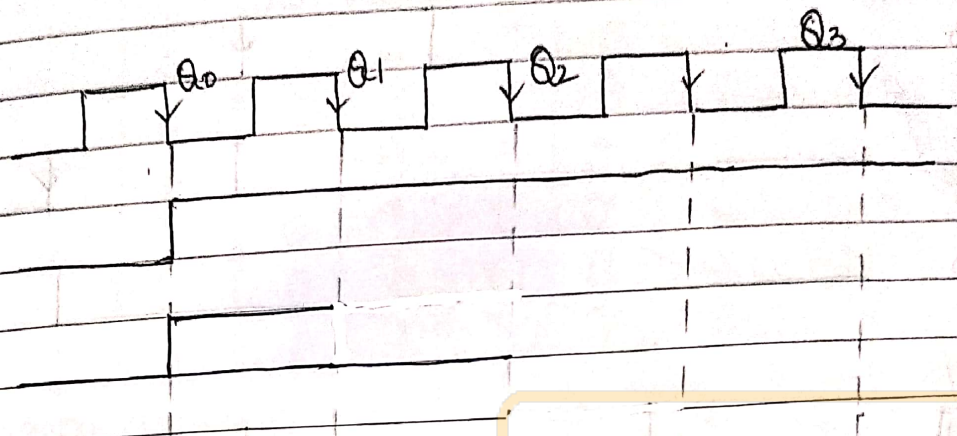


PIPO



Pin	Q_0	Q_1	Q_2	Q_3
	0	0	0	0
	1	0	0	1

Pout	Q_0	Q_1	Q_2	Q_3
	1	0	0	1



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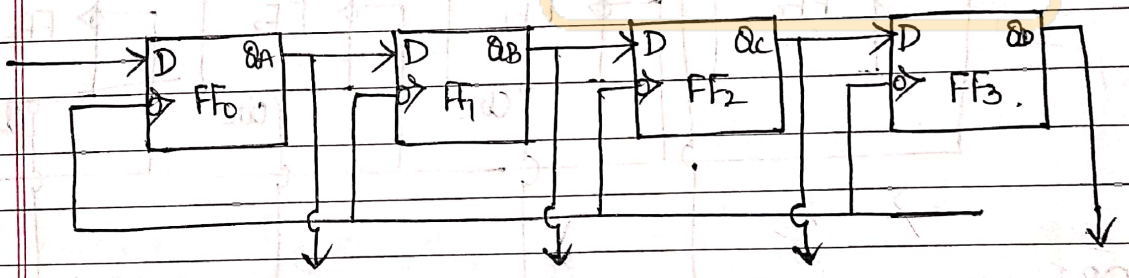
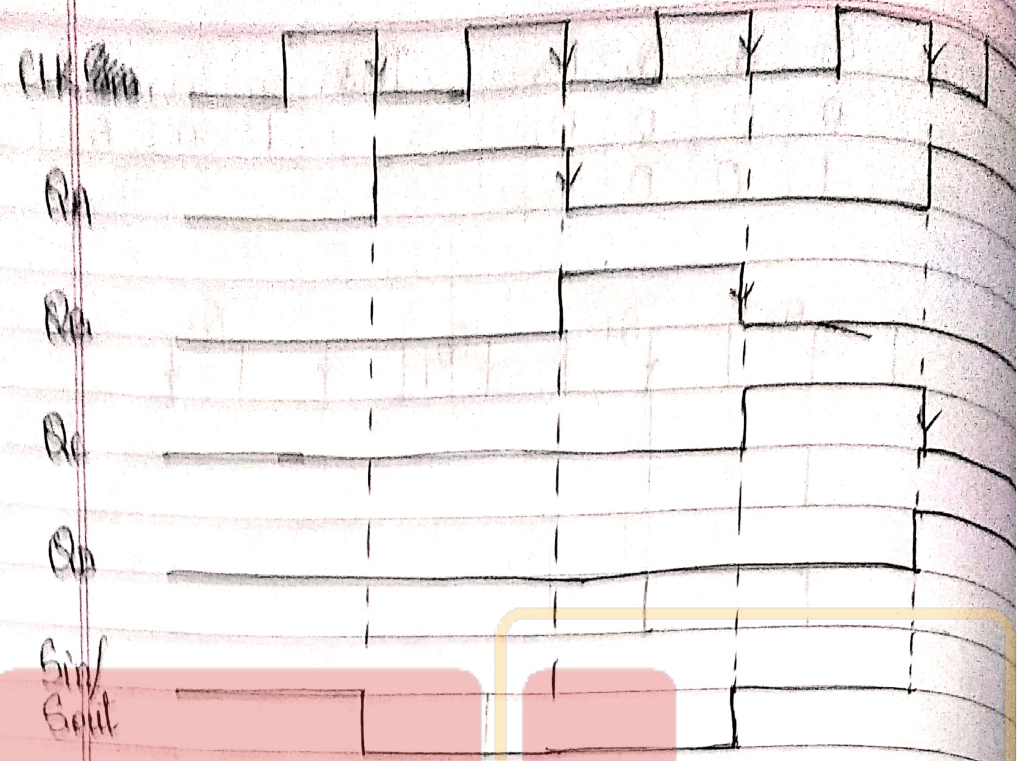
SIPO

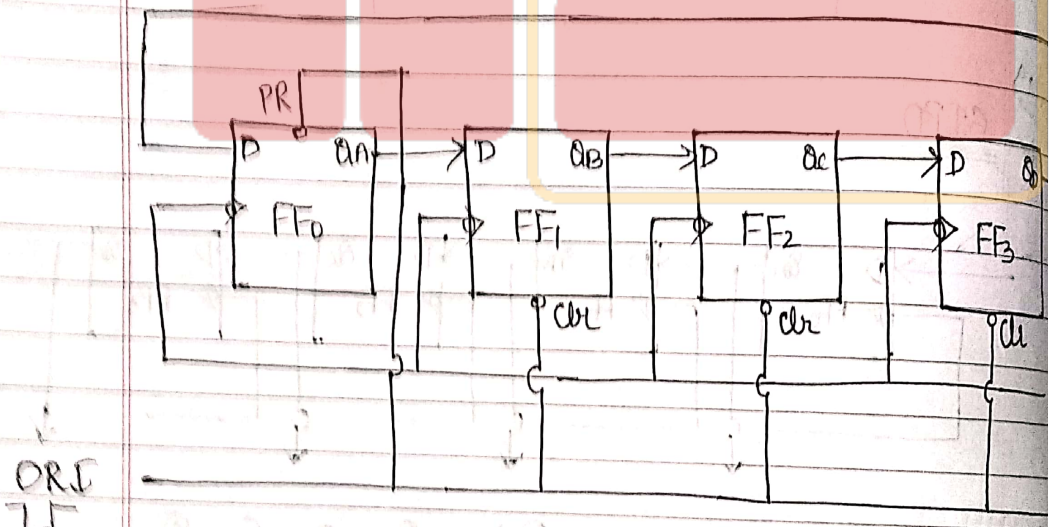


Sin	Q_A	Q_B	Q_C	Q_D
	0	0	0	0
	1	0	0	0
	0	1	0	0
	0	0	1	0
	1	0	0	1

Pout	Q_A	Q_B	Q_C	Q_D
Sin	1	0	0	1
Sout	↓	↓	↓	↓
	1	0	0	1



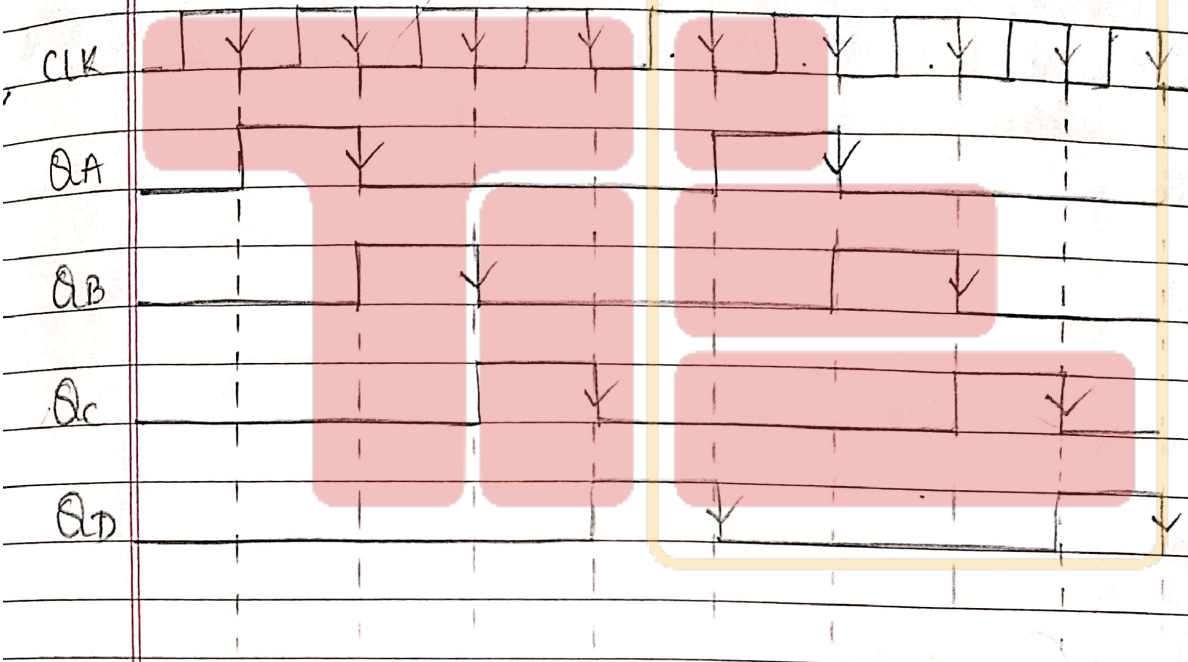
Ring Counter.



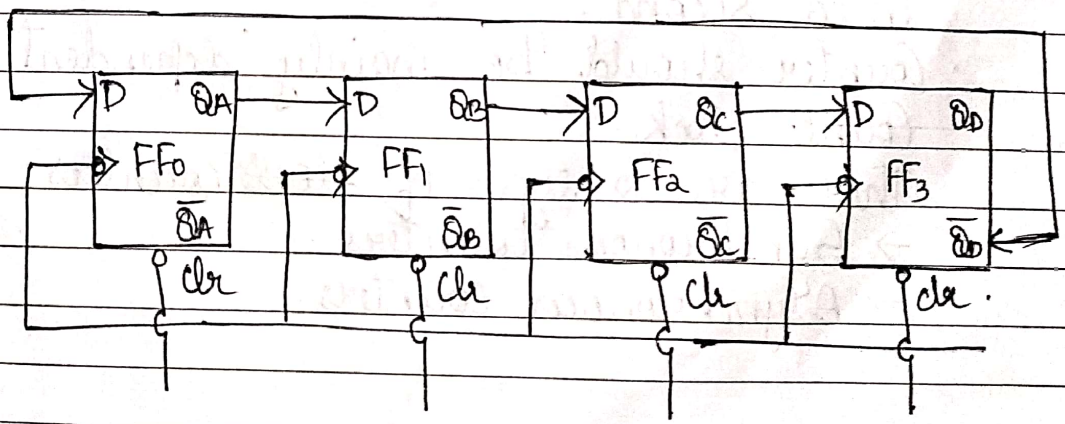
PR = 0 ; Q = 1 } PR = 1
Clr = 0 ; Q = 0 } Clr = 0.

ORI	CLK	Q_A	Q_B	Q_C	Q_D
⊓	X	0	0	0	0
	↓	1	0	0	0
	↓	0	1	0	0
	↓	0	0	1	0
	↓	0	0	0	1
	↓	1	0	0	0
	↓	0	1	0	0
	↓	0	0	1	0
	↓	0	0	0	1

Timing diagram.



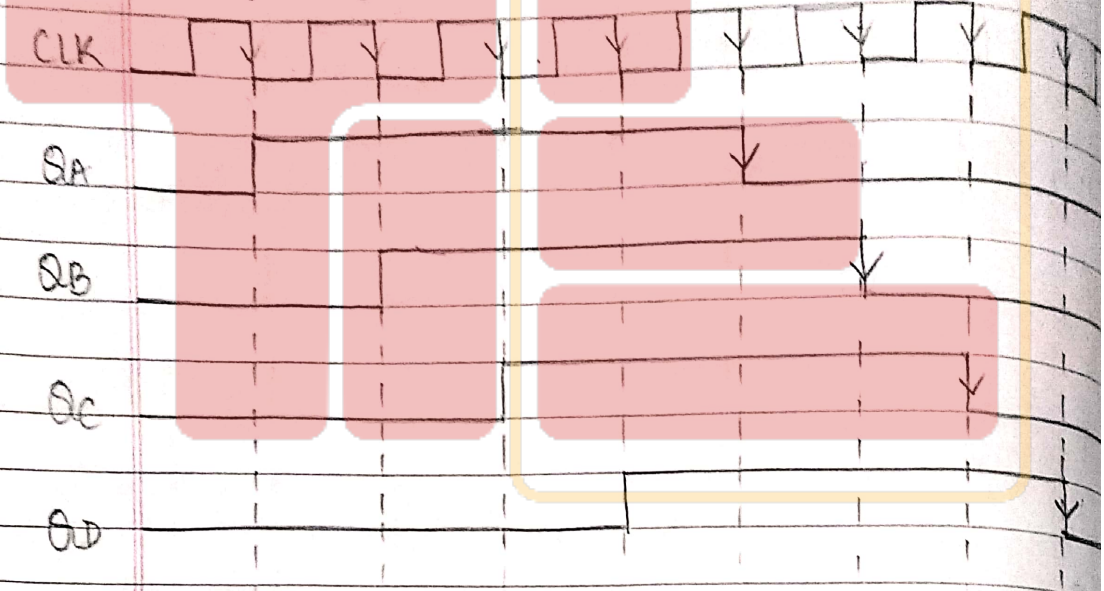
Switch Tail Counter / Johnson Counter / Twisted pair Counter.



Asynchronous (Ripple) Counter

CLK	Q_A	Q_B	Q_C	Q_D
↓	0	0	0	0
↓	1	0	0	0
↓	1	1	0	0
↓	1	1	1	0
↓	1	1	1	1
↓	0	1	1	1
↓	0	0	1	1
↓	0	0	0	1
↓	0	0	0	0

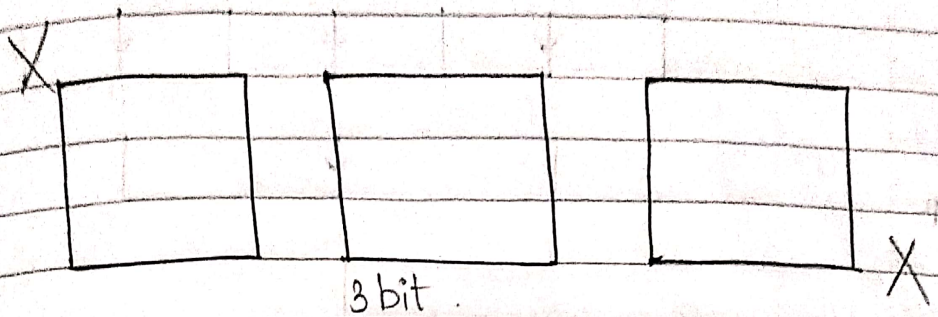
Timing diagram:



Counters

- Counter is defined as count the number in a second.
- Counter should be mainly dependent on ~~Count~~ clock.
- There are 2 types of ~~clock~~ counters:
  → Synchronous counters.
  → Asynchronous counters.

Asynchronous Counter (Ripple Up Counter)

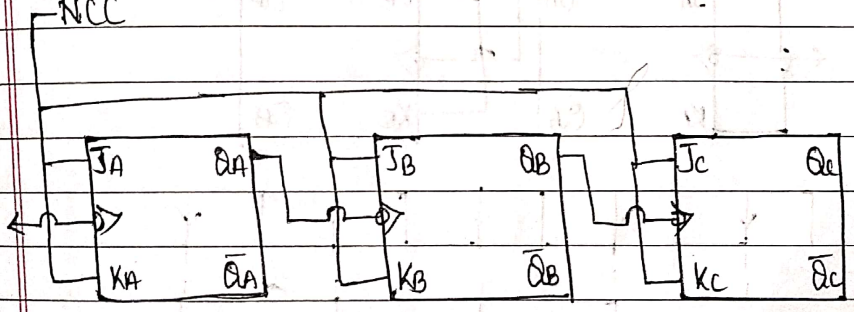


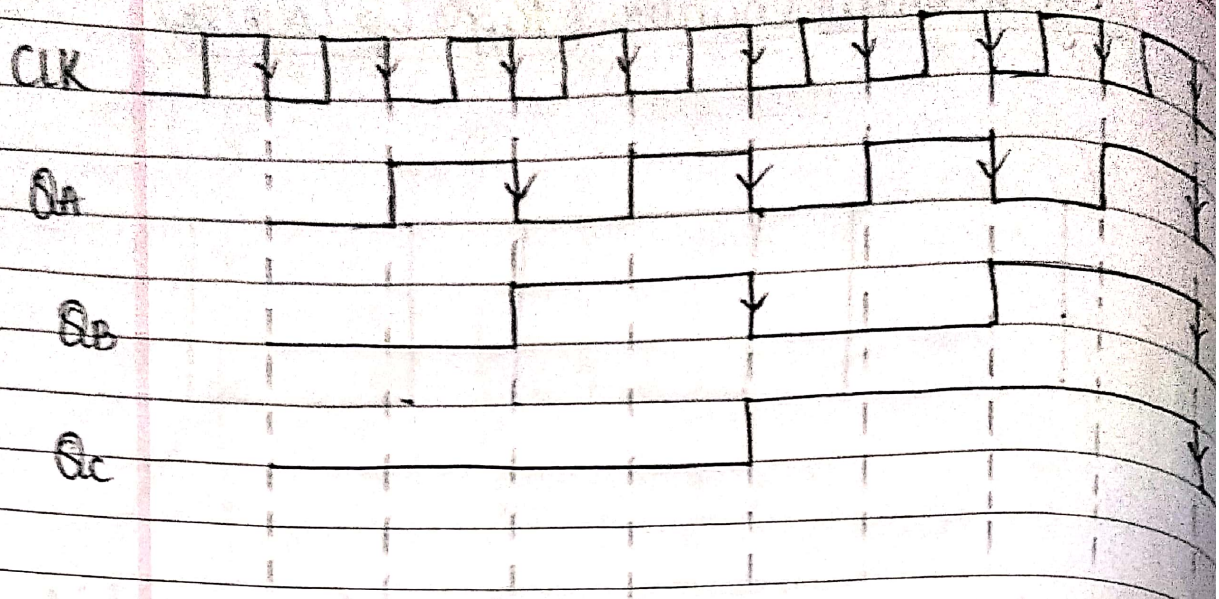
Asynchronous counter is a counter in which the output of the first flip flop is connected to clock of the second flip flop and so on.
There are 3 types of asynchronous counter:
- Up counter
- Down counter
- Up-Down counter

Up Counter:

There are 3 types of up counter.
i) 3-bit
ii) 4-bit
iii) 2-bit

3-bit asynchronous up counter:

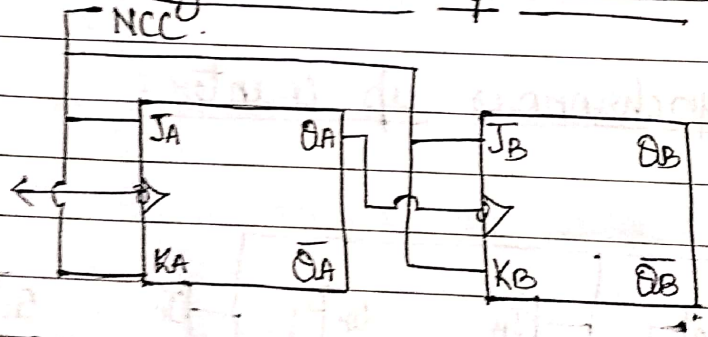


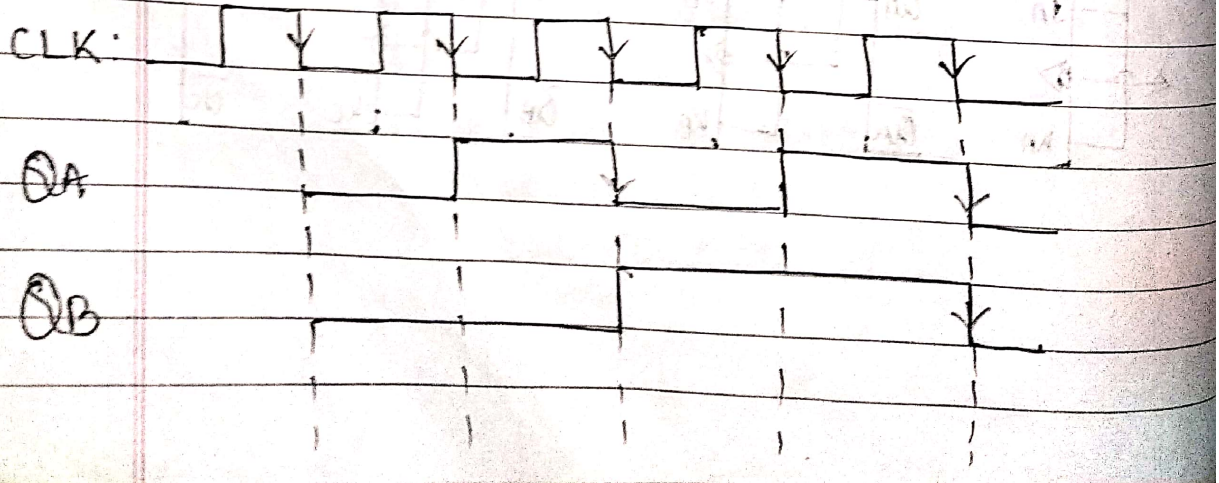


Q_A	Q_B	Q_C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

19/10/19.

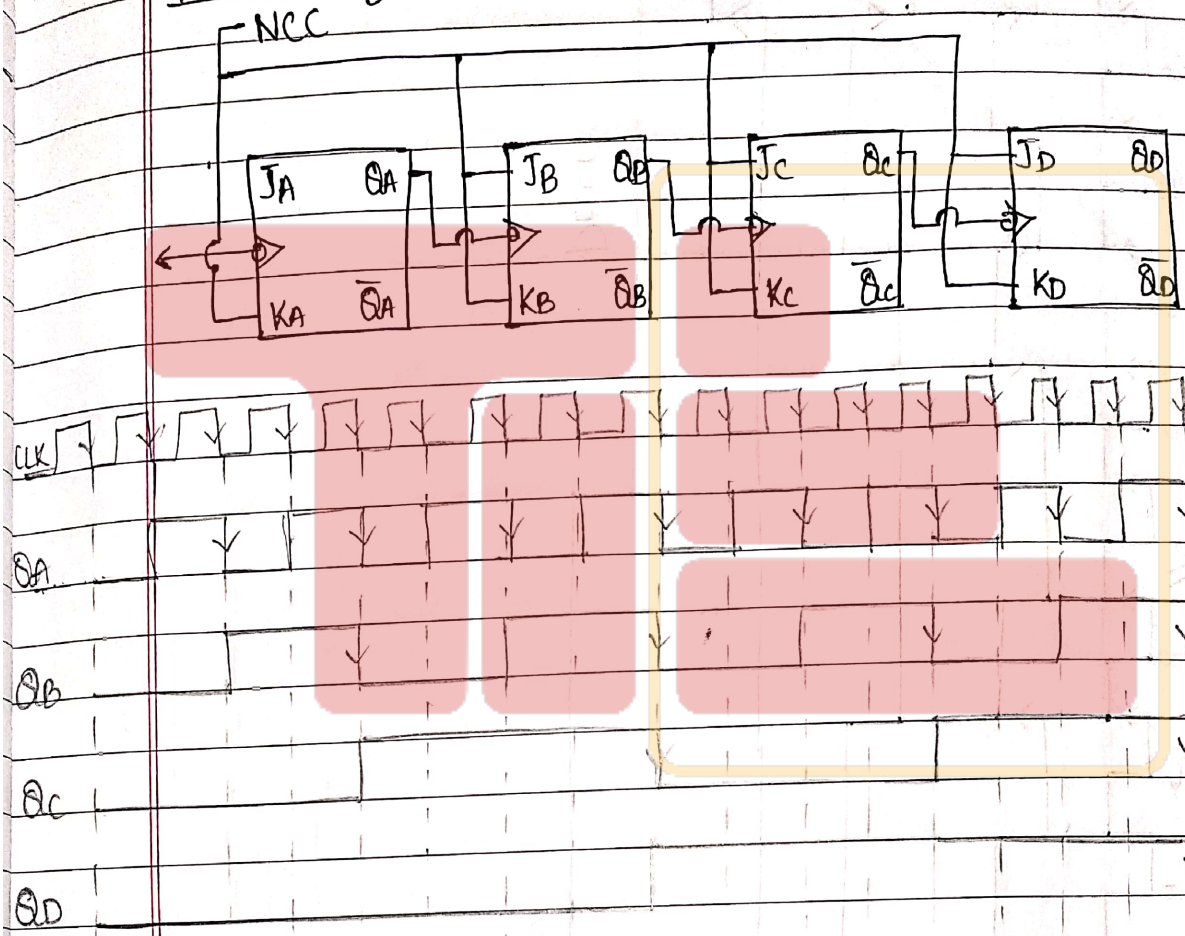
2-bit asynchronous up counter



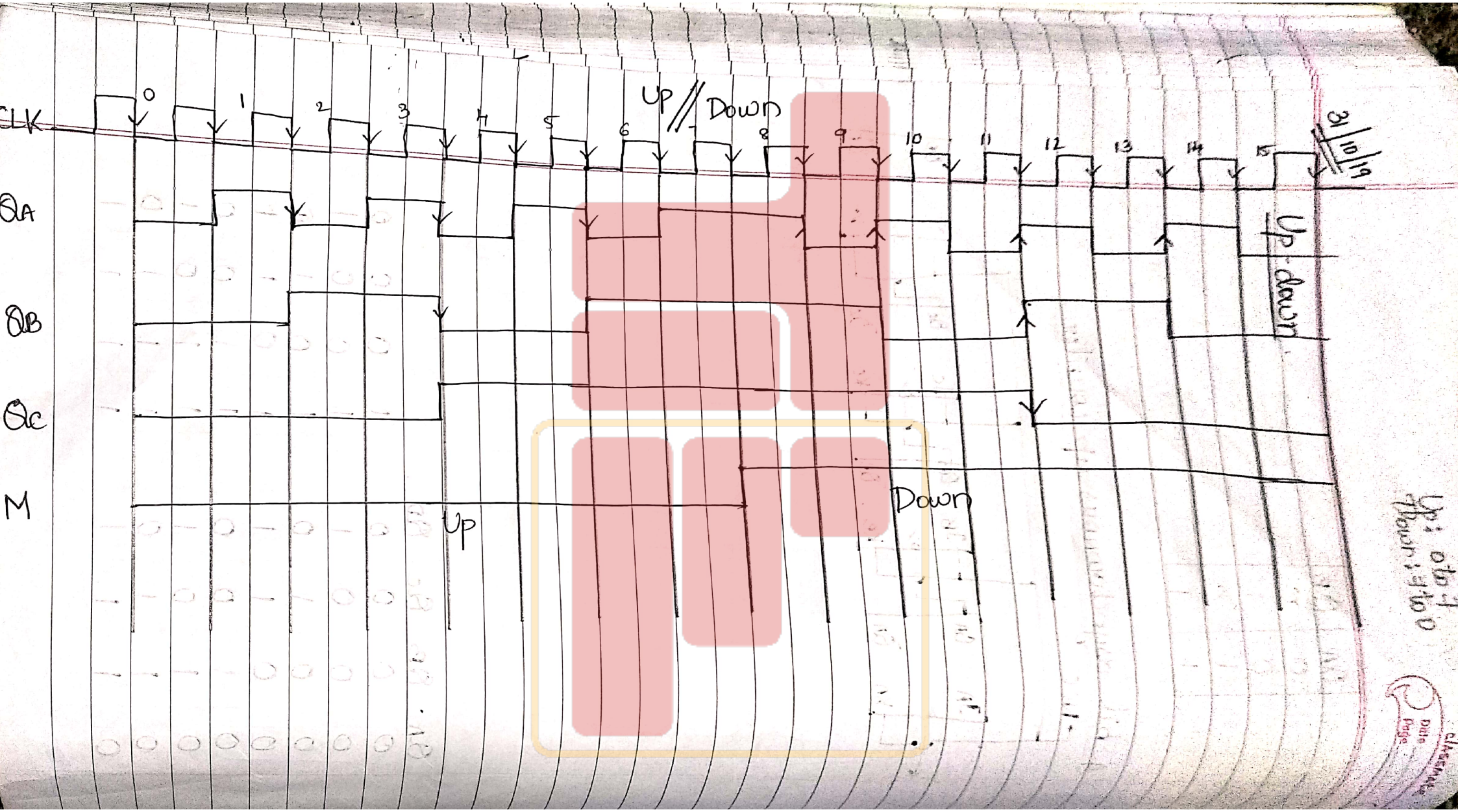


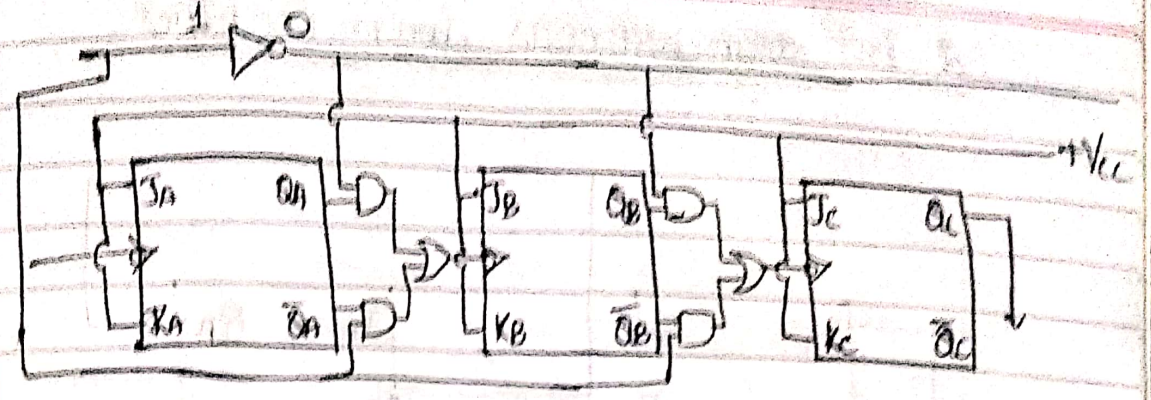
Q_A	Q_B
0	0
0	1
1	0
1	1

4-bit asynchronous up counter



Q_A	Q_B	Q_C	Q_D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

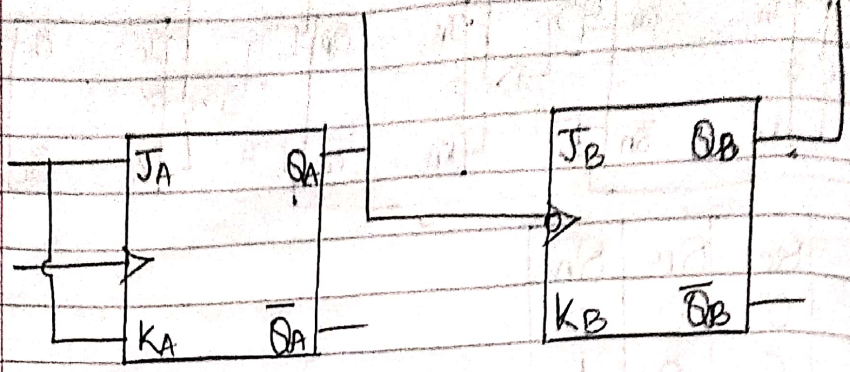

CLK
QA
QB
QC
M
0
1
2
3
4
5
6
Up // Down
8
9
10
11
12
13
14
15
Up down
Up
Down

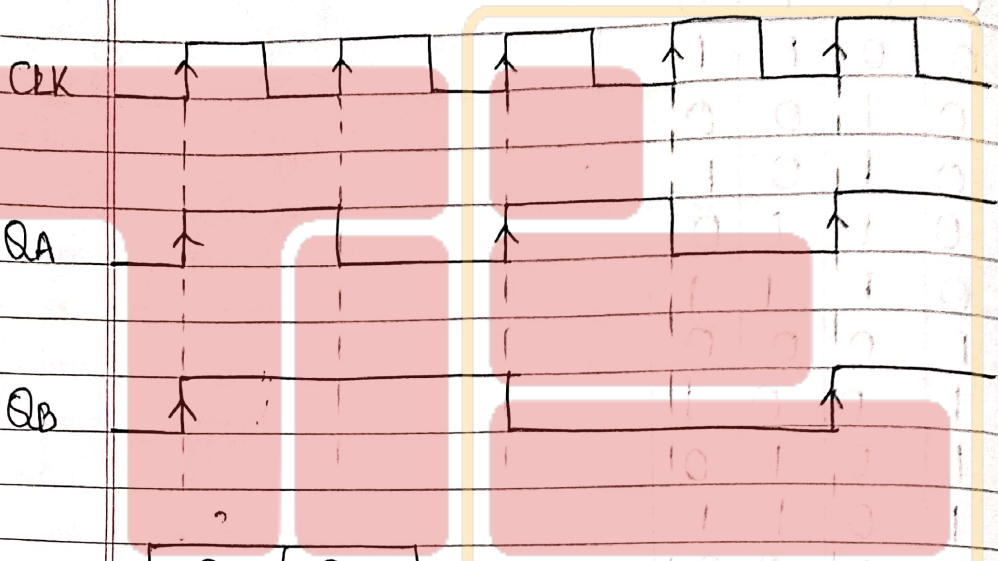


M	Q_C	Q_B	Q_A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Down Counters

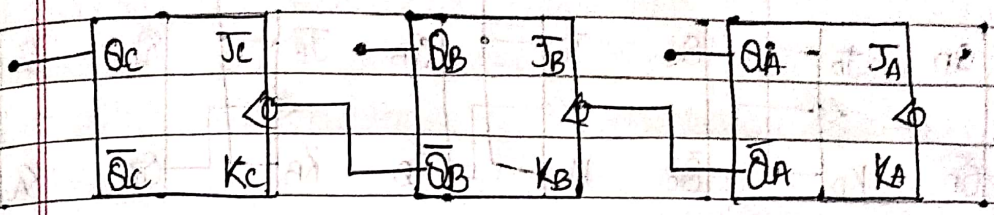
2-bit asynchronous down counters...

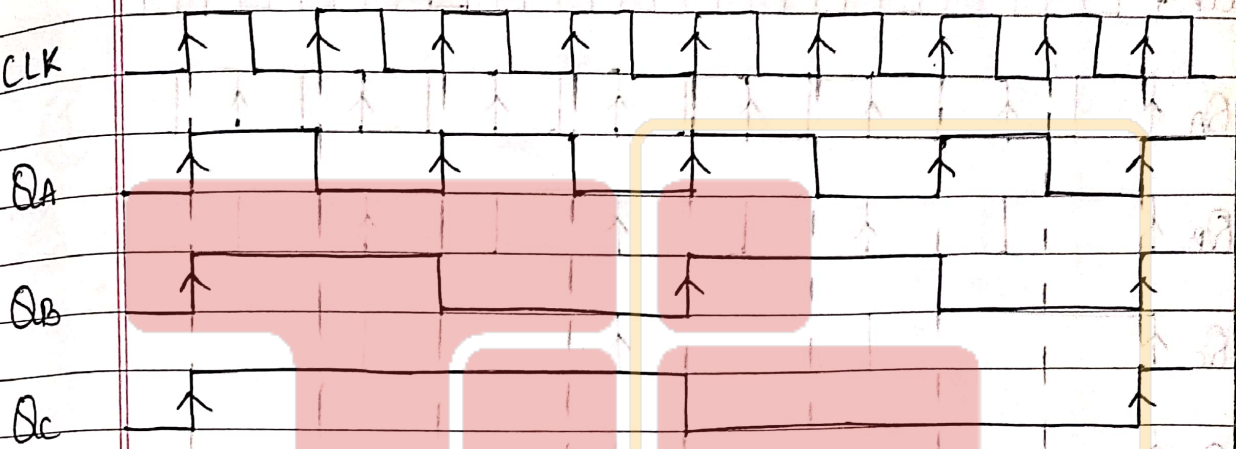




Q_A	Q_B
1	1
1	0
0	1
0	0

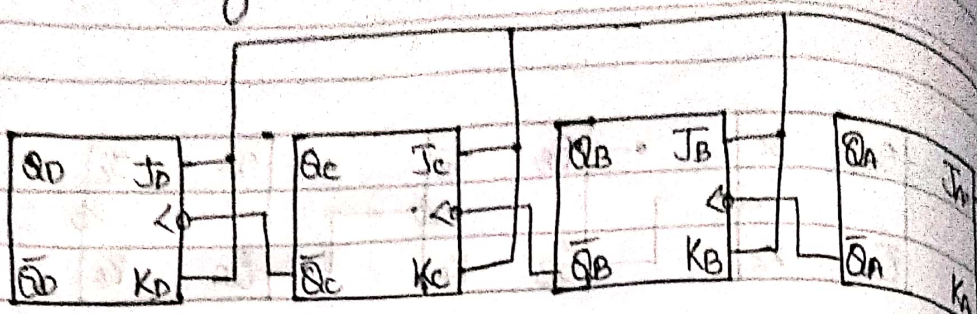
3-bit asynchronous down counter

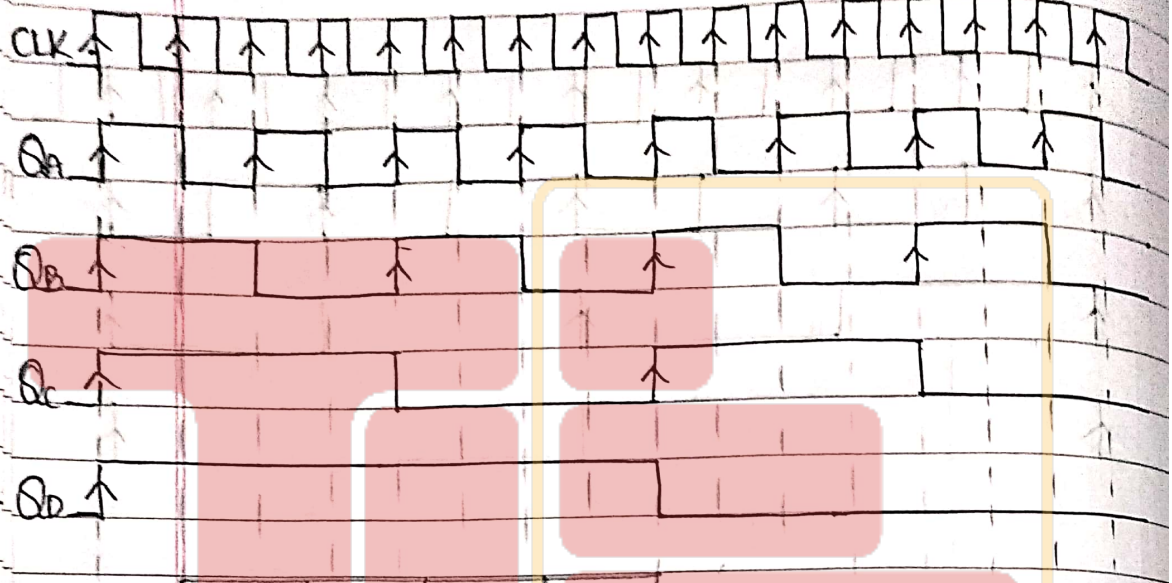




Q_A	Q_B	Q_C
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0

4 - bit asynchronous down counter





Q_A	Q_B	Q_C	Q_D
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0

Synchronous Counter.

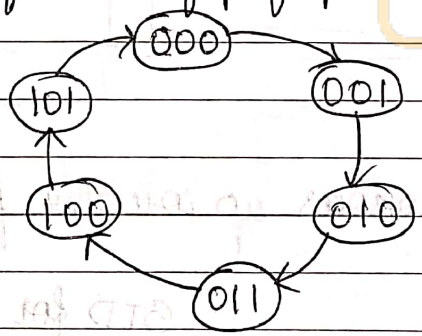
Step1: Identification of flip flop.
Step2: Write ET for given flip flop.
Step3: Write STD for given flip flop. (up, down, up-down)
Step4: Write Truth table for previous state & next state.
Step5: Write Boolean expression using K-map method.
Design a circuit for Synchronous counter.

(1) Design a Synchronous up counter for mod 6. (Using JK)

Sol:
- Using JK flip flop.
- ET for JK flip flop.

Qn	Qn+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- STD for JK flip flop



- TT for PS and NS.

Qc	QB	QA	Qc+1	QB+1	QA+1	Jc	Kc	JB	KB	JA	KA
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1

PS | NS (Using STD) | (Using FT of JK)

Q_C \ Q_BQ_A	00	01	11	10
0	0_0	0_1	1_3	0_2
1	X_4	X_5	X_7	X_6

$J_C = Q_B Q_A$.

Q_C \ Q_BQ_A	00	01	11	10
0	0_0	1_1	X_3	X_2
1	0_4	0_5	X_7	X_6

$J_B = \overline{Q_C} Q_A$.

Q_C \ Q_BQ_A	00	01	11	10
0	X_0	X_1	X_3	X_2
1	0_4	1_5	X_7	X_6

$K_C = Q_A$.

Q_C \ Q_BQ_A	00	01	11	10
0	X_0	X_1	1_3	0_2
1	X_4	X_5	X_7	X_6

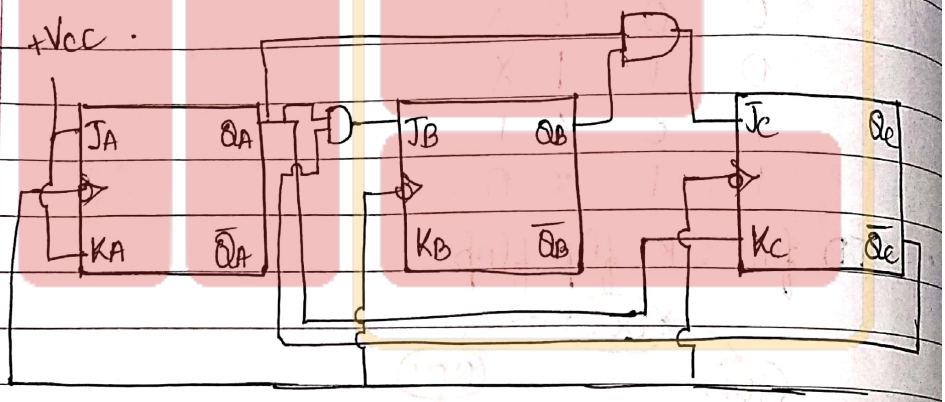
$K_B = Q_A$.

Q_C \ Q_BQ_A	00	01	11	10
0	1_0	X_1	X_3	1_2
1	1_4	X_5	X_7	X_6

$J_A = 1$

Q_C \ Q_BQ_A	00	01	11	10
0	1_0	1_1	1_3	X_2
1	X_4	1_5	X_7	X_6

$K_A = 1$



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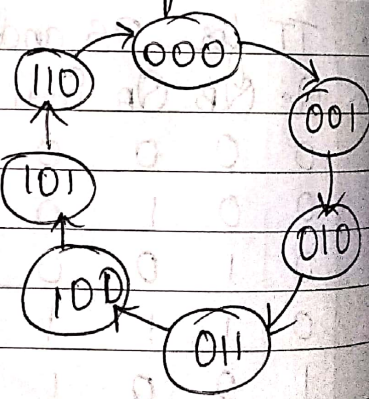
(2) Design a Synchronous up counter for Mod (Using SR or JK).

Soln: • ET for SR.

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

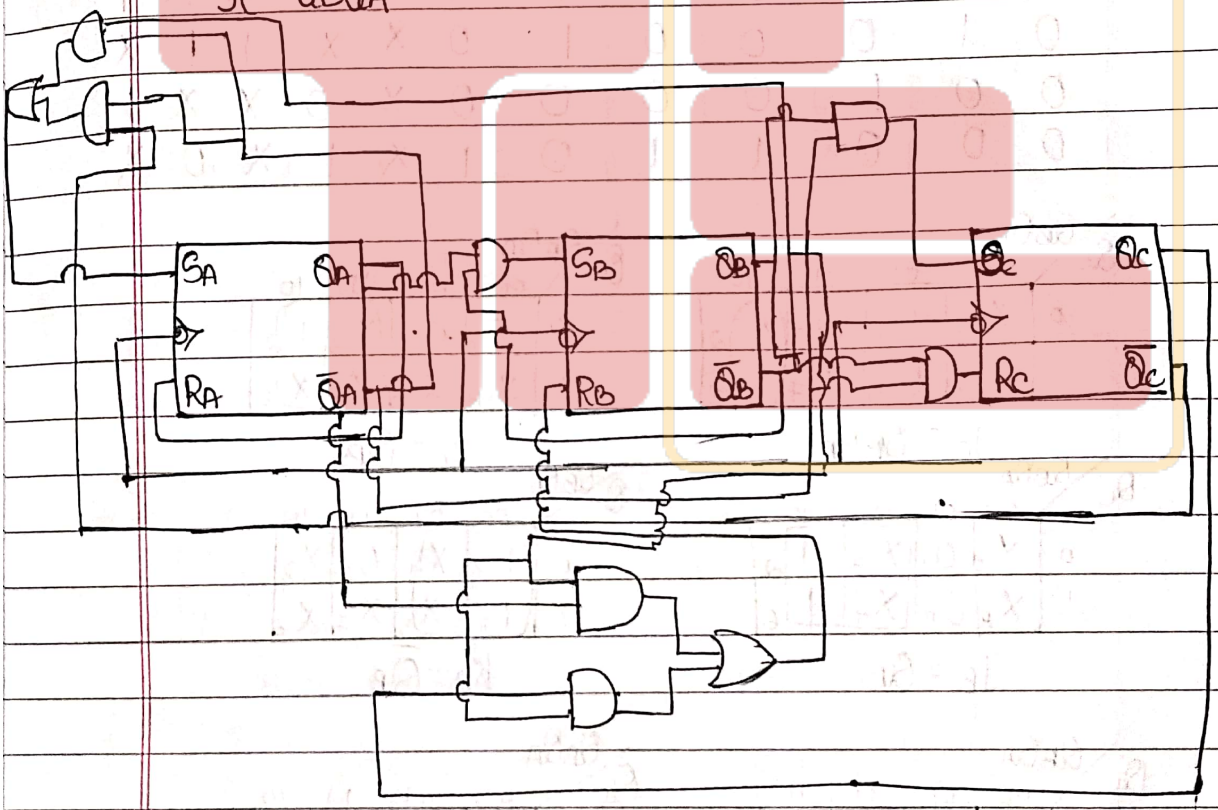
• STD for SR



Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	0	1	0	X	0	X	1	0
0	0	1	0	1	0	0	X	1	0	0	1
0	1	0	0	1	1	0	X	X	0	1	0
0	1	1	1	0	0	1	0	0	1	0	1
1	0	0	1	0	1	X	0	0	X	1	0
1	0	1	1	1	0	X	0	1	0	0	1
1	1	0	0	0	0	0	1	0	1	0	X

Q_C \ Q_BQ_A	00	01	11	10
0	0	0	1	0
1	X	X	X	0

- $S_C = Q_BQ_A$
- $R_C = Q_B\bar{Q}_A$
- $S_B = \bar{Q}_B Q_A$
- $R_B = Q_BQ_A + Q_C\bar{Q}_B$
- $S_A = \bar{Q}_B\bar{Q}_A + \bar{Q}_C\bar{Q}_A$
- $R_A = Q_A$

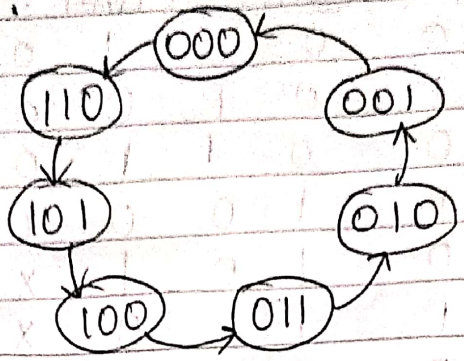


(3) Design a Synchronous down counter for Mod 7. Using JK.

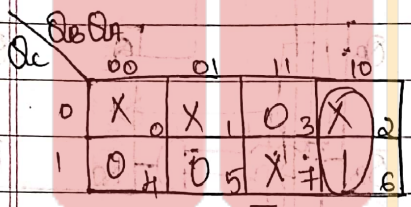
Soln ET for JK

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

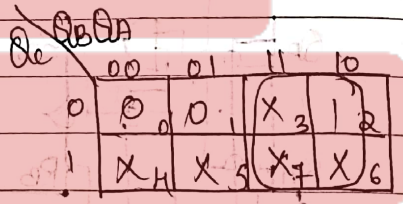
STD for JK:



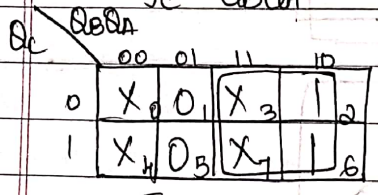
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
1	1	0	1	0	1	X	0	X	1	1	X
1	0	1	1	0	0	X	0	0	X	X	1
1	0	0	0	1	1	X	1	1	X	1	X
0	1	1	0	1	0	0	X	X	0	X	1
0	1	0	0	0	1	0	X	X	1	1	X
0	0	1	0	0	0	0	X	0	X	X	1
0	0	0	1	1	0	1	X	1	X	0	X



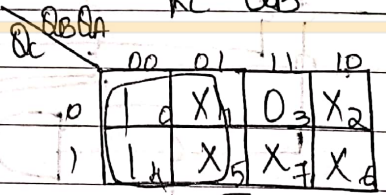
$J_C = Q_B \bar{Q}_A$



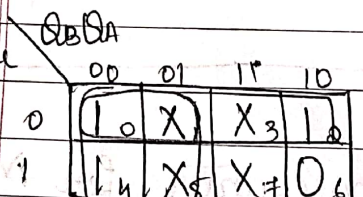
$K_C = Q_{\bar{B}}$



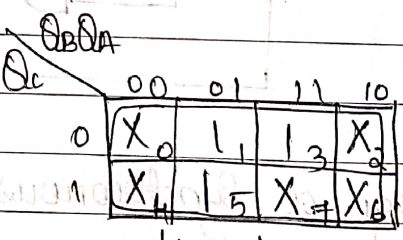
$J_B = Q_B$



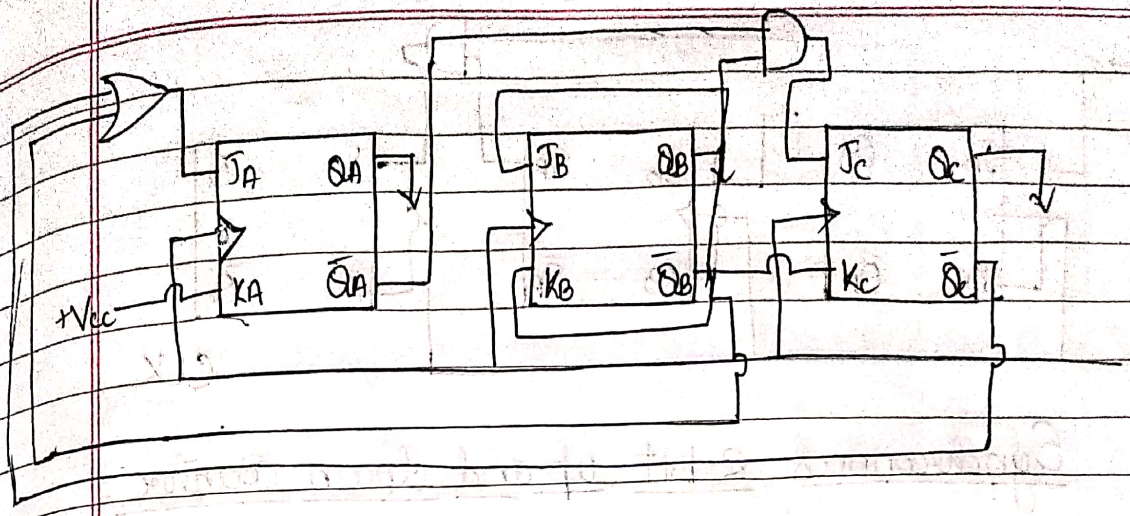
$K_B = \bar{Q}_B$



$J_A = \bar{Q}_B + \bar{Q}_C$



$K_A = 1$



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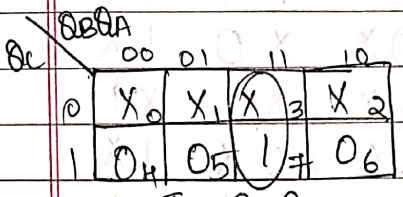
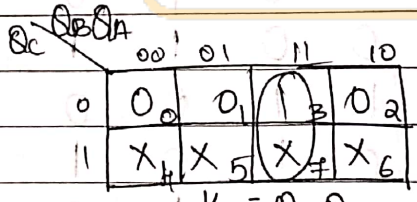
④ Design a Synchronous down Counter for Mod 8 :

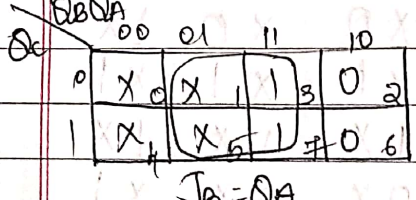
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
1	1	1	1	1	0	X	0	X	0	X	1
1	1	0	1	0	1	X	0	X	1	1	X
1	0	1	1	0	0	X	0	0	X	X	1
1	0	0	0	1	1	X	1	1	X	1	X
0	1	1	0	1	0	0	X	X	0	X	1
0	1	0	0	0	1	0	X	X	1	1	X
0	0	1	0	0	0	0	X	0	X	X	1
0	0	0	1	1	1	1	X	1	X	1	X



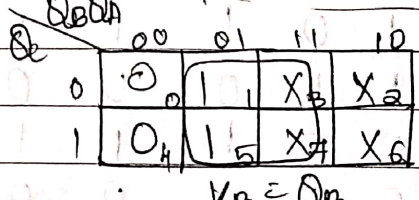
$J_C = Q_B Q_A$



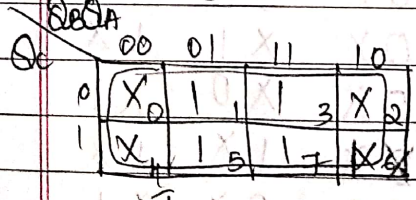
$K_C = Q_B Q_A$



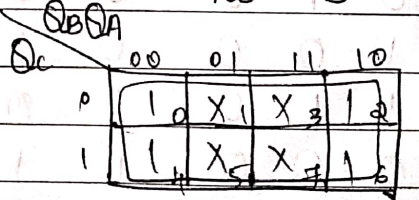
$J_B = Q_A$



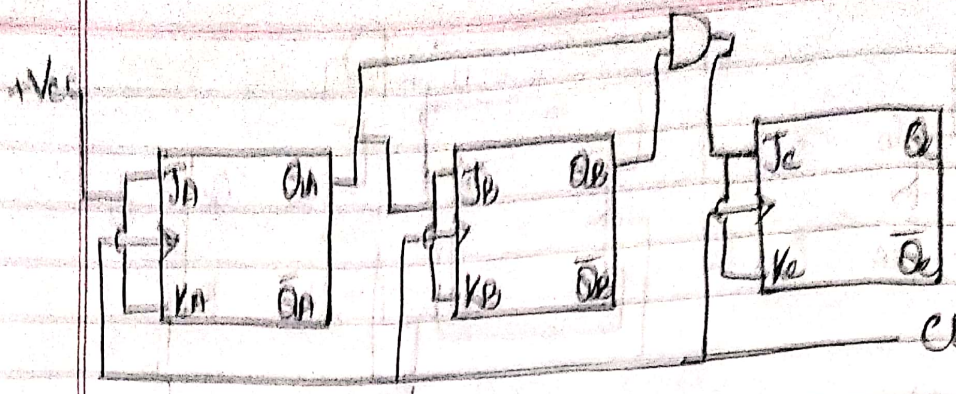
$K_B = Q_B$



$J_A = 1$



$K_A = 1$

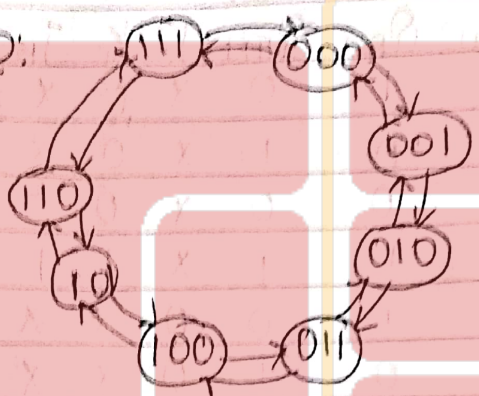


Synchronous 3-bit up and down counter.

ET for JK

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

STD:



M	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	$J_C K_C$	$J_B K_B$	$J_A K_A$
0	0	0	0	0	0	1	0 X	0 X	1 X
0	0	0	1	0	1	0	0 X	1 X	X 1
0	0	1	0	0	1	1	0 X	X 0	1 X
0	0	1	1	1	0	0	1 X	X 1	X 1
0	1	0	0	1	0	1	X 0	0 X	1 X
0	1	0	1	1	1	0	X 0	1 X	X 1
0	1	1	0	1	1	1	X 0	X 0	1 X
0	1	1	1	0	0	0	X 1	X 1	X 1
1	0	0	0	1	1	1	1 X	1 X	1 X
1	0	0	1	0	0	0	0 X	0 X	X 1
1	0	1	0	0	0	1	0 X	X 1	1 X
1	0	1	1	0	1	0	0 X	X 0	X 1
1	1	0	0	0	1	1	X 1	1 X	1 X
1	1	0	1	1	0	0	X 0	0 X	X 1
1	1	1	0	1	0	1	X 0	X 1	1 X
1	1	1	1	1	1	0	X 0	X 0	X 1

$Q_B Q_A$

Q_C

0 0	0 1	(1 1)	0 3
X 4	X 5	(X 7)	X 6
(X 12	X 13	X 15	X 14
(1 8	0 9	0 11	0 10

$J_C = \bar{M} Q_B Q_A + M \bar{Q}_B \bar{Q}_A$

$Q_B Q_A$

Q_C

X	X	(X	X
0	0	(1	0
(1	0	0	0
(X	X	X	X

$K_C = \bar{M} Q_B \bar{Q}_A + M \bar{Q}_B Q_A$

$Q_B Q_A$

Q_C

0	(1	X	X
0	(1	X	X
(1	0	X	X
(1	0	X	X

$J_B = \bar{M} Q_A + M \bar{Q}_A$

$Q_B Q_A$

Q_C

X	(X	1	0
X	X	1	0
X	X	0	(1
X	X	0	1

$K_B = \bar{M} Q_A + \bar{Q}_A M$

$Q_B Q_A$

Q_C

(1	X	X	1
1	X	X	1
1	X	X	1
1	X	X	1

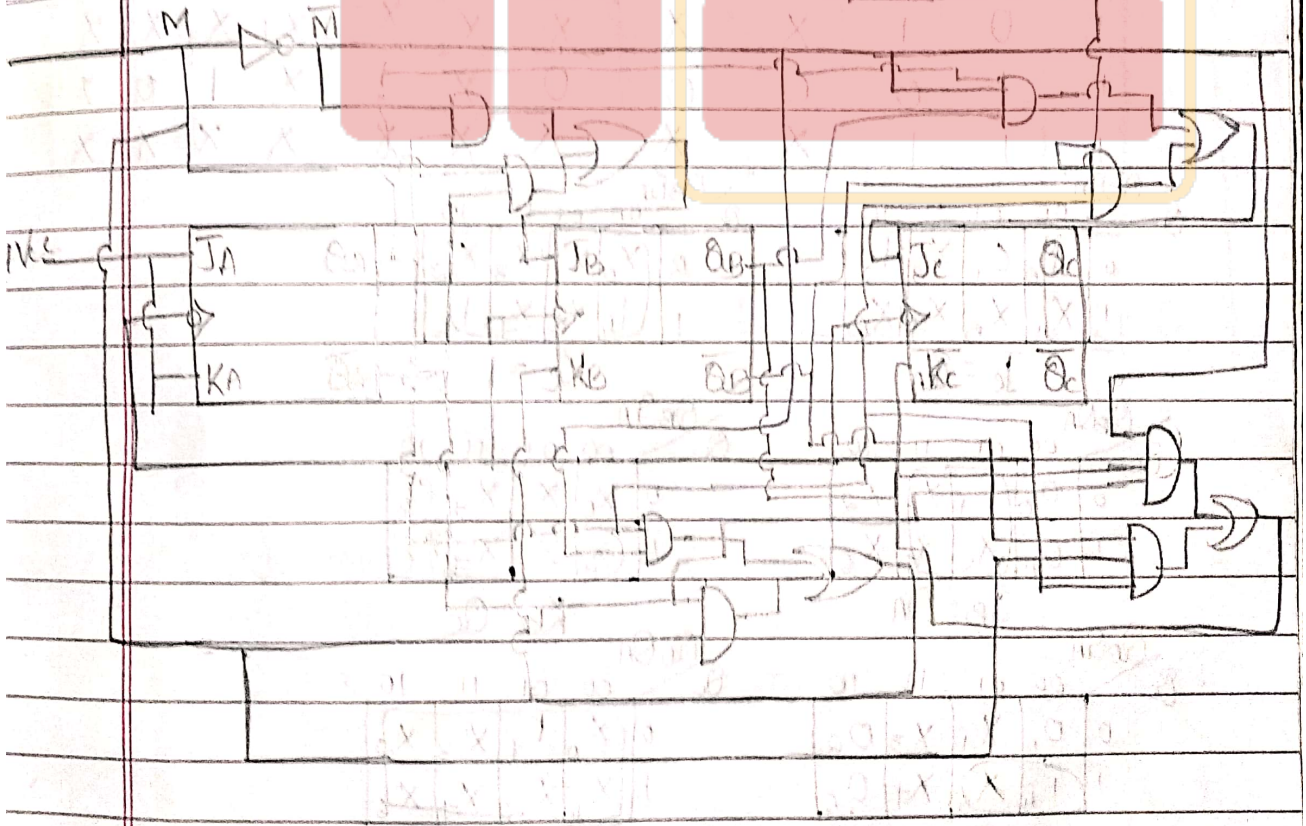
$J_A = 1$

$Q_B Q_A$

Q_C

(1	X	1	X
1	X	1	X
1	X	1	X
1	X	1	X

$K_A = 1$



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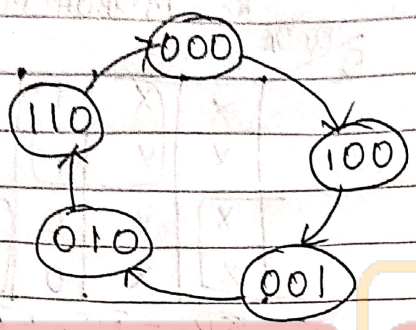
PS Counter (Re-Settable)

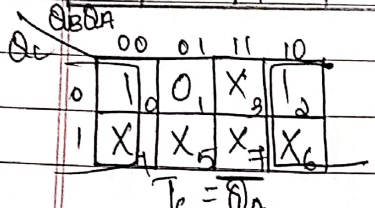
① Design a Synchronous Counter for the Sequ

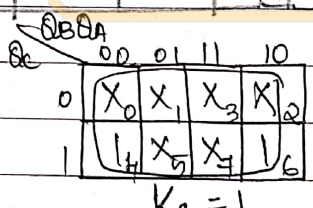
0 → 4 → 1 → 2 → 6 → 10 → 4.

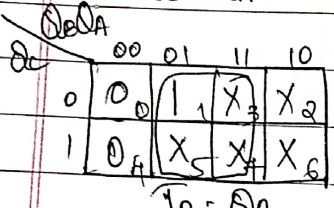


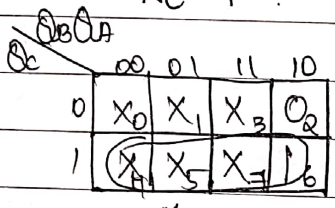
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

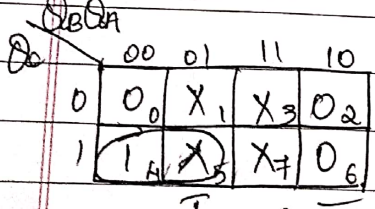
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	1	0	0	1	X	0	X	0	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	1	0	1	X	X	0	0	X
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	0	0	1	X	1	0	X	1	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	X	X	X	X	X	X	X	X	X

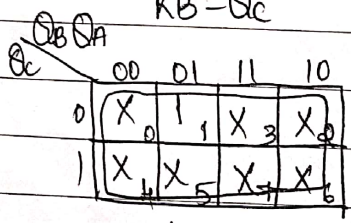


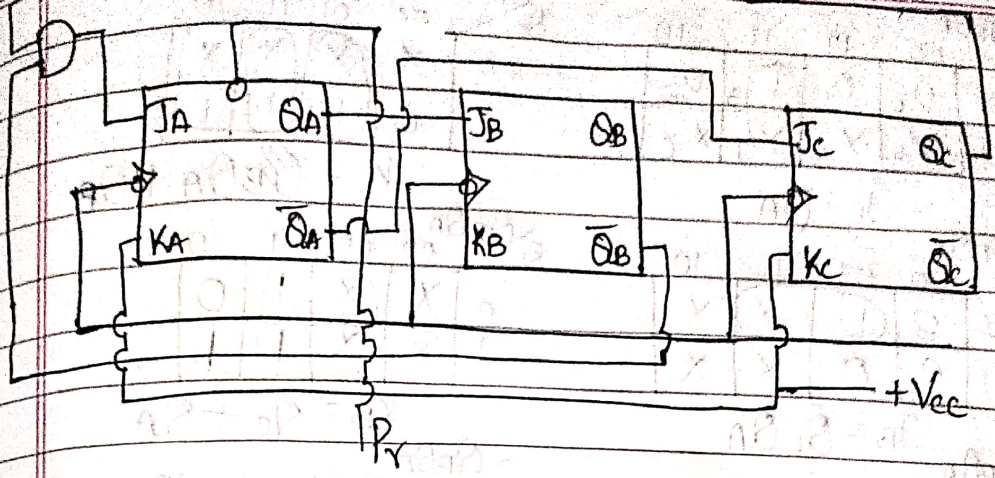












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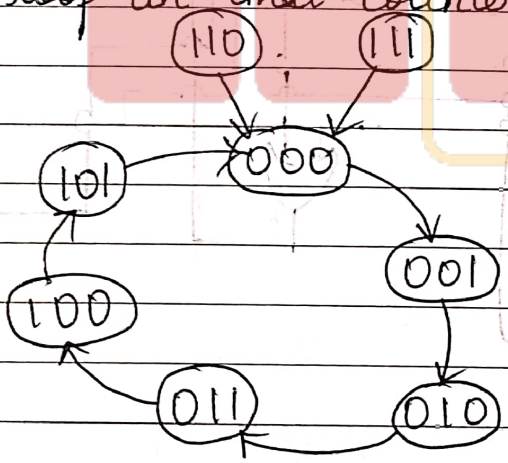
Synthesize Design (Self correcting Controlled Counter)
/ lock out condition.

(1) Consider a design of Mod6 counter, i.e it has to be count from 000 to 101. But by chance if 110 and 111 condition are counted by counter. It won't have any values and will log off the counter, i.e go for any of the loop in that counter.

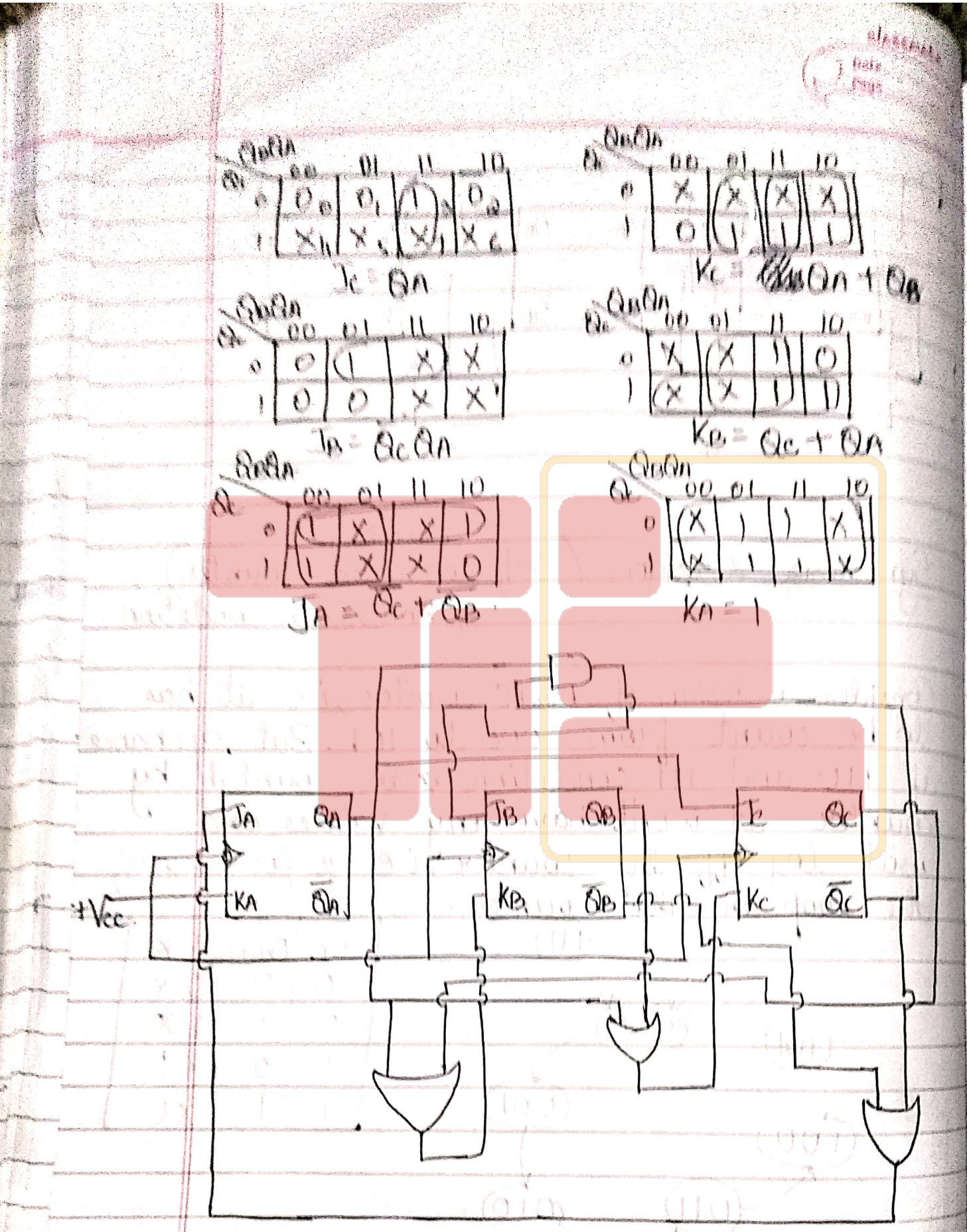
Mod 5 also

Soln:



Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1


$J_C = Q_A$
$K_C = \overline{Q_A} Q_B + Q_B$
$J_B = Q_C Q_A$
$K_B = Q_C + Q_A$
$J_A = Q_C + \overline{Q_B}$
$K_A = 1$
J_A Q_A K_A $\overline{Q_A}$
J_B Q_B K_B $\overline{Q_B}$
J_C Q_C K_C $\overline{Q_C}$
$+V_{cc}$