

3.5.1 Resistance Firing Circuit

The circuit in Fig. 3.11 shows a simple method for varying the trigger angle and therefore, the power in the load. Instead of using a gate pulse to trigger the SCR, the gate current is supplied by an a.c. source of voltage e_s through R_{\min} , R_v , and the series diode D . The circuit operates as follows:

- (i) As e_s goes positive, the SCR becomes forward-biased from anode to cathode; however, it will not conduct ($e_L = 0$) until its gate current exceeds $I_{g(\min)}$.
- (ii) The positive e_s also forward biases the diode and the SCRs gate–cathode junction; this causes flow of a gate current i_g .
- (iii) The gate current will increase as e_s increases towards its peak value. When i_g reaches a value equal to $I_{g(\min)}$, the SCR turns “on” and e_L will approximately equal e_s (refer to point P on the waveform in Fig. 3.11).
- (iv) The SCR remains “on” and $e_L \approx e_s$ until e_s decreases to the point where the load current is below the SCR holding-current. This usually occurs very close to the point until $e_s = 0$ and begins to go negative.
- (v) The SCR now turns “off” and remains “off” while e_s goes negative since its anode–cathode is reverse biased, and since the SCR is now an open switch, the load voltage is zero during this period.
- (vi) The purpose of the diode in the gate-circuit is to prevent the gate–cathode reverse bias from exceeding peak reverse gate voltage during the negative half-cycle of e_s . The diode is chosen to have peak reverse-voltage rating greater than the input voltage E_{\max} .
- (vii) The same sequence is repeated when e_s again goes positive.

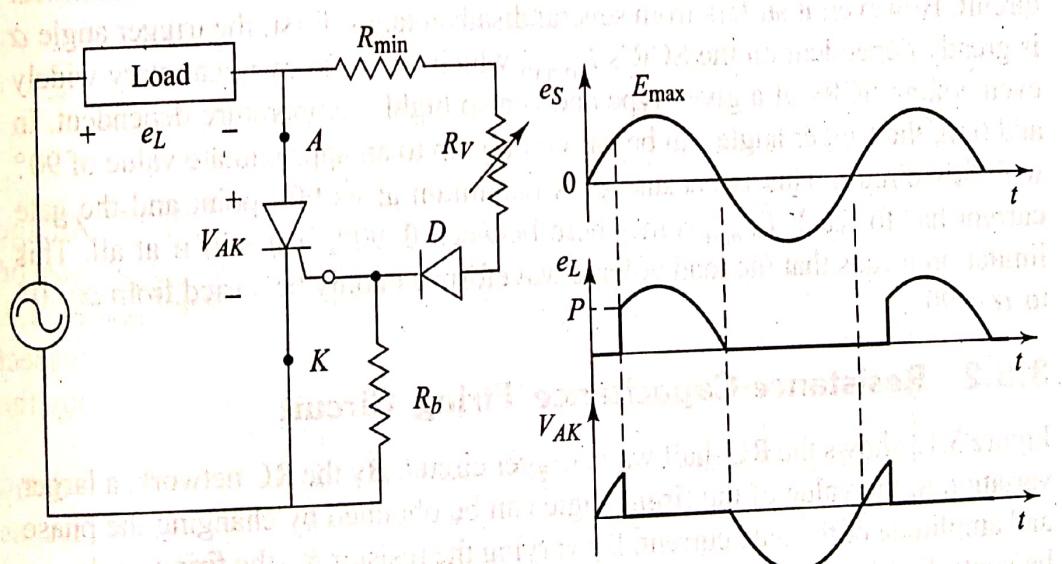


Fig. 3.11 R-firing circuit and associated voltage waveforms

The load-voltage waveform in Fig. 3.11 can be controlled by varying R_v which varies the resistance in the gate circuit. If R_v is increased, the gate current will

reach its trigger value $I_{g(\min)}$ at a greater value of e_s making the SCR to trigger at a latter point in the e_s positive half-cycle. Thus, the trigger angle α will increase. The opposite will occur if R_v is decreased. Of course, if R_v is made large enough the SCR gate current will never reach $I_{g(\min)}$ and the SCR will remain "off". The minimum trigger angle is obtained with R_v equal to zero.

As shown in Fig. 3.11, the limiting resistor $R_{(min)}$ is placed between anode and gate so that the peak gate current of the thyristor I_{gm} is not exceeded. In the worst case, that is when the supply voltage has reached its peak, E_{max} ,

$$R_{\min} \geq \frac{E_{\max}}{I_{gm}} \quad (3.1)$$

The stabilising resistor R_b should have such a value that the maximum voltage drop across it does not exceed maximum possible gate voltage $V_{g(\max)}$. From the voltage distribution,

$$R_b \leq \frac{(R_v + R_{\min}) \cdot V_{g(\max)}}{(E_{\max} - V_{g(\max)})} \quad (3.2)$$

The thyristor will trigger when the instantaneous anode voltage, e_s , is

$$e_s = I_{g(\min)} (R_v + R_{\min}) + V_d + V_{g(\min)} \quad (3.3)$$

where $I_{g(\min)}$ = minimum gate current to trigger the thyristor

V_d = voltage drop across the diode

$V_{g(\min)}$ = gate-voltage to trigger, corresponding to $I_{g(\min)}$.

The resistance trigger shown in Fig. 3.11 is the simplest and most economical circuit. However, it suffers from several disadvantages. First, the trigger angle α is greatly dependent on the SCR's $I_{g(\min)}$, which, as we known, can vary widely even among SCRs of a given type and is also highly temperature dependent. In addition, the trigger angle can be varied only up to an approximate value of 90° with this circuit. This is because e_s is maximum at its 90° point and the gate current has to reach $I_{g(\min)}$ somewhere between $0-90^\circ$, if it will if at all. This limitation means that the load voltage waveform can only be varied from $\alpha = 0^\circ$ to $\alpha = 90^\circ$.

3.5.2 Resistance-Capacitance Firing Circuit

Figure 3.12 shows the RC-half wave trigger circuit. By the RC network, a larger variation in the value of the firing angle can be obtained by changing the phase and amplitude of the gate current. By varying the resistor R_v , the firing angle can be controlled from 0 to 180° .

In the negative half-cycle, capacitor C charges through diode D_2 with lower constant at $-E_{\max}$ until supply voltage attains zero value. Now, as the SCR anode voltage passes through zero and becomes positive, capacitor C begins to charge

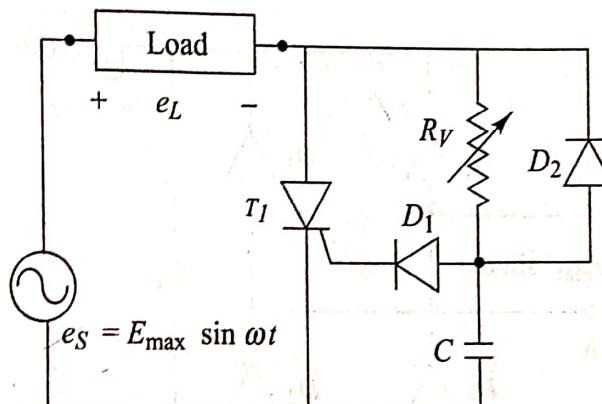
through R_v from the initial voltage $-E_{\max}$. When the capacitor charges to positive voltage equal to gate trigger voltage V_{gt} ($= V_{g(\min)} + V_{D1}$), SCR is triggered and after this, the capacitor holds to a small positive voltage, as shown in Fig. 3.12. During negative half-cycle, the diode D_1 prevents the breakdown of the gate to cathode junction. In the range of power-frequencies, the RC for zero output voltage is given by

$$R_v C \geq \frac{1.3T}{2} = \frac{4}{w} \quad (3.4)$$

where $T = 1/f$ = period of ac line frequency in seconds.

As discussed above, the thyristor will turn ON when the capacitor voltage e_c equals $(V_{g(\min)} + V_{D1})$, provided the gate current $I_{g(\min)}$ is available. Therefore, the maximum value of R_v is given by

$$e_s \geq I_{g(\min)} R_v + e_c$$



(a)

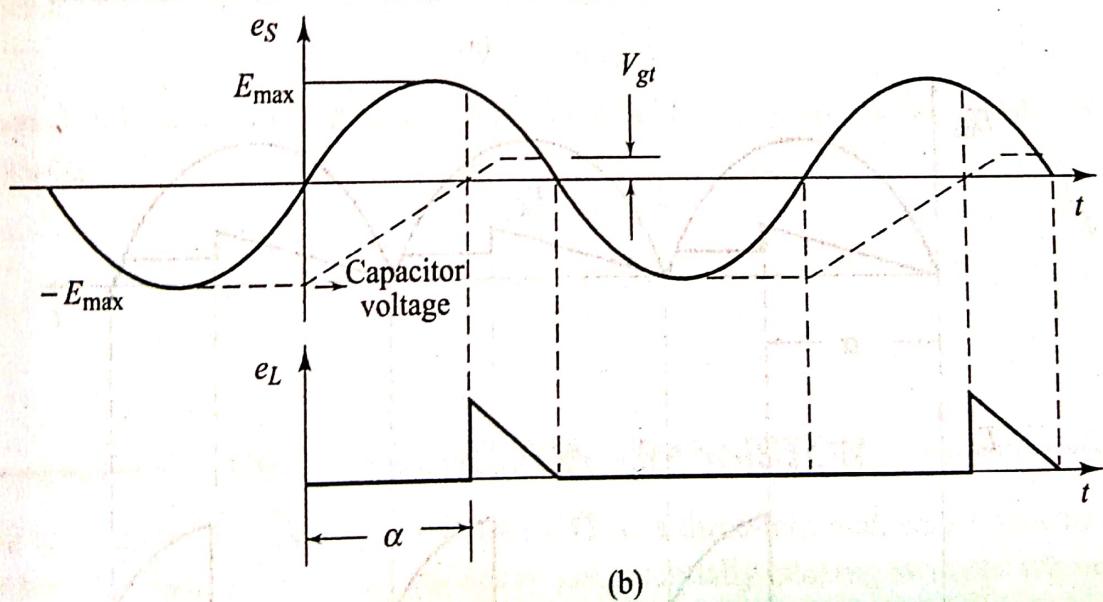


Fig. 3.12 (a) RC firing circuit, (b) voltage-waveform

$$= I_{g(\min)} R_v + V_{g(\min)} + V_{D1} \quad (3.5)$$

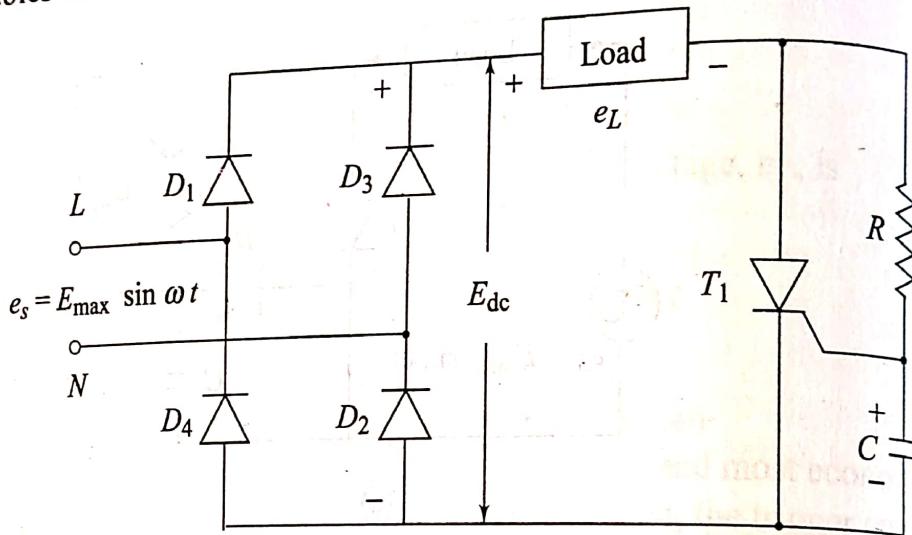
$$R_v \leq \frac{e_s - V_{g(\min)} - V_{D1}}{I_{g(\min)}} \quad (3.6)$$

or

where e_s is the instantaneous supply voltage at which the thyristor will turn ON. From Eqs 3.4 and 3.6, the suitable values of R_v and C can be obtained.

3.5.3 Resistor Capacitor-Full-Wave Trigger Circuit

Power can be delivered to the load in Fig. 3.12 only during the positive half-cycle of e_s because the SCR conducts only when it is forward biased. This limitation can be overcome in several ways, one of which is shown in Fig. 3.13. Here, the ac line voltage is converted to pulsating dc by the full-wave diode bridge. This allows the SCR to be triggered "on" for both half-cycles of the line voltage which doubles the available power to the load.



(a)

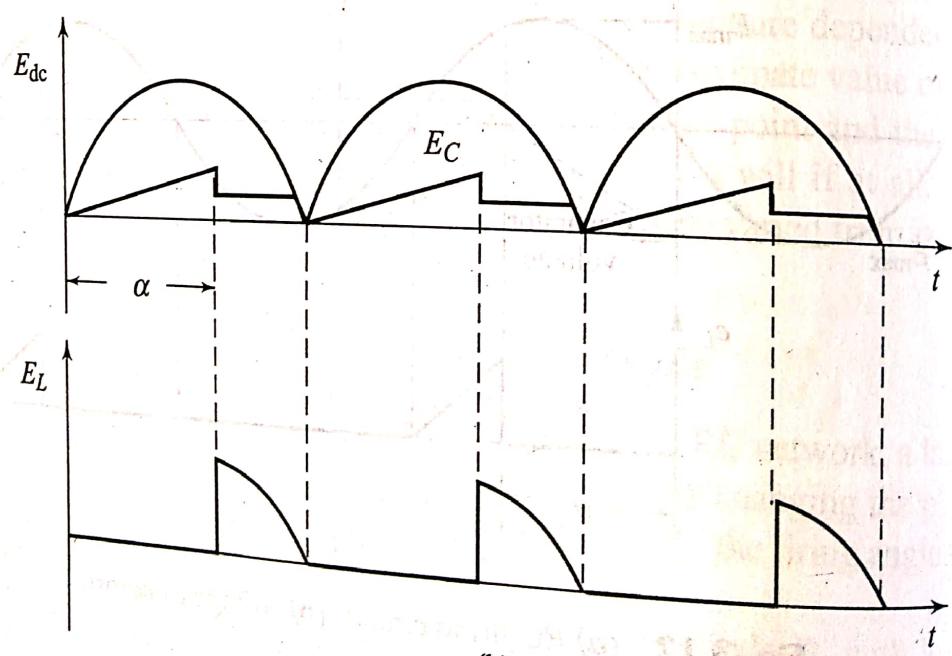


Fig. 3.13 (a) RCT ...

(b)

In this circuit, the initial voltage from which capacitor C charges is almost zero. Capacitor C is set to this low positive voltage (upper plate positive) by the clamping action of SCR gate. When the capacitor charges to a voltage equal to $V_{g(t)}$, SCR triggers and rectified voltage E_{dc} appears across load as e_L . The value of R_{vC} is obtained from the following relation:

$$R_v C \geq 50 \frac{T}{2} = \frac{157}{w} \quad (3.7)$$

As per Eq. 3.6, the value of R_v is given by

$$R_v \leq \frac{e_s - V_{gt}}{I_{g(\min)}} \quad (3.8)$$

SOLVED EXAMPLES

Example 3.1 The circuit in Fig. 3.11 uses an SCR with $I_{g(\min)} = 0.1$ mA and $V_{g(\min)} = 0.5$ V. The diode is silicon and the peak amplitude of the input is 24 Volts. Determine the trigger angle α for $R_V = 100$ k Ω and $R_{\min} = 10$ k Ω .

Solution: The first step is to determine the instantaneous value of e_s at which triggering will occur. At the SCR trigger point, $V_{g(\min)} = 0.5$ V and $I_{g(\min)} = 0.1$ mA.

Using KVL around the gate circuit, we have

$$e_s = I_g (R_V + R_{\min}) + V_D + V_g$$

At the trigger point,

$$e_{s(\text{trigger})} = 0.1 \text{ mA} (110 \text{ k}\Omega) + 0.7 \text{ V} + 0.5 \text{ V} = 12.2 \text{ V}$$

Since e_s is a sine-wave, it obeys the expression

$$e_s = E_{\max} \cdot \sin \omega t = E_{\max} \cdot \sin(2\pi ft)$$

where $2\pi ft$ is the phase angle at any instant of time. For our purposes, this angle is α . Thus, $E_{\max} = 24$ V,

$$e_s = 24 \sin \alpha \quad \therefore 12.2 = 24 \sin \alpha$$

$$\sin \alpha = \frac{12.2}{24} \quad \therefore \alpha = 30.6^\circ$$

3.6 UNIJUNCTION TRANSISTOR

The unijunction transistor, abbreviated UJT, is a three-terminal, single-junction device. The basic UJT and its variations are essentially latching switches whose operation is similar to the four-layer diode, the most significant difference being that the UJT's switching voltage can be easily varied by the circuit designer. Like the four-layer diode, the UJT is always operated as a switch and finds most frequent applications in oscillators, timing circuits and SCR/TRIAC trigger circuits.

3.6.1 Basic Operation

A typical UJT structure, pictured in Fig. 3.14, consists of a lightly doped, *N*-type silicon bar provided with ohmic contacts at each end. The two end connections are called base-1, designated B_1 and base-2, B_2 . A small, heavily doped *P*-region is alloyed into one side of the bar closer to B_2 . This *P*-region is the UJT emitter, E , and forms a *P-N* junction with the bar.

An interbase resistance, R_{BB} , exists between B_1 and B_2 . It is typically between 4 k Ω and 10 k Ω , and can easily be measured with an ohmeter with the emitter open. R_{BB} is essentially the resistance of the *N*-type bar. This interbase resistance can be broken up into two resistances, the resistance from B_1 to emitter, called R_{B_1} , and resistance from B_2 to emitter, called R_{B_2} . Since the emitter is closer to B_2 , the value of R_{B_1} is greater than R_{B_2} (typically 4.2 k Ω versus 2.8 k Ω).

The operation of the UJT can better be explained with the aid of an equivalent circuit. The UJT's circuit symbol and its equivalent circuit are shown in Fig. 3.15. The diode represents the *P-N* junction between the emitter and the base-bar (point x). The arrow through R_{B_1} indicates that it is variable since during normal operation it may typically range from 4 k Ω down to 10 Ω .

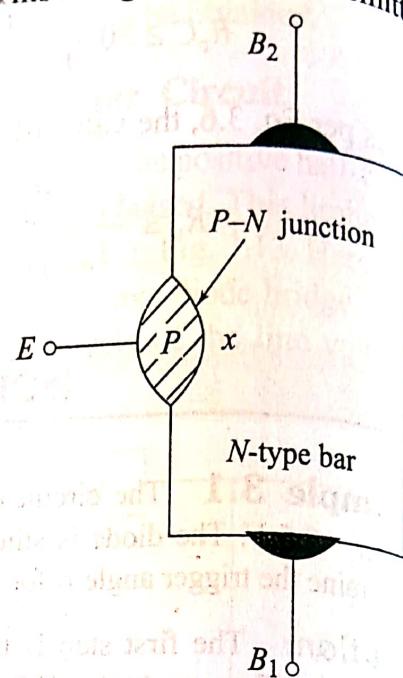


Fig. 3.14 Basic UJT structure

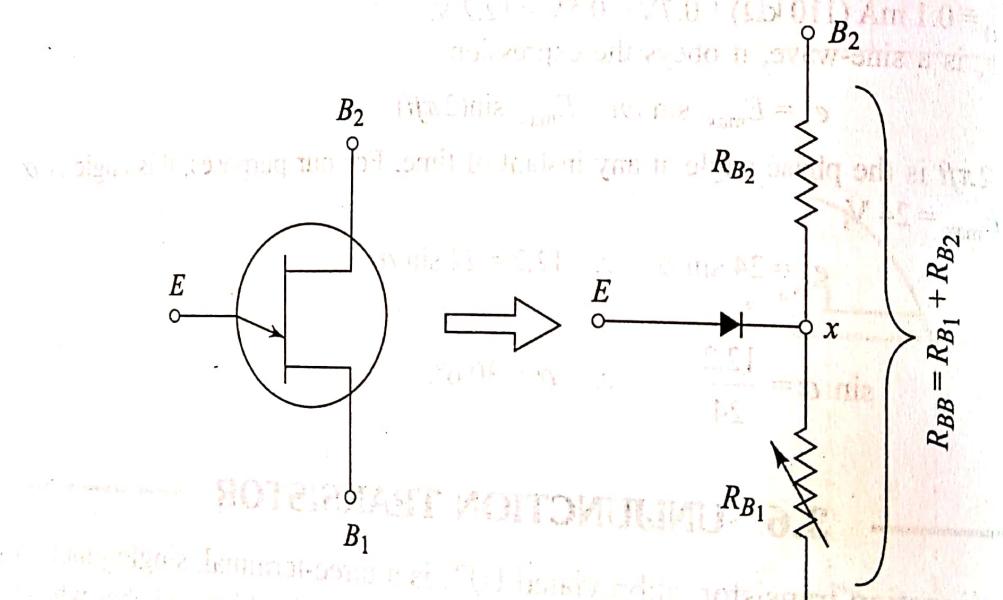


Fig. 3.15 UJT symbol and equivalent circuit

The essence of UJT operation can be stated as follows:

- When the emitter diode is reverse biased, only a very small emitter current flows. Under this condition, R_{B_1} is at its normal high-value (typically 4 k Ω). This is the UJT's "off" state.

- (b) When the emitter diode becomes forward biased, R_{B1} drops to a very low value (reason to be explained later) so that the total resistance between E and B_1 becomes very low, allowing emitter current to flow readily. This is the "on" state.

Circuit-operation The UJT is normally operated with both B_2 and E biased positive relative to B_1 as shown in Fig. 3.16. B_1 is always the UJT reference terminal and all voltages are measured relative to B_1 . The V_{BB} source is generally fixed and provides a constant voltage from B_2 to B_1 . The V_{EE} source is generally a variable voltage and is considered the input to the circuit. Very often, V_{EE} is not a source but a voltage across a capacitor.

We will analyze the UJT circuit operation with the aid of the UJT equivalent circuit, shown inside the dotted lines in Fig. 3.17(a). We will also utilize the UJT emitter-base-1 V_E - I_E curve shown in Fig. 3.17(b). The curve represents the variation of emitter current I_E , with emitter-base-1 voltage, V_E , at a constant B_2 - B_1 voltage. The important points on the curve are labelled, and typical values are given in parentheses.

The "Off" state If we neglect the diode for a moment, we can see in Fig. 3.17(a) that R_{B_1} and R_{B_2} form a voltage divider that produces a voltage V_x from point x relative to ground.

$$V_x = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} \times V_{BB} = \underbrace{\frac{R_{B_1}}{R_{BB}}}_{\eta} \times V_{BB}$$

or simply,

$$V_x = \eta V_{BB} \quad (3.9)$$

where η (the greek letter "eta") is the internal UJT voltage divider ratio $\frac{R_{B_1}}{R_{BB}}$ and is called the *intrinsic stand off ratio*.

Values of η typically range from 0.5 to 0.8 but are relatively constant for a given UJT.

The voltage at point x is the voltage on the N -side of the $P-N$ junction. The V_{EE} source is applied to the emitter which is the P -side. Thus, the emitter diode will be reverse-biased as long as V_{EE} is less than V_x . This is the "off" state and is shown on the V_E - I_E curve as being a very low current region. In the "off" state, then, we can say that the UJT has a very high resistance between E and B_1 , and I_E is usually a negligible reverse leakage current. With no I_E , the drop across R_E is zero and the emitter voltage, V_E , equals the source-voltage.

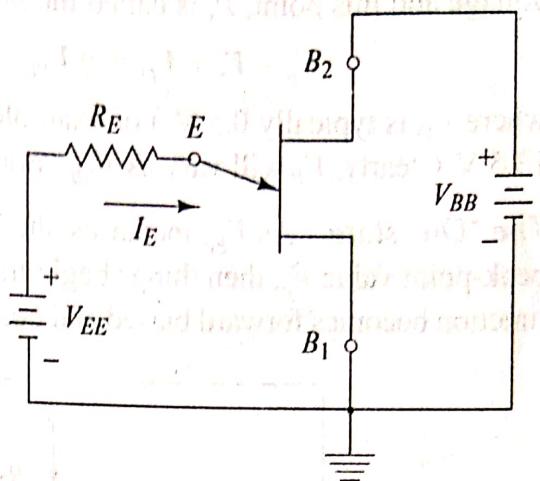


Fig. 3.16 Normal UJT biasing

The UJT "off" state, as shown on the $V_E - I_E$ curve, actually extends to the point where the emitter voltage exceeds V_x by the diode threshold voltage, V_D , which is needed to produce forward current through the diode. The emitter voltage and this point, P , is called the *peak-point voltage*, V_p , and is given by

$$V_p = V_x + V_D = \eta V_{BB} + V_D \quad (3.10)$$

where V_D is typically 0.5 V. For example, if $\eta = 0.65$ and $V_{BB} = 20V$, then $V_p = 13.5$ V. Clearly, V_p will vary as V_{BB} varies.

The "On" state As V_{EE} increases, the UJT stays "off" until V_E approaches the peak-point value V_p , then things begin to happen. As V_E approaches V_p , the $P-N$ junction becomes forward biased and begins to conduct in the opposite direction.

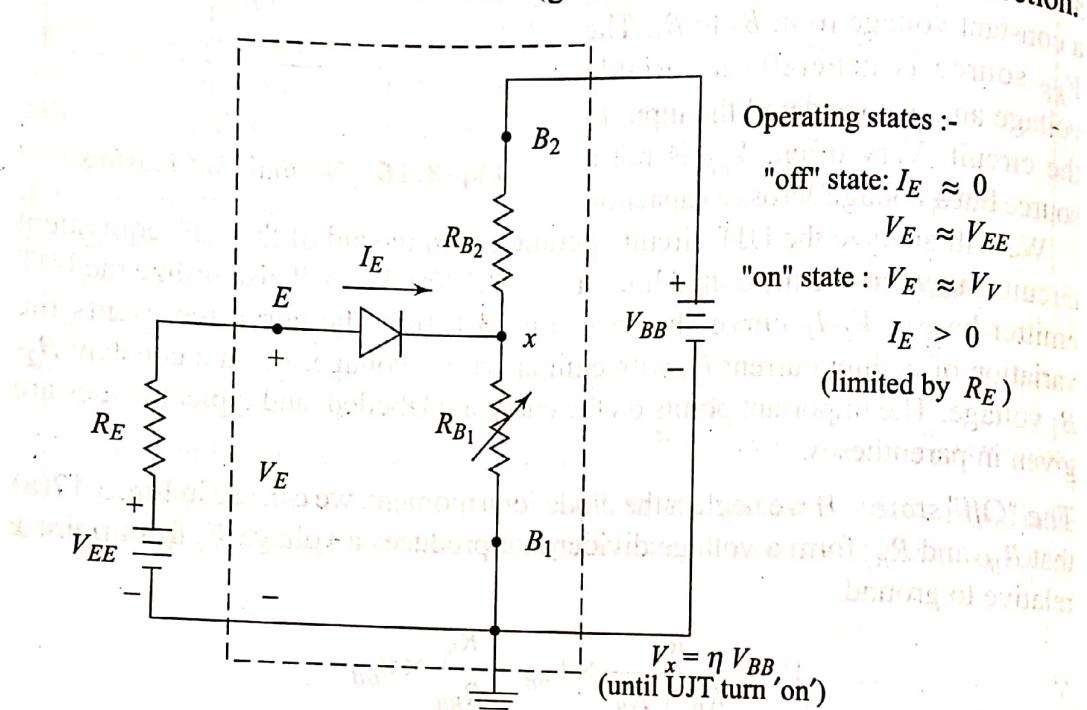


Fig. 3.17 (a) Equivalent-circuit for UJT analysis

Note on the $V_E - I_E$ curve that I_E becomes positive near the peak point P . When V_E exactly equals V_p , the emitter current equals I_p , the *peak-point current*. At this point, holes from the heavily doped emitter are injected into the N -type bar, specially into the B_1 region. The bar, which is lightly doped, offers very little chance for these holes to recombine. As such, the lower half of the bar becomes replete with additional current carriers (holes) and its resistance R_{B_1} is drastically reduced. The decrease in R_{B_1} causes V_x to drop. This drop in turn causes the diode to become more forward biased, and I_E increases even further. The larger I_E injects more holes into B_1 , further reducing R_{B_1} , and so on. When this *regenerative* or *snowballing* process ends, R_{B_1} has dropped to a very small value ($2-25 \Omega$) and I_E can become very large, limited mainly by external resistance R_E .

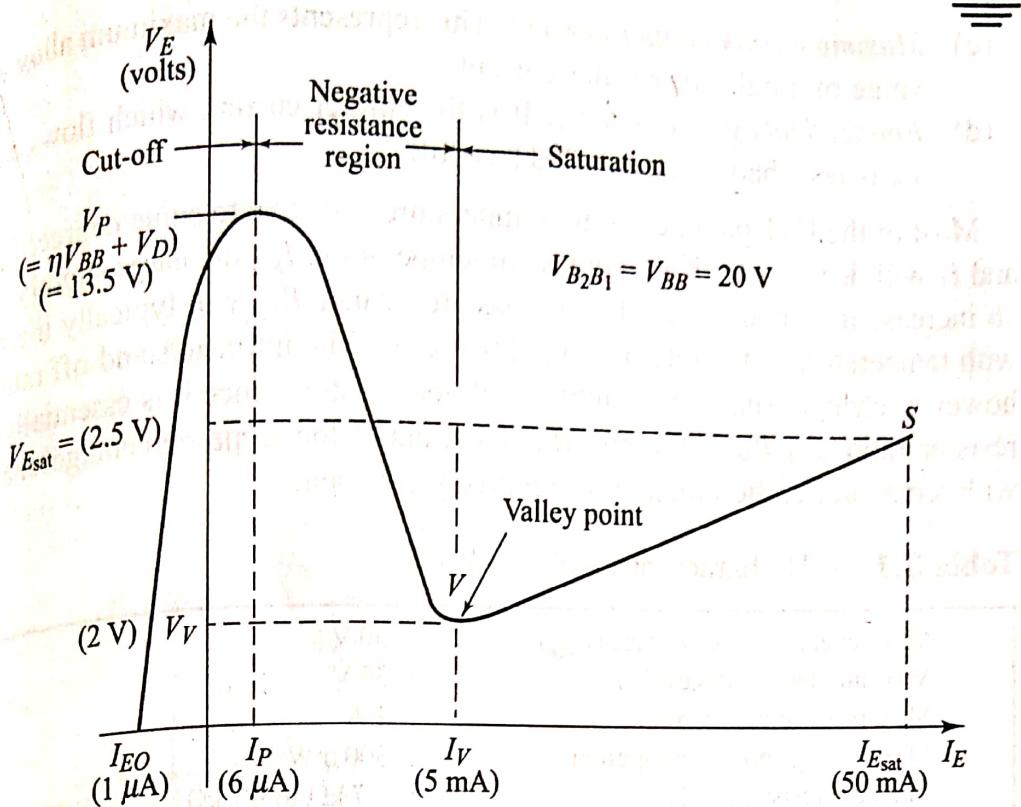


Fig. 3.17 (b) Typical UJT V-I characteristic curve

The UJT operation has switched to the low-voltage, high-current region of its $V_E - I_E$ curve. The slope of this "on" region is very steep, indicating a low resistance. In this region, the emitter voltage V_E , will be relatively small, typically 2 V, and remains fairly constant as I_E is increased up to its maximum rated value, $I_{E(\text{sat})}$. Thus, once the UJT is "on," increasing V_{EE} will serve to increase I_E while V_E remains around 2V.

Turning "Off" the UJT Once it is "on," the UJT's emitter current depends mainly on V_{EE} and R_E . As V_{EE} decreases, I_E will decrease along the "on" portion of the $V_E - I_E$ curve. When I_E decreases to point V , the valley point, the emitter current is equal to I_V , the *valley current*, which is essentially the holding current needed to keep the UJT "on". When I_E is decreased below I_V , the UJT turns "off" and its operation rapidly switches back to the "off" region of its $V_E - I_E$ curve, where $I_E \approx 0$ and $V_E = V_{EE}$. The valley current is the counterpart of the holding current in PNPN devices, and generally ranges between 1 and 10 mA.

3.6.2 UJT Parameters and Ratings

A set of parameter and ratings for a typical UJT (2N2646) are listed in Table 3.1. Some of the entries were defined earlier. Those which require explanation are:

- (a) *Maximum reverse emitter voltage V_{B2E}* : This is the maximum reverse bias which the emitter-base-2 junction can tolerate before breakdown occurs.
- (b) *Maximum interbase voltage*: This limit is caused by the maximum power that the N-type base bar can safely dissipate.

- (c) *Maximum peak emitter current.* This represents the maximum allowable value of a pulse of emitter current.
- (d) *Emitter leakage current I_{E0} .* It is the emitter current which flows when V_E is less than V_P and the UJT is "off."

Most of the UJT parameters are temperature-sensitive to some degree. V_{B2E} , I_P , and I_P will decrease with an increase in temperature. I_{E0} increases slightly with an increase in temperature. The interbase resistance R_{BB} will typically increase with temperature at the rate of around $0.8\%/\text{ }^{\circ}\text{C}$. The intrinsic stand-off ratio η , however, changes only very slightly with temperature since it is essentially the resistor ratio (R_{B1}/R_{BB}). R_{B1} and R_{BB} have about the same percentage change with temperature; therefore, stays relatively constant.

Table 3.1 UJT characteristics at $T_j = 25\text{ }^{\circ}\text{C}$

Max. reverse-emitter voltage (V_{B2E})	: 30 V
Max. interbase voltage (V_{BB})	: 35 V
Max. peak emitter current	: 2 A
Max. average power dissipation	: 300 mW
Interbase resistance (R_{BB})	: 4.7 k Ω to 9.1 k Ω
Intrinsic stand-off ratio (η)	: 0.56 to 0.75
Emitter-leakage current (I_{E0})	: 12 μA (max)
Valley current (I_v)	: 4 mA (min) at $V_{BB} = 20\text{ V}$
Valley voltage (V_v)	: 2 V (typical) at $V_{BB} = 20\text{ V}$
Peak-point current (I_P)	: 5 μA (max) at $V_{BB} = 25\text{ V}$

3.6.3 UJT Relaxation Oscillator

The UJT is often used as a trigger device for SCRs and TRIACs. Other applications include nonsinusoidal oscillators, sawtooth generators, phase-control, and timing circuits.

The most common UJT circuit in use today is the relaxation oscillator shown in Fig. 3.18. Also, this type of circuit is basic to other timing and trigger circuits. The operation is as follows:

Let us consider the situation in which the capacitor is at zero volts ($V_c = 0$) and the switch is suddenly closed at $t = 0$ applying E_{dc} to the circuit. Since $V_E = V_c = 0$, the UJT emitter diode is reverse-biased and the UJT is "off." The amount of reverse bias is V_x volts which can be obtained using the voltage divider rule:

$$V_x = \frac{(R_1 + R_{B1})E_{dc}}{R_1 + R_{B1} + R_2 + R_{B2}} \quad (3.11)$$

In many cases, R_1 and R_2 are much smaller than R_{B1} and R_{B2} , and V_x becomes approximately equal to ηE_{dc} (Eq. 3.9).

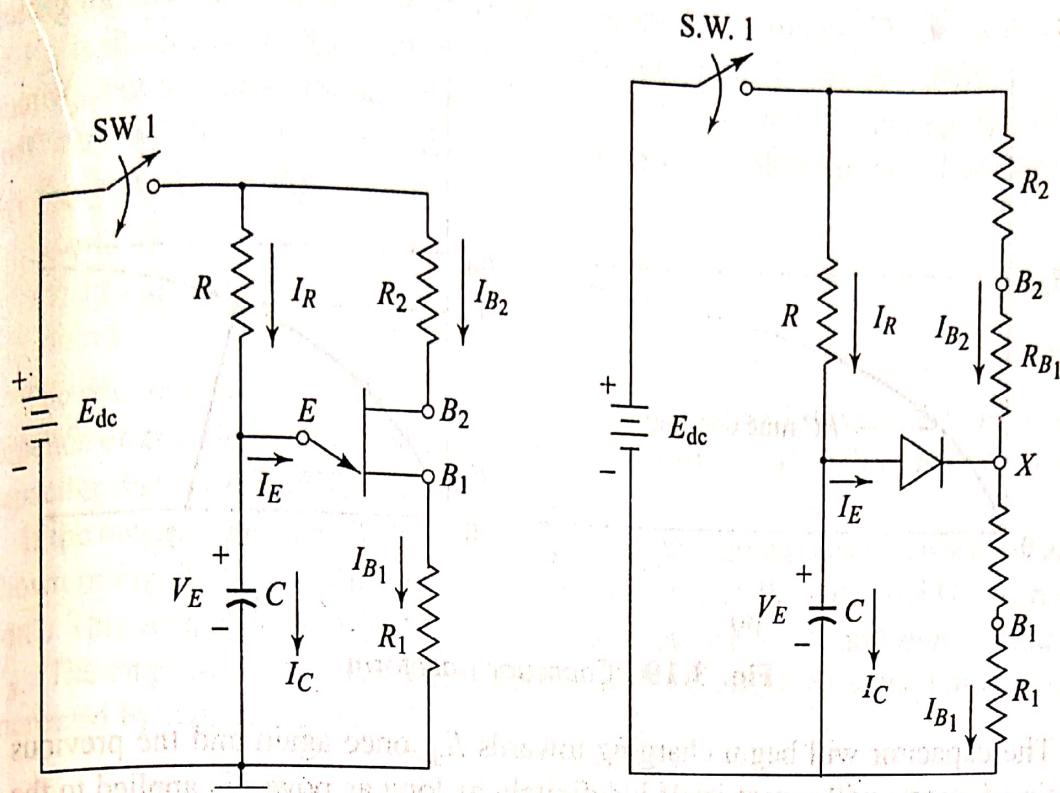


Fig. 3.18 (a) UJT basic-relation oscillator **(b)** its equivalent circuit

In this condition the only emitter current flowing will be small-reverse-leakage, I_{E0} . Also, R_{B_1} will be at its "off" value (typically $4\text{ k}\Omega$). Thus we can consider the emitter to be open ($I_E \approx 0$) and the capacitor will begin to charge toward the input voltage E_{dc} through resistor R . The capacitor voltage increases with a time constant of RC as illustrated in Fig. 3.19 (a). It will continue to increase until the voltage at the emitter reaches the peak-point value, V_{p_1} , given by Eq. (3.10). At this time, the emitter diode becomes forward biased and the UJT turns 'on' with R_{B_1} dropping to a very low value (typically 10 ohms). Since the diode is now forward-biased, the capacitor will discharge through the low-resistance path containing the diode, R_{B_1} and R_1 .

The capacitor discharge time constant is normally very short compared to its charging time constant (see Fig. 3.19(b)). An analytical expression for the discharge time constant is difficult to obtain since R_{B_1} will continually change as the current I_E decreases. The discharging capacitor provides the emitter current needed to keep the UJT "on"; it will remain "on" until I_E drops below the valley voltage I_V , at which time the UJT will turn "off." This occurs at time T_2 when the capacitor voltage has dropped to the valley voltage V_v (typically 2–3 volts). At this time, R_{B_1} returns to its "off" value, the diode is again reverse-biased and $I_E \approx 0$.

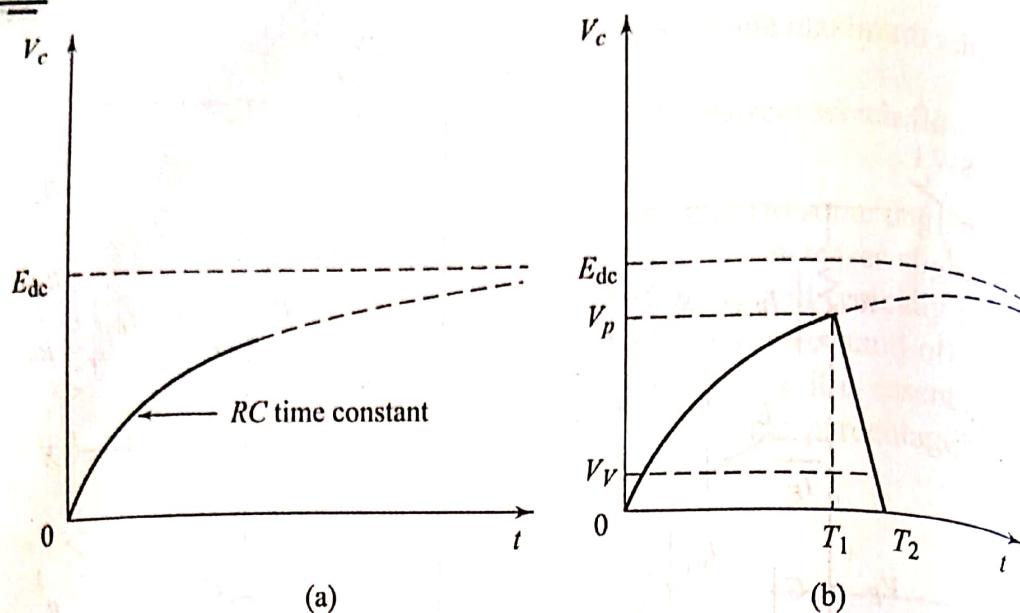


Fig. 3.19 Capacitor waveform

The capacitor will begin charging towards E_{dc} once again and the previous chain of events will repeat itself indefinitely as long as power is applied to the circuit. The result is a periodic sawtooth type waveform as shown in Fig. 3.20 (a).

To calculate the frequency of this waveform, we first calculate the period of one cycle. The length of one period, T_1 , is essentially the time it takes for the capacitor to charge to V_p since the discharge time T_2 is usually relatively short. Thus $T \approx T_1$ and is given by

$$T = R.C. \log_e \left(\frac{E_{dc}}{E_{dc} - V_p} \right) \quad (3.12)$$

In most cases, $V_p \approx \eta E_{dc} + V_0$ and the period can be written as

$$T \approx R.C. \log_e \left[\frac{E_{dc}}{E_{dc}(1 - \eta) - V_D} \right] \quad (3.13)$$

The small diode drop V_D can often be ignored if $E_{dc} > 10$ V, resulting in the more approximate expression,

$$T \approx R.C. \log_e \left[\frac{1}{1 - \eta} \right] \quad (3.14)$$

Examination of Eq. 3.14 brings out an important point, namely that T is relatively independent of supply voltage E_{dc} . This characteristic is important when designing a stable oscillator circuit. The oscillator frequency is given by $1/T$ and can be obtained by using either of the three previous equations for T .

Pulse outputs The UJT relaxation oscillator circuit can also supply pulse waveforms. If the output is taken from B_1 , the result is a train of pulses occurring

during the discharge of the capacitor through the UJT emitter. The waveforms of V_{B_1} is illustrated in Fig. 3.20(b). The amplitude of the B_1 pulses is always less than V_{P_i} but is greater for larger values of C . The voltage at B_1 during the UJT "off" time will be very small and is determined by the voltage divider formed by R_1 , R_{BB} and R_2 [see Fig. 3.18(b)] That is,

$$V_{B_1}(\text{off}) = \left(\frac{R_1}{R_1 + R_{BB} + R_2} \right) E_{dc} \quad (3.15)$$

The rise time of the pulses at B_1 is very short (less than $1 \mu\text{s}$), but the fall time depends on the values of C and R_1 . A larger value of C or R_1 will cause a slower capacitor discharge and a longer fall-time.

If the output is taken at B_2 , a waveform of negative going pulses is obtained as shown in Fig. 3.20(c). This results from the decrease in R_{B_1} when the UJT turns "on". This increases I_{B_2} which increases the drop across R_2 and thus reduces V_{B_2} . The amplitude of this pulses is usually about a couple of volts, but can be increased by increasing R_2 .

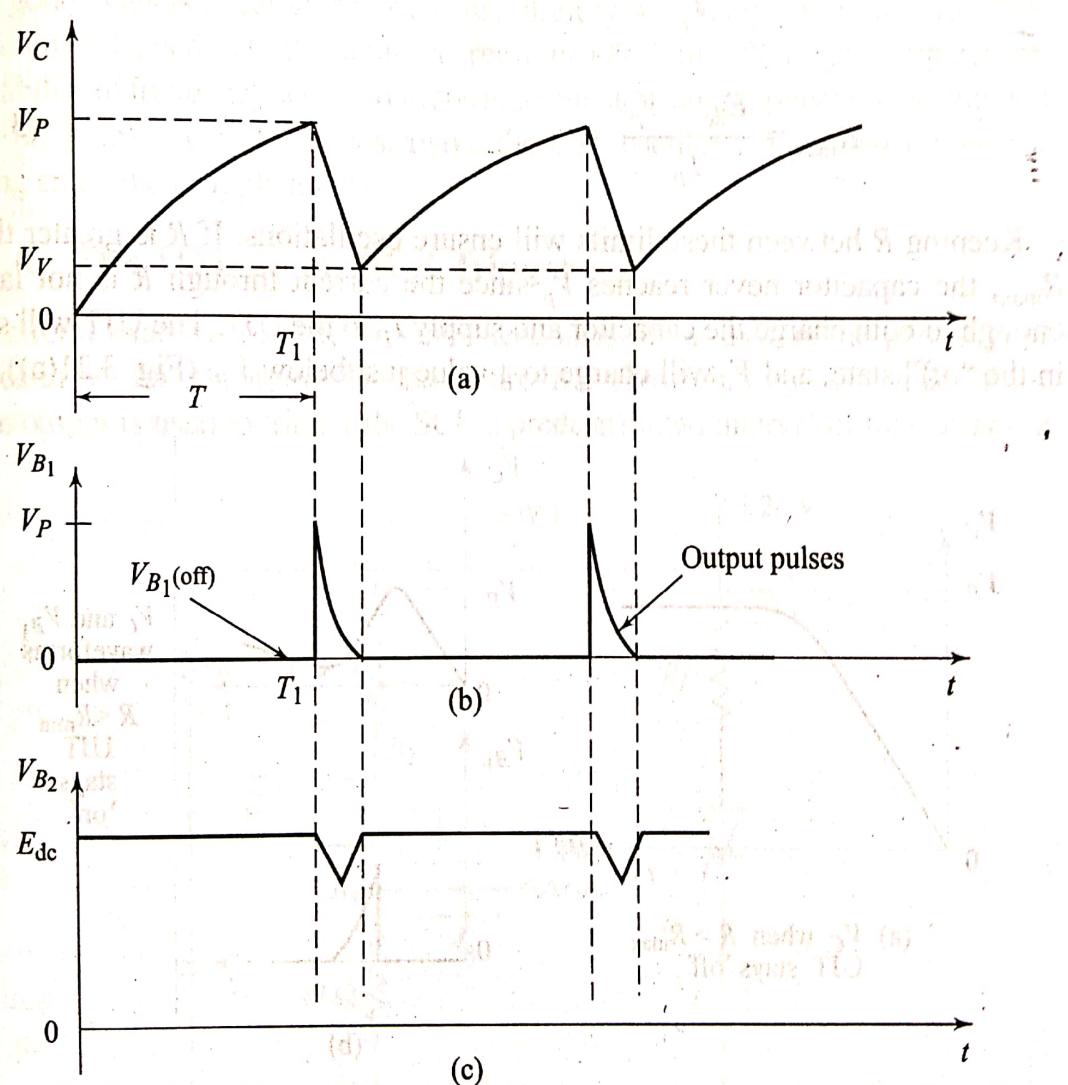


Fig. 3.20 Waveform for UJT relation — oscillator

The pulses at B_1 are usually the ones of most interest, they are of relatively high amplitude and are not affected by loading since they appear across a low-valued resistor R_1 . These positive pulses are often used to trigger SCRs or other gated PNP devices. The amplitude of these pulses is to some degree dependent on the value of C . For values of C of $1 \mu F$ or greater, the amplitude of the pulses is approximately equal to V_p (less than $2-3$ V VJT drop). As C becomes smaller, the B_1 pulse decrease in amplitude. The reason for this is that the smaller value for C discharges a significant amount during the time that the UJT is making its transition from the "off" to "on" state. Thus, when the UJT finally reaches the "on" state, C has lost some of its voltage (V_p) and less voltage can appear across R_1 as the capacitor continues its discharge.

Varying the frequency The frequency of oscillations is normally controlled by varying the charging time constant RC . There are, however, limits on R . These limits are:

$$R_{\min} = \frac{E_{dc} - V_v}{I_v} \quad (3.16)$$

$$R_{\max} = \frac{E_{dc} - V_p}{I_p} \quad (3.17)$$

Keeping R between these limits will ensure oscillations. If R is greater than R_{\max} , the capacitor never reaches V_p since the current through R is not large enough to both charge the capacitor and supply I_p to the UJT. The UJT will stay in the "off" state, and V_c will charge to a value just below V_p . (Fig. 3.21(a))

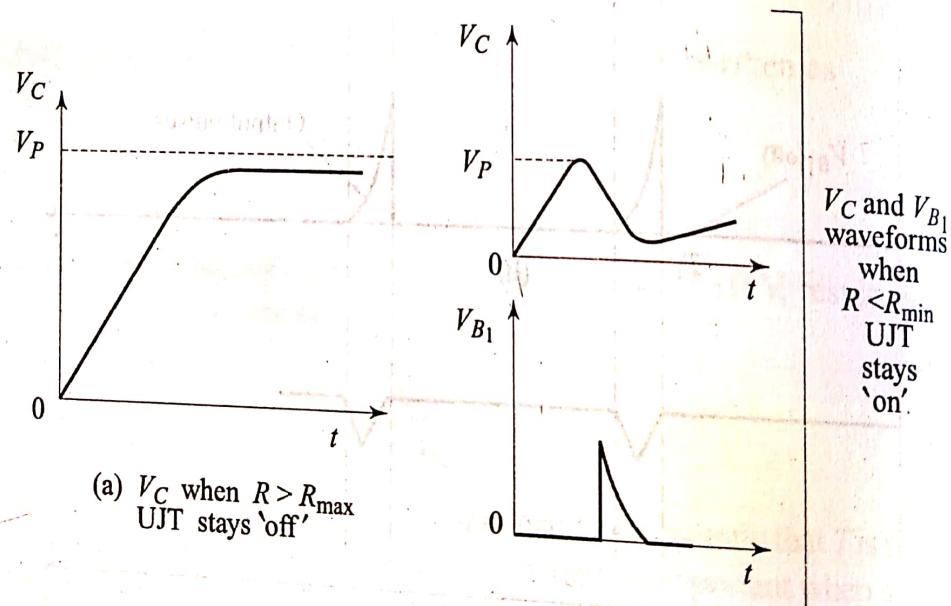


Fig. 3.21 (a) V_c waveform when $R > R_{\max}$; (b) V_c and V_{B_1} when $R < R_{\min}$