UJT

3.6.1 Basic Operation

A typical UJT structure, pictured in following figure, consists of a lightly doped, N-type silicon bar provided with ohmic contacts at each end. The two end connections are called base-1, designated B1, and base-2, B2, A small, heavily doped P-region is alloyed into one side of the bar closer to B2. This P-region is the UJT emitter E, and forms a P-N junction with the bar.

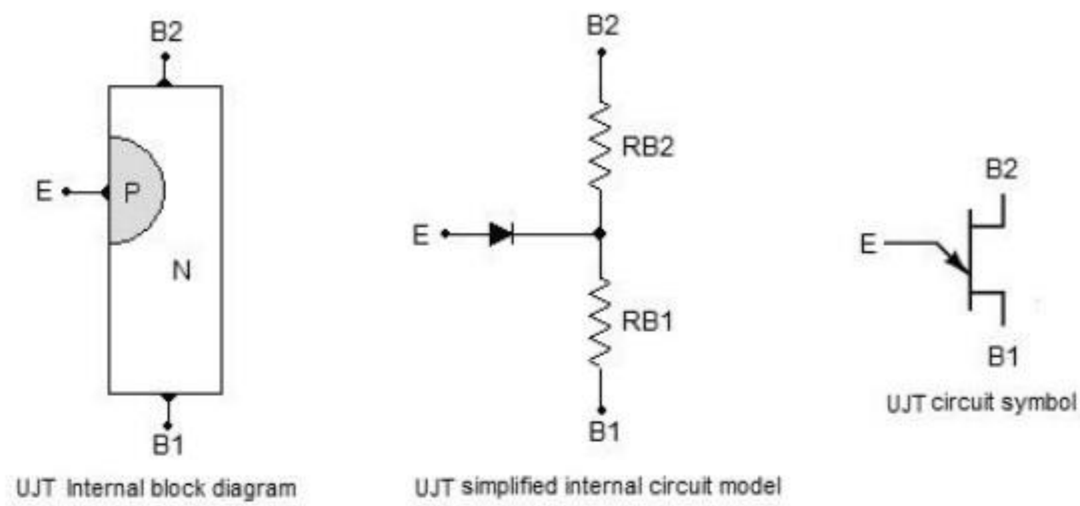


Figure 5.1 UJT structure, Equivalent circuit and Symbol

An interbase resistance, R_{BB} exists between B1, and B2. It is typically between 4 kΩ and 10 kΩ, and can easily be measured with an ohmeter with the emitter open. R_{BB} is essentially the resistance of the N-type bar. This interbase resistance can be broken up into two resistances, the resistance from B1 to emitter called R_{B1} and resistance from B2, to emitter called R_{B2}. Since the emitter is closer to B2, the value of R_{B1} is greater than R_{B2} (typically N-type bar 4.2 kΩ vs 2.8 kΩ).

The operation of the UJT can better be explained with the aid of an equivalent circuit. The UJT's circuit symbol and its equivalent B circuit are shown in Fig. 3.15. The diode represents the PN junction between the emitter and the base-bar (point x). The arrow through RB1 indicates that it is variable since during normal operation it may typically range from 4 kΩ down to 10Ω.

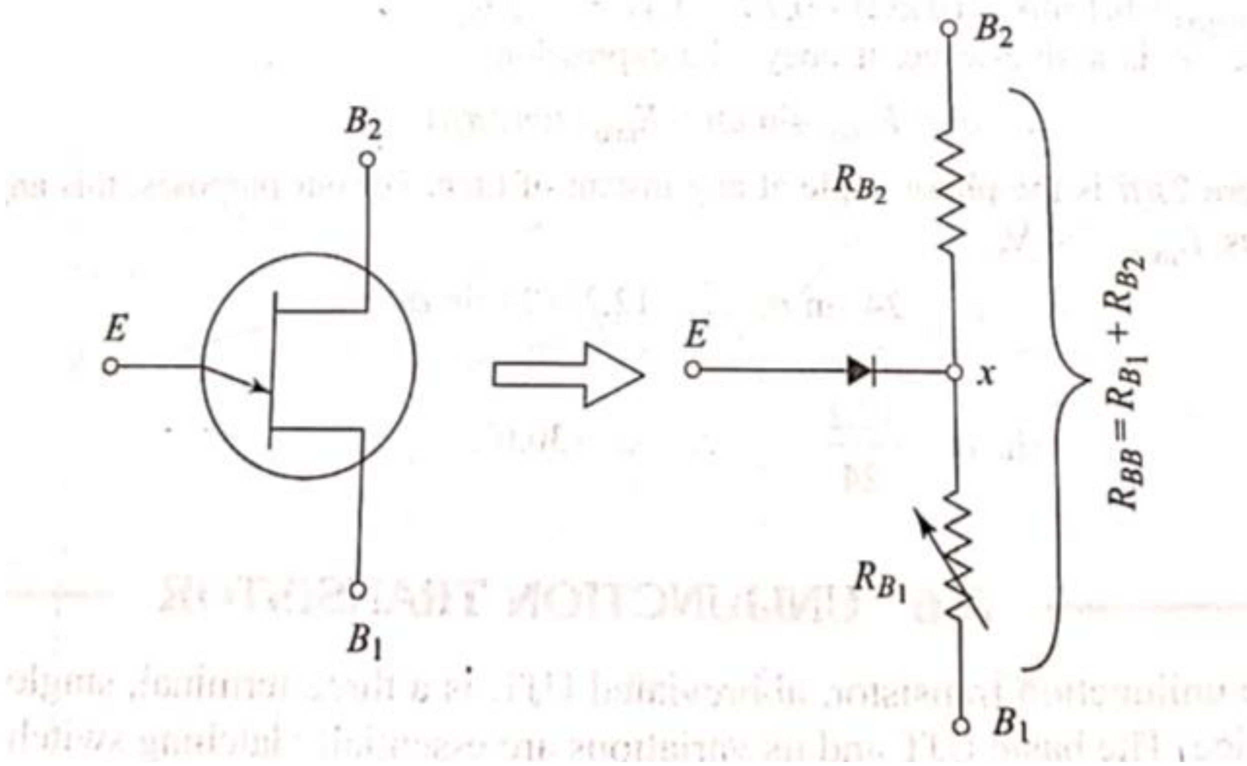


Fig. 3.15 UJT symbol and equivalent circuit

The essence of UJT operation can be stated as follows:

(a) When the emitter diode is reverse biased, only a very small emitter current flows. Under this condition, R, is at its normal high-value (typically 4 kΩ). This is the UJT's "off" state.

(b) When the emitter diode becomes forward biased, R drops to a very low value (reason to be explained later) so that the total resistance between E and B becomes very low, allowing emitter current to flow readily. This is the "on" state.

Circuit-operation The UJT is normally operated with both B2, and E biased positive relative to B1 as shown in Fig. 3.16. B1 is always the UJT reference terminal and all voltages are measured relative to B1. The V_{BB} source is generally fixed and provides a constant voltage from B2 to B1. The V_{EE} source is generally a variable voltage and is considered the input to the circuit. Very often, V_{EE} is not a source but a voltage across a capacitor.

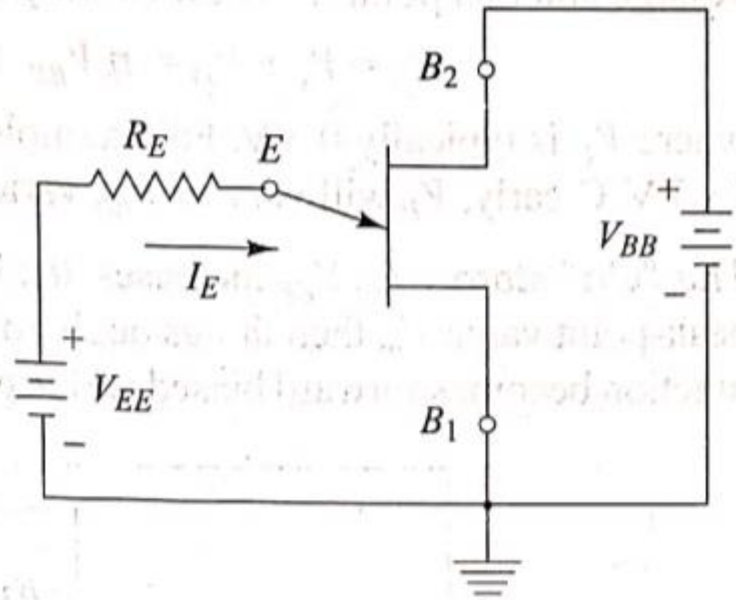


Fig. 3.16 *Normal UJT biasing*

We will analyze the UJT circuit operation with the aid of the UJT equivalent circuit, shown inside the dotted lines in Fig. 3.17(a). We will also utilize the UJT emitter-base-1 V_E-I_E curve shown in Fig. 3.17(b). The curve represents the variation of emitter current IE, with emitter-base-1 voltage, VE, at a constant B2-B1 voltage. The important points on the curve are labelled, and typical values are given in parentheses.

The "Off" state If We neglect the diode for a moment, we can see in Fig. 3.17(a) that R_{B1} and R_{B2} form a voltage divider that produces a voltage Vx from point x relative to ground.

$$V_x = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} \times V_{BB} = \frac{R_{B_1}}{R_{BB}} \times V_{BB}$$

or simply,

$$V_x = \eta V_{BB} \qquad (3.9)$$

where η (the greek letter "eta") is the internal UJT voltage divider ratio R_{B1}/R_{BB} and is called the intrinsic stand off ratio.

Values of n typically range from 0.5 to 0.8 but are relatively constant for a given UJT.

The voltage at point x is the voltage on the N-side of the P-N junction. The V_{EE} source is applied to the emitter which is the P-side. Thus, the emitter diode will be reverse-biased as long as V_{EE} is less than Vx. This is the "off" state, and is shown on the V_E-I_E curve as being a very low current region. In the "off" state, then, we can say that the UJT has a very high resistance between E and B1, and I_E is usually a negligible reverse leakage current. With no I_E, the drop across R_E is zero and the emitter voltage, V_E, equals the source-voltage.

The UJT "off" state, as shown on the V_E-I_E curve, actually extends to the point where the emitter voltage exceeds Vx by the diode threshold voltage, V_D, which is needed to produce forward current through the diode. The emitter voltage and this point, P, is called the peak point voltage,Vp, and is given by

$$V_p = V_x + V_D = \eta V_{BB} + V_D \qquad (3.10)$$

where V_D is typically 0.5 V. For example, if η=0.65 and V_{BB}=20V, then V_P = 13.5 V. Clearly,V_P will vary as V_{BB} varies.

The "On" state As V_{EE} increases, the UJT stays "off" until VE approaches the peak-point value V_P, then things begin to happen. As V_E approaches Vp, the P-N junction becomes forward biased and begins to conduct in the opposite direction.

Note on the VE-IE curve that IE becomes positive near the peak point P. When VE exactly equals VP, the emitter current equals IP, the peak-point current. At this point, holes from the heavily doped emitter are injected into the N-type bar, specially into the B, region. The bar, which is lightly doped, offers very little chance for these holes to recombine. As such, the lower half of the bar becomes replete with additional current carriers (holes) and its resistance RB1 is drastically reduced. The decrease in RB1 causes Vx to drop. This drop in turn causes the diode to become more forward biased, and IE increases even further. The larger IE injects more holes into B1, further reducing RB1, and so on. When this regenerative or snowballing process ends, RB1 has dropped to a very small value (2-25Ω) and IE can become very large, limited mainly by external resistance RE.

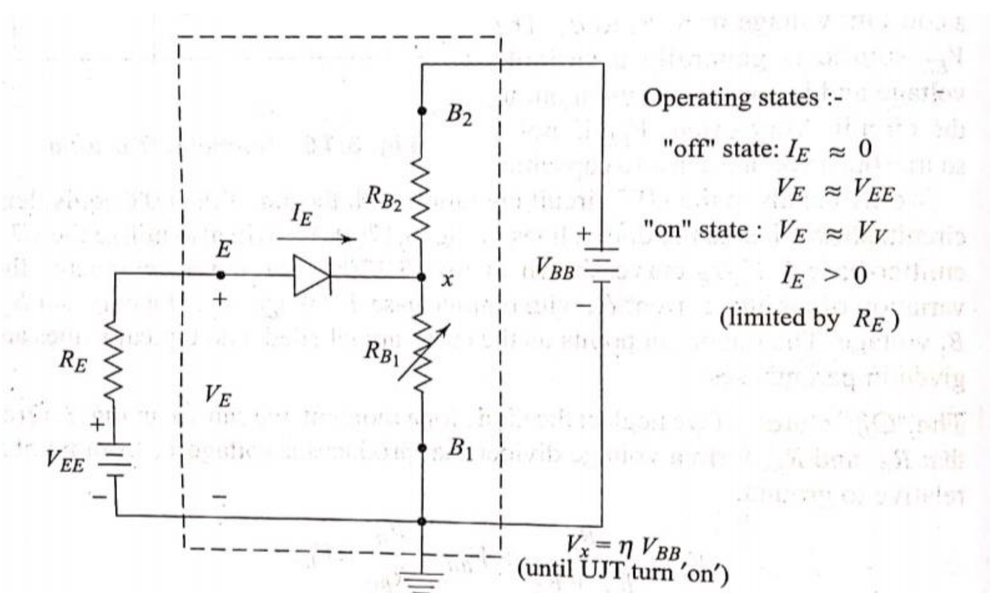


Fig. 3.17 ***(a)*** *Equivalent-circuit for UJT analysis*

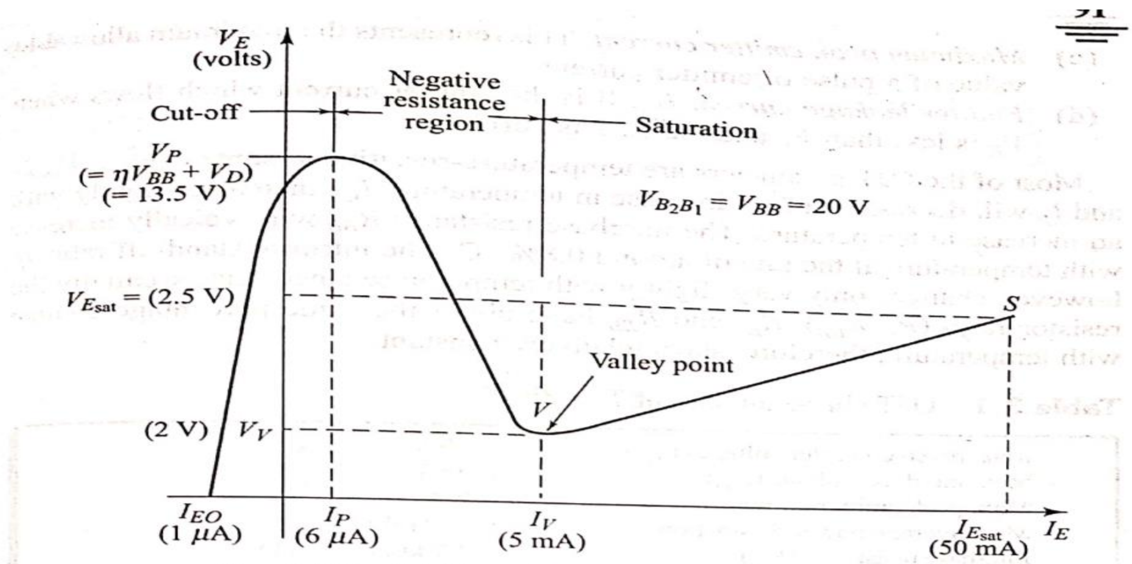


Fig. 3.17 ***(b)*** *Typical UJT V-I characteristic curve*

The UJT operation has switched to the low-voltage, high-current region of its V_E-I_E curve. The slope of this "on" region is very steep, indicating a low resistance. In this region, the emitter voltage V_E, will be relatively small, typically 2 V, and remains fairly constant as IE is increased up to its maximum rated value, $I_{E(sat)}$ Thus, once the UJT is on," increasing V_{EE} will serve to increase I_E while V_E remains around 2V.

Turning "Off" the UJT Once it is on," the UJT's emitter current depends mainly on V_{EE} and R_E. As V_{EE} decreases, IE will decrease along the "on" portion of the V_E-I_E curve. When I_E decreases to point V, the valley point, the emitter current is equal to IV, the valley current, which is essentially the holding current needed to keep the UJT"on". When IE is decreased below IV the UJT turns "off" and its operation rapidly switches back to the "off" region of its V_E-I_E curve, where I_E=0 and V_E- V_{EE}. The valley current is the counterpart of the holding current in PNPN devices, and generally ranges between 1 and 10 mA.

3.6.3 – UJT Relaxation Oscillator

The UJT is often used as a trigger device for SCRs, TRIACs, non-sinusoidal oscillators, sawtooth generators, phase-control, and timing circuits. The most common UJT circuit in use today is the relaxation oscillator shown in Fig. 3.18. Also, this type of circuit is basic to other timing and trigger circuits. The operation is as follows:

Let us consider the situation in which the capacitor is at zero volts and the switch is suddenly closed at t = 0 applying E_{dc} to the circuit. Since V_e= 0, the UJT emitter diode is reverse-biased and the UJT is "off" The amount of reverse bias is V_x volts which can be obtained using the voltage divider rule:

$$V_x = \frac{(R_1 + R_{B_1})E_{dc}}{R_1 + R_{B1} + R_2 + R_{B2}} \tag{3.11}$$

In many cases, R1 and R2 are much smaller than RB1 and rb2 and Vx becomes approximately equal to ηE_{dc} (Eq 3.9)

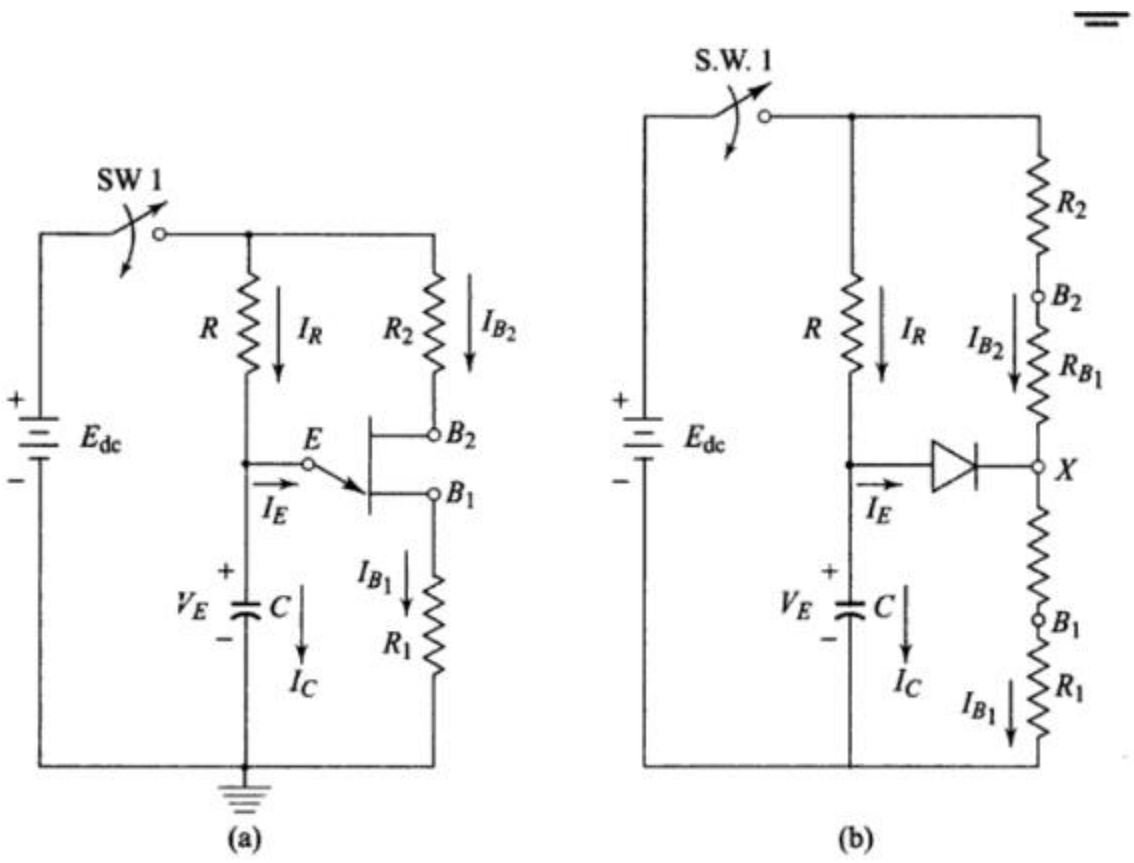


Fig. 3.18 ***(a)*** *UJT basic-relation oscillator* ***(b)*** *its equivalent circuit*

In this condition the only emitter current flowing will be small-reverse-leakage, I_{E0}. Also, R_{B1} will be at its "off" value (typically 4 KΩ). Thus we can consider the emitter to be open ($I_E \approx 0$) and the capacitor will begin to charge toward the input voltage E_{dc}, through resistor R. The capacitor voltage increases with a time constant of RC as illustrated in Fig. 3.19 (a). It will continue to increase until the voltage at the emitter reaches the peak-point value, V_{p1} given by Eq. (3.10). At this time, the emitter diode becomes forward biased and the UJT turns 'on' with R_{B1} dropping to a very low value (typically 10 ohms). Since the diode is now forward-biased, the capacitor will discharge through the low-resistance path containing the diode, R_{B1} and R_1.

The capacitor discharge time constant is normally very short compared to its charging time constant (see Fig. 3.19(b)). An analytical expression for the discharge time constant is difficult to obtain since R_{B1} will continually change as the current IE decreases. The discharging capacitor provides the emitter current needed to keep the UJT "on"; it will remain "on" until /E drops below the valley current /E, at which time the UJT will turn "off." This occurs at time T2 when the capacitor voltage has dropped to the valley voltage V, (typically 2-3 volts). At this time, RBI returns to its "off' value, the diode is again reverse-biased and $I_E \approx 0$.

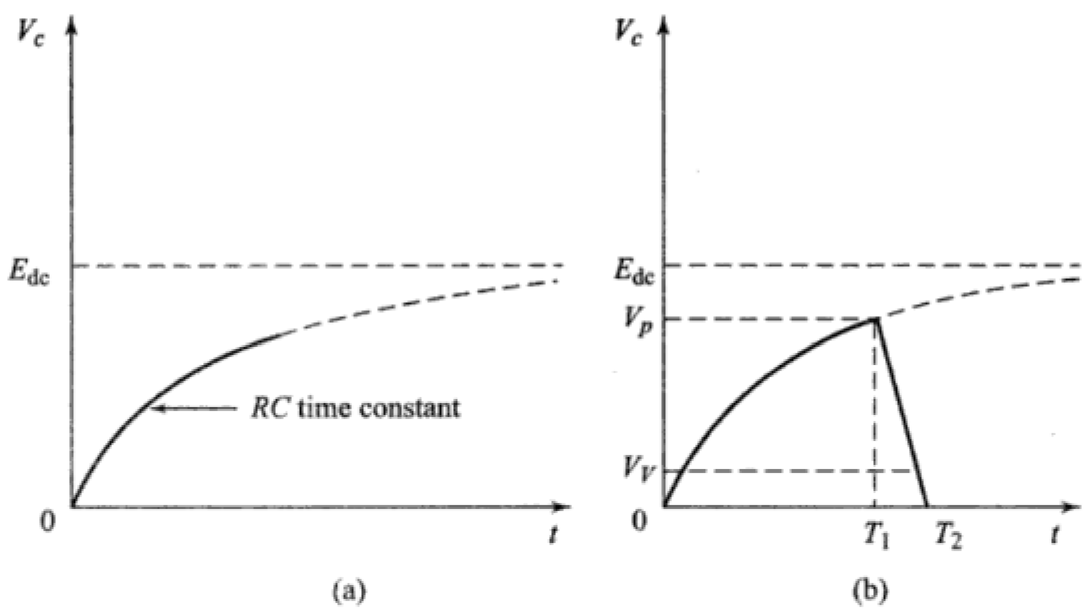


Fig. 3.19 *Capacitor waveform*

The capacitor will begin charging towards E_{dc} once again and the previous chain of events will repeat itself indefinitely as long as power is applied to the circuit. The result is a periodic sawtooth type waveform as shown in Fig. 3.20 (a).

To calculate the frequency of this waveform, we first calculate the period of one cycle. The length of one period, T1, is essentially the time it takes for the capacitor to charge to V_p since the discharge time T2 is usually relatively short. Thus $T \approx T_1$ and is given by

$$T = R.C.\ \log_e\left(\frac{E_{dc}}{E_{dc} - V_p}\right) \tag{3.12}$$

In most cases, $V_p \approx \eta E_{dc} + V_0$ and the period can be written as

$$T \approx R.C.\ \log_e\left[\frac{E_{dc}}{E_{dc}(1-\eta) - V_D}\right] \tag{3.13}$$

The small diode drop V_D can often be ignored if $E_{dc} > 10$ V, resulting in the more approximate expression,

$$T \approx R.C.\ \log_e\left[\frac{1}{1-\eta}\right] \tag{3.14}$$

Examination of Eq. 3.14 brings out an important point, namely that T is relatively independent of supply voltage E_{dc}. This characteristic is important when designing a stable oscillator circuit. The oscillator frequency is given by 1/T and can be obtained by using either of the three previous equations for T.

Pulse outputs

The UJT relaxation oscillator circuit can also supply pulse waveforms. If the output is taken from B_1, the result is a train of pulses occurring during the discharge of the capacitor through the UJT emitter. The waveforms of V81 is illustrated in Fig. 3.20(b). The amplitude of the B1 pulses is always less than V_{in} but is greater for larger values of C. The voltage at B1 during the UJT "off' time will be very small and is determined by the voltage divider formed by R1, Rim and R2 [see Fig. 3.18(b)] That is,

$$V_{B1}\ (\text{off}) = \left(\frac{R_1}{R_1 + R_{BB} + R_2}\right)E_{dc} \tag{3.15}$$

The rise time of the pulses at B_1 is very short (less than 1 its), but the fall time depends on the values of C and R1. A larger value of C or R1 will cause a slower capacitor discharge and a longer fall-time. If the output is taken at B2, a waveform of negative going pulses is obtained as shown in Fig. 3.20(c). This results from the decrease in RBI when the UJT turns "on". This increases IB7 which increases the drop across R2 and thus reduces V. The amplitude of this pulses is usually about a couple of volts, but can be increased by increasing R2.

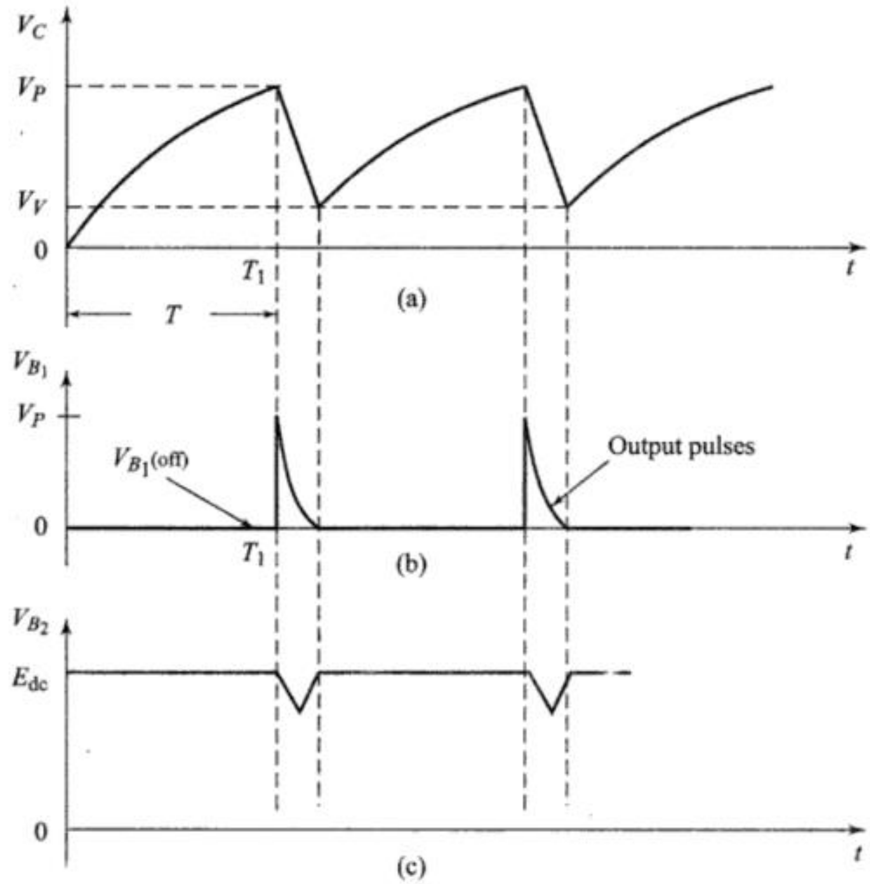


Fig. 3.20 *Waveform for UJT relation — oscillator*

The pulses at B1 are usually the ones of most interest, they are of relatively high amplitude and are not affected by loading since they appear across a low-valued resistor R1. These positive pulses are often used to trigger SCRs or other gated PNPN devices. The amplitude of these pulses is to some degree dependent on the value of C. For values of C of 1 j.iF or greater, the amplitude of the pulses is approximately equal to V41, (less than 2-3 V VJT drop). As C becomes smaller, the B1 pulse decrease in amplitude. The reason for this is that the smaller value for C discharges a significant amount during the time that the UJT is making its transition from the "off' to "on" state. Thus, when the UJT finally reaches the "on" state, C has lost some of its voltage (Vp) and less voltage can appear across RI as the capacitor continues its discharge.

Varying the frequency

The frequency of oscillations is normally controlled by varying the charging time constant RC. There are, however, limits on R. These limits are:

Rmin = (E_{dc}-Vv)/Iv ;   Rmax = (Edc-Vp)/Ip

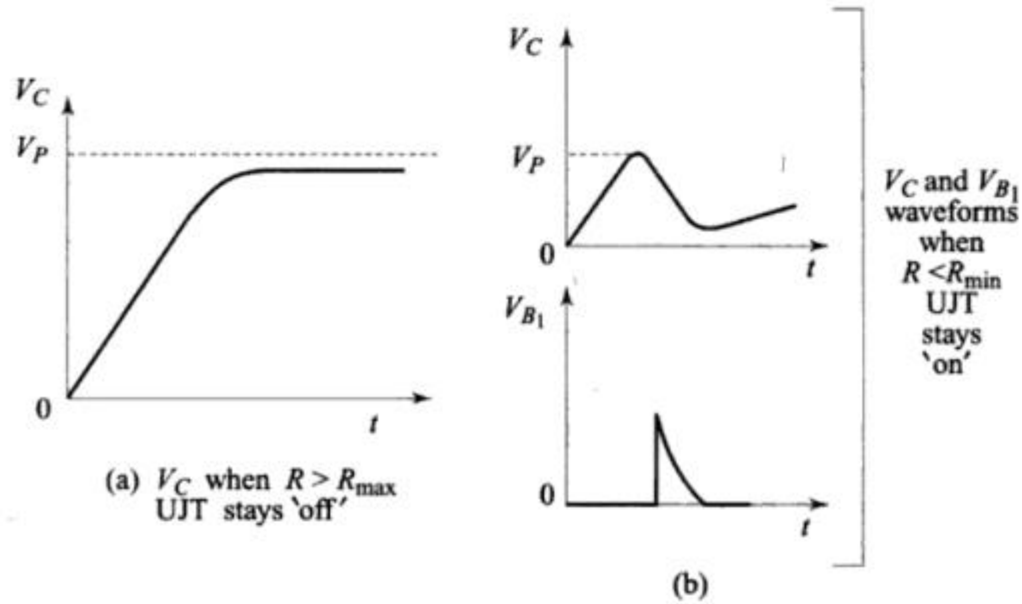


Fig. 3.21 ***(a)*** *V_c waveform when $R > R_{max}$;* ***(b)*** *V_c and R_{B_1} when $R<R_{min}$*

Keeping R between these limits will ensure oscillations. If R is greater than Rmax, the capacitor never charges to Vp since the current through R is not large enough to both charge capacitor and supply Ip to the UJT. The UJT remains in the off state.

If R is smaller than Rmin, the capacitor will reach Vp and discharge through the UJT, but the Ulf will not turn "off" since the current through R is greater than the Iv needed to hold the UJT "on". The capacitor and VB1 waveforms will consists of a single pulse (Fig. 3.21(b)) representing one charge and discharge interval. This single pulse operation is sometimes used in time delay applications. The time delay is given by Eq. 3.12.

Examination of Eq. 3.16 indicates that to obtain a greater upper limit on frequency (a lower value Rmin) the value of Iv should be made larger. Similarly, to obtain a smaller lower limit on frequency (a higher Rmax) the value of Ip should be made smaller. UJTs with Iv as high as 20 mA and I_p as low as 1 µA are presently available, resulting in a possible frequency range of 4000: 1.

The frequency may also be varied by varying C. The lower limit on C is normally around 0.001 µF, while the upper limit depends on the size of R1 (which limits on discharge current). In most applications of this circuit, the value of C is kept fixed and a variable resistor is used for R.

The temperature stability of the UJT relaxation oscillator frequency is normally very good. This is because η varies only slightly with temperature and the only variation in Vp, is due to the small decrease in VD (2 mV/°C) with temperature. Its stability of frequency with variations in temperature and supply voltage coupled with its simplicity and low cost make the UJT oscillator a popular circuit for timing and pulsing applications.

PHASE CONTROLLED CONVERTERS

6.2 CONTROL TECHNIQUES

Figure 6.2 shows the technique of controlled conversion from ac to do for a half-wave circuit which uses a unidirectional switch. When this switch S is turned-on, it conducts current in the direction of the arrow. The output voltage waveform depends on the switch control waveform and the pulse-triggered switch such as SCR, GTO and MCTs. Current pulses are required for triggering SCR and GTO whereas voltage pulses are required for MCTs, MOSFETs and IGBTs.

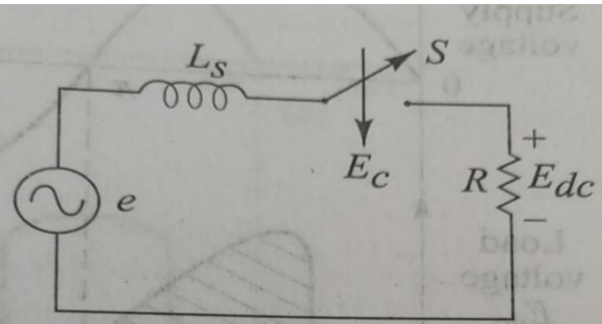


Fig. 6.2 *Half-wave controlled converter using unidrectional switch*

<u>Phase Angel-Control</u>

In ac circuits, the SCR can be turned on by the gate at any phase angle with respect to the applied voltage. The firing angle is measured with respect to a given reference, at which the firing pulses are applied to the thyristor gates. The reference point is the point at which the application of the gate pulses results in the maximum mean positive d.c.-terminal voltage of which the converter is capable. In other words, a firing-angle of 0° corresponds to the conditions when each thyristor in the circuit is fired at the instant its anode voltage-first becomes positive in case the circuit is fired at the instant its anode-first becomes positive in each cycle, under this condition, therefore, the converter operates in exactly the same manner as if it was an uncontrolled rectifier circuit. The α is the symbol for the firing angle.

Hence, the most efficient method to control the turning ‘on" of a thyristor is achieved by varying the firing-angle of thyristor. Such a method of control is called as phase-angle control.

Then converters which work on the principle of natural commutation are called "Line-commutated converters." There are many forms of phase-control possible with the thyristor. These various forms are discussed in the subsequent sections.

Figure 6.3 shows various waveforms obtained using phase-angle control for half wave-

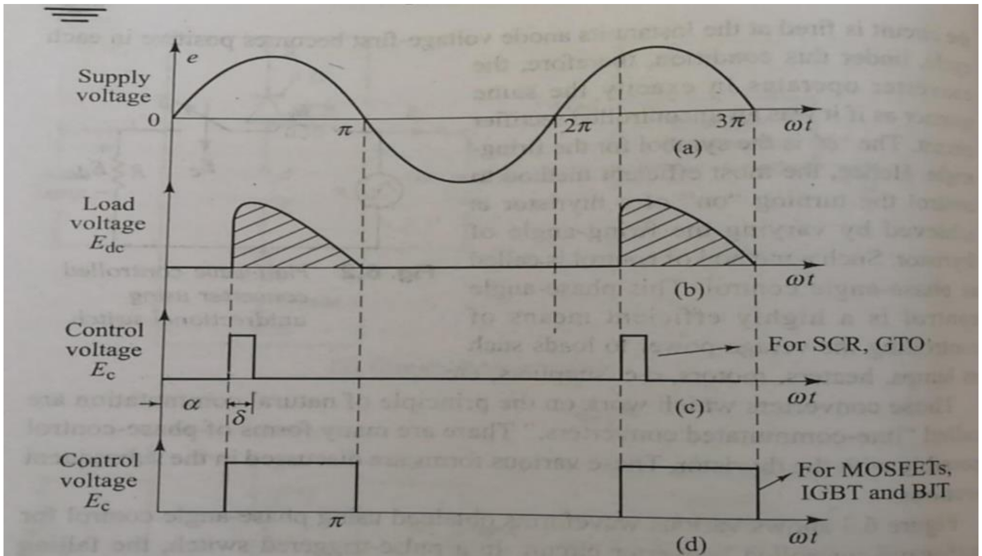


Fig. 6.3 *Phase-angle control*

controlled converter circuit. In a pulse-triggered switch, the falling edge of the control pulse (Vc) lies at an angle α + δ, as shown in Fig 6.3 (c), where δ is a short angle. Once the switch is turned-on, it remains ON even if the triggering pulse has subsided. It can be turned off only when the current through it is reduced below the holding current (in case of SCR).

In a level triggered switch, the falling edge lies at an angle π as shown in Fig 6.3 (d).

<u>Extinction Angle Control</u>

Figure 6.4 shows the output voltage waveform and the control pulses for the level-triggered and pulse-triggered switches. The rising edge of the control pulse coincides with the beginning of the input voltage waveform. The falling edge lies at a controllable angle (π-β). Angle β is called as the extinction angle. In a pulse triggered switch, the control pulse consists of two short pulses: one for turning on and the other for forced-turn-off.

6.2.3 Pulse Width Modulation Control (PWM)

6.3 Single Phase Half-Wave Controlled Rectifier

6.4 SINGLE-PHASE FULL-WAVE CONTROLLED RECTIFIER (TWO-QUADRANT CONVERTERS)

There are two basic configurations of full wave controlled rectifiers. Their classification is based on the type of SCR configuration employed. They are

(1) Mid-point converters. (2) Bridge converters

6.4.1 Mid-point Converters (M-2 Connection)

In a single phase full-wave controlled-rectifier circuit with mid-point configuration two SCRS (M-2) and a single-phase-transformer with centre-tapped secondary windings are employed. These converters are also referred to as two pulse converters as two triggering pulses or two sets of triggering pulses are to be generated during every cycle of the supply to trigger the various SCRs. Single phase full-wave circuit with transformer mid-point configuration are generally used for rectifiers of low ratings.

1. With Resistive Load

Figure 6.12 illustrates a 2-pulse mid-point converter circuit with resistive-load. This type of full-wave rectifier circuit uses two SCRs connected to the centre-tapped secondary of a transformer, as shown in Fig. 6.12. The input signal is coupled through the transformer to the centre tapped secondary.

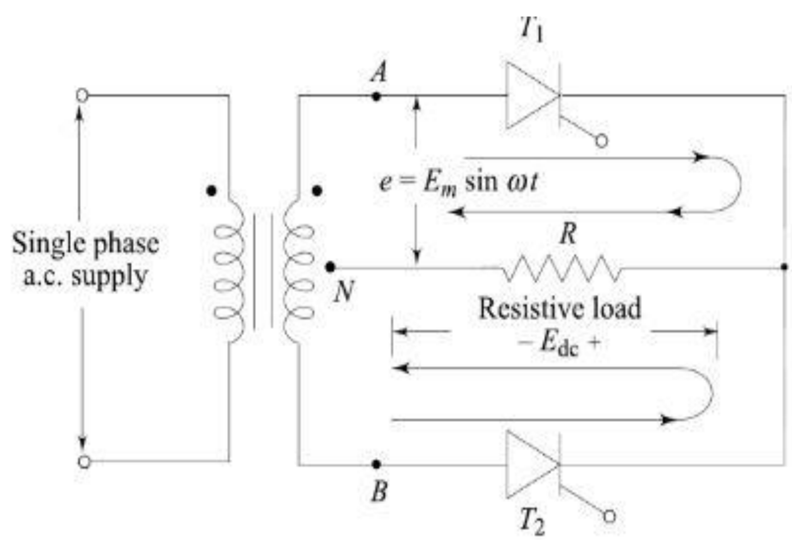


Fig. 6.12 *Full-wave mid-point circuit with resistive load*

During the positive half-cycle of the a.c. supply, i.e. when terminal A of the transformer is positive with respect to terminal B, or the secondary-winding terminal A is positive with respect to N, SCR, (T) is forward-biased and SCR(T) is reverse-biased. Since no triggering pulses are given to the gates of the SCRs, initially they are in off-state. When SCR, is triggered at a firing-angle a, current would flow from terminal A through SCR, the resistive load R and back to the centre-tap of the transformer i.e. terminal). This current path is also shown in Fig. 6.12. This current continuous to flow up to angle a when the line voltage reverses its polarity and SCR, is turned-off. Depending upon the value of a and the load circuit parameters, the conduction angle of SCR, may be any value between 0 and π.

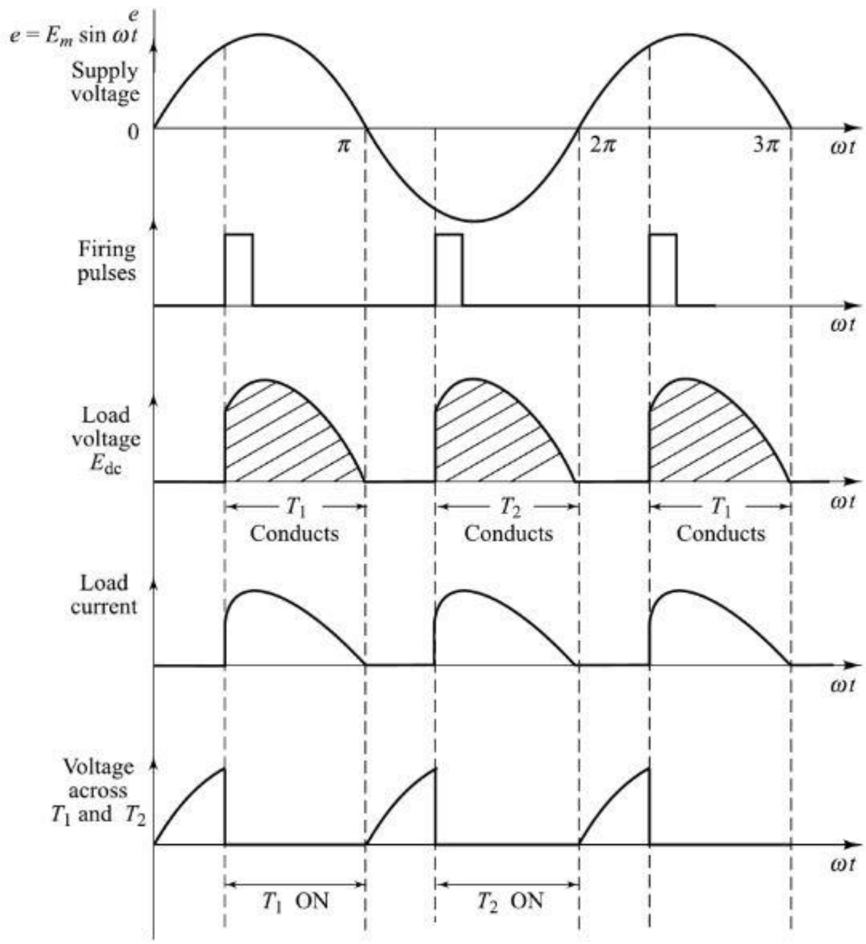


Fig. 6.13 *Waveforms for M-2 configuration with resistive-load*

During the negative half-cycle of the a.c. supply, the terminal B of the transformer is positive with respect to N. SCR, is forward-biased. When SCR, is triggered at an angle (π + α), current would flow from terminal B, through SCR, the resistive load and back to centre-tap of the transformer. This current continues till angle 2π, then SCR, is turned off. Here it is assumed that both thyristors are triggered with the same firing angle, hence they share the load current equally.

Each half of the input-wave is applied across the load. Thus, across the load, there are two pulses of current in the same direction. Hence the ripple frequency across the load is twice that of the input supply frequency. The voltage and current waveforms of this configuration is shown in Fig. 6.13. It is clear from Fig. 6.13 that with purely resistive load, the load current is always discontinuous.

The voltage and current relations are derived as follows:

(a) Average d.c. Output Voltage

The output d.c. voltage, Edc, across the resistive load is given by

$$E_{dc} = \frac{1}{\pi}\int_{\alpha}^{\pi} E_m . \sin \omega t \, d(\omega t) = \frac{E_m}{\pi}[-\cos \omega t]_{\alpha}^{\pi} = \frac{E_m}{\pi}[1+\cos \alpha] \qquad (6.9)$$

(b) Average-load Current The average-load current is given by

$$I_{dc} = \frac{E_m}{\pi \cdot R}[1+\cos \alpha] \qquad (6.10)$$

(c) RMS Load-voltage The RMS load-voltage for a given firing angle α is given by

$$E_{rms} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} E_m^2 \sin^2 \omega t \, d\,\omega t\right]^{\frac{1}{2}} = E_m \cdot \left[\frac{1}{\pi}\int_{\alpha}^{\pi} \sin^2 \omega t \, d\,\omega t\right]^{\frac{1}{2}}$$

$$= E_m \cdot \left[\frac{1}{\pi}\int_{\alpha}^{\pi}\left(\frac{1-\cos 2\omega t}{2}\right) d\,\omega t\right]^{\frac{1}{2}} = E_m \cdot \left[\frac{1}{2\pi}\left(\omega t - \frac{\sin 2\omega t}{2}\right)_{\alpha}^{\pi}\right]^{\frac{1}{2}}$$

$$= E_m \cdot \left[\frac{1}{2\pi}\left(\pi - \alpha + \frac{\sin 2\alpha - \sin 2\pi}{2}\right)\right]^{\frac{1}{2}} = E_m \cdot \left[\frac{1}{2\pi}\left(\pi - \alpha + \frac{\sin 2\alpha}{2} - 0\right)\right]^{\frac{1}{2}}$$

$$E_{rms} = E_m \cdot \left[\frac{\pi - \alpha}{2\pi} + \frac{\sin 2\alpha}{4\pi}\right]^{\frac{1}{2}} \qquad (6.11)$$

2. With Inductive Load:

CHOPPERS

1. Line commuted converters
2. AC link Chopper

   AC Link Chopper (inverter-rectifier) In this method the d. c. is first converted to a.c, by an inverter (dc to ac. converter). The Obtained ac is then stepped up or down by a transformer and then rectified back to dc by a rectifier. As the conversion is in two stages, dc to ac and ac to dc this technique is therefore, costly, bulky and less

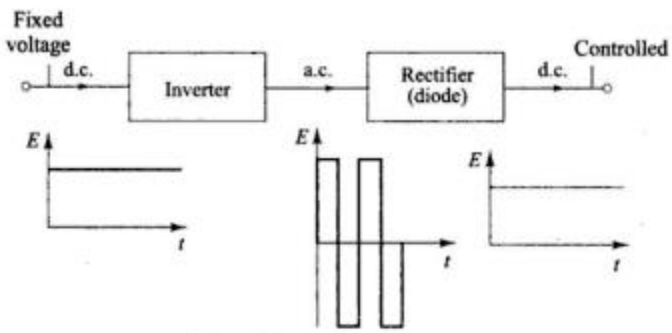


Fig. 8.1 *a.c.-link-chopper*

efficient. However, the transformer provides isolation between load and source.

DC Chopper

Power chopper is a static device (switch) used to obtain variable dc voltage from a source of constant dc voltage. Therefore, may be thought of as dc equivalent of an ac transformer since they behave in an identical manner.

They save power, the chopper offers greater efficiency, faster response, lower maintenance, small size, smooth control, and, for many applications, lower cost,

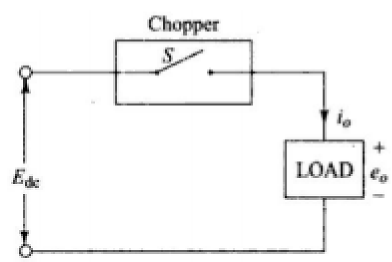


Fig. 8.2 *Basic chopper configuration*

than motor-generator sets or gas tubes approaches.

Basic Chopper Classification:

DC choppers can be classifiedas:

(A) According to the Input /Output Voltage Levels

(i) Step-down chopper: The output volt* is less than the input

(ii) Step-up chopper: The output voltage is greater than the input

(B) According to the Directions Of Output Voltage and Current

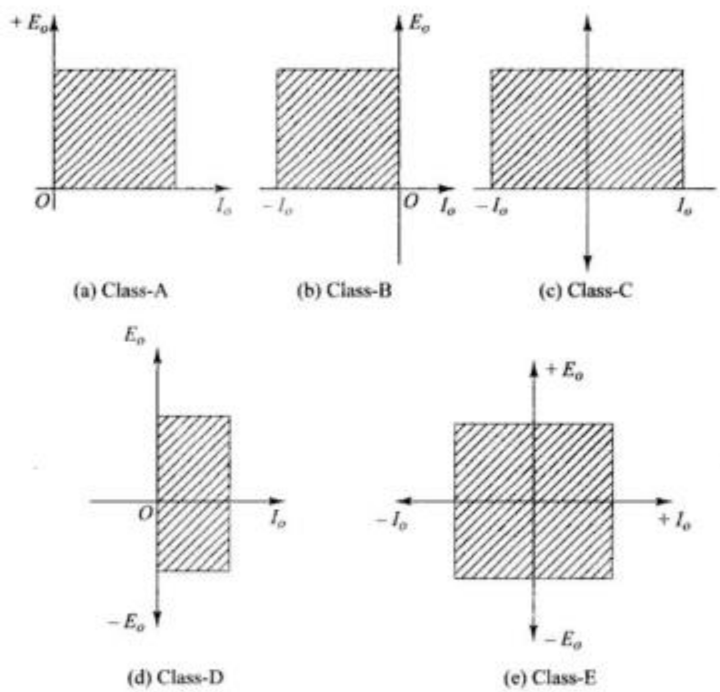
(i) Class A (type A) chopper

(ii) Class B (Type B) chopper

(üi) Class C (type C) chopper

(iv) Class D (type D) chopper

(v) Class E (type E) chopper



The voltage and Current directions for above classes are shown in fig

(C) Chopper According to Circuit operation

(i) **First-quadrant chopper**; The output voltage and must be positive. (Type A).

(ii) **Two-quadrant chopper**: The output voltage is positive current can be positive or negative (class-C) or the output current is positive and the voltage Can positive or negative (class-D).

(iii) **Four-quadrant chopper**: The output voltage current Can negative (class-E).

(D) According to Commutation Method

(a) voltage commutated chopper

(b) Current-commutated choppers

(c) Load-commutated choppers

(d) Impulse-commutated choppers

Principle of Step-Down Chopper (Buck-Converter)

In general, dc chopper consists of power semiconductor devices (SCR. BJT, power MOSFET, IGBT, GTO, MCT, etc., which works as a switch), input dc power supply, elements (R, L, C etc.) and output load. (Fig 8.4). The average output voltage across the load is controlled by varying on-period and off-period (or duty Cycle) of the switch.

A commutation circuitry is required for SCR based chopper circuit. Therefore, in general, gate-commutation devices-based choppers have replaced the SCR- based choppers. However. for high voltage and high-current applications. SCR based choppers are used. The variations in on and off periods of the switch provides an output voltage with an adjustable value the (Dp) in freewheeling to provide a path to load-current when switch (S) is OFF. The smoothing inductor filters out ripples in the load current. Switch S is kept conducting for period a T_{on} is blocked for period T_{off}. The chopped load voltage waveform is shown in Fig. 8.5.

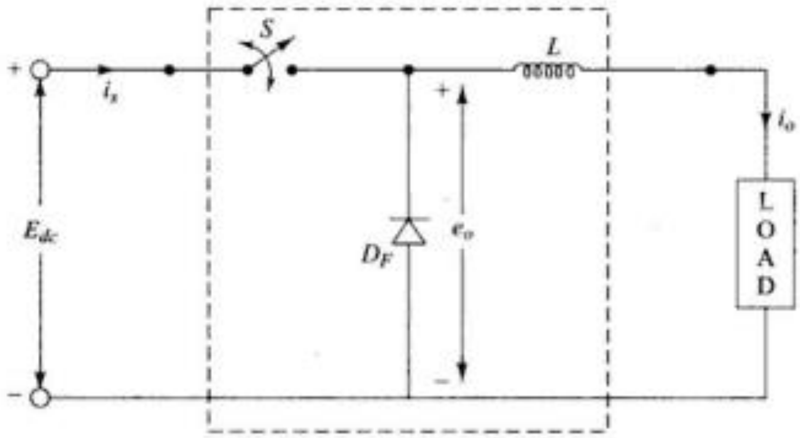


Fig. 8.4 *Basic chopper circuit*

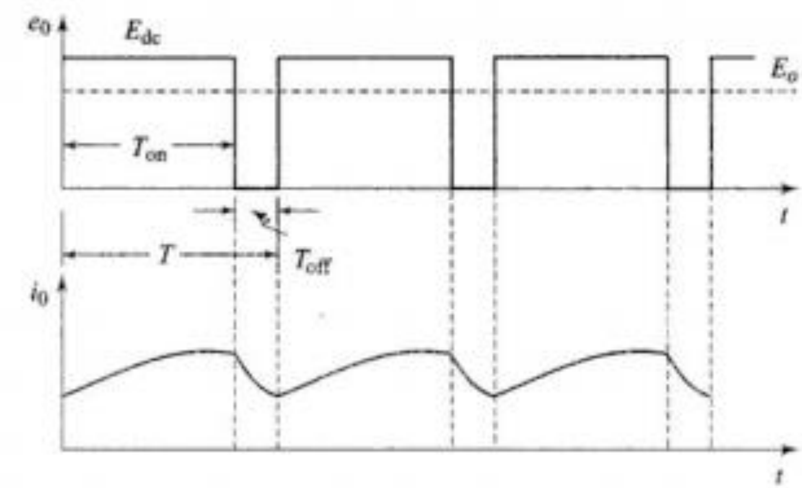


Fig. 8.5 *Output voltage and current waveforms*

During the period when the chopper is on, the supply terminals are connected to the load, terminals. During the interval T off, when the chopper is off, load current through the freewheeling diode Df as a result, load terminals are short circuited by Df and load voltage is therefore, zero during In this manner, a chopped dc voltage is produced at the load terminals. From Fig the load voltage is given by

$E_0 = E_{dc} [T_{on} / (T_{on}+T_{off})]$

T_{on} = on time

T_{off} = off time of chopper

$T = T_{on} + T_{off}$; chopping period

$E_0 = E_{dc} . (T_{on}/T)$

$E_0 = E_{dc} . \alpha$

Thus, the load voltage can be controlled by varying the duty cycle of the chopper.

$E_0 = E_{dc} . (T_{on}/T) = E_{dc} . T_{on} . f$

Where f=chopping frequency

The average value of load current is given by

$I_0 = E_0/R = \alpha . E_{dc}/R$

The effective RMS value of the output is given by

$E_{0(rms)} = \sqrt{[(E_{dc}^2 . T_{on})/T]} = E_{dc} . \sqrt{(T_{on}/T)}$

$= E_{dc} \sqrt{\alpha}$

8.3.2 Principle of Step-up Chopper

The chopper configuration of Fig. 8.4 is capable of giving a maximum voltage that Slightly smaller than the input d.c. voltage (i.e. $E_o < E_{dc}$). Therefore, the chopperconfiguration of Fig. 8.4 is called as step-down choppers. However, the chopper can also be used to produce higher voltages at the load than the input voltage i.e. ($E_o \geq E_{dc}$) This is called as step-up chopper and is illustrated in Fig. 8.6.

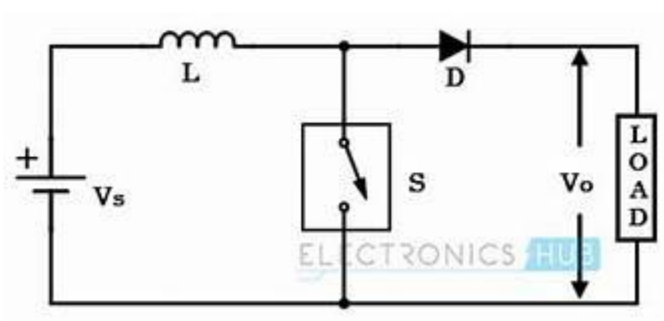


Fig. 8.6 Step-up chopper or boost choppers

When the chopper is ON, the inductor L is connected to the supply E_{dc} and inductor stores energy during on-period, T_{on}

When the chopper is OFF, the inductor current is forced to flow through the diode and load for a period T_{OFF} As the current tends to decrease, polarity of the emf induced in inductor Is reversed to that of shown in Fig. 8.6, and as a result voltage across the load E_0 becomes

$$E_0 = E_{dc} + L\frac{di_s}{dt}$$

that is, the inductor voltage adds to the source voltage to force the inductor current into the load. In this manner, the energy stored in the inductor is released to the load. Here, higher value of inductance L is preferred for getting lesser ripple in the output.

During the time T_{ON} when the chopper is ON, the energy input to the inductor from the source is given by

$$W_i = E_{dc}\, I_s T_{on}$$

Equation 8.7 is based on the assumption that the source current is free from ripples.

Now, during the time T when chopper is OFF, energy released by
inductor to the load is given by

$$W_0 = (E_0 - E_{dc})\, I_s\, T_{off}$$

Considering the system to be lossless, and, in the steady-state, these energies will be equal

$$\therefore \quad E_{dc} \cdot I_s\, T_{on} = (E_0 - E_{dc})\, I_s\, T_{off}$$

$$\text{or} \quad E_0 = E_{dc}\frac{T_{on} + T_{off}}{T_{off}}$$

$$\text{or} \quad E_0 = E_{dc}\frac{T}{T - T_{on}}$$

$$\text{or} \quad E_0 = E_{dc}\frac{1}{T/T - T_{on}/T}, \text{ But, } \frac{T_{on}}{T} = \alpha$$

$$\therefore \quad E_0 = \frac{E_{dc}}{1-\alpha}$$

For $\alpha = 0, E_0 = E_{dc}$; and $\alpha = 1, E_0 = \infty$.

For α=0, E_0=Edc and α=1, E_0= infinity
Hence, for variation of a duty cycle in the range 0 < α < 1, the output voltage Eo will vary in the range Edc < Eo < ∞ . This principle of step-up chopper can be employed for regenerative braking of the d.c. motors even at lower operating speeds. Let Edc represent the d.c. motor

generated voltage and Eo the d.c. source voltage in Fig. 8.6. Regenerative braking takes place when

$\left(E_{dc} + L\frac{di_s}{dt}\right)$ exceeds Eo. Even at decreasing motor speeds, duty cycle α can

be so adjusted that $\left(E_{dc} + L\frac{di_s}{dt}\right)$ is more than the fixed supply voltage Eo.

SOLVED EXAMPLE

Example 8.4

A step-up chopper is used to deliver load voltage of 500 V from 220V d.c. source. If the blocking period of the thyristor is 80 pus, compute the required pulse width

Solution: From Eq. (8.10) we have, $E_0 = E_{dc}\frac{T_{on} + T_{off}}{T_{off}}$

$$\therefore \quad 500 = 220\,\frac{T_{on} + 80\times10^{-6}}{80\times10^{-6}}, \qquad \therefore T_{on} = 101.6\times10^{-6} = 101.6\ \mu s.$$

<u>8.3.3 Principle of Step-Up/Down Chopper</u>

A chopper can also be used both in step-up and step-down modes by continuously varying its duty cycle. The principle of operation is illustrated in Fig 8.7. As shown, the output, voltage polarity is opposite to that of input voltage Edc.

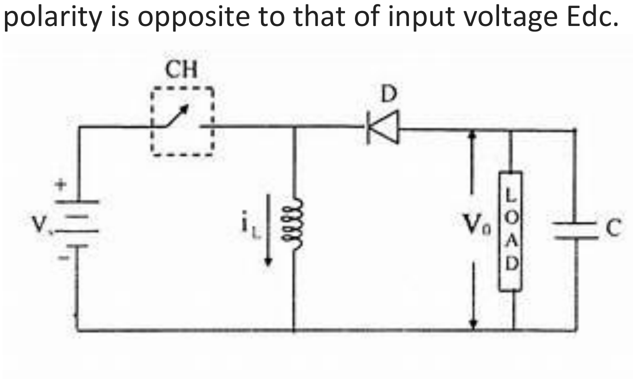


Fig. 8.7 Step-up/down chopper.

When the chopper is ON, the supply current flows through the path Edc+ -CH-L-Edc. Hence, inductor L stores the energy during the Ton period.

When the chopper CH is OFF, the inductor current tends to decrease and as a result, the polarity of the emf induced in L is reversed as shown in Fig. 8.7
Thus, the inductance energy discharges in the load through the path,

$$L_+ - Load - D - L_-.$$

During T_{on}, the energy stored in the inductance is given by,

$$W_i = E_{dc} I_s T_{on} \tag{8.12}$$

During T_{off}, the energy fed to the load is

$$W_o = E_0 I_s T_{off} \tag{8.13}$$

For a lossless system, in steady-state: Input energy, W_i = output energy, W_o

$$\therefore \quad E_{dc} \cdot I_s \cdot I_{on} = E_0 I_s T_{off}, \text{ or } E_0 = E_{dc} \cdot \frac{T_{on}}{T_{off}} \tag{8.14}$$

or
$$E_0 = E_{dc} \cdot \frac{T_{on}}{T - T_{on}} = E_{dc} \cdot \frac{1}{T/T_{on} - T_{on}/T_{on}}$$

Substituting $\frac{T_{on}}{T} = \alpha$, we get, $E_0 = E_{dc} \cdot \frac{1}{1/\alpha - 1}$

or
$$E_0 = E_{dc} \frac{\alpha}{1-\alpha} \tag{8.15}$$

For $0 < \alpha < 0.5$, the step-down chopper operation is achieved and for **$0.5 < \alpha < 1$, step-up chopper** operation is obtained.

INVERTERS

9.2 CLASSIFICATION OF INVERTERS

Inverters can be classified on the basis of a number of factors:

(a) Classification According to the Nature of Input Source Based on the nature of input power source inverters are classified as

(i) Voltage source inverters (VSI)

(ii) Current source inverters (CSI)

In case of VSI, the input to the inverter is provided by a ripple free dc voltage Source whereas in CSI, the voltage source is first converted into a current source and then used to supply the power to the inverter

(b) Classification According to the Wave Shape of the Output Voltage

The inverters can be classified according to the nature of output voltage waveform as:

i) Square-wave inverter

(i)Quasi-square wave inverter

(iii) Pulse-width modulated (PWM) inverters

A square-wave inverter produces a square-wave ac voltage of a constant magnitude. The output voltage of this type of inverter can only be varied by controlling the input de voltage. Square-wave ac-output voltage of an inverter is adequate for low and medium power applications. However, the sine-wave output voltage is the ideal waveform for many high-power applications. Two methods can be used to make the output closer to a sinusoid. One is to use a filter circuit on the output side of the inverter. This filter must be capable of handling the large power output of the inverter, so it must be large and will therefore add to the cost and weight of the inverter. Moreover, the efficiency will be reduced due to the additional power-losses in the filter.

The second method, pulse-width modulation (PWM) uses a switching scheme within the inverter to modify the shape of the output voltage waveform.

9.2.1 Thyristor Inverter Classification

The thyristor inverters can be classified in the following category

1. According to the method of commutation.

2. According to the connections.

(a) Classification According to the Method of Commutation According to the method of commutation, the SCR inverters can mainly be categorized in two types, viz.

1. Line commutated inverters

2. Forced commutated inverters.

1. ***Line Commutated Inverters*** In case of a.c.circuits, a.c. line voltage is available across the device. When the current in the SCR goes through a natural zero, the device is turned-off. This process is known as natural commutation process a the inverters based on this principle are known as line commutated inverters

2. ***Forced Commutated Inverters*** In case of d.c. circuits, since the supply voltage does not go through the zero point, some external source is reo commutate the device. This process is known as the forced commutation and the inverters based on this principle are called as forced commutated inverter. As the device is to be commutated forcefully, these types of inverter complicated commutation circuitries. These inverters are further classified

(i) Auxiliary commutated inverters and (ii) Complementary commutated inverter

(b) Classifications According to Connections According to the connections of the thyristors and commutating components, the inverters can be classified mainly in three groups. These are:

1. Series inverters.

2. Parallel inverters.

3. Bridge inverters.: Bridge inverters are further classified as: (i) Half-bride and (ii) Full-Bridge.

9.3 SINGLE-PHASE HALF-BRIDGE VOLTAGE-SOURCE INVERTERS

Figure 9.1 shows the basic configuration of single-phase half-bridge inverter Switches S1 and S2, are the gate commutated devices such as power BJTS, MOSFETs, GTO, IGBT MCT, etc. When closed, these switches conducts and current flows in the direction of arrow. The operation of this inverter for different types of load is explained in the following sections:

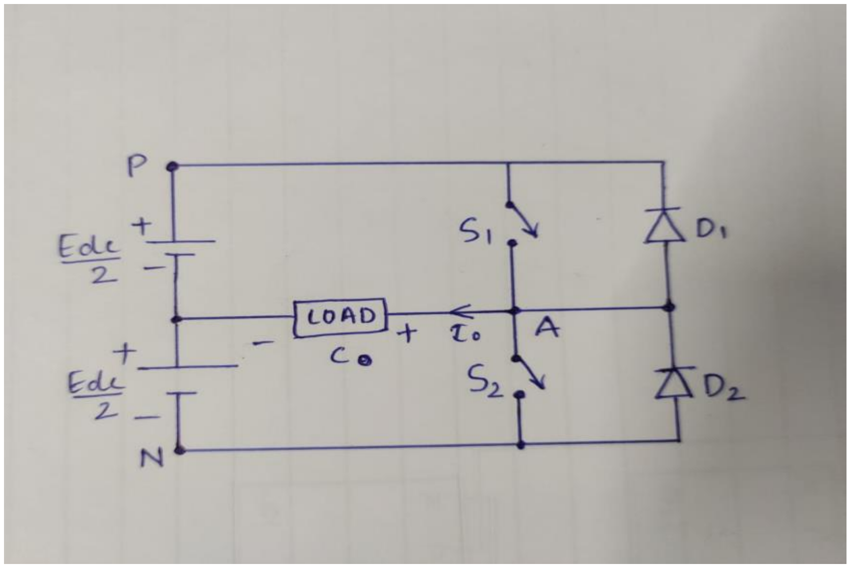


Fig.9.1 Half-bridge inverter

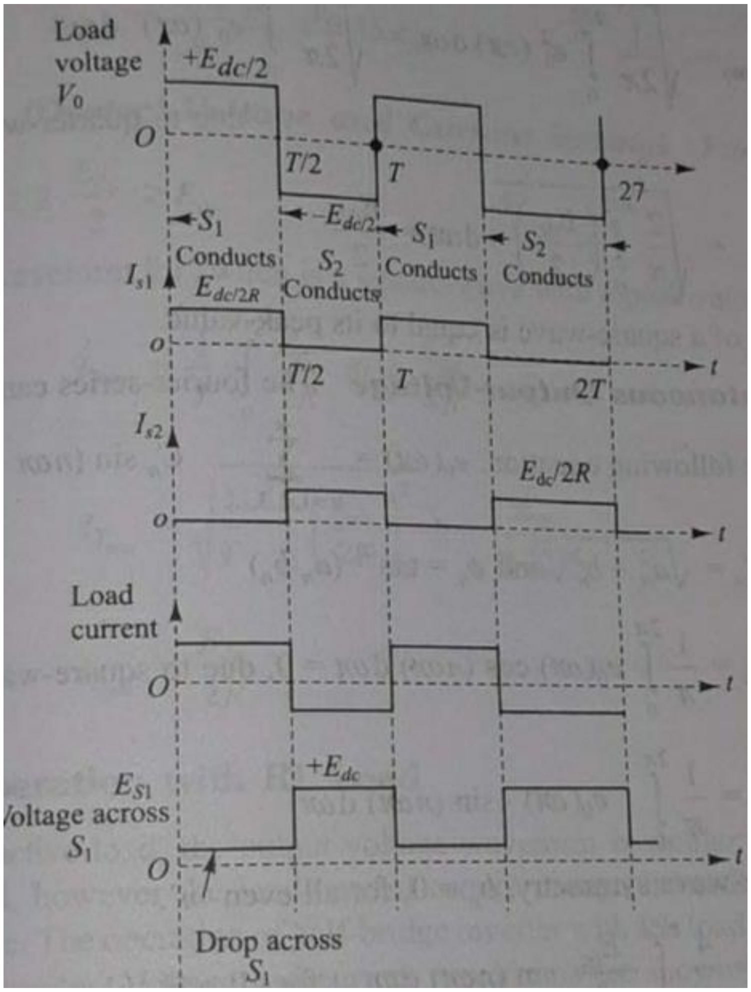
9.3.1 Operation with Resistive Load

The operation of the circuit can be divided into two periods:

(i) Period-I, where switch S is conducting from 01T72 and

(ii) Period-II, where switch S2 is conducting from T/2 sts T.

where T= 1/f and fis the frequency of the output voltage waveform. Figure 9.2 shows the waveforms for the output voltage and switch currents for a resistive-load



Switch S1 is closed for half-time period (T/2) of the desired ac output. It connects point p of the dc source to point A and the output voltage e, becomes equal to +Edc/2.

ALT= 1/2, gating signal is removed from S and it turns-off. For the next half-time period (T/2 <t<T), the gating signal is given to S2. It connects point N of the dc source to point A and the output voltage reverses. Thus, by closing S1 and S2 alternately, for half-time periods, a square-wave ac voltage is obtained at the output. With resistive load, waveshape of load current is identical to that of

Output voltage. Simply by controlling the time periods of the gate-drive signals, the frequency can be varied. Here diodes D1, and D2, do not play any role. The voltage across the switch when it is OFF is Edc. Gating circuit should be designed such that switches S1 and S2, should not turn-on at the same time.

9.3.2 Operation with RL Load

With an inductive-load, the output voltage waveform is similar to that with a resistive-load, however the load-current cannot change immediately with the output voltage. The operation of half-bridge inverter with RL load is divided into four distinct modes. Voltage and current waveforms are shown in Fig. 9.3. D1 and D2, are known as the feedback diodes.

Mode I (t1 < t < t2): S1 is turned-on at instant t1, the load voltage is equal to +Edc/2 and the positive load current increases gradually. At instant t2, the load current reaches the peak value. Switch S1 is turned-off at this instant. Due tonsame-polarity of load voltage and load current, the energy is stored by the load Fig. 9,4(a))

Mode II (t2<t<t3): Due to inductive-load, the load current direction will be maintained even-after S1, is turned-off. The self-induced voltage in the load will be negative. The load current flows through lower half of the supply and D2 as shown in Fig. 9.4(b). In this mode, the stored energy in load is fedback to the half of the source and the load voltage is clamped to – Edc/2.

Mode III (t3 < t<t4): At instant t3, the load-current goes to zero, indicating that a1, the stored energy, has been returned back to the lower half of supply. At instant t3, S2 is turned-on. This will produce a negative load voltage e0=-Edc/2 and a negative load current. Load current reaches a negative peak at the end this interval (Fig. 9.4(c)].

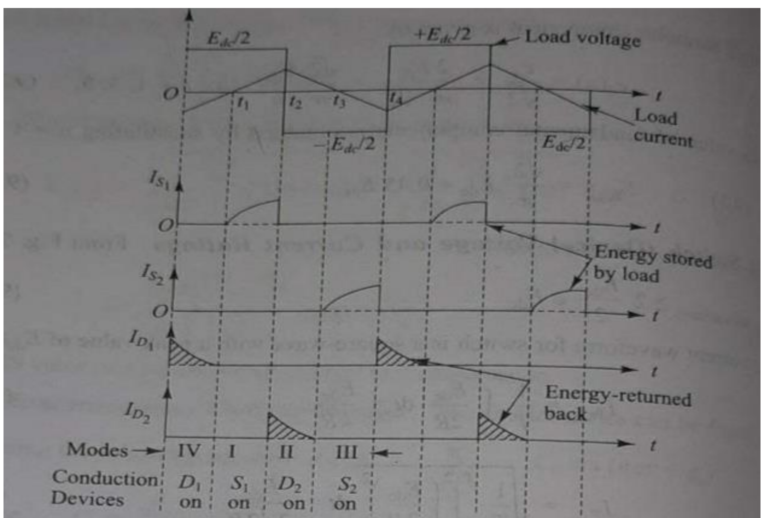


Fig. 9.3 *Voltage and current waveforms with RL load*

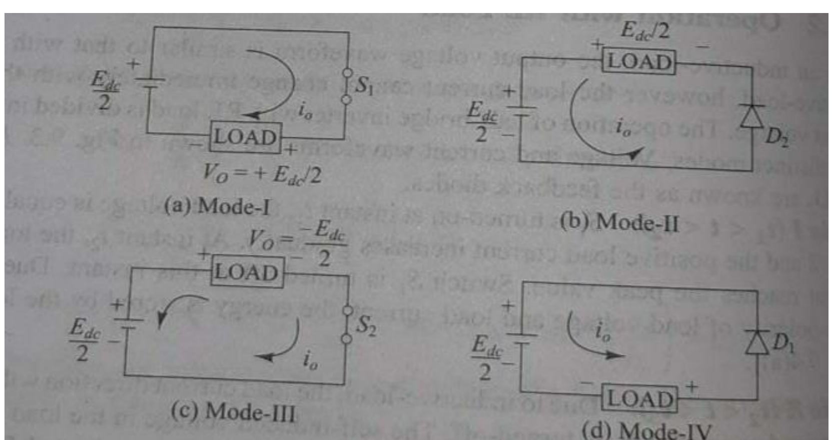


Fig. 9.4 *Operating modes*

Mode IV (to <t<t): Switch S2,is turned-off at instant t4 .The self induced voltage in the inductive load will maintain the load current. The load voltage changes its polarity to become positive Edc/2, load current remains negative and the stored energy in the load is returned back to the upper half of the dc source (Fig. 9.4(d).

At t_5, the load current goes to 0 and S_1 can be turned-on again. This cycle of operation repeats.

Circuit-Equations

(i) Instantaneous Current i_0:- With RL load, the equation for instantaneous current i_0 can be obtained from Eq. (9.2), as

$$i_0(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2\,E_{dc}}{n\,\pi\,\sqrt{R^2+(n\,\omega L)^2}} \sin(n\omega t - \theta_n) \qquad (9.9)$$

Here, $Z_n = \sqrt{R^2+(n\,\omega L)^2}$ is the impedance offered by the load to the n^{th} harmonic component, $\frac{2\,E_{dc}}{n\,\pi}$ is the peak amplitude of n^{th} harmonic voltage, and

$$\theta_n = \tan^{-1}\left(\frac{n\,\omega L}{R}\right) \qquad (9.10)$$

(ii) Fundamental Output Power: The output power at fundamental frequency ($n = 1$) is given by

$$P_{1_{rms}} = E_{1_{rms}} \cdot I_{1_{rms}} \cdot \cos\theta_1 = I_{1_{rms}}^2 \cdot R \qquad (9.11)$$

where $E_{1_{rms}}$ = RMS value of fundamental output voltage.

$I_{1_{rms}}$ = RMS value of fundamental output current

$\theta_1 = \tan^{-1}(\omega L/R)$

But

$$I_{1_{rms}} = \frac{2\,E_{dc}}{\sqrt{2}\cdot\pi\cdot\sqrt{R^2+(\omega L)^2}} \qquad (9.12)$$

$$P_{1_{rms}} = I_{1_{rms}}^2 \cdot R = \left[\frac{2\,E_{dc}}{\pi\cdot\sqrt{2}\,\sqrt{R^2+(\omega L)^2}}\right]^2 \cdot R \qquad (9.13)$$

$$= \left[\frac{4\,E_{dc}^2\cdot R}{2\pi^2\,(R^2+\omega^2 L^2)}\right] = \left[\frac{2\,E_{dc}^2\cdot R}{\pi^2\,(R^2+\omega^2 L^2)}\right] \qquad (9.14)$$

Importance of fundamental power is that in many applications such as electric motor drives, the output power due to fundamental current is generally the useful power and the power due to harmonic current is dissipated as heat and increases the load dissipation.

9.4 SINGLE-PHASE FULL-BRIDGE INVERTERS

Figure 9.5 shows the power diagram of the single-phase bridge inverter. The inverter uses two pairs of controlled switches (S1S2, and S3S4) and two pairs of diodes (D1, D2, and D3 D4). The devices of one pair operate simultaneously. In order to develop a positive voltage (+ E0) across the load, switches S1, and S2, are turned on simultaneously whereas to have a negative voltage (E) across the load, we need to turn on the switches S3, and S4. Diodes D1, D2, D3 and D4 are known as the feedback diodes.

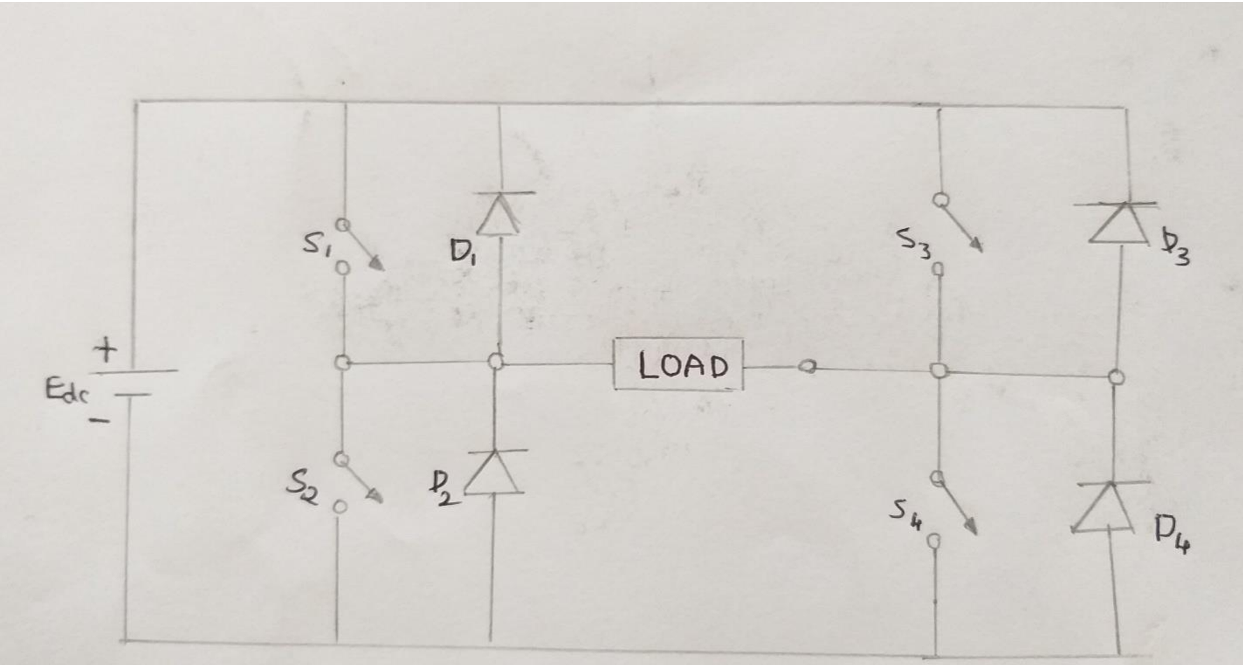


Fig 9.5 Single phase full bridge inverter

9.4.1 Operation with Resistive Load

Voltage and current waveforms with resistive-load are shown in Fig. 9.6. The bridge-inverter operates in two-modes in one-cycle of the output.

(a) Mode-I (0 < t <T/2): In this mode, switches S1 and S2 conducts simultaneously. The load voltage is +Edc and load current flows from P to Q. The equivalent circuit for mode-I is shown in Fig. 9.7(a). At t = T/2, S1 and S2 are turned-off and S3 and S4 are turned-on.

(ii) Mode-II (T/2 <t<T): At=1/2, switches S3 and S4 are turned-on and S1 and S2, are turned-off. The load voltage is - Edc and load current flows from Q to P. The equivalent circuit for mode-II is shown in Fig. 9.7

(b) At=T, S3 and S4 are turned-off and S1 and S2, are turned-on again.

As the load is resistive, it does not store any energy. Therefore, feedback diodes are not effective here.

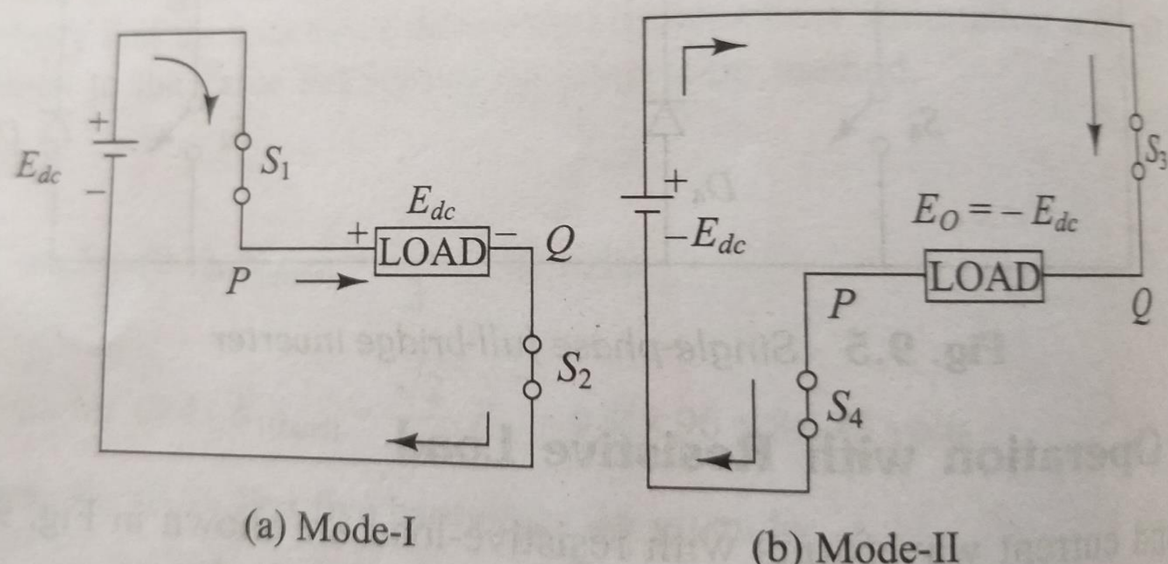


Fig. 9.7 *Equivalent circuit*

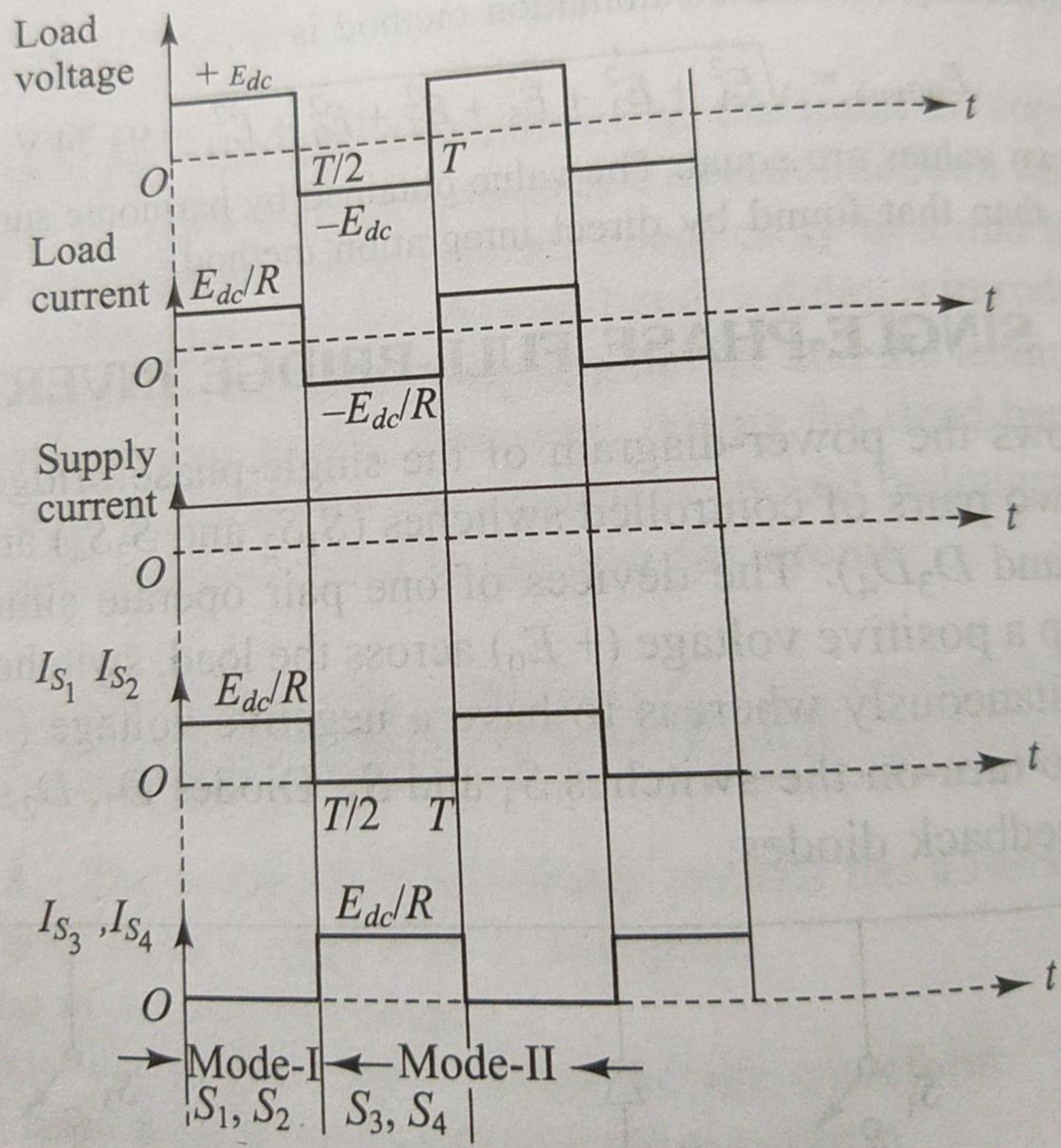


Fig. 9.6 *Voltage and current waveforms*