

clock C	Q_1	Q_2	Q_3	Q_4
-	0	0	0	0
-	0	0	0	0
-	0	0	0	0
-	0	0	0	0
-	1	1	1	0
-	0	1	1	1
-	0	0	1	1
mod 4	0	0	0	1

mod 4

Counting sequence

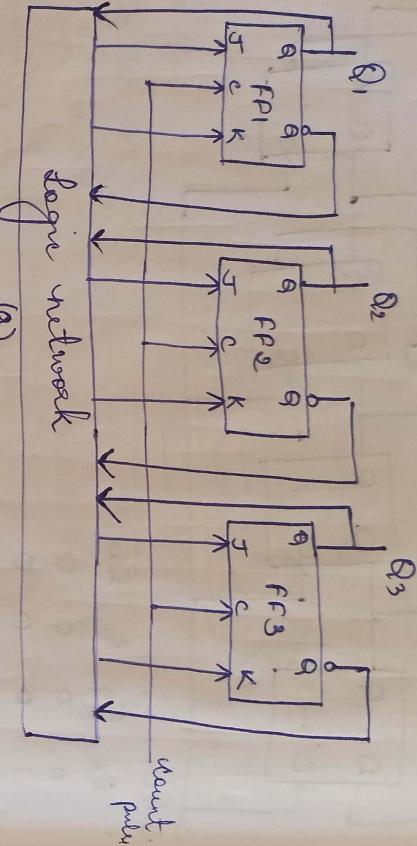
0 0 0 1
0 0 1 1
0 1 1 1
1 1 1 0

Design of Synchronous counters:
Counting sequence for mod 8 counter

	Q_1	Q_2	Q_3
0	0	0	0
0	0	1	0
0	1	0	0
0	1	0	1
1	0	1	0
1	0	0	1
0	0	1	1

Design of Asynchronous mod - 6 counter using clock J-K flip flop.
Consider a general structure assuming the use of clock J-K flip flop as shown below.

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(a)

Note: Explanation for the above structure is important.

a) → General structure of synchronous mod 6 counter using positive edge triggered T-K flip flops.

The below table shows the excitation table for Synchronous mod -6 counter using Dclock T-K flip flops.

Present state | Next state | flip flop inputs

Q_1	Q_2	Q_3	Q_1^+	Q_2^+	Q_3^+	J_1	K_1	J_2	K_2	J_3	K_3
0	0	0	0	1	0	0	-	1	-	0	-
0	1	0	0	-	-	-	-	0	-	1	-
0	-	-	-	-	-	-	-	-	-	-	-
1	-	0	-	0	-	-	-	0	-	-	-
-	0	-	0	-	-	-	-	-	-	-	-
0	-	0	0	-	-	-	-	-	-	-	-

The application table for clock $J-K$
flip flop.

Q	Q^+	J	K
0	0	0	-
0	-	1	-
-	0	-	1
1	1	-	0

From the above excitation table the inputs $J_1, K_2, J_2, K_2, J_3, K_3$ are derived from the above application table of clock $J-K$ flip flop.

J_1	Q_1	Q_2	Q_3	00	01	11	10
0	0	0	0	0	1	0	-
1	-	-	-	-	-	0	-

$$J_1 = \overline{Q_2} Q_3$$

K_1	Q_1	Q_2	Q_3	00	01	11	10
0	-	-	-	-	-	-	-
1	-	1	-	1	0	0	0

$$K_1 = \overline{Q}_2 \text{ or } Q_3$$

J_2	Q_1	Q_2	Q_3	00	01	11	10
0	-	0	-	-	-	-	-
1	-	0	-	-	-	-	-

$$J_2 = \overline{Q}_3$$

K_2	Q_1	Q_2	Q_3	00	01	11	10
0	-	-	-	-	-	-	-
1	-	-	-	-	-	-	-

$$K_2 = Q_1$$

J_3	Q_1	Q_2	Q_3	00	01	11	10
0	0	-	-	-	-	-	-
1	-	-	-	-	-	-	-

K_3	Q_1	Q_2	Q_3	00	01	11	10
0	-	1	1	-	-	-	-
1	-	0	-	-	-	-	-

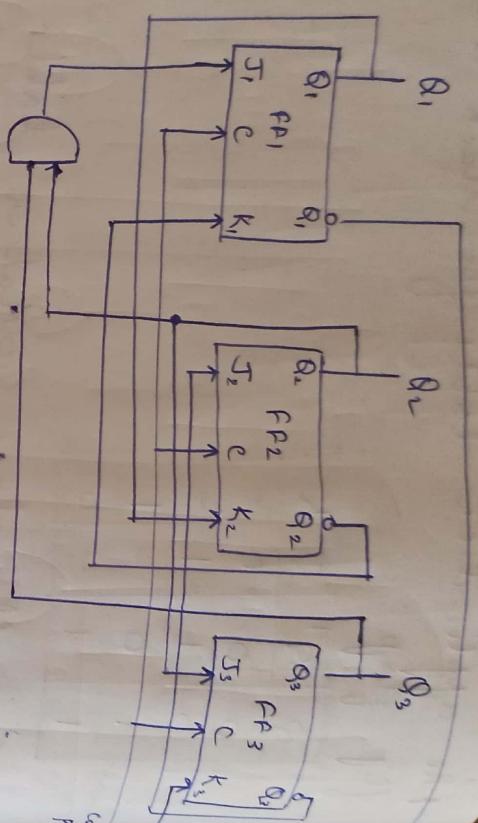
$$K_3 = \overline{Q}_1$$

$$J_3 = \overline{Q}_2$$

Write the application table for
 D flip flop

Q	Q^+	D
0	0	0
0	1	-
1	0	0
1	-	0

The initiation table for mod-6 counter using D flip flop

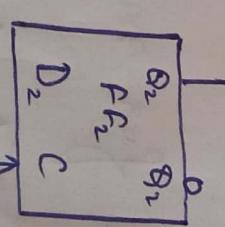
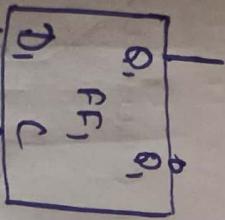


D_1	$Q_2 Q_3$	Q_1	D_1
0	00	01	10
0	01	11	10
-	10	0	10
0	11	1	10

$$D_2 = \overline{D}_2 \overline{D}_3 + \overline{D}_1 D_2$$

	D_1	\overline{D}_1
D_2	00	01
\overline{D}_2	11	10

$$D_1 = \overline{Q_1 Q_2} + \overline{Q_2 + Q_3}$$



Count

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Application table for 7-flip flop

Q Q^+ T

0	0	0
0	1	1
1	0	1
1	1	0
0	0	0
0	1	0
0	1	1
1	1	0
0	0	1
0	1	0
0	1	1
1	0	0
0	0	1
0	1	0
0	1	1
1	0	0

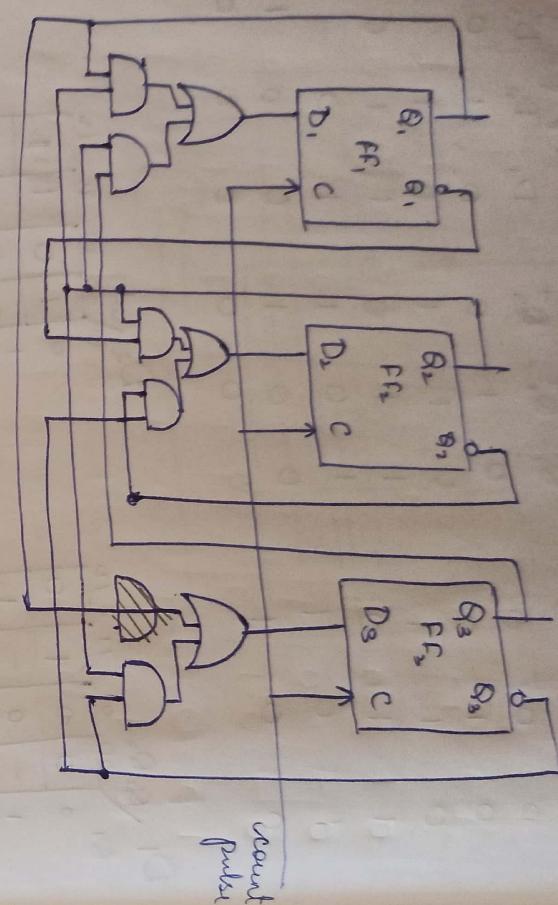
Excitation table for mod-6 counter using
7 flip flop.

present state

next state
 Q_1^+ Q_2^+ Q_3^+

Q_1 Q_2 Q_3

0	0	0	0	0	1	0
0	0	0	0	1	0	1
0	1	0	0	1	0	0
0	1	1	1	1	0	1
1	1	0	1	0	0	0
0	0	1	0	0	1	0
0	1	0	0	1	0	1
0	1	1	0	0	1	0
1	0	0	1	0	0	1
0	0	1	1	1	0	0



count
pulse

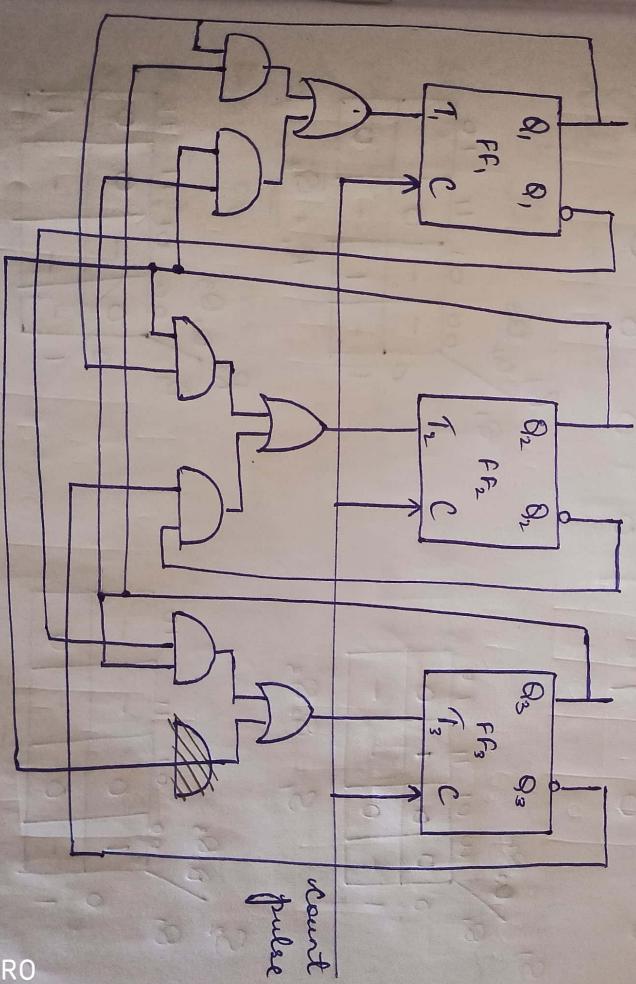
T_3	$Q_1 Q_2$	$Q_2 Q_3$	$Q_1 Q_3$	$\bar{Q}_1 \bar{Q}_2$	$\bar{Q}_2 \bar{Q}_3$	$\bar{Q}_1 \bar{Q}_3$
0	0 0	0 0	1 1	1 0	1 0	1 0
0	0 0	0 1	1 1	1 0	0 0	0 0
1	1 0	1 1	1 0	0 1	0 1	0 1

$$T_1 = Q_1 Q_3 + Q_2 Q_3$$

$$T_2 = \bar{Q}_2 \bar{Q}_3 + Q_1 Q_2$$

T_1	$Q_2 Q_3$	$Q_1 Q_3$	$Q_1 Q_2$	$\bar{Q}_2 \bar{Q}_3$	$\bar{Q}_1 \bar{Q}_3$	$\bar{Q}_1 \bar{Q}_2$
0	0 0	0 0	1 1	1 0	1 0	1 0
0	0 0	0 1	1 1	1 0	0 0	0 0
1	1 0	1 1	1 0	0 1	0 1	0 1

$$T_3 = Q_2 + \bar{Q}_1 Q_3$$



Application table for SR flip flop

Q	Q^+	S	R
0	0	0	-
0	0	1	0
1	1	1	0
1	0	0	1



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Excitation table for
using SR flip flop
Present state Next state
 $S_1 Q_1$ $S_2 Q_2$ $S_3 Q_3$
 Q_1^+ Q_2^+ Q_3^+
 $S_1 R_1$ $S_2 R_2$ $S_3 R_3$

0	0	0	0	1	0	0	0	-1	0
0	0	0	0	0	1	-1	0	-1	0
0	0	0	0	0	0	1	-1	0	-1
0	0	0	0	0	0	0	1	-1	0
0	0	0	0	0	0	0	0	1	-1
1	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	1

S_1		
$Q_1 Q_2 Q_3$		
Q_1	00	01
0	0	1
0	0	1
1	0	-
-	0	-

$$S_1 = Q_2 Q_3$$

S_2		
$Q_1 Q_2 Q_3$		
Q_1	00	01
0	1	-
0	1	-
1	0	-
-	0	0

$$S_2 = \bar{Q}_2 \bar{Q}_3$$

R_1		
$Q_1 Q_2 Q_3$		
Q_1	00	01
0	-	0
0	-	0
1	-	-
-	-	-

$$R_1 = \bar{Q}_2$$

R_2		
$Q_1 Q_2 Q_3$		
Q_1	00	01
0	0	0
0	0	0
1	-	-
-	-	-

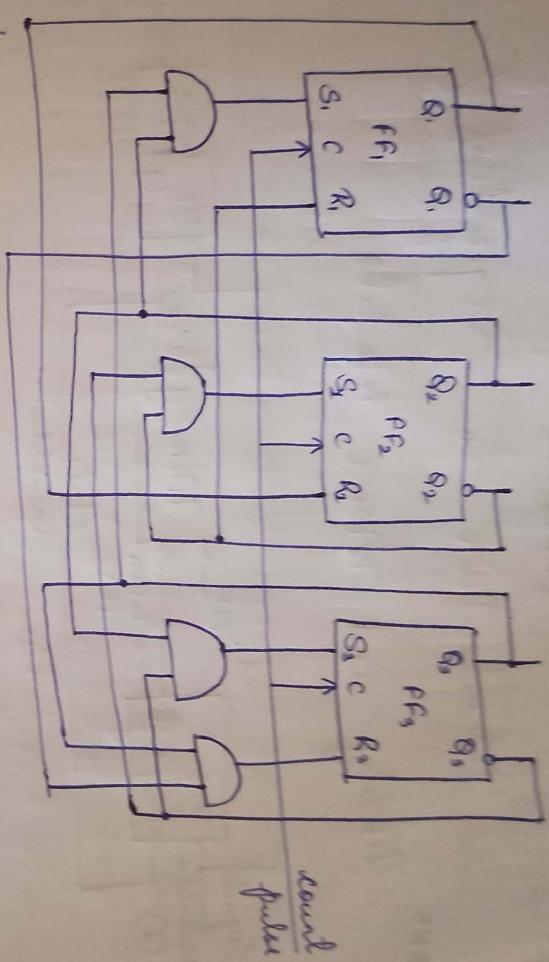
$$R_2 = \underline{\underline{Q_1}}$$

S_3		
$Q_1 Q_2 Q_3$		
Q_1	00	01
0	0	0
0	0	0
0	0	0
1	1	1

R_3		
$Q_1 Q_2 Q_3$		
Q_1	00	01
0	-	1
1	1	1
0	0	0
0	0	0

Self Correction Counters

The counter in which all the states are not included in original counting sequence eventually leads to normal counting sequence after one or more count pulse. Once one or more control inputs C is said applied to control inputs C is said to be self correcting counters to be self correcting counters to avoid having counter hangup if it should be always self correcting

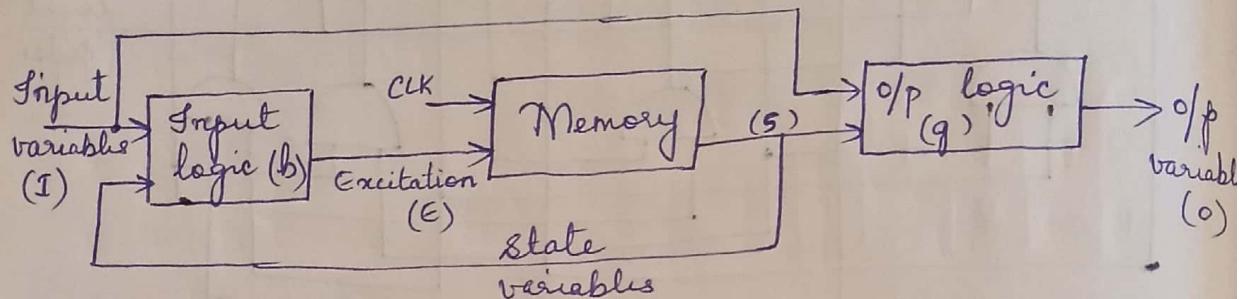


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Module - 4

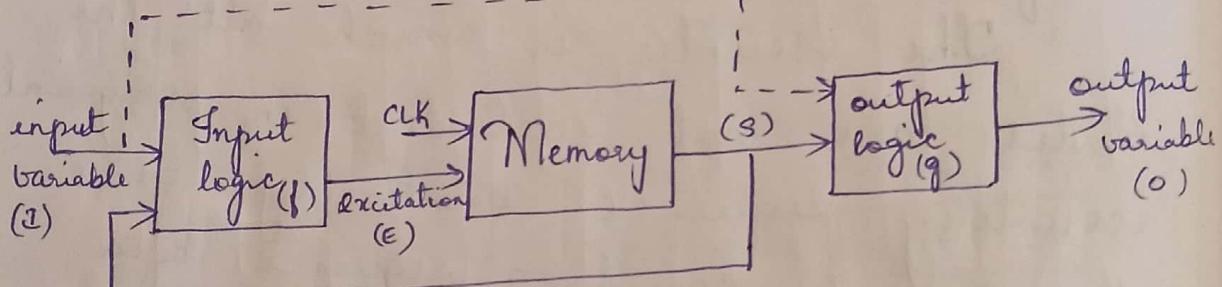
Introduction to Sequential Circuits

*** Mealy and Moore Models:



Mealy Sequential circuit Model.

(dotted lines means not connected)



Mealy Sequential circuit model

The logic functions shown in model diagrams translate into input and flip flop output information. The input logic produces excitation inputs to the flip flop and output logic converts input and flip flop data to satisfy the output variable requirements.

In a mealy machine the internal input variables (I) and state variables (S) are applied to the

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output logic function (g) to generate output (o). A memory circuit output is dependent only on state variables.

(3)

State machine notation

Input variables

All variables that originate outside sequential machine are said to be input variables.

Output variables:

All variables that exit the sequential machine are output variables.

State variables:

The output of memory (flip flop) defines the state of sequential machine. These are the flip flop output.

Excitation variable:

There are inputs to memory when flip flop are used for system memory, the excitation variables are inputs (J, K, S, R, D, T) to flip flop.

State:

The state of sequential machine is defined by content of memory (Q output). State variables and state are related

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 $x^2 = y$ where

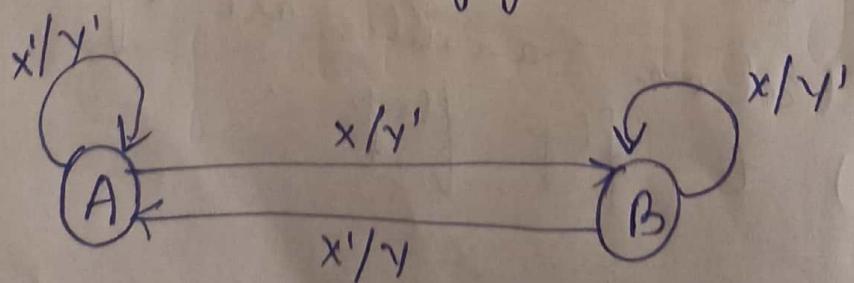
$x \rightarrow$ number of state variables
(flip flop) and
 $y \rightarrow$ maximum number of states
possible

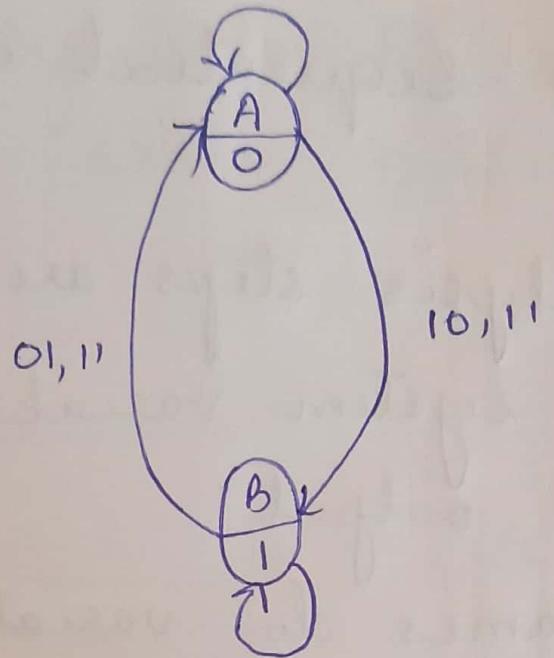
Present State, next state:

The status of all variables at some time (t) before the next clock edge represents present state. The status of all state variables at some time ($t+1$) represents next state.

State diagram:

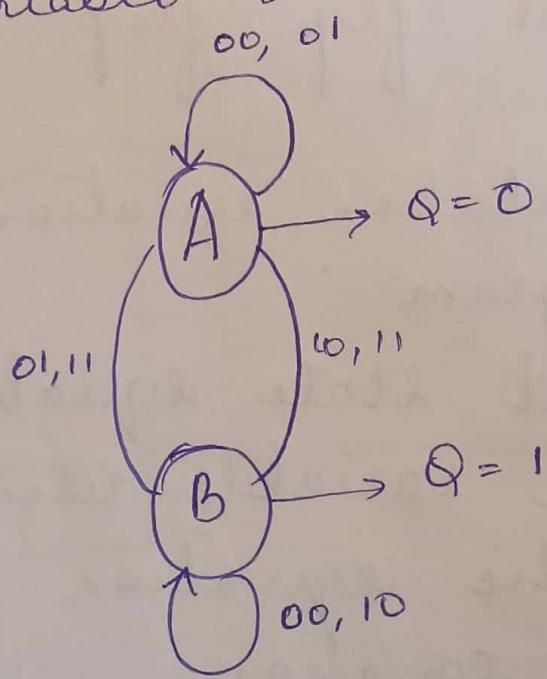
It is a graphical representation of sequential circuit where individual states are represented by circle with an identifying symbol located inside changes from state to state to are indicated by directed arcs as shown in the figure below.





(Explanation
text book)

- a) Output variable written under state variable name.



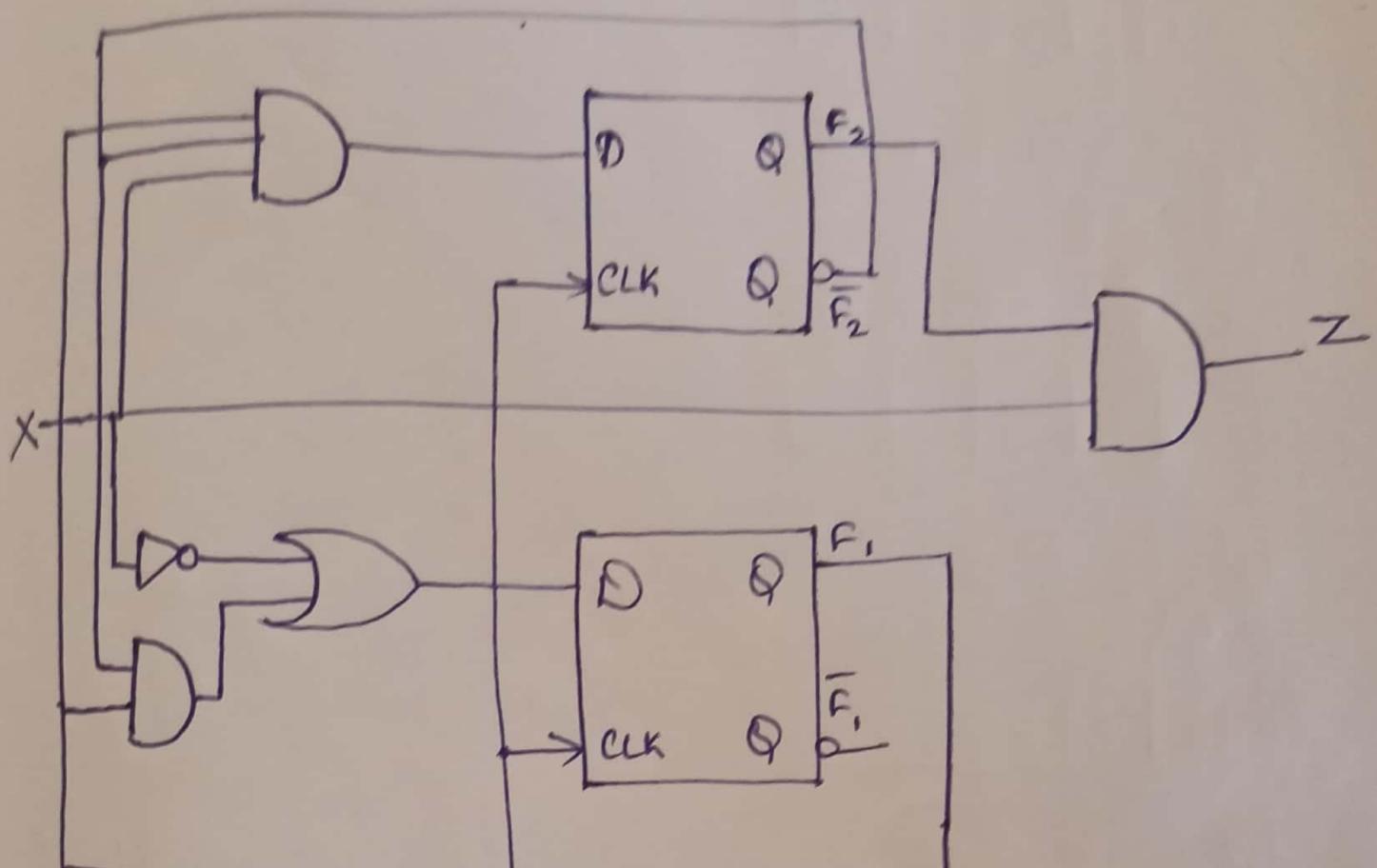
- b) Output variables indicated by notation
clocked are moore circuit notation
of JK flip flop.

Synchronous sequential circuit analysis

The analysis steps are as follows

- * Determine system variables, input state and output
- * Assign names to variables
- * Determine the flip flop type - write characteristic equation as needed for flip flop used in circuit.
- * Write excitation equation from logic diagram
- * Write next state equation for each state variable using characteristic equation and circuit excitation equation
- * Write output variables equation
- * Construct transition table identify

Design symbols to state and construct state table or state diagram.



11119

$$D_2 = \bar{F}_2 F_1 X$$

f_2 \ $f_1 X$

	00	01	11	10
0	0	0	1	0
1	0	0	0	0

$$D_1 = \bar{X} + \bar{F}_2 F_1$$

f_2 \ $f_1 X$

	00	01	11	10
0	1	0	1	1
1	1	0	0	1

F_2^+ \ $f_1 X$

	00	01	11	10
0	0	0	1	0
1	0	0	0	0

F_1^+ \ $f_1 X$

	00	01	11	10
0	1	0	1	1
1	1	0	0	1

Z \ $f_1 X$

	00	01	11	10
0	0	0	0	0
1	0	1	1	0

from the canonical next state equation we construct transition table as shown below:

In the case of D flip flop, it is also the excitation table.

Present state		Next state xyz					
		0			1		
F_2	F_1	F_2	F_1	Z	F_2	F_1	Z
0	0	0	1	0	0	0	0
0	1	0	1	0	1	1	0
1	0	0	1	0	0	0	1
1	1	0	1	0	0	0	1

Transition and excitation table:

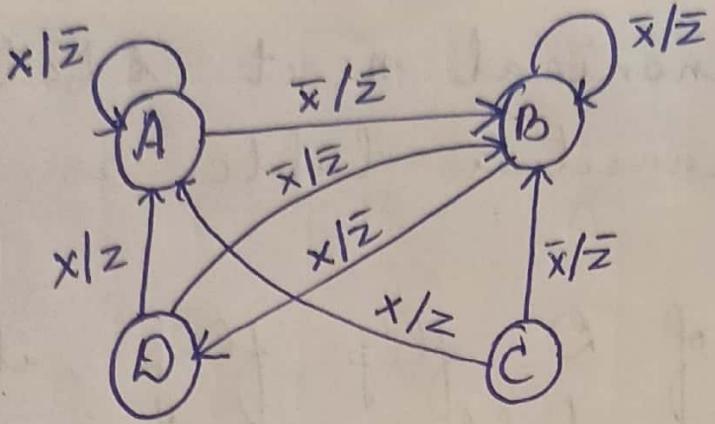
The S Assign state table symbols and construct a state table or diagram.
let the state symbols be

State	F_2	F_1
A	0	0
B	0	1
C	1	0
D	1	1

State diagram is constructed from the table given below.

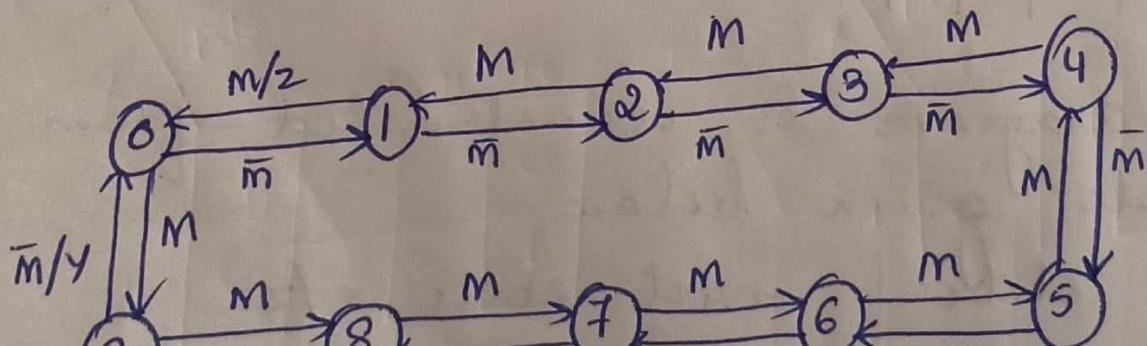
Present state | next state xyz

Present state	0	Z	1	Z
A	B	0	A	0
B	B	0	D	0
D	B	0	A	1



Construction of state diagrams

- 1) Create the state diagram for a synchronous decade counter, the counter used to count up or down in binary depending on the value of mod control input signal M. When $M=0$ the counter should count up and when $M=1$ it should count down. The counter output Y is to be 1 if counting up else and terminal count is reached another output Z is to be one at the terminal count if counting down.



5/11/19
 1) Design a Synchronous circuit using positive edge triggered JK flip flop with minimal combinational gating to generate the following sequence

0 - 1 - 2 - 0 if input $x = 0$ &
 0 - 2 - 1 - 0 if input $x = 1$
 provide an output which goes high
 to indicate non-zero states in the
 0-1-2-0 sequence. Is this a mealy
 machine.

Excitation table:

Input	Present state		Next state		Flip flop outputs			
	A	B	A^+	B^+	J_A	K_A	J_B	K_B
x								Z

Input	Present state		Next state		Flip flop inputs				Output	
X	A	B	A ⁺	B ⁺	J _A	K _A	J _B	K _B	-	
0	0	0	0	1	0	-	1	-	0	0
0	0	1	1	0	1	-	-	-	1	1
0	1	0	0	0	0	-	1	0	-	1
0	1	1	-	-	-	-	-	-	-	-
1	0	0	1	0	0	1	-	0	-	0
1	0	1	0	0	0	0	-	-	1	0
1	1	0	0	1	-	-	1	-	1	0
1	1	1	-	-	-	-	-	-	-	0

check power
state ↓

J_A

		AB	
		00	01
X		00	1
0	0	1	-
1	1	0	-

$$\begin{aligned} J_A &= \bar{X}B + X\bar{B} \\ &= \underline{\underline{X \oplus B}} \end{aligned}$$

J_B

		AB	
		00	01
X		00	1
0	0	1	-
1	0	-	1

$$\begin{aligned} J_B &= \bar{X}\bar{A} + XA \\ &= \underline{\underline{X \oplus A}} \end{aligned}$$

K_A

		AB	
		00	01
X		00	1
0	0	-	-
1	0	-	1

$$K_A = 1$$

K_B

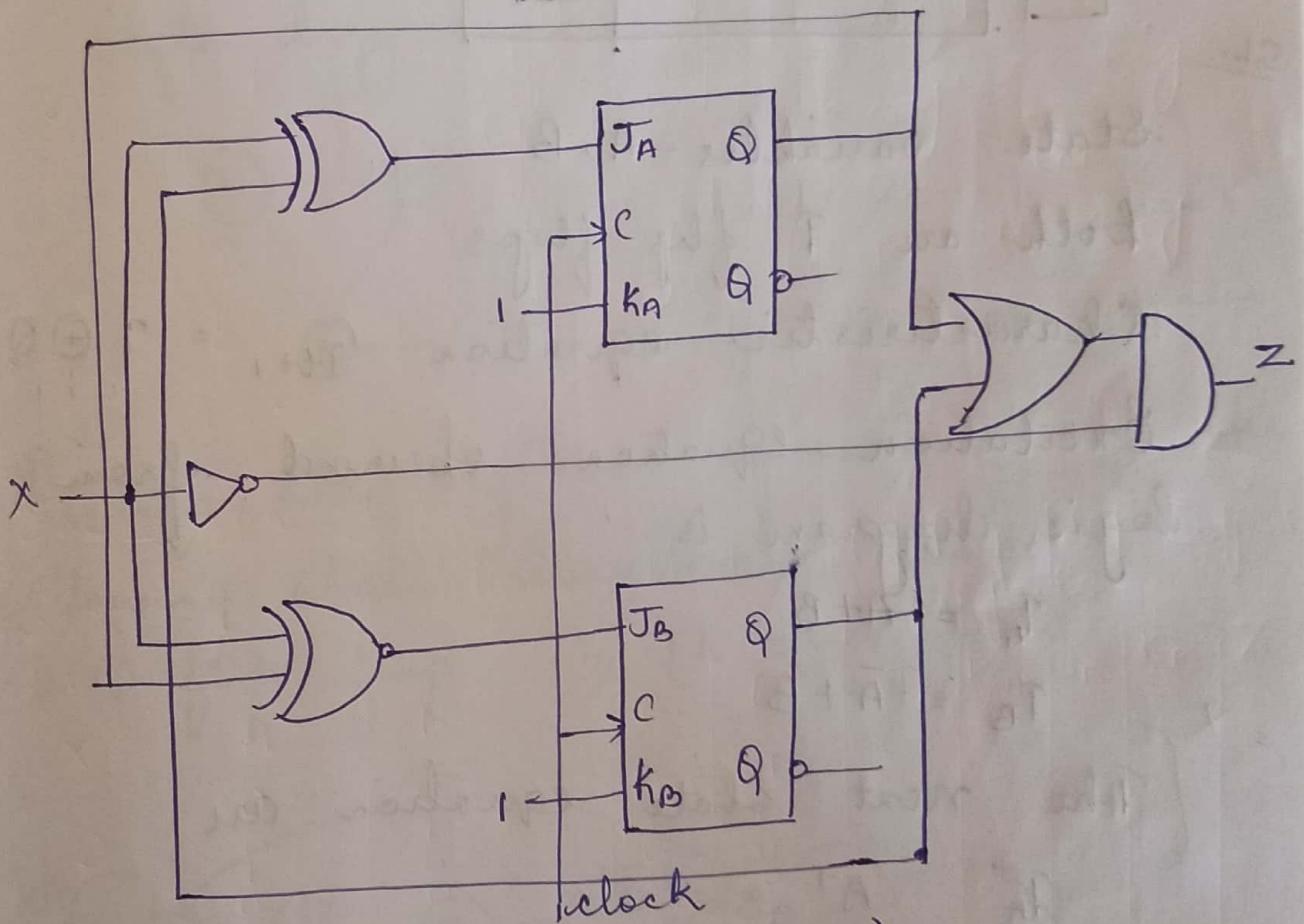
		AB	
		00	01
X		00	1
0	0	1	-
1	0	-	-

$$K_B = 1$$

Z

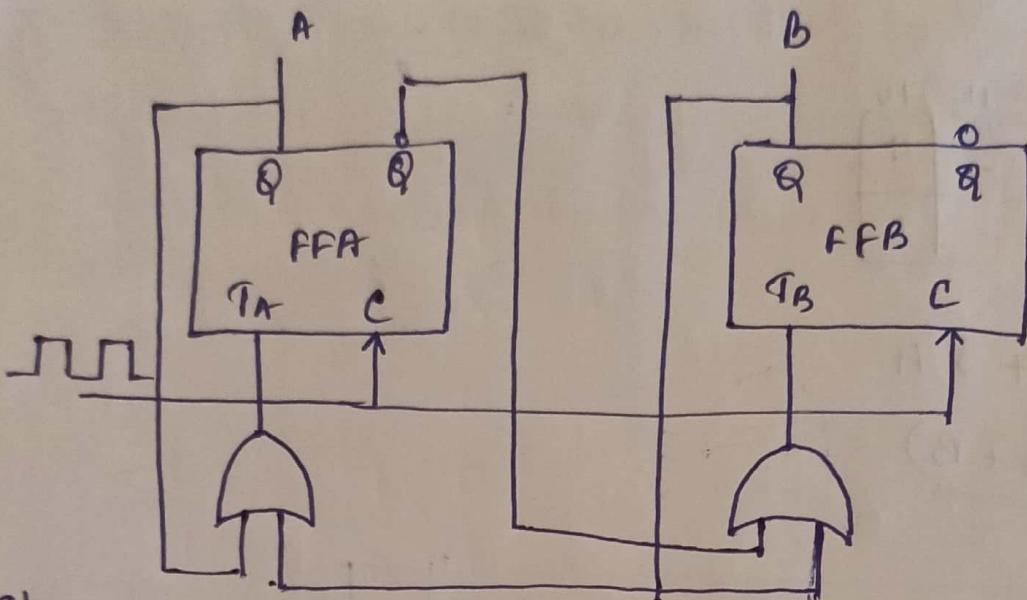
	A\B	00	01	11	10
0	0	1	-	1	0
1	0	0	-	0	

$$Z = \bar{X}B + \bar{X}A \\ = \bar{X}(A + B)$$



Since $Z = f(Q_A, B) = \bar{X}(A + B)$
It is a mealy machine.

Analyse the following synchronous
Mealy machine.



Solu.

State variables - A, B

both are T flip flops

Characteristic equation $Q_{t+1} = T \oplus Q$

Excitation equation observed from logic diagram is :

$$T_A = A + B$$

$$T_B = \bar{A} + B$$

The next state equation are

$$\begin{matrix} T_A \\ T_B \end{matrix} \quad \begin{matrix} \bar{A}^+ \\ B^+ \end{matrix} =$$

$$\begin{matrix} T_A \\ T_B \end{matrix} \quad \begin{matrix} \bar{A}^+ \\ B^+ \end{matrix} =]$$

T_A	B	0	1
0	A	0	1
1	B	1	0

T_B	B	0	1
0	A	1	1
1	B	0	1

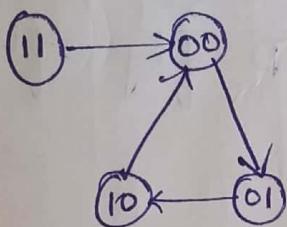
$$T_B = \bar{A} + B$$

T	Q^+	Present state		Next state		Flip flop outputs	
		A	B	A'	B'	T_A	T_B
0	Q	0	0	0	01	0	1
1	\bar{Q}	0	1	1	0	1	1
		1	0	0	0	1	0
		1	1	0	0	1	1

deactivation table

Transition table

State diagram:



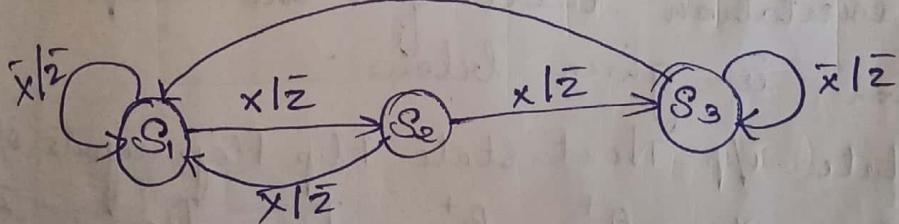
T_B

(mod 4)

self correction counter

Realize the system represented by the following state diagrams using
 i) D flip flop ii) JK flip flop.

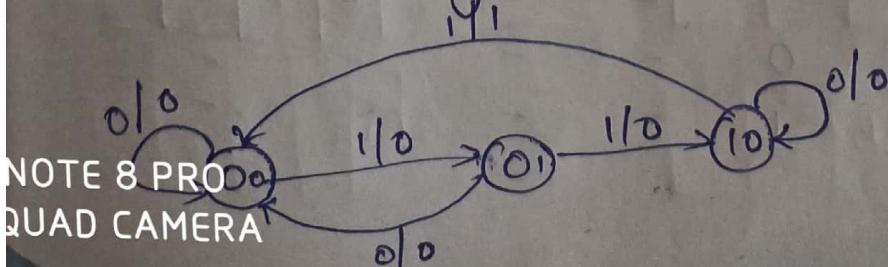
x/z



Solution: There are 3 states S_1, S_2, S_3
 Let the state assignment be $S_1 = 00$
 $S_2 = 01$
 $S_3 = 10$

Let the state be called AB

the state diagram now becomes.



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State transition table

below:

Present state i/p			Next state		Output
A	B	X	A ⁺	B ⁺	Z
0	0	0			
0	1	0			
1	0	1			
-	-	1			

Excitation table for D flip flop is given below

Q	Q ⁺	D
0	0	0
0	1	1
1	0	0
1	1	1

The excitation table for the required transition is given below.

Present state i/p			Next state		Flip flop inputs		o/p
A	B	X	A ⁺	B ⁺	D _A	D _B	Z
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	0	0	0	0	0
0	1	1	1	0	1	0	0
1	0	0	1	0	1	0	0
1	0	1	0	0	0	0	1
1	1	0	-	-	-	-	-
1	1	1	-	-	-	-	-

D_A	A	Bx	00	01	11	10
	0		0	0	1	0
	1		1	0	-	-

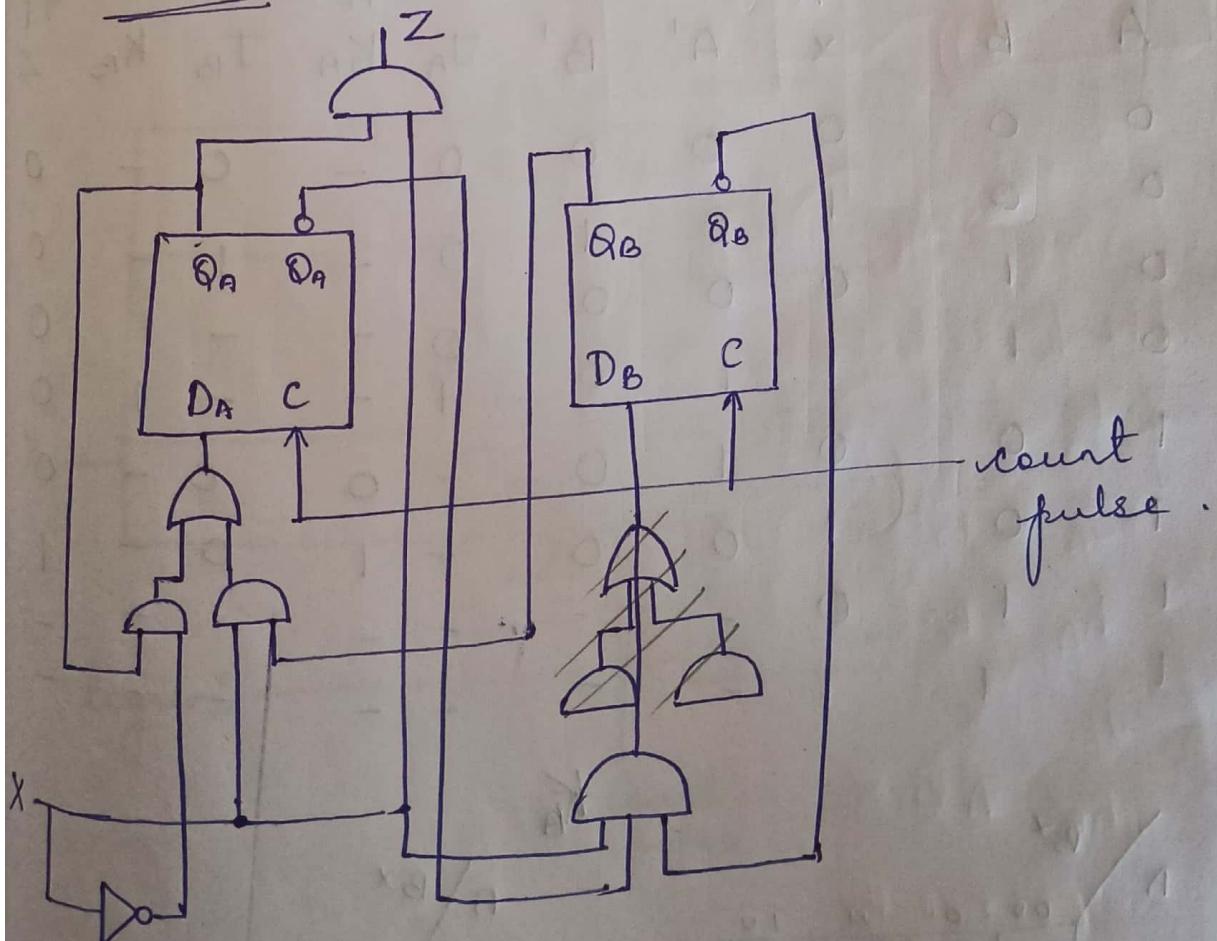
$$\underline{D_A} = \underline{A} \bar{x} + Bx$$

D_B	A	Bx	00	01	11	10
	0		0	1	0	0
	1		0	0	-	-

$$D_B = \underline{\underline{A}} \bar{B} x$$

Z	A	Bx	00	01	11	10
	0		0	0	0	0
	1		0	1	-	-

$$\underline{Z} = \underline{\underline{A}} X$$



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JK flip flop:

Excitation table for JK flip flop.

Q	Q ⁺	J	K
0	0	0	-
0	1	1	-
1	0	-	1
1	1	-	0

Excitation table required for transition is given below

Present state i/p		Next state		F/F i/p's		o/p Z			
A	B	X	A ⁺	B ⁺	J _A	K _A	J _B	K _B	
0	0	0	0	0	0	-	0	-	0
0	0	1	0	1	0	-	1	-	0
0	1	0	0	0	0	-	-	1	0
0	1	1	1	0	1	-	-	1	0
1	0	0	1	0	-	0	0	-	1
1	0	1	0	0	-	1	0	-	1
1	1	0	-	-	-	-	-	-	-
1	1	1	-	-	-	-	-	-	-

J _A	B ⁺			
	00	01	11	10
0	0	0	0	0
1	-	-	-	-

A	B ⁺			
	00	01	11	10
0	-	-	-	-
1	0	1	-	-

J_B

		00	01	11	10
		0	1	-	-
P	0	0	0	-	-
I	1	0	0	-	-

K_B

		00	01	11	10
		0	-	1	1
A	0	-	-	-	-
I	1	-	-	-	-

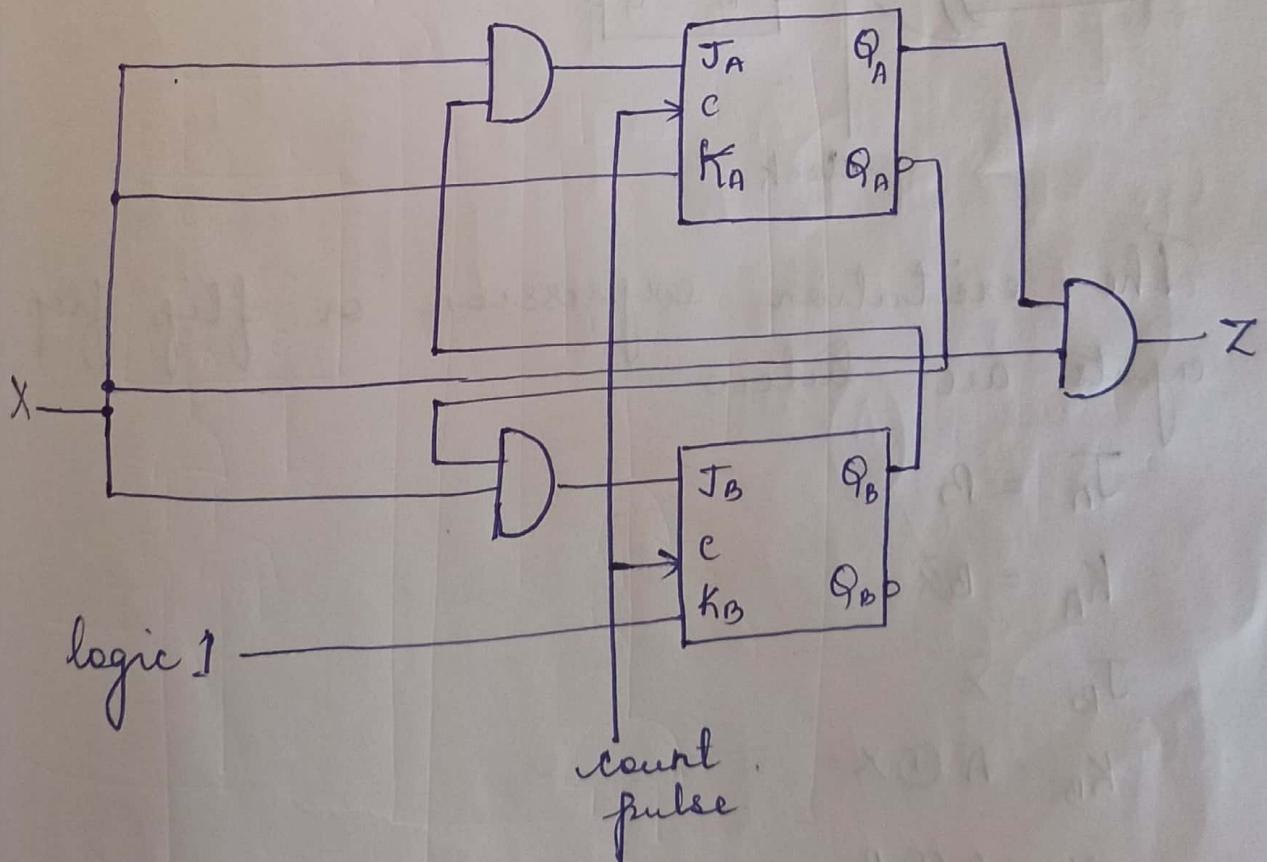
$$\underline{J_B = \bar{A}X}$$

$$K_B = 1$$

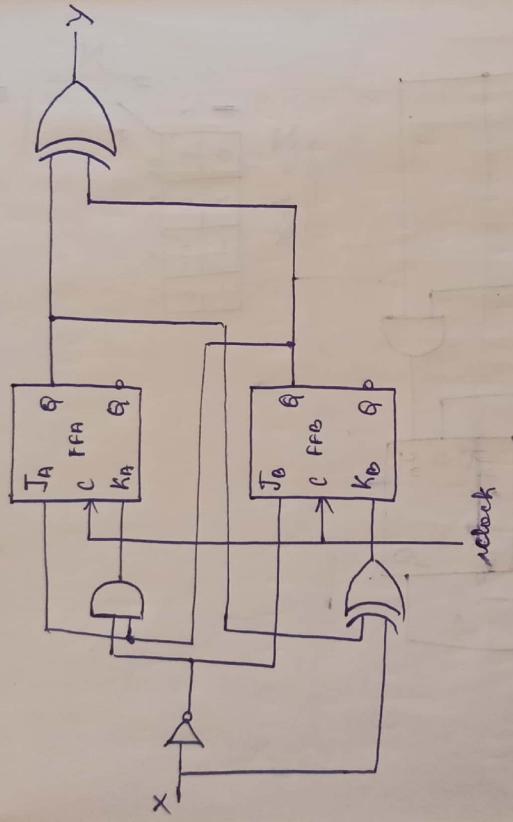
Z

		00	01	11	10
		0	0	0	0
A	0	0	0	0	0
I	1	0	0	-	-

$$\underline{Z = AX}$$



Construct the excitation table, transition table, state stable and state diagram for the Moore Sequential circuit shown below.



The excitation expression or flip flop inputs are below

$$J_A = B$$

$$K_A = B\bar{X}$$

$$J_B = \bar{X}$$

$$K_B = A \oplus X$$

$$Y = A \oplus B$$

J_A

$B\bar{X}$	00	01	11	10
0	0	0	1	1
1	0	0	1	1

K_A	$B\bar{X}$	00	01	11	10
0	0	0	0	1	1
1	0	0	0	1	1

				-
		0	0	1
		0	0	0
		0	1	0
		0	0	0

K_B

				-
		0	0	1
		0	0	0
		0	1	0
		0	0	0

0 0 0 0 0

				-
		0	0	1
		0	0	0
		0	1	0
		0	0	0

Y

Design a sequence counter.

1) Draw the state diagram of a Moore machine to output a one if the if has been one for 3 consecutive clock cycles.

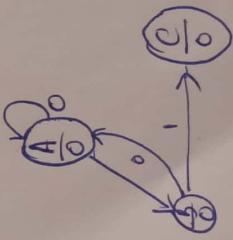
Solution: Let input be x and output be z . A sample input-output sequence is shown below.

x	0	1	1	1	1	1	0	1	1	1	0
z	0	0	0	0	1	1	1	0	0	0	0

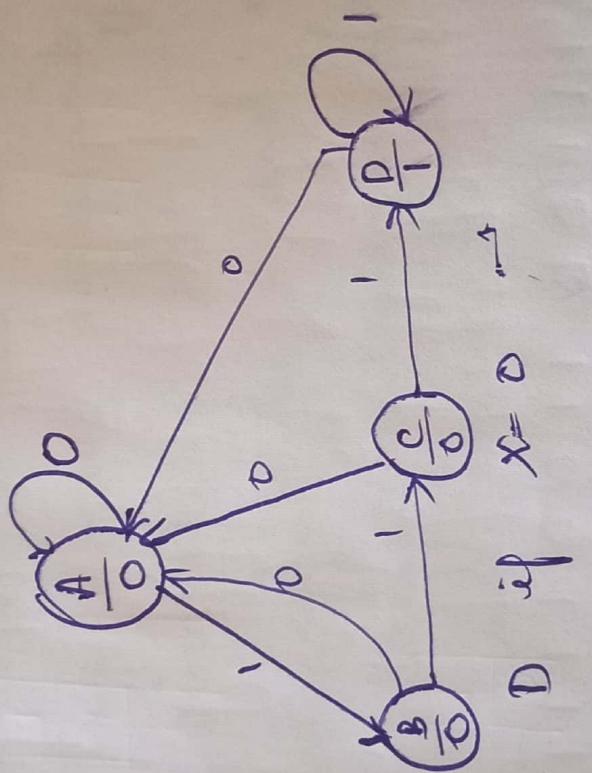
Step 1: Start at State A. If $x = 0$ remain at A implies zero 1's. Go to State B implying the occurrence of 1 as shown below.



Step 2: At B if $x = 0$



Step 3: At C if $x=0$ do to A else
next state



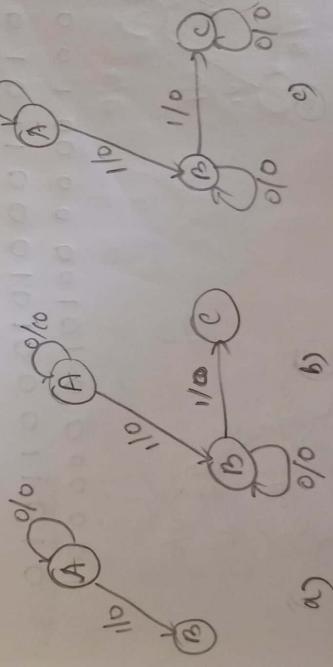
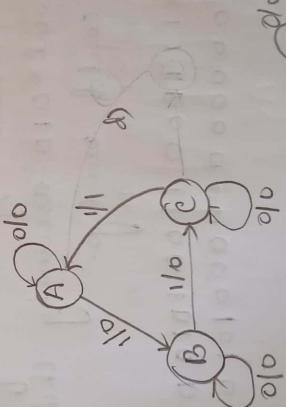
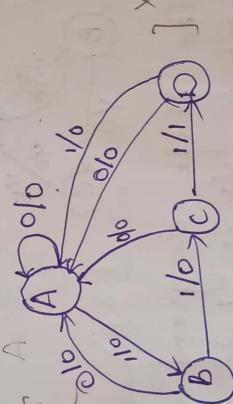
Step 4: At D if $x=0$ 1

Draw the state diagram of a Mealy machine whose output is one for every odd input being 1 and necessarily consecutive but non overlapping:

Solution: Let input be x and output be
2. The sample sequence for the problem is given below.

$$\begin{array}{l} x \ 0 \ 1 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 1 \\ z \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 \end{array}$$

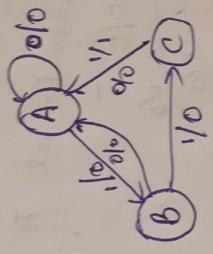
Step 1: At State Start at A, if $x=0$



3) Draw the state diagram of a Mealy machine whose op is 1 if the last 3 cycles but now overlapping

Solution: Let x be the input and z be the output.

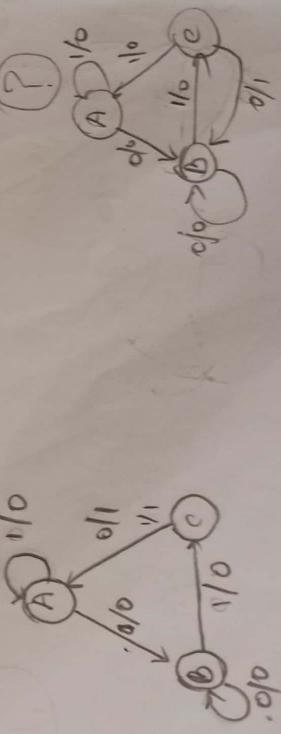
$$\begin{array}{l} x \ 001110011001111100 \\ z \ 00001000000000100100 \end{array}$$



4) Draw the state diagram of a Mealy machine whose op is 1, if last three inputs were 010 assuming that the sequence could overlap.

$$\begin{array}{l} x \ 001110001100101001100 \\ z \ 0000000000000101000000 \end{array}$$

$$\begin{array}{l} x \ 1010110000101000011010 \\ z \ 00010000001010000001 \end{array}$$



Design a sequence detector circuit in
that any input sequence ending in
will produce an output $x = 1$
coincident with the last one.

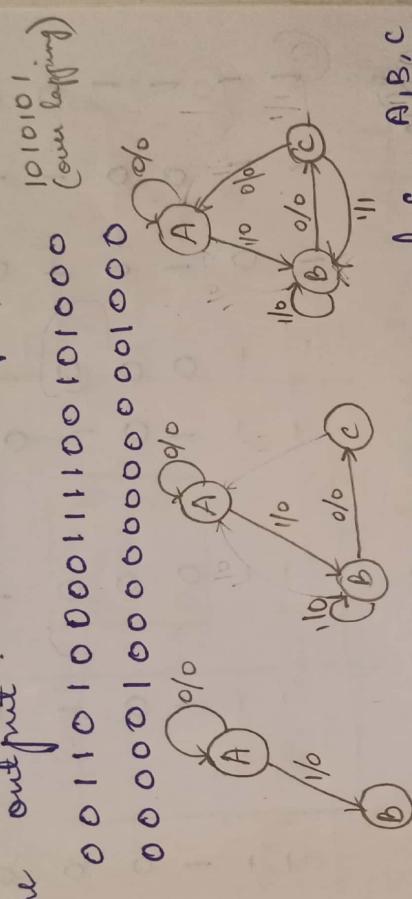
Solution: Let x be the input and x be
the output.

1010101
(overlapping)

$x \quad 00110100001100101000$

$\times \quad 0000010000000000001000$

$= \quad 000000000000000000000000$



There are 3 states s_1, s_2 and s_3 .
 $s_1 = A, s_2 = B, s_3 = C$

Present state Next state Output
 $x=0$ $x=1$ $x=0$
A B 0
B C 0
C A 1

Present state Next state Output
 $x=0$ $x=1$ $x=1$
A B⁺ Z
B A⁺ Z
C A⁻ Z

Present state		Next state		Flip flop inputs output	
A	B	A^+	B^+	D_A	D_B
0	0	0	0	0	0
0	0	1	0	0	1
0	0	0	1	1	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	0	1
1	1	0	-	-	-
1	1	1	-	-	-

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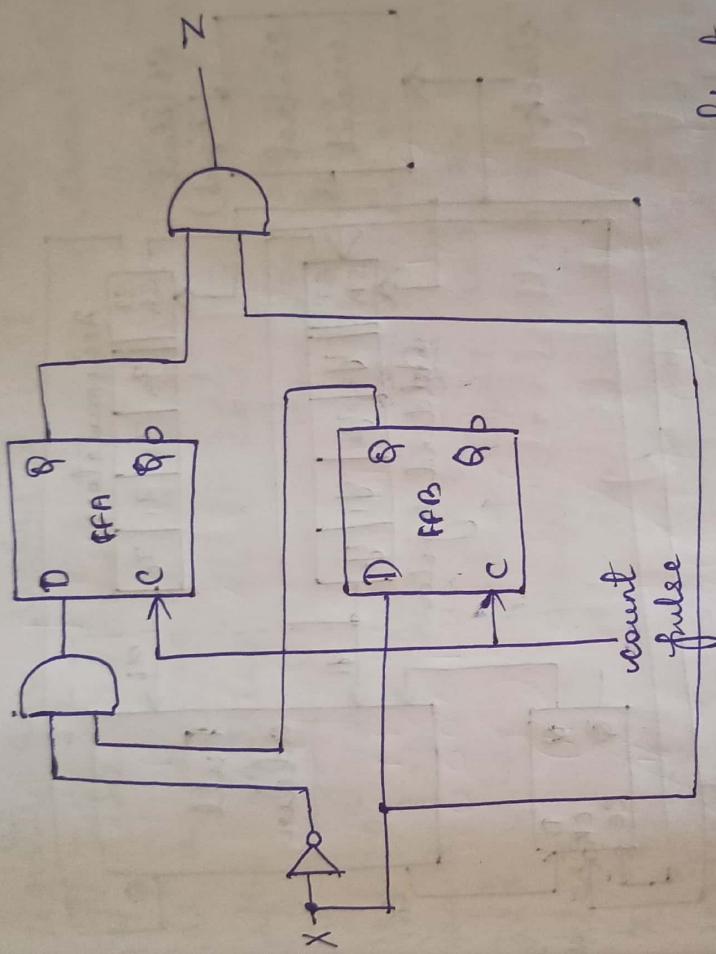
Q_A		B^X		D_A	
A	B^X	00	01	11	10
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	-	-	-	-

$$D_A = B\bar{X}$$

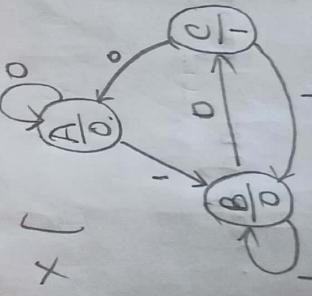
Z		B^X		A	
00	01	11	10	0	1
0	0	1	0	0	1
0	1	0	1	1	0
1	0	-	-	-	-

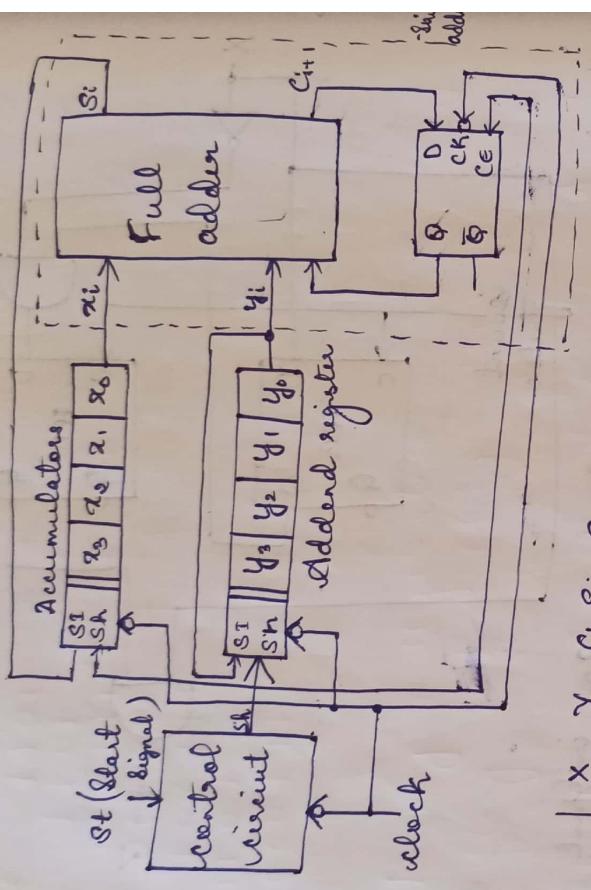
Q_B		B^X		D_B	
A	B^X	00	01	11	10
0	0	0	1	1	0
0	1	0	0	0	1
1	0	1	0	1	-
1	1	-	-	-	-

$$D_B - D_B = X$$



A circuit should produce an output of 1 only if an input sequence ending in 101 is detected (as a Moore machine) as shown (pg 159 - 163)





	X	Y	C _i	S _i	C _{i+1}
t ₀	011 0111	0	0	1	
t ₁	0010 1011	1	0	1	
t ₂	0001 1101	1	1	1	
t ₃	1000 1110	1	1	0	
t ₄	1100 0111	0	(1)	(0)	

operation of serial adder.

The above figure shows the block diagram of a serial adder with accumulator. Two shift registers are used to hold the four bit numbers to be added X & Y. The X register serves as an accumulator and the Y register serves as an addend. When the addition is

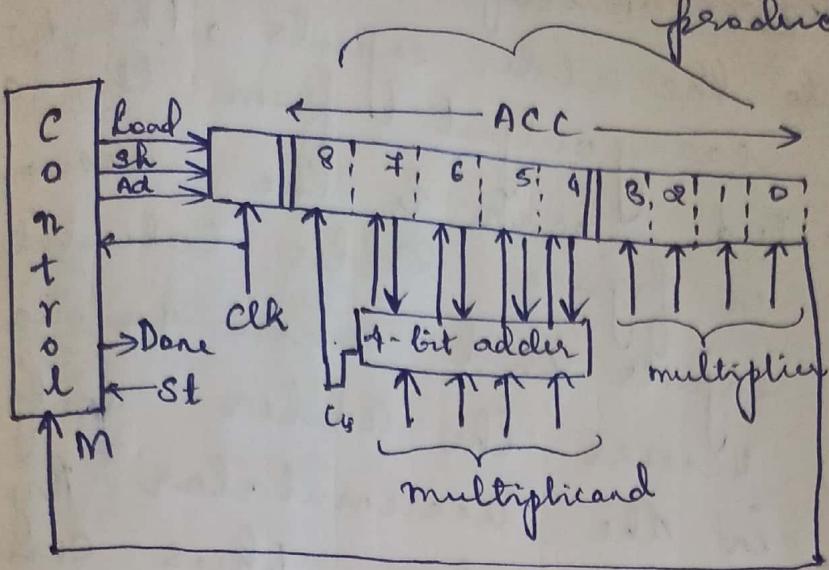
completed, the contents of the X and register are replaced with sum of X and y . The addend register is connected as a cyclic shift register. So that after shifting four times it is back in its original state. The box at the left of each shift register shows the inputs sh (shift signal), SI (serial input) and clock. When $Sh=1$ and an active clock edge occurs SI is entered into x_3 or y_3 ; At the same time as the contents of the register are shifted one place to the right at each clock time one pair of bits is added when the falling clock edge shifts the $Sh=1$ the falling edge stores the sum bit into the accumulator stores the carry bit in the carry flip flop and update the addend register one place to the right because sh is connected to the right because sh is only 1 on the flip flop the carry is only updated when shifting occurs.
[Explain 1 or 2 iteration by taking any example]

Design of a Binary Multiplier:

$$\begin{array}{r}
 \text{multiplicand} \rightarrow 1101 \quad (13) \\
 \text{multiplier} \rightarrow 1011 \quad (11) \\
 \hline
 & 1101 \\
 & 1101 \\
 \hline
 & 100111 \\
 & 0000 \\
 \hline
 & 100111 \\
 & 1101 \\
 \hline
 & 10001111 \leftarrow \text{Product} \\
 \hline
 & (143)
 \end{array}$$

} partial products

Binary multiplication requires only shifting and adding. The above example shows how each partial product is added as soon as it is formed. The multiplication of 4 bit numbers requires a 4 bit multiplicand register, a 4 bit multiplier register and an eight bit register for the product. The product register serves as an accumulator to accumulate the sum of the partial products instead of shifting the multiplicand left by one each time before it is added. It is more convenient to shift the product register to the right each time. The below figure shows a block diagram for such a multiplier.



~~$$\begin{array}{r}
 00000|1011 \leftarrow M(11) \\
 | \\
 1101 \\
 \hline
 01101|1011 \\
 | \\
 00110|101 \\
 | \\
 1101 \\
 \hline
 100111|101 \\
 | \\
 0100111|10 \leftarrow M
 \end{array}
 \quad (13)$$~~

initial contents of product register (add multiplicand as $M=1$)

after addition

after shift

(add multiplicand as $M=1$)

after addition

after shift

(skip addition as $M=0$)

after shift

(add multiplicand as $M=1$)

after addition

after shift final

~~$$\begin{array}{r}
 00000|1011 \leftarrow M(11) \\
 | \\
 1101 \\
 \hline
 01101|1011
 \end{array}
 \quad M(13)$$~~

~~$$\begin{array}{r}
 01101|1011
 \end{array}$$~~

~~$$\begin{array}{r}
 00110|101 \\
 | \\
 1101 \\
 \hline
 100111|101
 \end{array}$$~~

~~$$\begin{array}{r}
 00110|101 \\
 | \\
 1101 \\
 \hline
 100111|101
 \end{array}$$~~

~~$$\begin{array}{r}
 0100111|10 \leftarrow M
 \end{array}$$~~

~~$$\begin{array}{r}
 00100111|11 \leftarrow M
 \end{array}$$~~

~~$$\begin{array}{r}
 1101 \\
 | \\
 1000111|11
 \end{array}$$~~

~~$$\begin{array}{r}
 1000111|11
 \end{array}$$~~

~~$$\begin{array}{r}
 01000111|11
 \end{array}$$~~

(143)

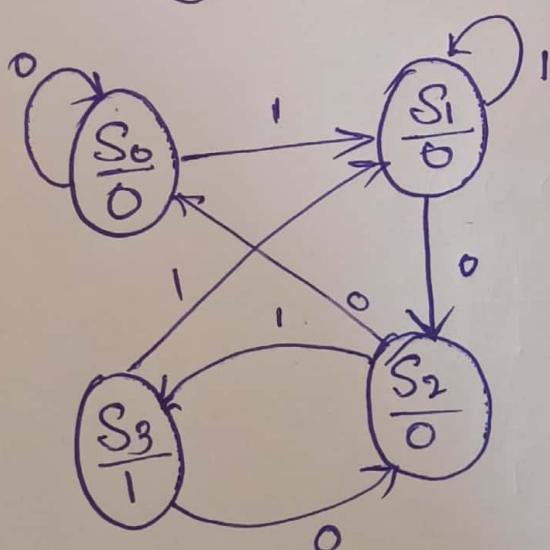
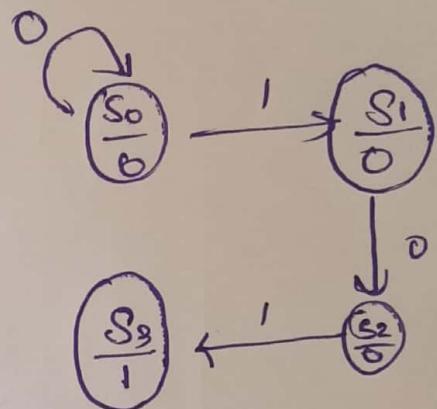
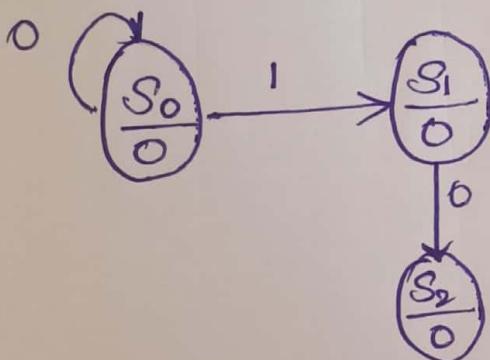
↓ dividing
line b/w product of
multiplicand



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4-bit from the accumulator and 4 bits from the multiplicand register are connected to the adder inputs. The 4-bit sum and carry output from the adder are connected back to the accumulator as shown in figure. Adder calculates the sum of its inputs and when an add signal (A_d) occurs the adder outputs are stored in the accumulator. By the next rising clock edge. Thus causing the multiplicand to be added to the accumulator and extra bit at the left end of the product register temporarily stores any carry (C_4) which is generated when the multiplicand is added to the accumulator. The load signal loads the multiplier into the lower 4-bits of accumulator and at the same time clear the upper 5-bits. The shift signal causes the contents of the product register to be shifted one place to the right. The control circuit puts out proper sequence of add and shift signals after a start signal ($S_t = 1$) has been received. If $M=1$, the multiplicand is added to the accumulator followed by a right shift. If $M=0$ the addition is skipped & only the

* A circuit should produce an output of 1 only if an input sequence ending in 101 as occurred (It's a moore machine).



$$x = 0101101000101101 \\ z = 0001001000001001$$