

THE FIELD EFFECT TRANSISTOR

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Preview

In this chapter we will cover the physics of the junction field-effect transistor. Although we discussed the bipolar and MOS transistors in the previous chapters, the material in this chapter presumes a knowledge only of semiconductor material properties and the characteristics of *pn* and Schottky barrier junctions.

The Junction Field-Effect Transistor (JFET), in conjunction with other circuit elements, is capable of voltage gain and signal-power gain. There are two general categories of junction field-effect transistors. The first is the *pn* junction FET, or *pn* JFET, and the second is the METal-Semiconductor Field-Effect Transistor (MESFET). The *pn* JFET is fabricated with a *pn* junction, and the MESFET with a Schottky barrier rectifying junction.

The current in a junction field-effect transistor is through a semiconductor region known as the channel, with ohmic contacts at each end. The basic transistor action is the modulation of the channel conductance by an electric field that is perpendicular to the channel. The modulating electric field is induced in the space charge region of a reverse-biased *pn* junction or a reverse-biased Schottky barrier junction and is, therefore, a function of a gate voltage. The modulation of the channel conductance by the gate voltage modulates the channel current. We will initially derive the ideal current-voltage characteristics of the *pn* JFET in terms of the semiconductor and geometrical properties of the device. We will then consider the transistor gain, or transconductance, of the *pn* JFET, develop the special properties of the MESFET, and describe some nonideal effects of the JFETs.

A specialized JFET structure is considered. This device is called a High-Electron Mobility Transistor (HEMT) and utilizes a heterojunction. Electrons, confined in a potential well at the heterojunction interface, can easily move in the channel parallel to the junction. The electrons in the channel are separated from the ionized donors so that ionized impurity scattering is minimized; thus electron mobility is not degraded. A large mobility results in a large transistor gain and good high-frequency characteristics.

In JFET and MESFET gate leakage currents are considerably high, so to reduce gate leakage current another type of FET, i.e. MOSFET (Metal Oxide Semiconductor Field Effect Transistors) comes in. In MOSFET there is an insulator (generally oxide) layer between gate electrode and channel. For this reason MOSFET is sometimes called a Metal Insulator Semiconductor Field Effect Transistor (MISFET). MOSFET plays an important role in the digital world and in power electronics.

JFET CONCEPTS

9.1

9.1.1 Basic *pn* JFET Operation

The first type of field-effect transistor is the *pn* junction field-effect transistor, or *pn* JFET. A simplified cross section of a symmetrical device is shown in Fig. 9.2. The *n*-region between the two *p*-regions is known as the channel and, in this *n*-channel device, majority carrier electrons flow between the source and drain terminals. The source is the terminal from which carriers enter the channel from the external circuit, the drain is the terminal where carriers leave, or are drained from, the device, and the gate is the control terminal. Two gate terminals shown in Fig. 9.2 are tied together to form a single gate connection. Since majority carrier electrons are primarily involved in the conduction in this *n*-channel transistor, the JFET is a majority-carrier device or an unipolar device.

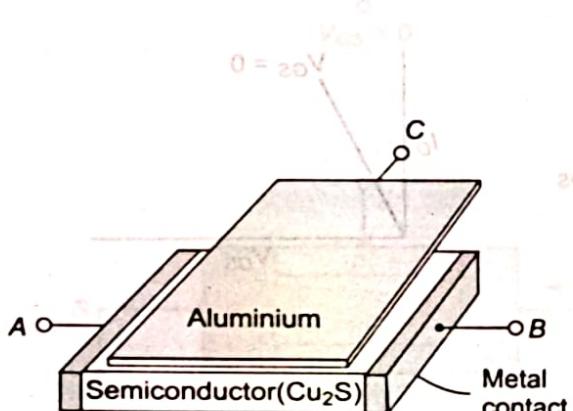


Fig. 9.1 Idealization of the Lilienfeld transistor
(From Pierret [10])

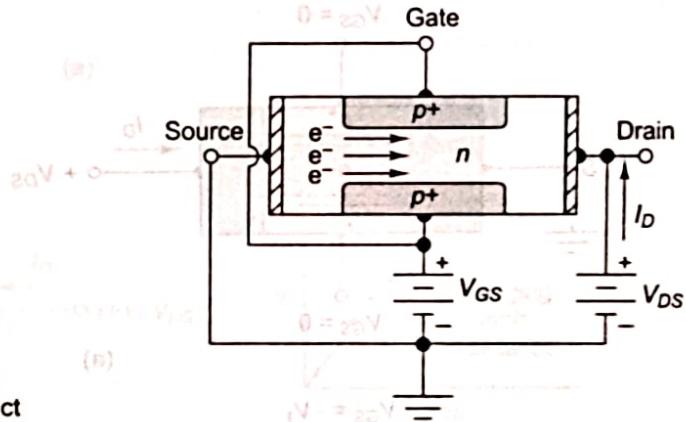


Fig. 9.2 Cross section of a symmetrical n-channel *pn* junction FET

A complementary *p*-channel JFET can also be fabricated in which the *p*- and *n*-regions are reversed from those of the *n*-channel device. Holes will flow in the *p*-type channel between source and drain and the source terminal will now be the source of the holes. The current direction and voltage polarities in the *p*-channel JFET are the reverse of those in the *n*-channel device. The *p*-channel JFET is generally a lower frequency device than the *n*-channel JFET due to the lower hole mobility.

Figure 9.3(a) shows an *n*-channel *pn* JFET with zero volts applied to the gate. If the source is at ground potential, and if a small positive drain voltage is applied, a drain current I_D is produced between the source and drain terminals. The *n* channel is essentially a resistance so the I_D versus V_{DS} characteristic, for small V_{DS} values, is approximately linear, as shown in the figure.

When we apply a voltage to the gate of a *pn* JFET with respect to the source and drain, we alter the channel conductance. If a negative voltage is applied to the gate of the *n*-channel *pn* JFET shown in Fig. 9.3, the gate-to-channel *pn* junction becomes reverse biased. The space charge region now widens so the channel region becomes narrower and the resistance of the *n* channel increases. The slope of the I_D versus V_{DS} curve, for small V_{DS} , decreases. These effects are shown in Fig. 9.3(b). If a larger negative gate voltage is applied, the condition shown in Fig. 9.3(c) can be achieved. The reverse-biased gate-to-channel space charge region has completely filled the channel region. This condition is known as *pinchoff*. The drain current at pinchoff is essentially zero, since the depletion region isolates the source and drain terminals. Figure 9.3(c) shows the I_D versus V_{DS} curve for this case, as well as the other two cases.

The current in the channel is controlled by the gate voltage. The control of the current in one part of the device by a voltage in another part of the device is the basic transistor action. This device is a normally on or *depletion mode* device, which means that a voltage must be applied to the gate terminal to turn the device off.

Now consider the situation in which the gate voltage is held at zero volts, $V_{GS} = 0$, and the drain voltage changes. Figure 9.4(a) is a replica of Fig. 9.3(a) for zero gate voltage and a small drain voltage. As the drain voltage increases (positive), the gate-to-channel *pn* junction becomes reverse biased near the drain terminal so that the space charge region extends further into the channel. The channel is essentially a resistor, and the effective channel resistance increases as the space charge region widens; therefore, the slope of the I_D versus V_{DS} characteristic decreases as shown in Fig. 9.4(b). The effective channel resistance now varies along the channel length and, since the channel current must be constant, the voltage drop through the channel becomes dependent on position.

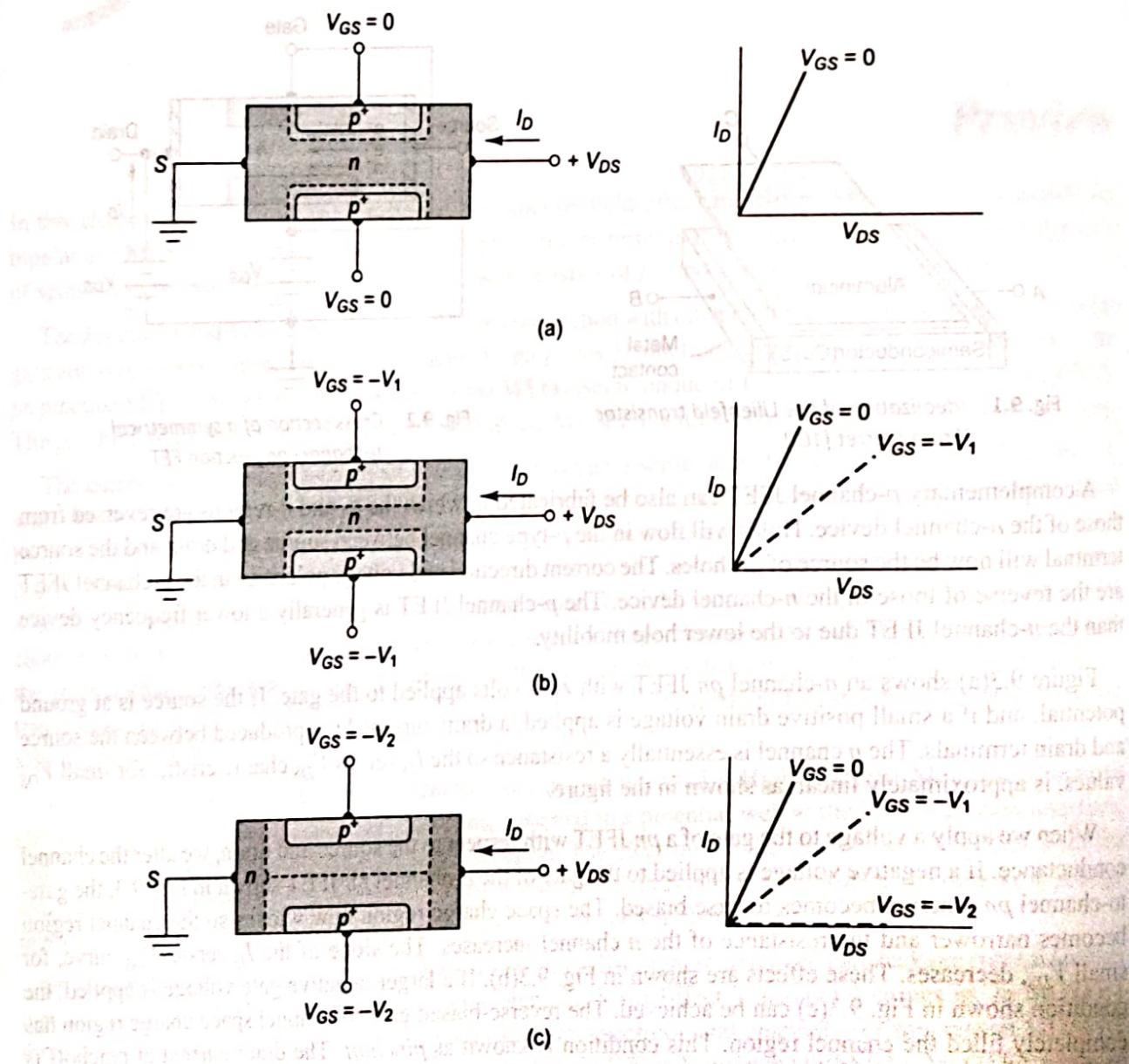


Fig. 9.3 Gate-to-channel space charge regions and I - V characteristics for small V_{DS} values and for (a) zero gate voltage, (b) small reverse-biased gate voltage, and (c) a gate voltage to achieve pinchoff

If the drain voltage increases further, the condition shown in Fig. 9.4(c) can result. The channel has been pinched off at the drain terminal. Any further increase in drain voltage will not cause an increase in drain current. The $I-V$ characteristic for this condition is also shown in this figure. The drain voltage at pinchoff is referred to as $V_{DS}(\text{sat})$. For $V_{DS} > V_{DS}(\text{sat})$, the transistor is said to be in the saturation region and the drain current, for this ideal case, is independent of V_{DS} . At first glance, we might expect the drain current to go to zero when the channel becomes pinched off at the drain terminal, but we will show why this does not happen.

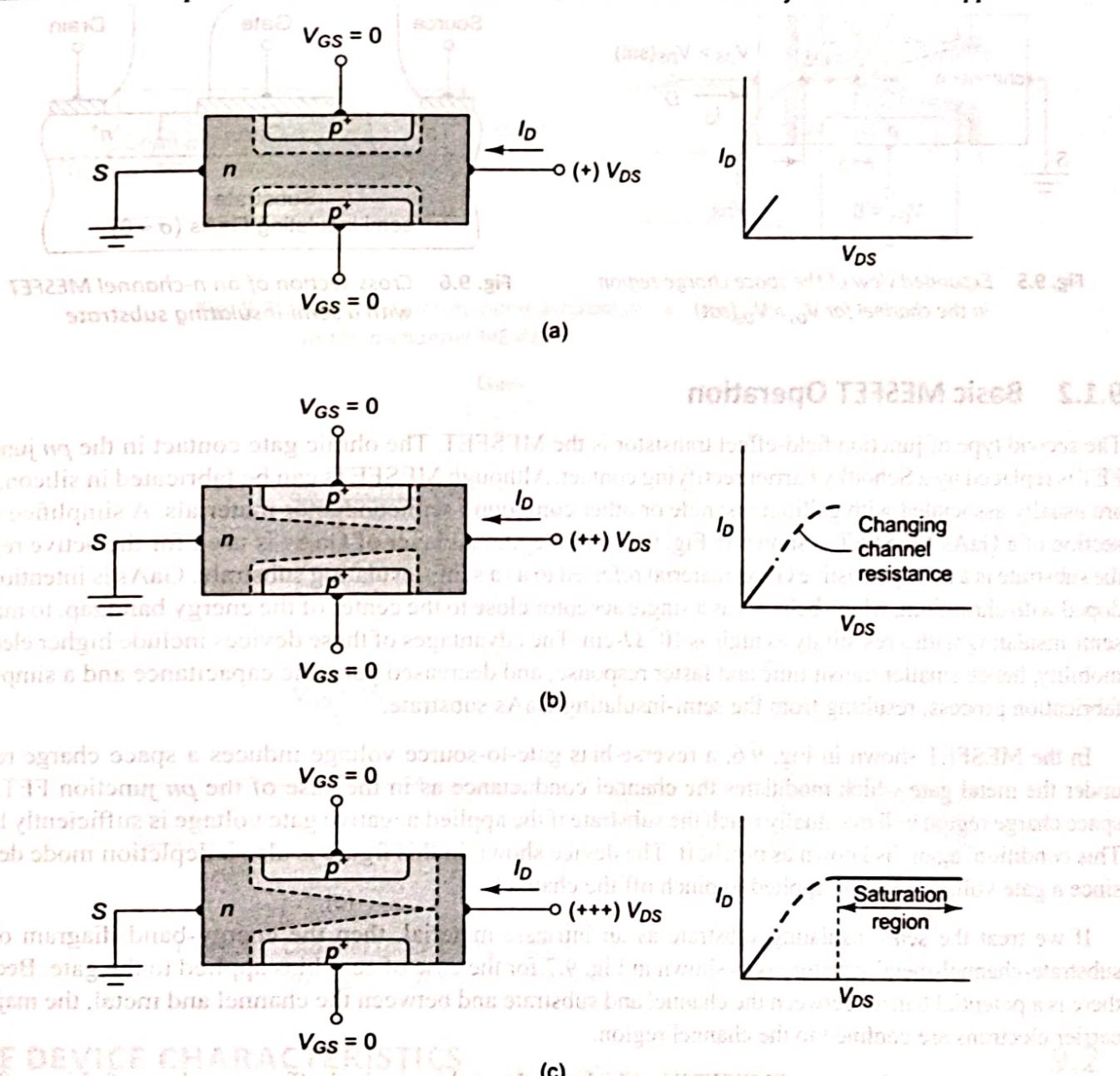


Fig. 9.4 (a) Gate-to-channel space charge regions and I_V characteristics for zero gate voltage and for (a) a small drain voltage, (b) a larger drain voltage, and (c) a drain voltage to achieve pinchoff at the drain terminal

Figure 9.5 shows an expanded view of the pinchoff region in the channel. The n -channel and drain terminal are now separated by a space charge region which has a length ΔL . The electrons move through the n -channel from the source and are injected into the space charge region where, subjected to the E -field force, they are swept through into the drain contact area. If we assume that $\Delta L \ll L$, then the electric field in the n -channel

region remains unchanged from the $V_{DS}(\text{sat})$ case; the drain current will remain constant as V_{DS} changes. Once the carriers are in the drain region, the drain current will be independent of V_{DS} ; thus, the device looks like a constant current source.

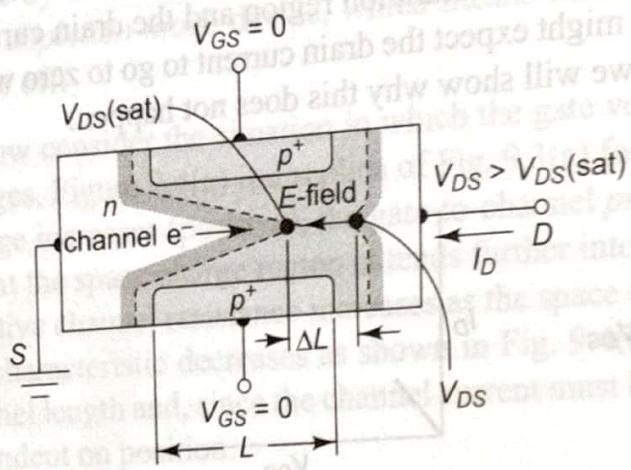


Fig. 9.5 Expanded view of the space charge region in the channel for $V_{DS} > V_{DS}(\text{sat})$

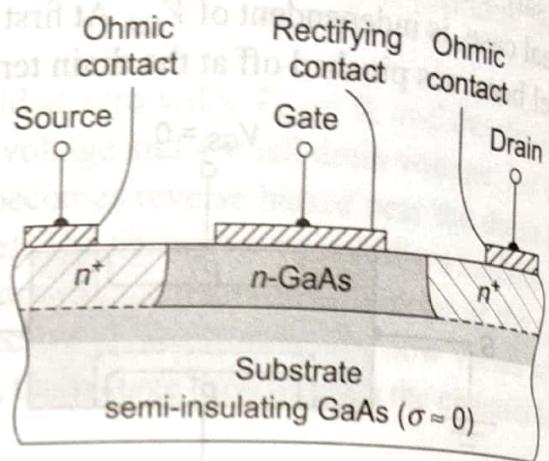


Fig. 9.6 Cross section of an n-channel MESFET with a semi-insulating substrate

EQUIVALENT CIRCUIT AND FREQUENCY LIMITATIONS

9.4

In order to analyze a transistor circuit, one needs a mathematical model or equivalent circuit of the transistor. One of the most useful models is the small-signal equivalent circuit, which applies to transistors used in linear amplifier circuits. This equivalent circuit will introduce frequency effects in the transistor through the equivalent capacitor-resistor circuits. The various physical factors in the JFET affecting the frequency limitations will be considered here and a transistor cutoff frequency, which is a figure of merit, will then be defined.

9.4.1 Small-Signal Equivalent Circuit

The cross section of an *n*-channel *pn* JFET is shown in Fig. 9.16, including source and drain series resistances. The substrate may be semi-insulating gallium arsenide or it may be a *p*⁺ type substrate.

Figure 9.17 shows a small-signal equivalent circuit for the JFET. The voltage $V_{g's'}$ is the internal gate-to-source voltage that controls the drain current. The r_{gs} and C_{gs} parameters are the gate-to-source diffusion resistance and junction capacitance, respectively. The gate-to-source junction is reverse biased for depletion mode devices and has only a small forward-bias voltage for enhancement mode devices, so that normally r_{gs} is large. The parameters r_{gd} and C_{gd} are the gate-to-drain resistance and capacitance, respectively. The resistance r_{ds} is the finite drain resistance, which is a function of the channel length modulation effect. The C_{ds} capacitance is mainly a drain-to-source parasitic capacitance and C_s is the drain-to-substrate capacitance.

The ideal small-signal equivalent circuit is shown in Fig. 9.18(a). All diffusion resistances are infinite, the series resistances are zero, and at low frequency the capacitances become open circuits. The small-signal drain current is now given by,

where $V_{g's'}$ is the transconductance voltage and r_{ds} is the drain-to-source drain saturation resistance. This saturation effect occurs as a drain voltage increases. The drain voltage is designated V_{DS} and I_{DS} and V_{DS} will be smaller than V_{DS} .

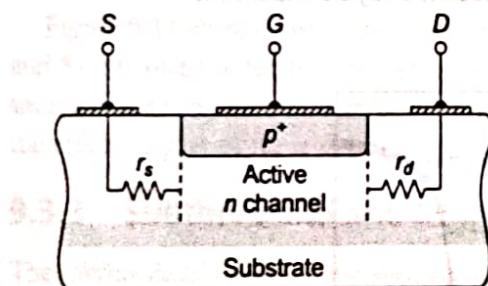


Fig. 9.16 Cross section of JFET with source and drain series resistance

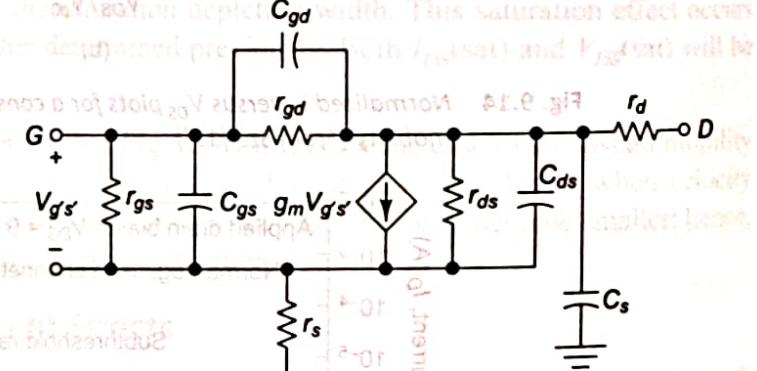
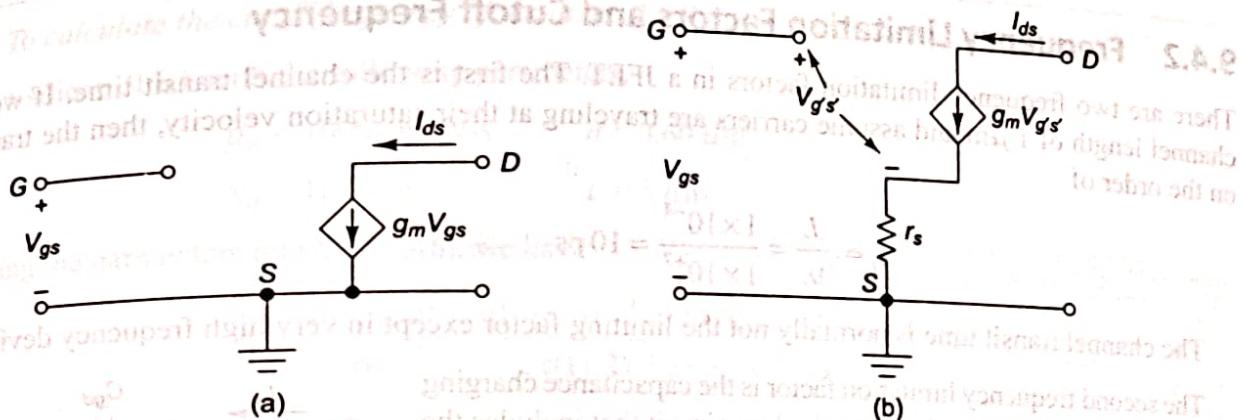


Fig. 9.17 Small-signal equivalent circuit of JFET

which is a function only of the transconductance and the input-signal voltage.

The effect of the source series resistance can be determined using Fig. 9.18(b). We have

$$I_{ds} = g_m V_{g's'} \quad (9.37)$$



**Fig. 9.18 (a) Ideal low-frequency small-signal equivalent circuit
(b) Ideal equivalent circuit including r_s**

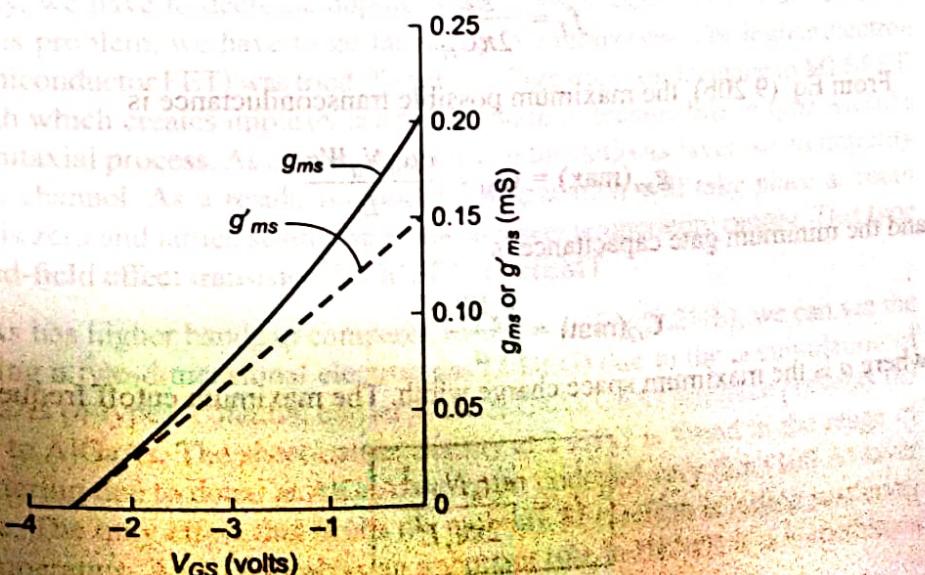
The relation between V_{gs} and $V_{g's'}$ can be found from the ideal equivalent circuit. At negative biasing (single-supply case), we have $V_{gs} = V_{g's'} + (g_m V_{g's'}) r_s = (1 + g_m r_s) V_{g's'}$. (9.38)

Equation (9.37) can then be written as

$$I_{ds} = \left(\frac{g_m}{1 + g_m r_s} \right) V_{gs} = g'_m V_{gs} \quad (9.39)$$

The effect of the source resistance is to reduce the effective transconductance or transistor gain.

Recall that g_m is a function of the dc gate-to-source voltage, so g'_m will also be a function of V_{GS} . Equation (9.20b) is the relation between g_m and V_{GS} when the transistor is biased in the saturation region. Figure 9.19 shows a comparison between the theoretical and experimental transconductance values using the parameters from Example 9.3 and letting $r_s = 2000 \Omega$. (A value of $r_s = 2000 \Omega$ may seem excessive, but keep in mind that the active thickness of the semiconductor may be on the order of 1 μm or less; thus, a large series resistance may result if special care is not taken.)



**Fig. 9.19 JFET transconductance versus V_{GS}
(a) without, and (b) with a source series resistance**

FREQUENCY LIMITATION AND CUTOFF FREQUENCIES

9.4.2 Frequency Limitation Factors and Cutoff Frequency

There are two frequency limitation factors in a JFET. The first is the channel transit time. If we assume a channel length of $1 \mu\text{m}$ and assume carriers are traveling at their saturation velocity, then the transit time is on the order of

$$\tau_t = \frac{L}{v_s} = \frac{1 \times 10^{-4}}{1 \times 10^7} = 10 \text{ ps} \quad (9.40)$$

The channel transit time is normally not the limiting factor except in very high frequency devices.

The second frequency limitation factor is the capacitance charging time. Figure 9.20 is a simplified equivalent circuit that includes the primary capacitances and ignores the diffusion resistances. The output current will be the short-circuit current. As the frequency of the input-signal voltage V_{gs} increases, the impedance of C_{gd} and C_{gs} decreases so the current through C_{gd} will increase. For a constant $g_m V_{gs}$, the I_{ds} current will then decrease. The output current then becomes a function of frequency.

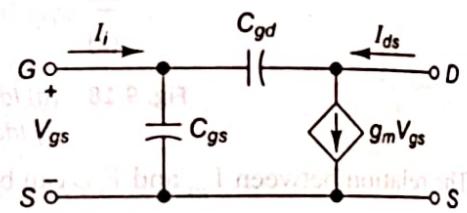


Fig. 9.20 A small-signal equivalent circuit with capacitance

If the capacitance charging time is the limiting factor, then the cutoff frequency f_T is defined as the frequency at which the magnitude of the input current I_i is equal to the magnitude of the ideal output current $g_m V_{gs}$ of the intrinsic transistor. We have, when the output is short-circuited,

$$I_i = j\omega(C_{gs} + C_{gd})V_{gs} \quad (9.41)$$

If we let $C_G = C_{gs} + C_{gd}$ then at the cutoff frequency

$$|I_i| = 2\pi f_T C_G V_{gs} = g_m V_{gs} \quad (9.42)$$

or

$$f_T = \frac{g_m}{2\pi C_G} \quad (9.43)$$

From Eq. (9.20b), the maximum possible transconductance is

$$g_{ms}(\max) = G_{01} = \frac{e\mu_n N_d W a}{L} \quad (9.44)$$

and the minimum gate capacitance is

$$C_G(\min) = \frac{\epsilon_s W L}{a} \quad (9.45)$$

where a is the maximum space charge width. The maximum cutoff frequency can be written as

$$f_T = \frac{e\mu_n N_d a^2}{2\pi\epsilon_s L^2} \quad (9.46)$$

Example 9.5

Objective To calculate the cutoff frequency of a silicon JFET.

Consider a silicon JFET with the following parameters:

$$\mu_n = 1000 \text{ cm}^2/\text{V-s} \quad a = 0.60 \mu\text{m}$$

$$N_d = 10^{16} \text{ cm}^{-3} \quad L = 5 \mu\text{m}$$

Substituting the parameters into Eq. (9.46), we have

$$f_T = \frac{e\mu_n N_d a^2}{2\pi\epsilon_s L^2} = \frac{(1.6 \times 10^{-19})(1000)(10^{16})(0.6 \times 10^{-4})^2}{2\pi(11.7)(8.85 \times 10^{-14})(5 \times 10^{-4})^2} = 3.54 \text{ GHz}$$

Comment This example shows that even silicon JFETs can have relatively large cutoff frequencies.

For gallium arsenide JFETs or MESFETs with very small geometries, the cutoff frequency is even larger. The channel transit time may also become a factor in very high frequency devices, in which case the expression for cutoff frequency would need to be modified.

One application of GaAs FETs is in ultrafast digital integrated circuits. Conventional GaAs MESFET logic gates can achieve propagation delay times in the sub-nanosecond range. These delay times are at least comparable to, if not shorter than fast-ECL, but the power dissipation is 3 orders of magnitude smaller than in the ECL circuits. Enhancement mode GaAs JFETs have been used as drivers in logic circuits, and depletion mode devices may be used as loads. Propagation delay times of as low as 45 ps have been observed. Special JFET structures may be used to further increase the speed. These structures include the modulation-doped field-effect transistor, which is discussed in the following section.

HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) 9.5

One of the major disadvantages of a normal FET is the degradation of mobility due to very high doping in the channel region. To increase mobility, we have to decrease doping which causes reduction of carrier in the channel region. So, to overcome this problem, we have to go for bandgap engineering. For higher electron mobility GaAs MESFET (Metal Semiconductor FET) was tried. To achieve high transconductance in MESFET, doping in the channel should be high which creates impurity scattering. So to overcome this, *n*-type AlGaAs is grown on undoped GaAs using epitaxial process. As all the donors are in the AlGaAs layer, so no impurity scattering will happen in the GaAs channel. As a result, no mobility degradation will take place at room temperature (as impurity scattering is zero and lattice scattering is low at lower temperature range). This type of device is called modulation doped-field effect transistor (MODFET) or HEMT.

In AlGaAs/GaAs HEMT, AlGaAs has higher bandgap compared to GaAs. In Fig. 9.21(b), we can see the two-dimensional electron gas (2 DEG) due to the accumulation of

9.6.2. Energy-Band Diagrams

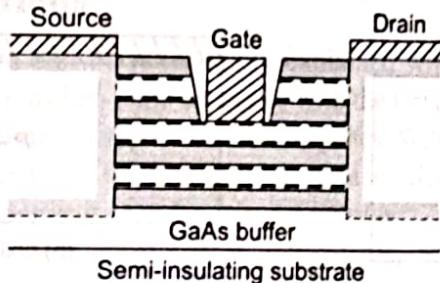


Fig. 9.29 A multi-channel HEMT

HEMTs can be used in light-speed logic circuits. They have been used in flip-flop circuits operating at clock frequencies of 5.5 GHz at $T = 300$ K. As small-signal, high-frequency amplifier, HEMT shows reasonable gains up to 35 GHz. The maximum frequency increases as the channel length decreases. Cutoff frequencies on the order of 100 GHz have been measured with channel length of 0.25 μm .

It seems clear that HEMTs are inherently superior to other FET technologies in terms of achieving higher speeds of operation, lower power dissipation and lower noise. These advantages derive directly from the superior transport properties obtained by using undoped GaAs as channel in an FET. One way to achieve an adequate carrier concentration in an undoped channel is to accumulate the carriers at a semiconductor heterojunction interface. In fabrication point of view, HEMT fabrication process are much complicated.

MOSFET

9.6

The heart of the MOSFET is a metal–oxide–semiconductor structure known as an MOS capacitor. The energy bands in the semiconductor near the oxide–semiconductor interface bend as a voltage is applied across the MOS capacitor. The position of the conduction and valence bands relative to the Fermi level at the oxide–semiconductor interface is a function of the MOS capacitor voltage, so that the characteristics of the semiconductor surface can be inverted from *p*-type to *n*-type, or from *n*-type to *p*-type, by applying the proper voltage. The operation and characteristics of the MOSFET are dependent on this inversion and the creation of an inversion charge density at the semiconductor surface. The threshold voltage is defined as the applied gate voltage required to create the inversion layer charge and is one of the important parameters of the MOSFET.

The various types of MOSFETs are examined and a qualitative discussion of the current–voltage characteristics is initially presented. A mathematical derivation of the current–voltage relation is then covered in detail. The frequency response and limitations of the MOSFET are also considered.

We have discussed the fabrication process of MOSFET using flow diagram in Fig. 9.31. In this figure we have described the formation of *n*-channel enhancement mode device.

9.6.1 The Two-terminal MOS Structure

The two terminal MOS capacitor structure is shown in Fig. 9.30. The metal may be aluminum or some other type of metal, although in many cases, it is actually a high-conductivity polycrystalline silicon that has been deposited on the oxide; however, the term metal is usually still used. The parameter t_{ox} in the figure is the thickness of the oxide and ϵ_{ox} is the permittivity of the oxide.

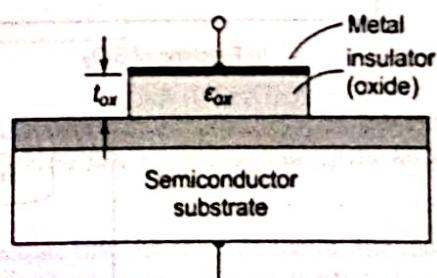
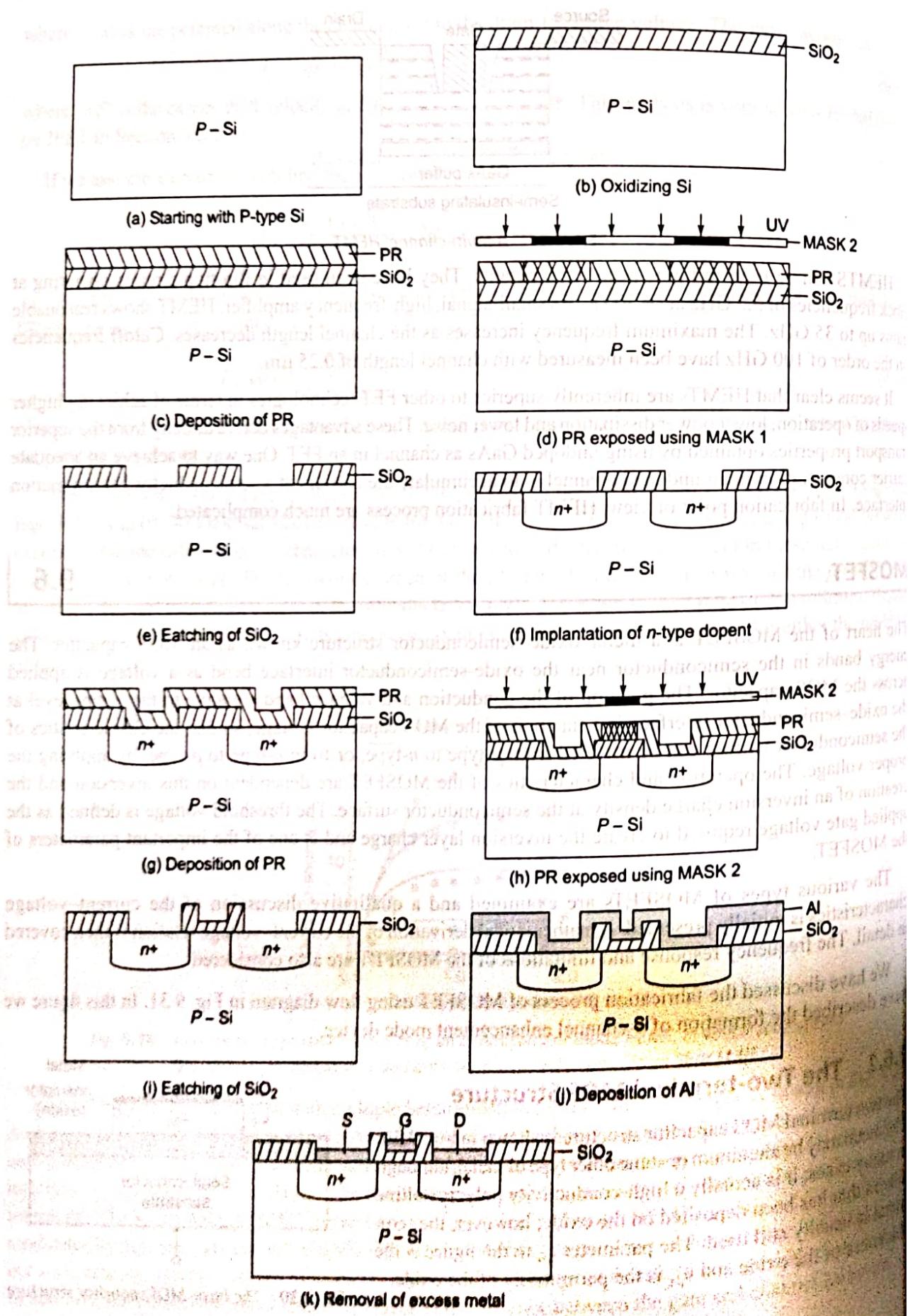


Fig. 9.30 The basic MOS capacitor structure



9.6.2. Energy-Band Diagrams

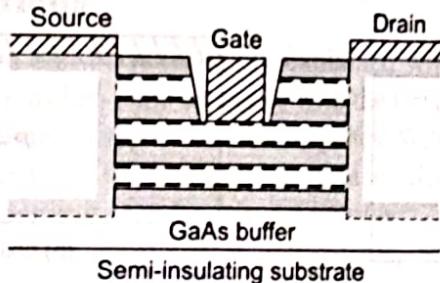


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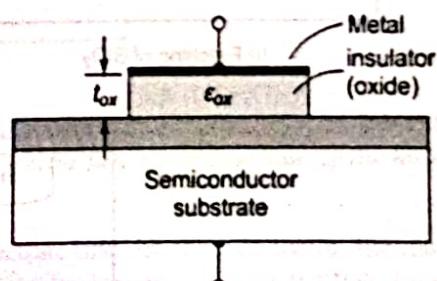


Fig. 9.30 The basic MOS capacitor structure

9.6.2 Energy-Band Diagrams

The physics of the MOS structure can be more easily explained with the aid of the simple parallel-plate capacitor. Figure 9.32(a) shows a parallel-plate capacitor with the top plate at a negative voltage with respect to the bottom plate. An insulator material separates the two plates. With this bias, a negative charge exists on the top plate, a positive charge exists on the bottom plate, and an electric field is induced between the two plates as shown. The capacitance per unit area for this geometry is

$$C' = \frac{\epsilon}{d} \quad (9.55)$$

where ϵ is the permittivity of the insulator and d is the distance between the two plates. The magnitude of the charge per unit area on either plate is

$$Q' = C'V \quad (9.56)$$

where the prime indicates charge or capacitance per unit area. The magnitude of the electric field is

$$E = \frac{V}{d} \quad (9.57)$$

Figure 9.32(b) shows an MOS capacitor with a *p*-type semiconductor substrate. The top metal gate is at a negative voltage with respect to the semiconductor substrate. From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced with

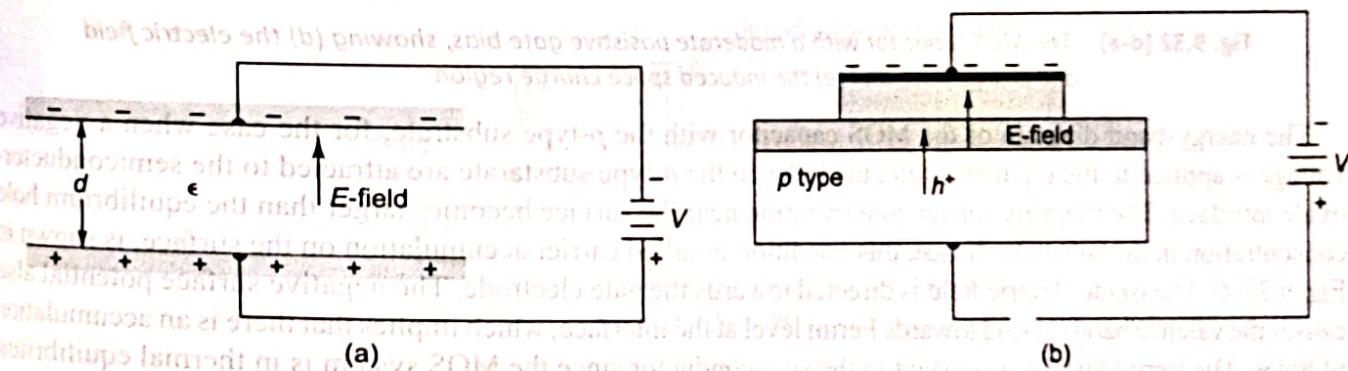


Fig. 9.32(b) The electric field and charge flow in an MOS capacitor.

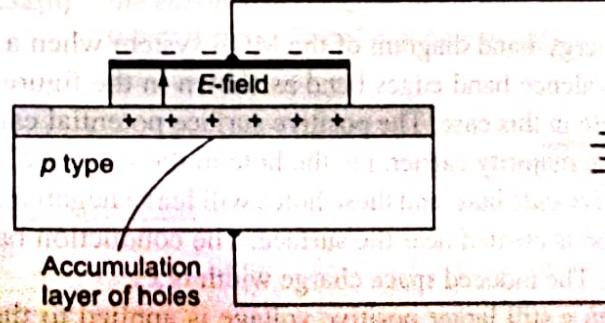


Fig. 9.32 (a-c) (a) A parallel-plate capacitor showing the electric field and conductor charges (b) A corresponding MOS capacitor with a negative gate bias showing the electric field and charge flow (c) The MOS capacitor with an accumulation layer of holes

the direction shown in the figure. If the electric field were to penetrate into the semiconductor, the majority carrier holes would experience a force toward the oxide-semiconductor interface. Figure 9.32(c) shows the

equilibrium distribution of charge in the MOS capacitor with this particular applied voltage. An **accumulation layer** of holes in the oxide-semiconductor junction corresponds to the positive charge on the bottom "plate" of the MOS capacitor.

Figure 9.32(d) shows the same MOS capacitor in which the polarity of the applied voltage is reversed. A positive charge now exists on the top metal plate and the induced electric field is in the opposite direction as shown. If the electric field penetrates the semiconductor in this case, majority carrier holes will experience a force away from the oxide-semiconductor interface. As the holes are pushed away from the interface, a negative space charge region is created because of the fixed ionized acceptor atoms. The negative charge in the induced depletion region corresponds to the negative charge on the bottom "plate" of the MOS capacitor. Figure 9.32(e) shows the equilibrium distribution of charge in the MOS capacitor with this applied voltage.

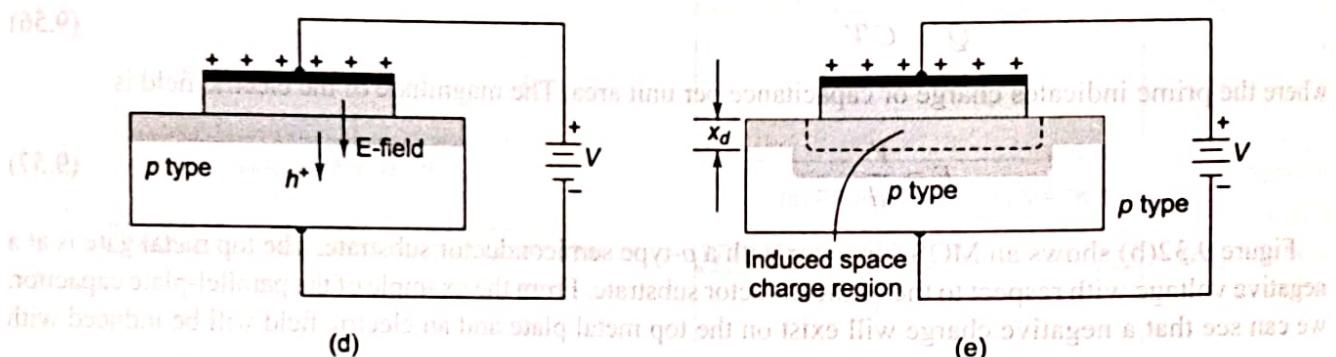


Fig. 9.32 (d-e) The MOS capacitor with a moderate positive gate bias, showing (d) the electric field and charge flow, and (e) the induced space charge region

The energy-band diagram of the MOS capacitor with the *p*-type substrate, for the case when a negative voltage is applied to the top metal gate, the holes in the *p*-type substrate are attracted to the semiconductor-oxide interface. The majority carrier concentration near the surface becomes larger than the equilibrium hole concentration in the substrate; hence, this condition is called carrier accumulation on the surface, is shown in Fig. 9.32(f). The oxide electric field is directed towards the gate electrode. The negative surface potential also causes the valence band to bend towards Fermi level at the interface, which implies that there is an accumulation of holes. The Fermi level is a constant in the semiconductor since the MOS system is in thermal equilibrium and there is no current through the oxide.

Figure 9.32(g) shows the energy-band diagram of the MOS system when a positive voltage is applied to the gate. The conduction and valence band edges bend as shown in the figure. The oxide electric field will be directed towards the substrate in this case. The positive surface potential causes the energy bands to bend downward near the surface. The majority carrier, i.e. the hole in the substrate, will be repelled back into the substrate as a result of the positive gate bias, and these holes will leave negatively charged fixed acceptor ions behind. Thus, a depletion region is created near the surface. The conduction band and intrinsic Fermi levels move closer to the Fermi level. The induced space charge width is x_d .

Now consider the case when a still larger positive voltage is applied to the top metal gate of the MOS capacitor. We expect the induced electric field to increase in magnitude and the corresponding positive and negative charges on the MOS capacitor to increase. Larger negative charge in the MOS capacitor implies a larger induced space charge region and more band bending. Figure 9.32(h) shows such a condition. The intrinsic Fermi level at the surface is now below the Fermi level; thus, the conduction band is closer to the Fermi level than the valence band is. This result implies that the surface in the semiconductor adjacent to the oxide-semiconductor interface is *n* type. By applying a sufficiently large positive gate voltage, we have inverted

the surface of the semiconductor from a *p*-type to an *n*-type semiconductor. We have created an *inversion layer* of electrons at the oxide–semiconductor interface.

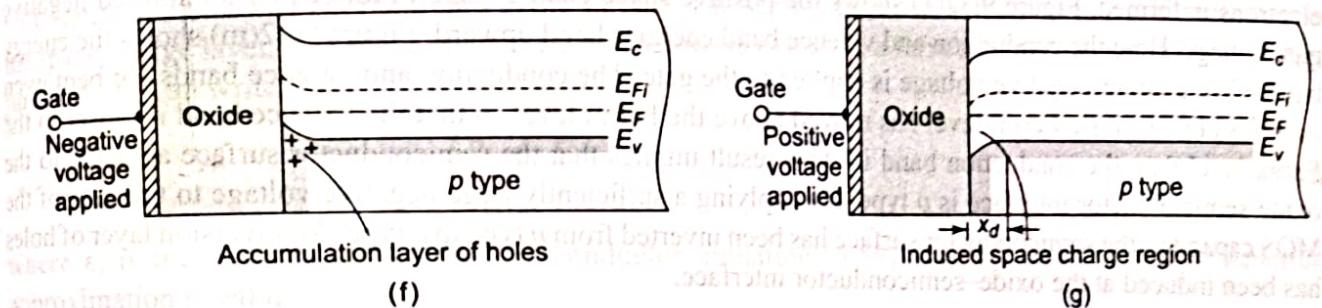


Fig. 9.32 (f-g) The energy-band diagram of an MOS capacitor with a *p*-type substrate for (f) a negative gate bias, and (g) a moderate positive gate bias.

In the MOS capacitor structure that we have just considered, we assumed a *p*-type semiconductor substrate. The same type of energy-band diagrams can be constructed for an MOS capacitor with an *n*-type semiconductor substrate. Figure 9.32(i) shows the MOS capacitor structure with a positive voltage applied to the top gate terminal. A positive charge exists on the top gate and an electric field is induced with the direction shown in the figure. An accumulation layer of electrons will be induced in the *n*-type substrate. The case when a negative voltage is applied to the top gate is shown in Fig. 9.32(j). A positive space charge region is induced in the *n*-type semiconductor in this situation.

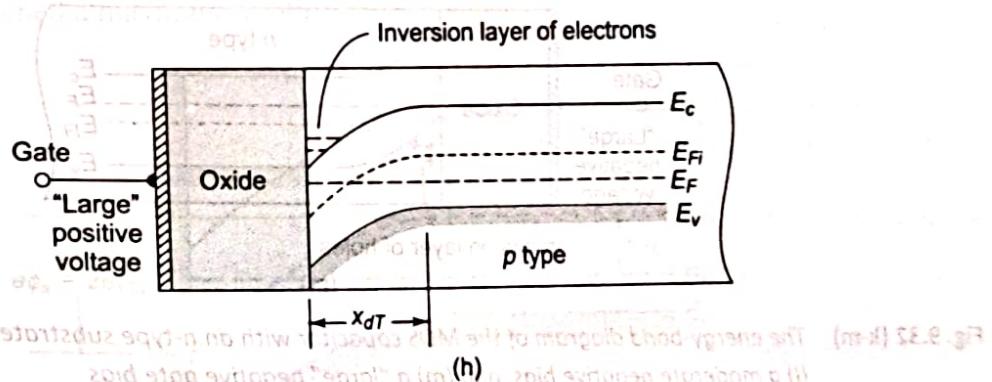


Fig. 9.32(h) The energy-band diagram of the MOS capacitor with a *p*-type substrate for a "large" positive gate bias.

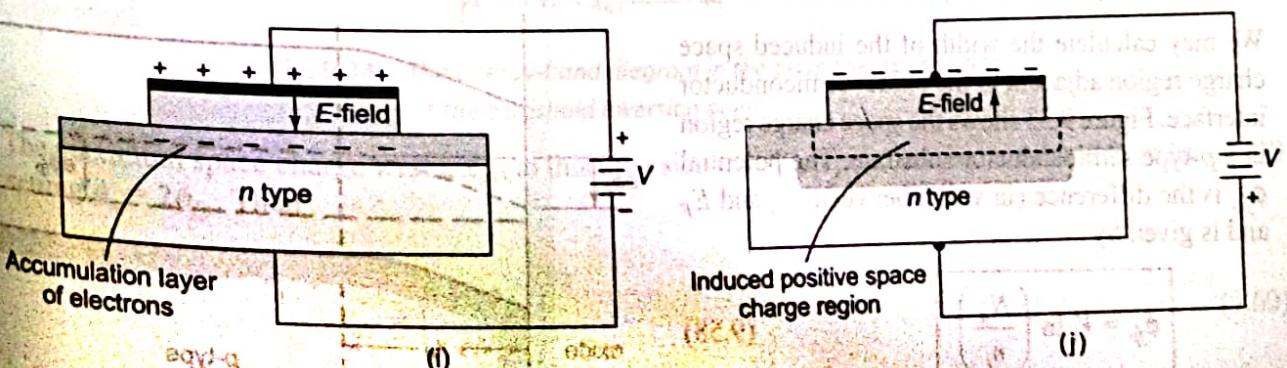


Fig. 9.32 (i-j) The MOS capacitor with an *n*-type substrate for (i) a positive gate bias, and (j) a moderate negative gate bias.

The energy-band diagrams for this MOS capacitor with the *n*-type substrate are shown in Figure 9.32 (k-m). Figure 9.32(k) shows the case when a positive voltage is applied to the gate and an accumulation layer of electrons is formed. Figure 9.32(l) shows the positive space charge region induced by an applied negative gate voltage. Here the conduction and valence band energies bend upward. Figure 9.32(m) shows the energy band when a larger negative voltage is applied to the gate. The conduction and valence bands are bent even more and the intrinsic Fermi level has moved above the Fermi level so that the valence band is closer to the Fermi level than the conduction band is. This result implies that the semiconductor surface adjacent to the oxide-semiconductor interface is *p* type. By applying a sufficiently large negative voltage to the gate of the MOS capacitor, the semiconductor surface has been inverted from *n* type to *p* type. An inversion layer of holes has been induced at the oxide-semiconductor interface.

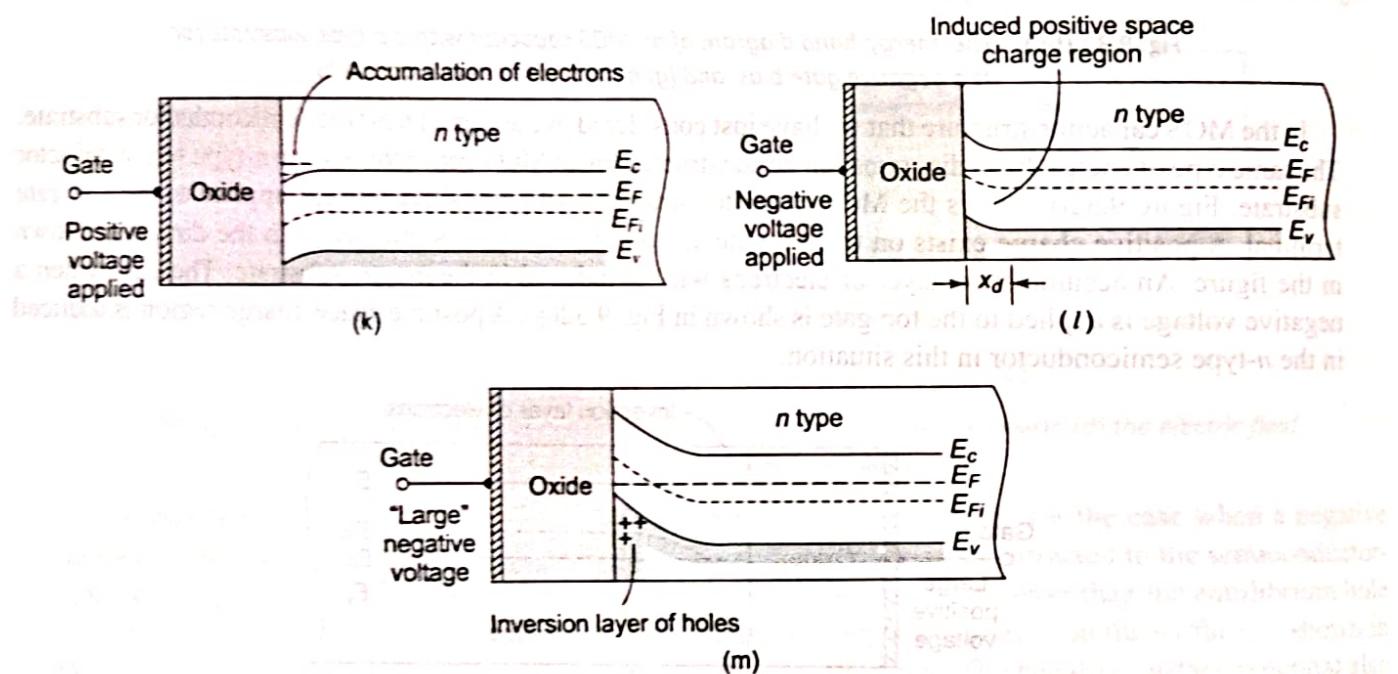


Fig. 9.32 (k-m) The energy-band diagram of the MOS capacitor with an *n*-type substrate for (k) a positive gate bias, (l) a moderate negative bias, and (m) a "large" negative gate bias

9.6.3 Depletion Layer Thickness

We may calculate the width of the induced space charge region adjacent to the oxide-semiconductor interface. Figure 9.33 shows the space charge region in a *p*-type semiconductor substrate. The potential ϕ_{fp} is the difference (in volts) between E_{Fi} and E_F and is given by

$$\phi_{fp} = V_t \ln \left(\frac{N_a}{n_i} \right) \quad (9.58)$$

where N_a is the acceptor doping concentration and n_i is the intrinsic carrier concentration.

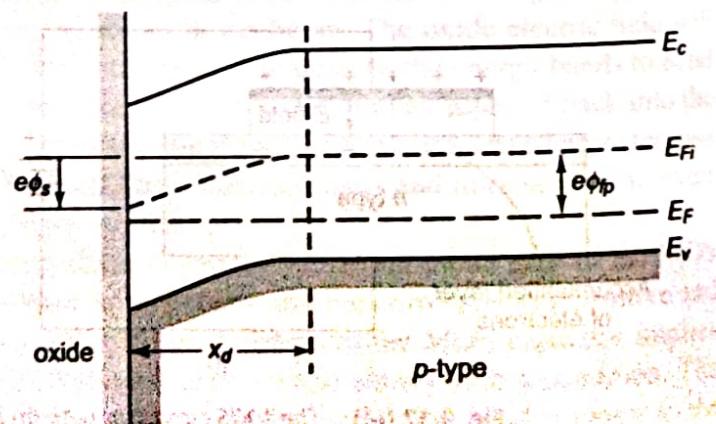


Fig. 9.33 The energy-band diagram in the *p*-type semiconductor, indicating surface potential

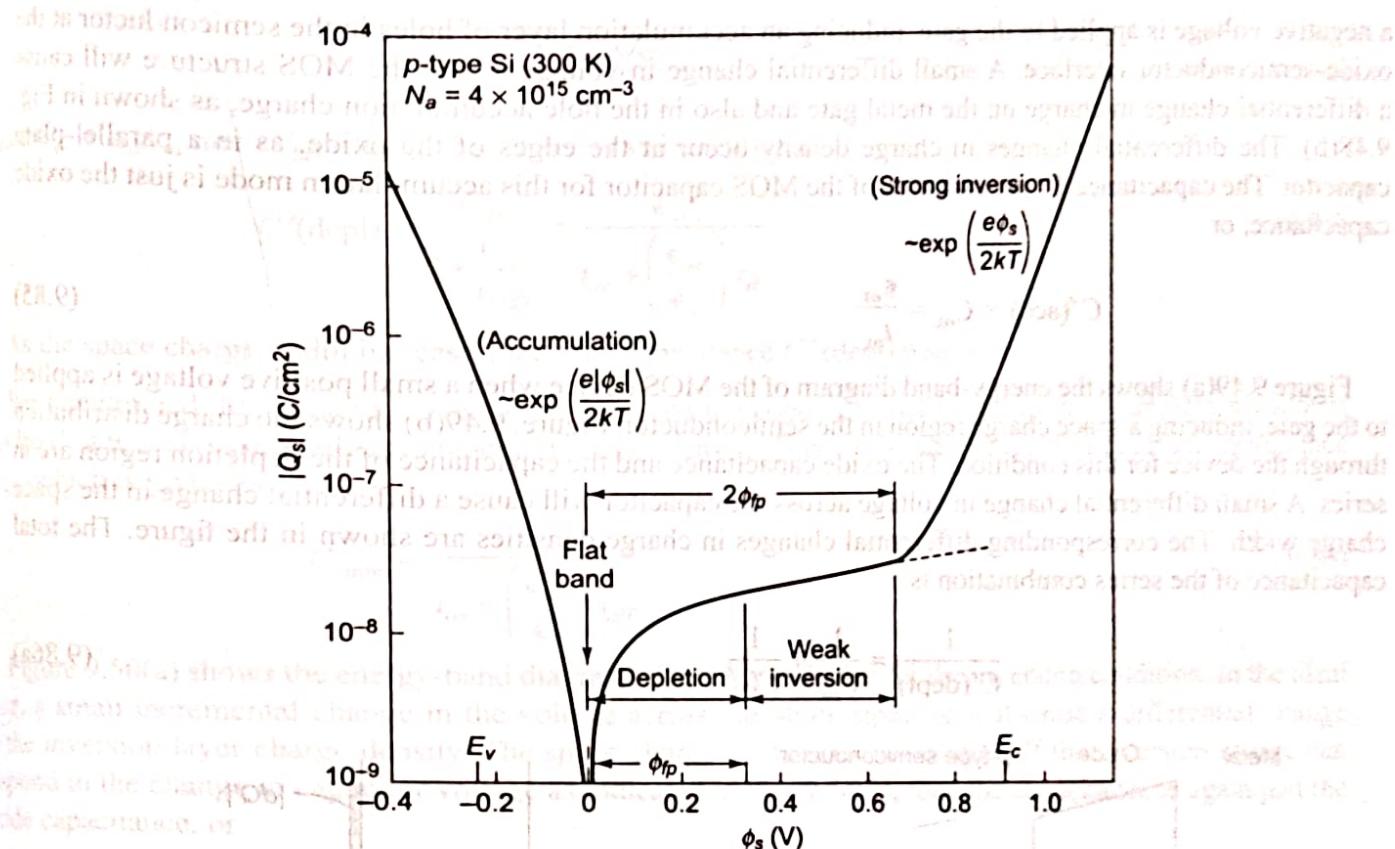


Fig. 9.47 Variation of surface charge density for p-type Si MOS (accumulation charge and inversion charge) as a function of surface potential (From Sze [16])

CAPACITANCE–VOLTAGE CHARACTERISTICS

9.7

The MOS capacitor structure is the heart of the MOSFET. A great deal of information about the MOS device and the oxide–semiconductor interface can be obtained from the capacitance versus voltage or C – V characteristics of the device. The capacitance of a device is defined as

$$C = \frac{dQ}{dV} \quad (9.84)$$

where dQ is the magnitude of the differential change in charge on one plate as a function of the differential change in voltage dV across the capacitor. The capacitance is a small-signal or ac parameter and is measured by superimposing a small ac voltage on an applied dc gate voltage. The capacitance, then, is measured as a function of the applied dc gate voltage.

9.7.1 Ideal C–V Characteristics

First we will consider the ideal C – V characteristics of the MOS capacitor and then discuss some of the deviations that occur from these idealized results. We will initially assume that there is zero charge trapped in the oxide and also that there is no charge trapped at the oxide–semiconductor interface.

There are three operating conditions of interest in the MOS capacitor: accumulation, depletion and inversion. Figure 9.48(a) shows the energy-band diagram of a MOS capacitor with a p-type substrate for the case when

a negative voltage is applied to the gate, inducing an accumulation layer of holes in the semiconductor at the oxide-semiconductor interface. A small differential change in voltage across the MOS structure will cause a differential change in charge on the metal gate and also in the hole accumulation charge, as shown in Fig. 9.48(b). The differential changes in charge density occur at the edges of the oxide, as in a parallel-plate capacitor. The capacitance C' per unit area of the MOS capacitor for this accumulation mode is just the oxide capacitance, or

$$C'(\text{acc}) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad (9.85)$$

Figure 9.49(a) shows the energy-band diagram of the MOS device when a small positive voltage is applied to the gate, inducing a space charge region in the semiconductor. Figure 9.49(b) shows the charge distribution through the device for this condition. The oxide capacitance and the capacitance of the depletion region are in series. A small differential change in voltage across the capacitor will cause a differential change in the space charge width. The corresponding differential changes in charge densities are shown in the figure. The total capacitance of the series combination is

$$\frac{1}{C'(\text{depl})} = \frac{1}{C_{ox}} + \frac{1}{C'_{SD}} \quad (9.86a)$$

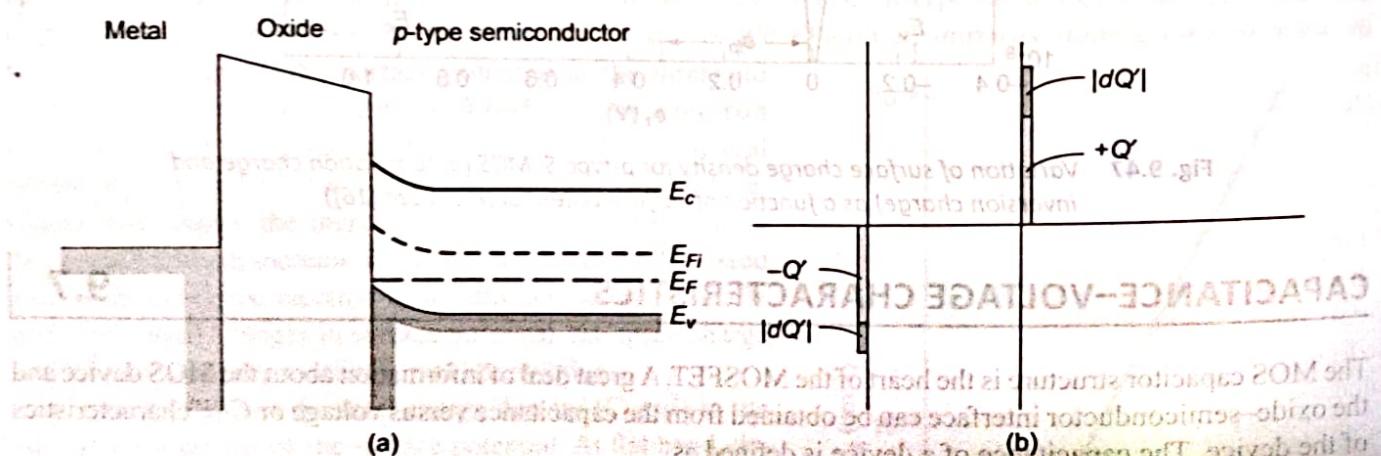


Fig. 9.48 (a) Energy-band diagram through a MOS capacitor for the accumulation mode **(b)** Differential charge distribution at accumulation for a differential change in gate voltage

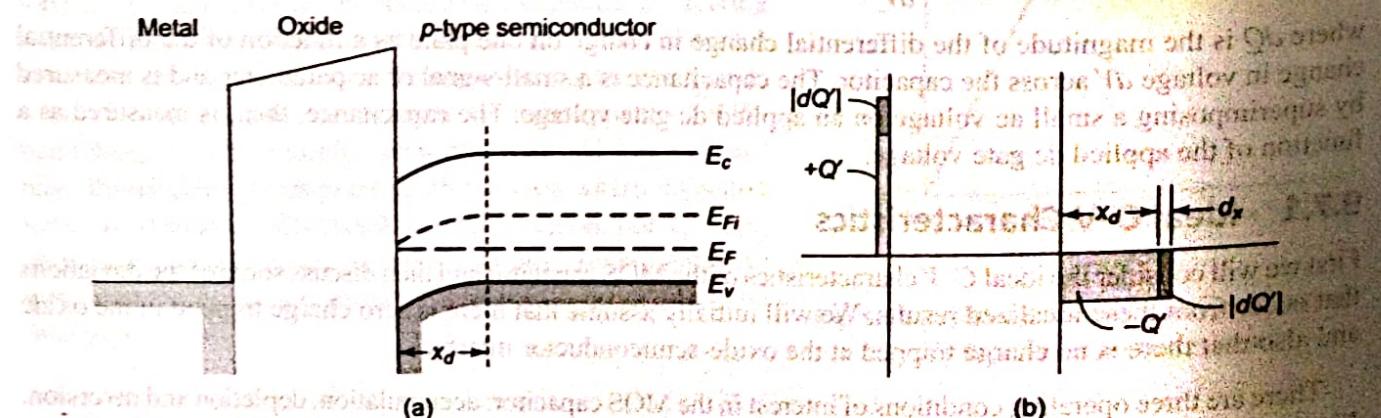


Fig. 9.49 (a) Energy-band diagram through a MOS capacitor for the depletion mode **(b)** Differential charge distribution at depletion for a differential change in gate voltage

$$C'(\text{depl}) = \frac{C_{\text{ox}} C'_{SD}}{C_{\text{ox}} + C'_{SD}} \quad (9.86\text{b})$$

$C_{\text{ox}} = \epsilon_{\text{ox}} / t_{\text{ox}}$ and $C'_{SD} = \epsilon_s / x_d$, Eq. (9.86b) can be written as

$$C'(\text{depl}) = \frac{C_{\text{ox}}}{1 + \frac{C_{\text{ox}}}{C'_{SD}}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}} + \left(\frac{\epsilon_{\text{ox}}}{\epsilon_s} \right) x_d} \quad (9.87)$$

As the space charge width increases, the total capacitance $C'(\text{depl})$ decreases.

We had defined the threshold inversion point to be the condition when the maximum depletion width is reached but there is essentially zero inversion charge density. This condition will yield a minimum capacitance C'_{\min} which is given by

$$C'_{\min} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}} + \left(\frac{\epsilon_{\text{ox}}}{\epsilon_s} \right) x_{dT}} \quad (9.88)$$

Figure 9.50(a) shows the energy-band diagram of this MOS device for the inversion condition. In the ideal case, a small incremental change in the voltage across the MOS capacitor will cause a differential change in the inversion layer charge density. The space charge width does not change. If the inversion charge can respond to the change in capacitor voltage as indicated in Fig. 9.50(b), then the capacitance is again just the oxide capacitance, or

$$C'(\text{inv}) = C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} \quad (9.89)$$

Figure 9.51 shows the ideal capacitance versus gate voltage, or $C-V$ characteristics of the MOS capacitor with a p-type substrate. The three dashed segments correspond to the three components C_{ox} , C'_{SD} , and C'_{\min} . The solid curve is the ideal net capacitance of the MOS capacitor. Moderate inversion, which is indicated in the figure, is the transition region between the point when only the space charge density changes with gate voltage and when only the inversion charge density changes with gate voltage.

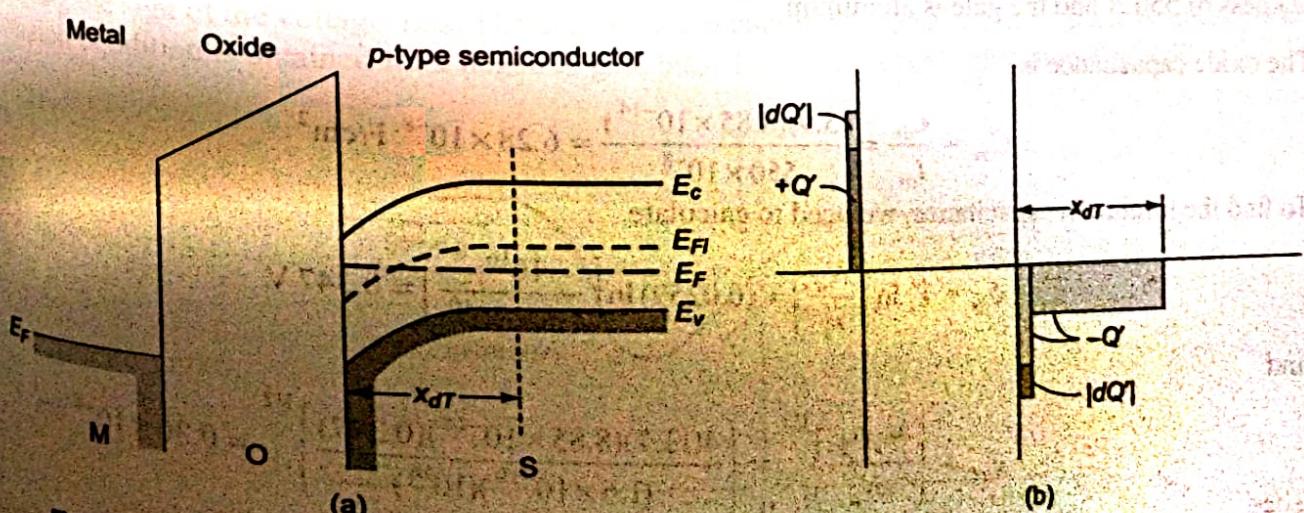


Fig. 9.50 (a) Energy-band diagram through an MOS capacitor for the inversion mode (b) Differential charge distribution at inversion for a low-frequency differential change in gate voltage

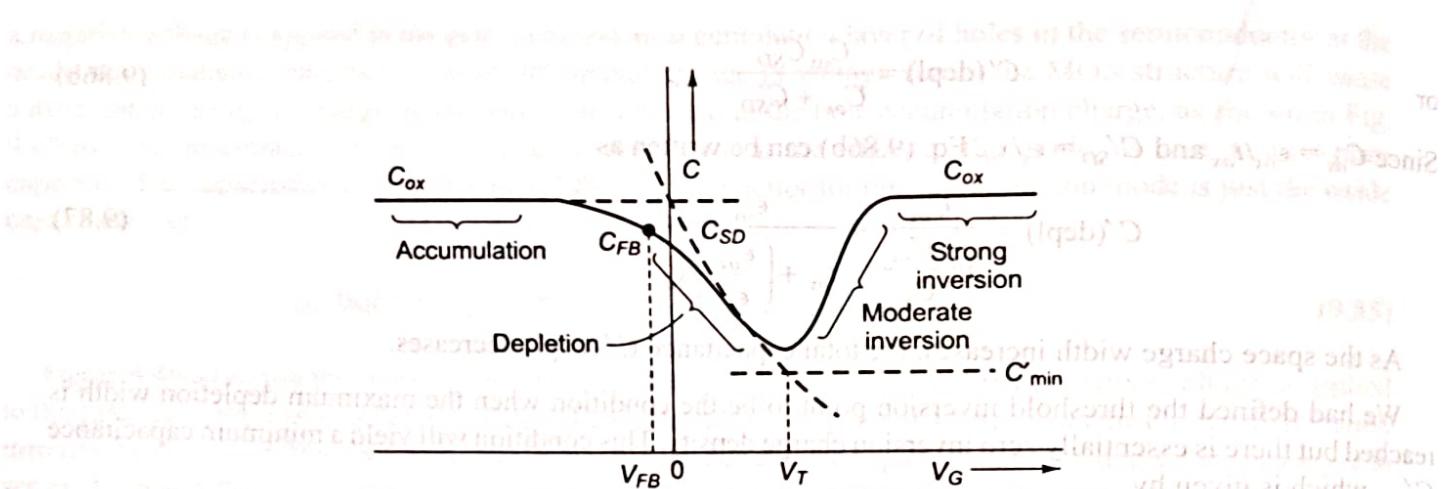


Fig. 9.51 Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate. Individual capacitance components are also shown.

The point on the curve that corresponds to the flat-band condition is of interest. The flat-band condition occurs between the accumulation and depletion conditions. The capacitance at flat band is given by

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s} \right) \sqrt{\left(\frac{kT}{e} \right) \left(\frac{\epsilon_s}{eN_a} \right)}} \quad (9.90)$$

We may note that the flat-band capacitance is a function of oxide thickness as well as semiconductor doping. The general location of this point on the C-V plot is shown in Fig. 9.51.

Example 9.11

Objective To calculate C_{ox} , C'_{min} , and C'_{FB} for an MOS capacitor.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{16}$ cm $^{-3}$. The oxide is silicon dioxide with a thickness of 550 Å and the gate is aluminum.

The oxide capacitance is

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{550 \times 10^{-8}} = 6.28 \times 10^{-8} \text{ F/cm}^2$$

To find the minimum capacitance, we need to calculate

$$\phi_{fp} = V_t \ln \left(\frac{N_a}{n_i} \right) = (0.0259) \ln \left(\frac{10^{16}}{1.5 \times 10^{10}} \right) = 0.347 \text{ V}$$

and

$$x_{dT} = \left\{ \frac{4\epsilon_s \phi_{fp}}{eN_a} \right\}^{1/2} = \left\{ \frac{4(11.7)(8.85 \times 10^{-14})(0.347)}{(1.6 \times 10^{-19})(10^{16})} \right\}^{1/2} = 0.30 \times 10^{-4} \text{ cm}$$

Then

$$C'_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s} \right) x_{dT}} = \frac{(3.9)(8.85 \times 10^{-14})}{(550 \times 10^{-8}) + \left(\frac{3.9}{11.7} \right) (0.3 \times 10^{-4})} = 2.23 \times 10^{-8} \text{ F/cm}^2$$

We may note that

$$\frac{C'_{\min}}{C_{ox}} = \frac{2.23 \times 10^{-8}}{6.28 \times 10^{-8}} = 0.355$$

The flat-band capacitance is

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s} \right) \sqrt{\left(\frac{kT}{e} \right) \left(\frac{\epsilon_s}{eN_a} \right)}} \quad (3.9)$$

$$(8.85 \times 10^{-14})$$

$$(550 \times 10^{-8}) + \left(\frac{3.9}{11.7} \right) \sqrt{(0.0259)(11.7)(8.85 \times 10^{-14}) / (1.6 \times 10^{-9})(10^{16})}$$

$$= 5.03 \times 10^{-8} \text{ F/cm}^2$$

We may also note that

$$\frac{C'_{FB}}{C_{ox}} = \frac{5.03 \times 10^{-8}}{6.28 \times 10^{-8}} = 0.80$$

Comment The ratios of C'_{\min} to C_{ox} and of C'_{FB} to C_{ox} are typical values obtained in $C-V$ plots.

Typical values of channel length and width are $2 \mu\text{m}$ and $20 \mu\text{m}$, respectively. The total gate oxide capacitance for this example is then

$$C_{oxT} = (6.28 \times 10^{-8})(2 \times 10^{-4})(20 \times 10^{-4}) = 0.025 \times 10^{-12} \text{ F} = 0.025 \text{ pF}$$

The total oxide capacitance in a typical MOS device is quite small.

The same type of ideal $C-V$ characteristics are obtained for an MOS capacitor with an n -type substrate by changing the sign of the voltage axis. The accumulation condition is obtained for a positive gate bias and the inversion condition is obtained for a negative gate bias. This ideal curve is shown in Fig. 9.52.

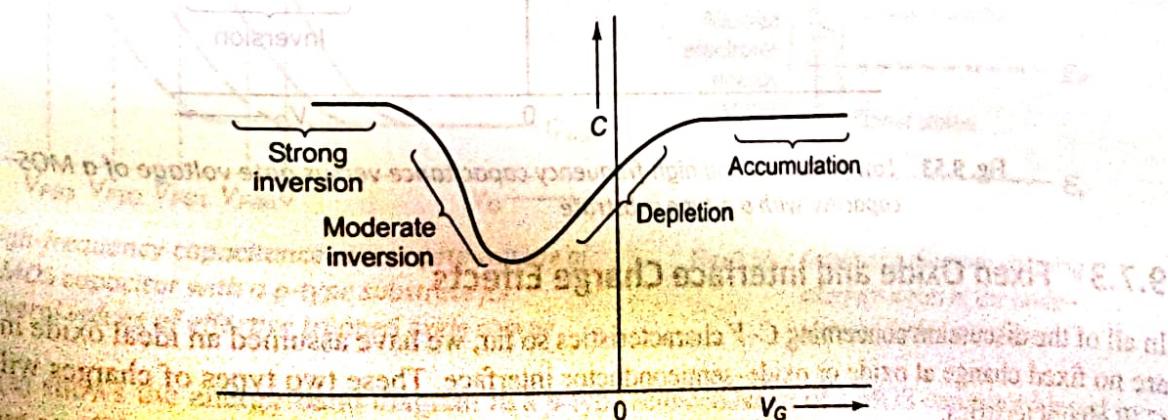


Fig. 9.52 Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with an n -type substrate

9.7.2 Frequency Effects

Figure 9.50(a) showed the MOS capacitor with a *p*-type substrate and biased in the inversion condition. We have argued that a differential change in the capacitor voltage in the ideal case causes a differential change in the inversion layer charge density. However, we must consider the source of electrons that produces a change in the inversion charge density.

There are two sources of electrons that can change the charge density of the inversion layer. The first source is by diffusion of minority carrier electrons from the *p*-type substrate across the space charge region. This diffusion process is the same as that in a reverse-biased *pn* junction that generates the ideal reverse saturation current. The second source of electrons is by thermal generation of electron-hole pairs within the space charge region. This process is again the same as that in a reverse-biased *pn* junction generating the reverse-biased generation current. Both of these processes generate electrons at a particular rate. The electron concentration in the inversion layer, then, cannot change instantaneously. If the ac voltage across the MOS capacitor changes rapidly, the change in the inversion layer charge will not be able to respond. The *C*–*V* characteristics will then be a function of the frequency of the ac signal used to measure the capacitance.

In the limit of a very high frequency, the inversion layer charge will not respond to a differential change in capacitor voltage. At a high-signal frequency, the differential change in charge occurs at the metal and in the space charge width in the semiconductor. The capacitance of the MOS capacitor is then C'_{\min} , which we discussed earlier.

The high-frequency and low-frequency limits of the *C*–*V* characteristics are shown in Fig. 9.53. In general, high frequency corresponds to a value on the order of 1 MHz and low frequency corresponds to values in the range of 5 to 100 Hz. Typically, the high-frequency characteristics of the MOS capacitor are measured.

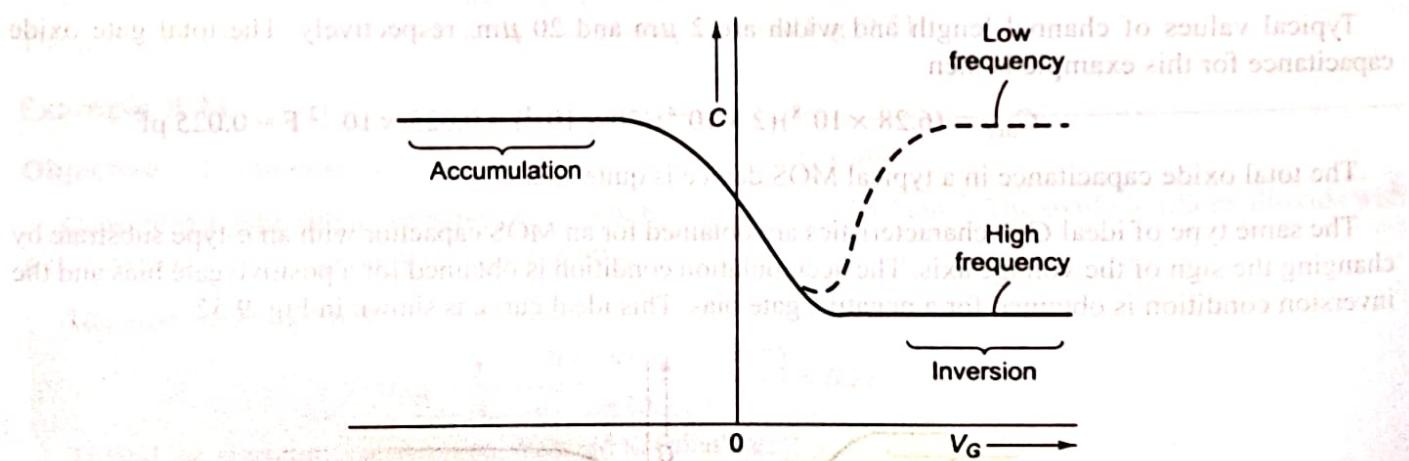


Fig. 9.53 Low-frequency and high-frequency capacitance versus gate voltage of a MOS capacitor with a *p*-type substrate

9.7.3 Fixed Oxide and Interface Charge Effects

In all of the discussion concerning *C*–*V* characteristics so far, we have assumed an ideal oxide in which there are no fixed charge at oxide or oxide–semiconductor interface. These two types of charges will change the *C*–*V* characteristics.

We previously discussed how the fixed oxide charge affects the threshold voltage. This charge will also affect the flat-band voltage. The flat-band voltage from Eq. (9.75) was given by

THE BASIC MOSFET OPERATION

9.8

9.8.1 MOSFET Structures

There are four basic MOSFET device types. Figure 9.58(a) shows an *n*-channel enhancement mode MOSFET. Implicit in the enhancement mode notation is the idea that the semiconductor substrate is not inverted directly under the oxide with zero gate voltage. A positive gate voltage induces the electron inversion layer, which then "connects" the *n*-type source and the *n*-type drain regions. The source terminal is the source of carriers that flow through the channel to the drain terminal. For this *n*-channel device, electrons flow from the source to the drain so the conventional current will enter the drain and leave the source. The conventional circuit symbol for this *n*-channel enhancement mode device is also shown in Fig. 9.59(a).

Figure 9.58(b) shows an *n*-channel depletion mode MOSFET. An *n*-channel region exists under the oxide with zero volts applied to the gate. However, we have shown that the threshold voltage of a MOS device with a *p*-type substrate may be negative; this means that an electron inversion layer already exists with zero gate voltage applied. Such a device is also considered to be a depletion mode device. The *n*-channel shown in this figure can be an electron inversion layer or an intentionally doped *n*-region. The conventional circuit symbol for the *n*-channel depletion mode MOSFET is also shown in the Fig. 9.59(b).

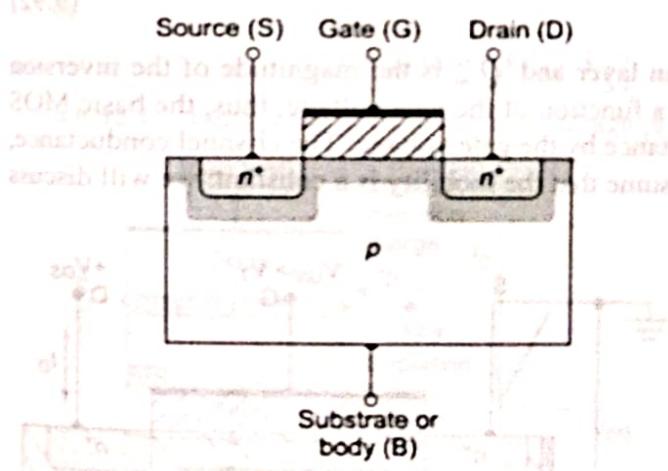


Fig. 9.58(a) Cross section and circuit symbol for an *n*-channel enhancement-mode MOSFET

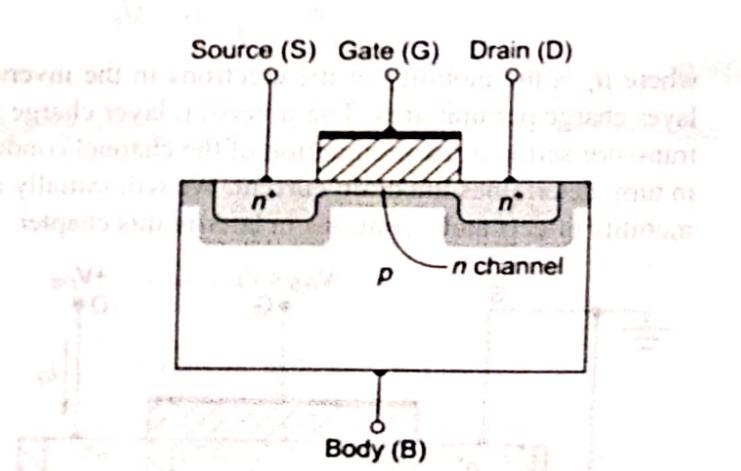


Fig. 9.58(b) Cross section and circuit symbol for an *n*-channel depletion-mode MOSFET

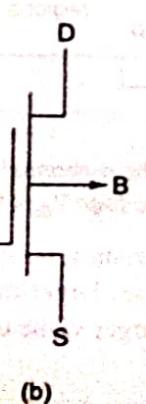
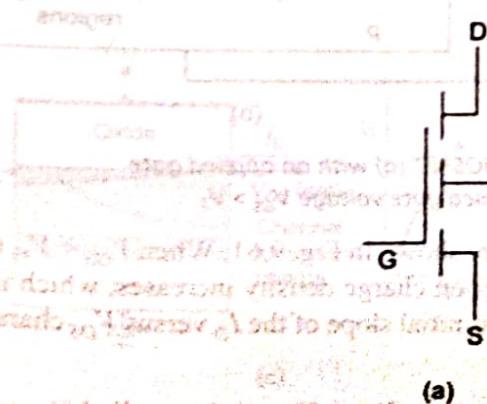


Fig. 9.59 Circuit symbol of *p*-channel (a) enhancement, and (b) depletion type of MOSFET

9.8.2 Current-Voltage Relationship: Concepts

Figure 9.60(a) shows an *n*-channel enhancement mode MOSFET with a gate-to-source voltage that is less than the threshold voltage and with only a very small drain-to-source voltage. The source and substrate, or body, terminals are held at ground potential. With this bias configuration, there is no electron inversion layer; the drain-to-substrate *pn* junction is reverse biased, and the drain current is zero (disregarding *pn* junction leakage currents).

Figure 9.60(b) shows the same MOSFET with an applied gate voltage such that $V_{GS} > V_T$. An electron inversion layer has been created so that, when a small drain voltage is applied, the electrons in the inversion layer will flow from the source to the positive drain terminal. The conventional current enters the drain terminal and leaves the source terminal. In this ideal case, there is no current through the oxide to the gate terminal.

For small V_{DS} values, the channel region has the characteristics of a resistor, so we can write

$$I_D = g_d V_{DS} \quad (9.91)$$

where g_d is defined as the channel conductance in the limit as $V_{DS} \rightarrow 0$. The channel conductance is given by

$$g_d = \frac{W}{L} \cdot \mu_n |Q'_n| \quad (9.92)$$

where μ_n is the mobility of the electrons in the inversion layer and $|Q'_n|$ is the magnitude of the inversion layer charge per unit area. The inversion layer charge is a function of the gate voltage; thus, the basic MOS transistor action is the modulation of the channel conductance by the gate voltage. The channel conductance, in turn, determines the drain current. We will initially assume that the mobility is a constant; we will discuss mobility effects and variations in later in this chapter.

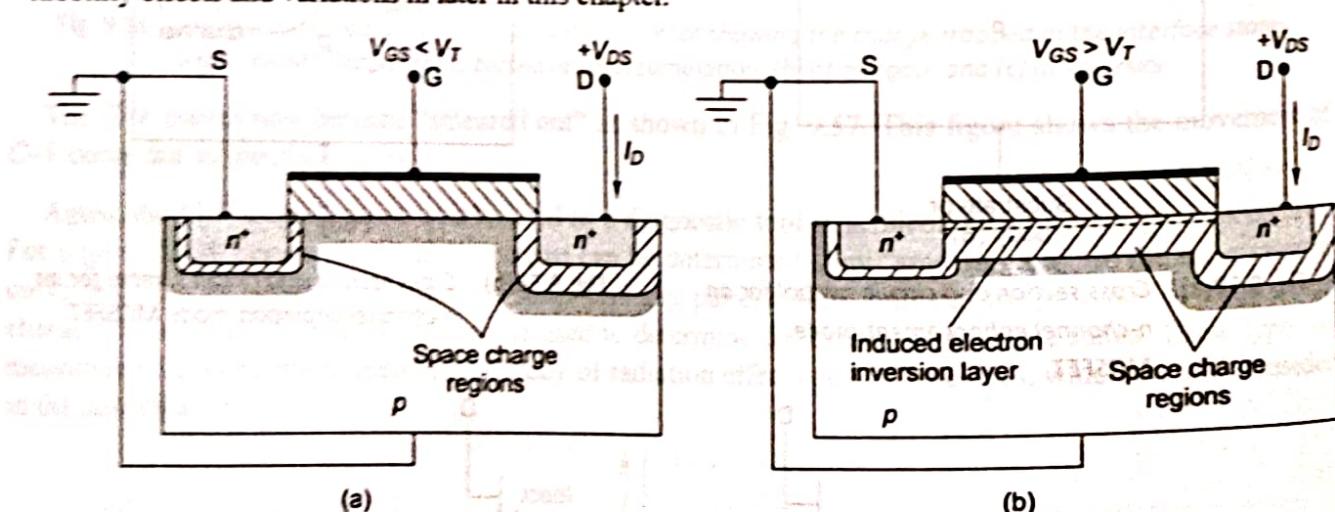


Fig. 9.60 The *n*-channel enhancement mode MOSFET (a) with an applied gate voltage $V_{GS} < V_T$, and (b) with an applied gate voltage $V_{GS} > V_T$

The I_D versus V_{DS} characteristics, for small values of V_{DS} , are shown in Fig. 9.61. When $V_{GS} < V_T$, the drain current is zero. As V_{GS} becomes larger than V_T , channel inversion charge density increases, which increases the channel conductance. A larger value of g_d produces a larger initial slope of the I_D versus V_{DS} characteristic as shown in the figure.

Figure 9.62(a) shows the basic MOS structure for the case when $V_{GS} > V_T$ and the applied V_{DS} voltage is small. The thickness of the inversion channel layer in the figure qualitatively indicates the relative charge

density, which is essentially constant along the entire channel length for this case. The corresponding I_D versus V_{DS} curve is shown in the figure.

Figure 10.62(b) shows the situation when the V_{DS} value increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases. The incremental conductance of the channel at the drain decreases, which then means that the slope of the I_D versus V_{DS} curve will decrease. This effect is shown in the I_D versus V_{DS} curve in the figure.

When V_{DS} increases to the point where the potential drop across the oxide at the drain terminal is equal to V_T , the induced inversion charge density is zero at the drain terminal. This effect is schematically shown in Fig. 9.62(c). At this point, the incremental conductance at the drain is zero, which means that the slope of the I_D versus V_{DS} curve is zero. We can write

$$V_{GS} - V_{DS}(\text{sat}) = V_T \quad (9.93)$$

or

$$V_{DS}(\text{sat}) = V_{GS} - V_T \quad (9.94)$$

where $V_{DS}(\text{sat})$ is the drain-to-source voltage producing zero inversion charge density at the drain terminal.

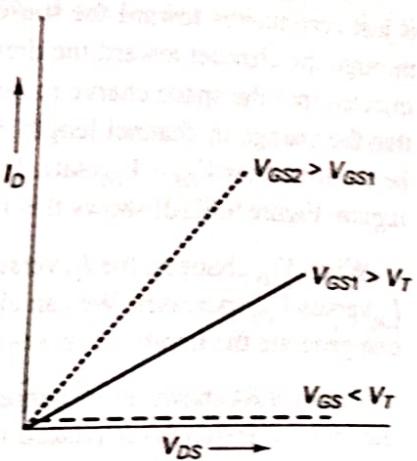


Fig. 9.61 I_D versus V_{DS} characteristics for small values of V_{DS} at three V_{GS} voltages

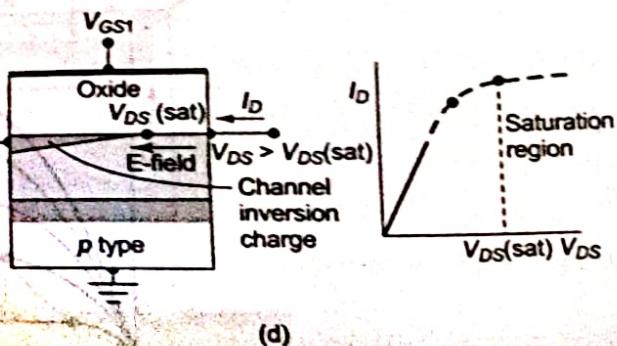
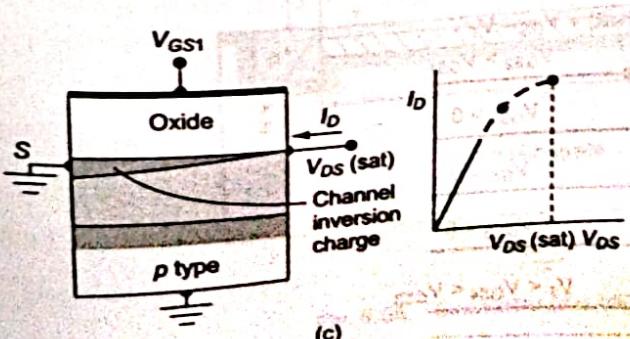
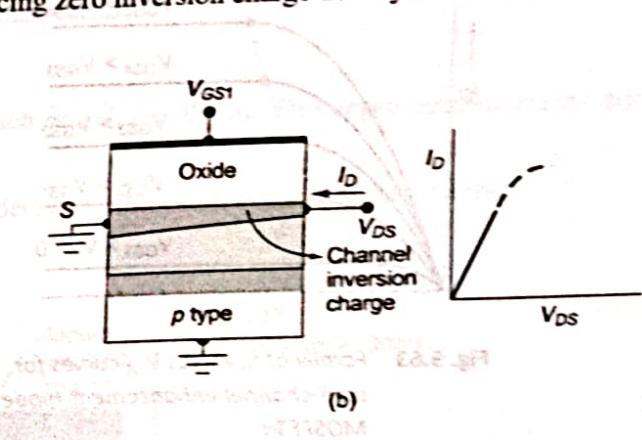
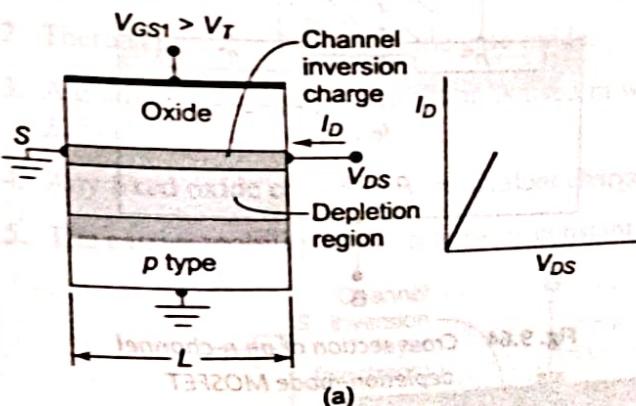


Fig. 9.62 Cross section and I_D versus V_{DS} curve when $V_{GS} < V_T$ for (a) a small V_{DS} value, (b) a larger V_{DS} value, and (c) a value of $V_{DS} = V_{DS}(\text{sat})$, and (d) a value of $V_{DS} > V_{DS}(\text{sat})$.

When V_{DS} becomes larger than the $V_{DS}(\text{sat})$ value, the point in the channel at which the inversion charge is just zero moves toward the source terminal. In this case, electrons enter the channel at the source, travel through the channel toward the drain, and then, at the point where the charge goes to zero, the electrons are injected into the space charge region where they are swept by the E -field to the drain contact. If we assume that the change in channel length ΔL is small compared to the original length L , then the drain current will be a constant for $V_{DS} > V_{DS}(\text{sat})$. The region of the I_D versus V_{DS} characteristic is referred to as the *saturation region*. Figure 9.62(d) shows this region of operation.

When V_{GS} changes, the I_D versus V_{DS} curve will change. We saw that, if V_{GS} increases, the initial slope of I_D versus V_{DS} increases. We can also note from Eq. (9.94) that the value of $V_{DS}(\text{sat})$ is a function of V_{GS} . We can generate the family of curves for this *n*-channel enhancement mode MOSFET as shown in Fig. 9.63.

Figure 9.64 shows an *n*-channel depletion mode MOSFET. If the *n*-channel region is actually an induced electron inversion layer created by the metal-semiconductor work function difference and fixed charge in the oxide, the current-voltage characteristics are exactly the same as we have discussed, except that V_T is a negative quantity. A positive gate voltage will create an electron accumulation layer, which increases the drain current. One basic requirement for this device is that the channel thickness t_c must be less than the maximum induced space charge width in order to be able to turn the device off. The general I_D versus V_{DS} family of curves for an *n*-channel depletion mode MOSFET is shown in Fig. 9.65.

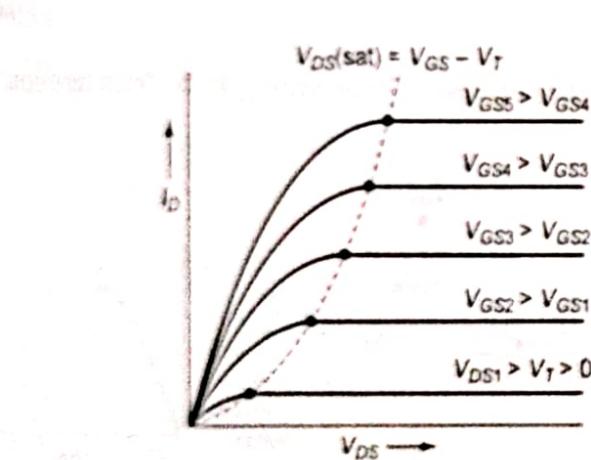


Fig. 9.63 Family of I_D versus V_{DS} curves for an *n*-channel enhancement-mode MOSFET

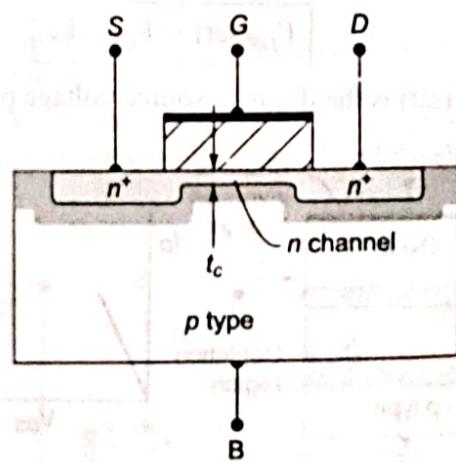


Fig. 9.64 Cross section of an *n*-channel depletion-mode MOSFET

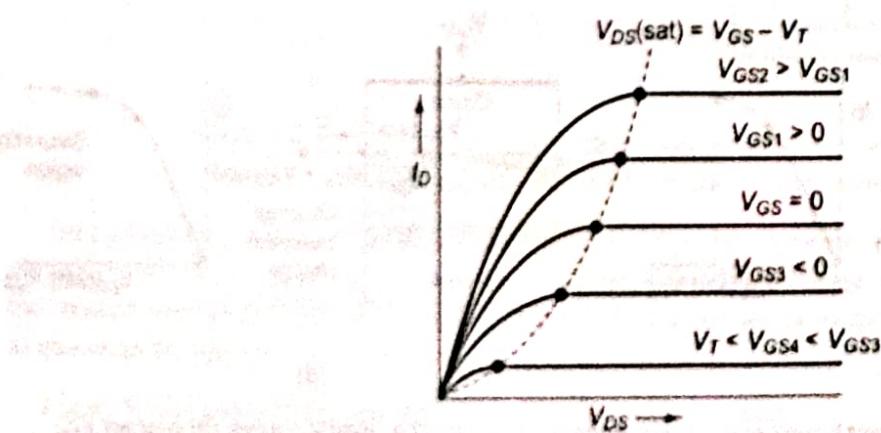


Fig. 9.65 Family of I_D versus V_{DS} curves for an *n*-channel depletion-mode MOSFET

In the next section we will derive the ideal current-voltage relation for the *n*-channel MOSFET. In the nonsaturation region, we will obtain

$$I_D = \frac{W\mu_n C_{ox}}{2L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad (9.95)$$

and, in the saturation region, we will have

$$I_D = \frac{W\mu_n C_{ox}}{2L} (V_{GS} - V_T)^2 \quad (9.96)$$

The operation of a *p*-channel device is the same as that of the *n*-channel device, except the charge carrier is the hole and the conventional current direction and voltage polarities are reversed.

9.8.3 Current-Voltage Relationship: Mathematical Derivation

In the previous section, we qualitatively discussed the current-voltage characteristics. In this section, we will derive the mathematical relation between the drain current, the gate-to-source voltage, and the drain-to-source voltage. Figure 9.66 shows the geometry of the device that we will use in this derivation.

In this analysis, we will make the following assumptions:

1. The current in the channel is due to drift rather than diffusion.
2. There is no current through the gate oxide.
3. A gradual channel approximation is used in which $\partial E_y / \partial y \gg \partial E_x / \partial x$. This approximation means that E_x is essentially a constant.
4. Any fixed oxide charge is an equivalent charge density at the oxide-semiconductor interface.
5. The carrier mobility in the channel is constant.

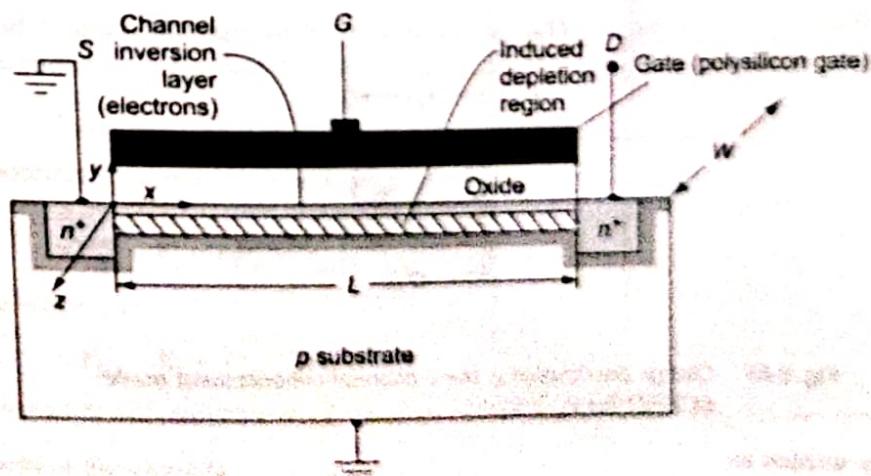


Fig. 9.66 Geometry of a MOSFET for I_D versus V_{DS} derivation.

THE BASIC MOSFET OPERATION

9.8

9.8.1 MOSFET Structures

There are four basic MOSFET device types. Figure 9.58(a) shows an *n*-channel enhancement mode MOSFET. Implicit in the enhancement mode notation is the idea that the semiconductor substrate is not inverted directly under the oxide with zero gate voltage. A positive gate voltage induces the electron inversion layer, which then "connects" the *n*-type source and the *n*-type drain regions. The source terminal is the source of carriers that flow through the channel to the drain terminal. For this *n*-channel device, electrons flow from the source to the drain so the conventional current will enter the drain and leave the source. The conventional circuit symbol for this *n*-channel enhancement mode device is also shown in Fig. 9.59(a).

Figure 9.58(b) shows an *n*-channel depletion mode MOSFET. An *n*-channel region exists under the oxide with zero volts applied to the gate. However, we have shown that the threshold voltage of a MOS device with a *p*-type substrate may be negative; this means that an electron inversion layer already exists with zero gate voltage applied. Such a device is also considered to be a depletion mode device. The *n*-channel shown in this figure can be an electron inversion layer or an intentionally doped *n*-region. The conventional circuit symbol for the *n*-channel depletion mode MOSFET is also shown in the Fig. 9.59(b).

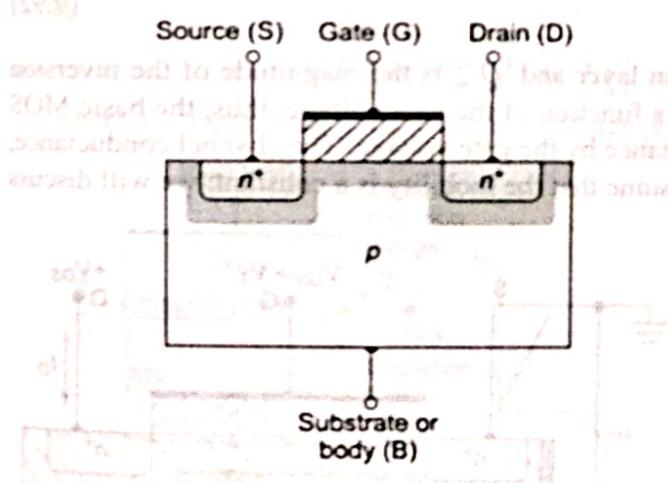


Fig. 9.58(a) Cross section and circuit symbol for an *n*-channel enhancement-mode MOSFET

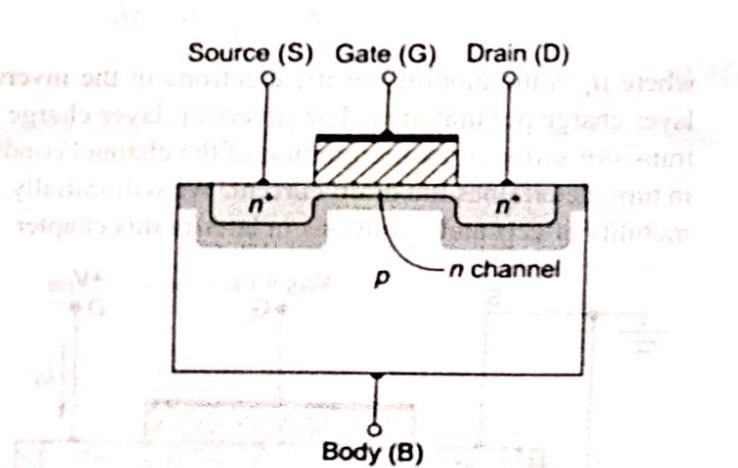


Fig. 9.58(b) Cross section and circuit symbol for an *n*-channel depletion-mode MOSFET

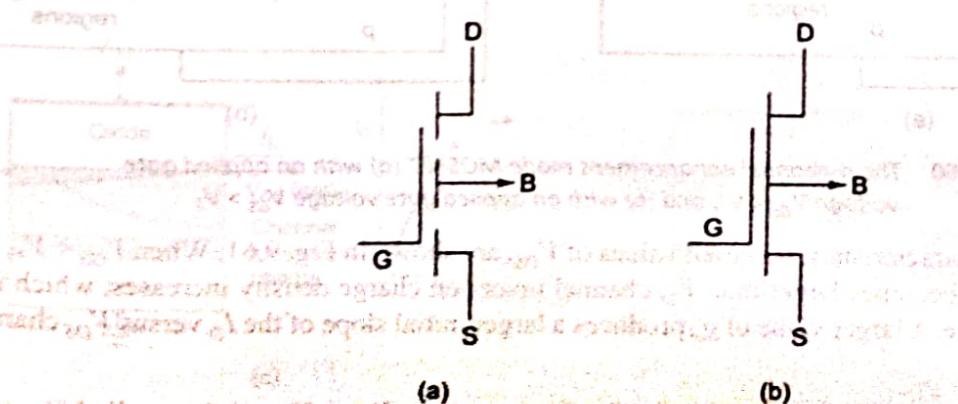


Fig. 9.59 Circuit symbol of *p*-channel (a) enhancement, and (b) depletion type of MOSFET