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BJT FABRICATION

The first transistor invented by Bardeen and Brattain in 1947 was the point contact transistor. In this device two sharp metal wires, formed an "emitter" of carriers & a "collector" of carriers. These wires were simply pressed onto a slab of Ge which provided a "base" support, through which the injected carriers flowed. This basic invention led to the BJT, in which charge injection & collection was achieved using two p-n junction in proximity to each other. The pn junctions in BJTs can be formed in a variety of ways using thermal diffusion, but modern devices are generally made using ion implantation.

Process flow of double polysilicon, self aligned npn Si BJT

The n-p-n transistors is more widely used than p-n-p transistors because of the higher mobility of electrons compared with holes.

A p-type Si substrate is oxidized, windows are defined using photolithography and etched in the oxide. Using the photo resist and oxide as an implant mask, a donor with very small diffusivity in Si, such as As or Sb, is implanted into the open window to form a highly conductive n^+ layer.

Subsequently, the photoresist and the oxide are removed, and a lightly doped n-type epitaxy layer is grown. During this high temperature growth, the implanted n^+ layer diffuses only slightly toward the surface & becomes a conductive buried collector (also called a sub-collector).

The n^+ sub-collector layer guarantees a low collector ohmic contact, sometimes through the use of an optional, masked deep n^+ "sinker" implant or diffusion only in the collector contact region. The lightly doped n-type collector region above the n^+ sub-collector in the part of the BJT where the base and emitter are formed ensures a high base-collector reverse breakdown voltage.

For integrated circuits involving many interconnected transistors, the electrical cross-talk between them can be achieved by LOCOS isolation. The LOCOS (Local oxidation of silicon) forms a field oxide isolation oxides after a B channel stops implant.

Another isolation scheme is used for high-density bipolar circuits. Which involves the formation of shallow trenches by (RIE) Reactive ion etching, backfilled with oxide and polysilicon. A nitride layer is patterned and used as an etch mask for an anisotropic etch of the silicon to form the trench. Oxidation inside the trench forms an insulating layer, and the trench is then filled with oxide by low-pressure chemical vapor deposition (LPCVD).

A polysilicon layer is deposited by LPCVD, and doped heavily p^+ with B either during deposition or by ion implantation. An oxide layer is deposited next by LPCVD. Using photolithography with the base/emitter mask, a window is etched in the polysilicon/oxide stack by RIE.

A heavily doped "extrinsic" p^+ base is formed by diffusion of B into the substrate, in order to provide a low-resistance, high-speed base ohmic contact. An oxide layer is then deposited

deposited by LPCVD and B is implanted into the base window. This base implant forms a more lightly p doped "intrinsic" base through which most of the current flows from the emitter to the collector.

Another LPCVD oxide layer is deposited to close up the base window further, and the oxide is etched all the way to the Si substrate by RIE, leaving oxide spacers on the sidewalls. Heavily n+ doped (As) polisilicon is then deposited on the substrate, patterned and etched, forming polysilicon emitter (poly emitter) and collector contact.

In this process two LPCVD polysilicon layers are used, so it is referred to as the double-polysilicon process. Arsenic from the polysilicon is diffused into the substrate to form the n+ emitter region nested within the base in a self-aligned manner, as well as the n+ collector contact. The n+ emitter region is made to lie within the intrinsic base by using oxide sidewall spacers. This is critical because otherwise the emitter gets shorted to the collector. It also maintains a gap between the n+ emitter and the p+ extrinsic base, otherwise the emitter-base junction capacitance becomes too high. The difference between the emitter-base junction and the base-collector junction determines the base width. This is made very narrow in high gain, high speed BJTs.

Finally, an oxide layer is deposited by CVD, windows are etched in it corresponding to the emitter (E), base (B), and collector (C) contacts.