It should be noted that the  $\alpha_{\max}$  must be kept below 50%, so that when the consformer voltage is clamped through the tertiary winding, the integral of the olt-seconds between the input voltage, when  $Q_1$  is ON, and the clamping level, then  $Q_1$  is OFF, amounts to zero. Duty cycles above 50 per cent, will upset the olt-seconds balance, driving the transformer into saturation, which in turn roduces high collector current spikes that may destroy the switching transistor.

Also, care must be taken during construction to couple the tertiary winding ghtly to the primary (bifilar wound) to eliminate fatal voltage spikes caused by akage inductance.

## 16.3.2.2 Two-Transistor Forward Converters

Figure 16.15(a) shows the circuit diagram of the two-transistor forward converter, and the associated waveforms are shown in Fig. 16.15(b). This configuration educes the voltage ratings of the transistor to  $E_{\rm dc(max)}$  instead of  $2\,E_{\rm dc(max)}$  (Single-ded configuration). The circuits operate as follows:

- Mode  $I(Q_1, Q_2 \text{ and } D_3 \text{ ON})$ : At t=0, transistors  $Q_1$  and  $Q_2$  are turned on multaneously. The supply voltage  $E_{\rm dc}$  is connected across the primary winding. The primary current starts increasing linearly from  $I_{\rm min}$  to  $I_{\rm max} + I_{\rm mg}$ , where  $I_{\rm mg}$  the magnetizing component shown by shaded area in the primary current aveform. Due to the specific winding directions, the induced voltage in the entiary winding will reverse bias diode  $D_{\rm m}$  and the induced voltage in the secondary winding will forward bias the rectifying diode  $D_3$ . The secondary will deliver ower to the inductance L, capacitor C and the load as shown in Fig. 16.15(b).
- ii) Mode II ( $Q_1$ ,  $Q_2$ , OFF and  $D_4$ .  $D_m$ ): At  $t = t_1$ , both the transistors  $Q_1$  and  $Q_2$  are turned-off simultaneously. Due to the sudden interruption of primary turrent, the induced voltage across the primary winding will change its polarities shown in Fig. 16.15(b). This voltage will forward bias the diodes  $D_1$ ,  $D_2$  and they will clamp the primary voltage to  $E_{dc}$  volts.

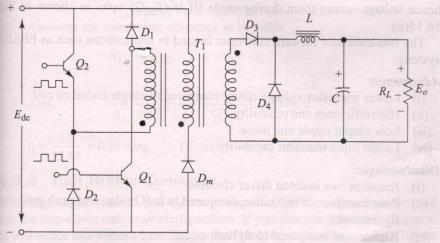


Fig. 16.15(a) Two-transistor forward converter