MODULE - 4

Design synchronous mod-6 counter counting sequence is 000, 001, 100, 110, 111, 101, 000 etc by obtaining its minimal sum equ. using SR flipflop :

→ Application table :

Q	Q^+	S	R
0	0	0	–
0	1	1	0
1	0	0	1
1	1	–	0

Excitation table :

Present state			Next state			outputs					
Q_a	Q_b	Q_c	Q_a^+	Q_b^+	Q_c^+	S_a	R_a	S_b	R_b	S_c	R_c
0	0	0	0	0	1	0	–	0	–	1	0
0	0	1	1	0	0	1	0	0	–	0	1
1	0	0	1	1	0	–	0	1	0	0	–
1	1	0	1	1	1	–	0	–	0	1	0
1	1	1	1	0	1	–	0	0	1	–	0
1	0	1	0	0	0	0	1	0	–	0	1

Sa

$Q_a \backslash Q_bQ_c$	00	01	11	10
0	0	1	–	–
1	–	0	–	–

$S_a = \overline{Q}_a Q_c$

R_a

$Q_a \backslash Q_bQ_c$	00	01	11	10
0	–	0	–	–
1	0	1	0	0

$R_a = Q_a \overline{Q}_b Q_c$

S_b

$Q_a \backslash Q_bQ_c$	00	01	11	10
0	0	0	–	–
1	1	0	0	–

$S_b = Q_a\overline{Q_c}$

R_b

$Q_a \backslash Q_bQ_c$	00	01	11	10
0	–	–	–	–
1	0	–	1	0

$R_b = Q_c$

S_c

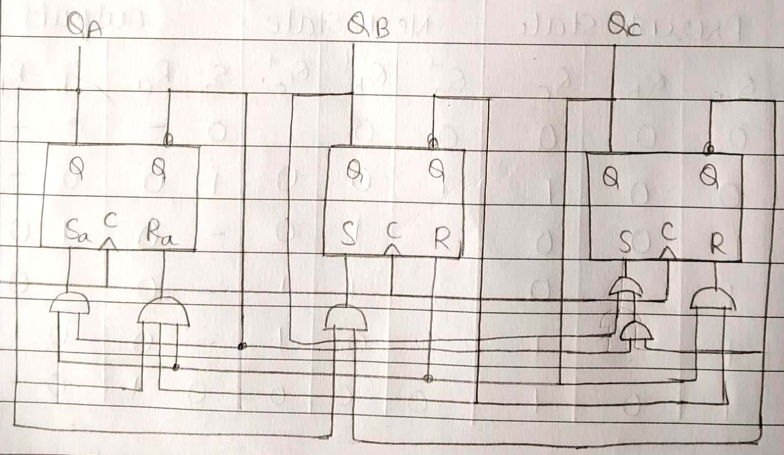
$Q_a \backslash Q_bQ_c$	00	01	11	10
0	1	0	–	–
1	0	0	0	1

$S_c = \overline{Q_a}\,\overline{Q_c} + Q_b$

R_c

$Q_a \backslash Q_bQ_c$	00	01	11	10
0	0	1	–	–
1	–	1	0	0

$R_c = \overline{Q_b}Q_c$



Realize 3 bit binary synchronous up-counter using JK flipflop.

Application table :

Q	Q^+	J	K
0	0	0	-
0	1	1	-
1	0	-	1
1	1	-	0

Excitation table

Q_1	Q_2	Q_3	Q_1^+	Q_2^+	Q_3^+	J_1	K_1	J_2	K_2	J_3	K_3
0	0	0	0	0	1	0	-	0	-	1	-
0	0	1	0	1	0	0	-	1	-	-	1
0	1	0	0	1	1	0	-	-	0	1	-
0	1	1	1	0	0	1	-	-	1	-	1
1	0	0	1	0	1	-	0	0	-	1	-
1	0	1	1	1	0	-	0	1	-	-	1
1	1	0	1	1	1	-	0	-	0	1	-
1	1	1	0	0	0	-	1	-	1	-	1

J_1

$Q_1 \backslash Q_2Q_3$	00	01	11	10
0	0	0	1	0
1	-	-	-	-

$J_1 = Q_2 Q_3$

K_1

$Q_1 \backslash Q_2Q_3$	00	01	11	10
0	-	-	-	-
1	0	0	1	0

$K_1 = Q_2 Q_3$

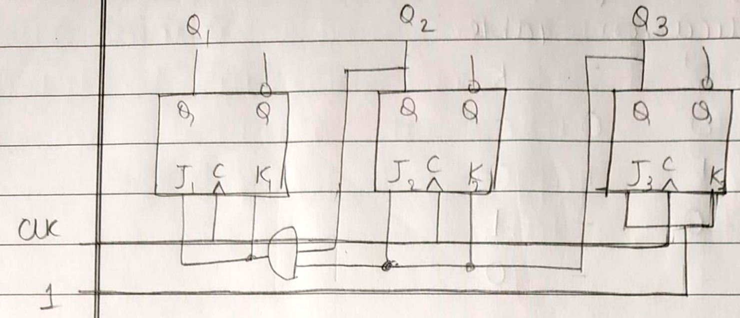
$Q_1 \backslash Q_2Q_3$	00	01	11	10
0	0	1	-	-
1	0	1	-	-

$J_2 = Q_3$

$Q_1 \backslash Q_2Q_3$	00	01	11	10
	-	-	1	0
	-	-	1	0

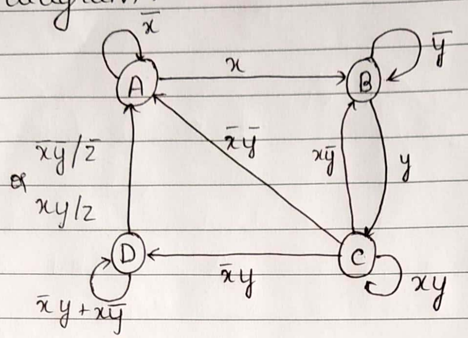
$K_2 = Q_3$

$J_3 = K_3 = 1$



state diagrams tables :

These are tabular forms of state diagram.



State table :

Present Sent	00	Z	01	Z	11	Z	10	Z
A	A	0	A	0	B	0	B	0
B	B	0	C	0	C	0	B	0
C	A	0	D	0	C	0	B	0
D	A	0	D	0	A	1	D	0

(Next state)

~~Do again~~ Transition table

Construct a mealy state diagram that will detect input sequence 10110 when input pattern is detected Z is asserted high. Write the state diagram

X = 10110110110

Z = 00001001001

Step 1: A as th

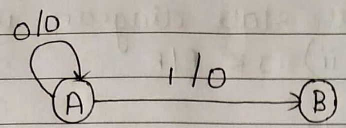
Step 2: o

Step 3: 0/0

Step4: 0/0

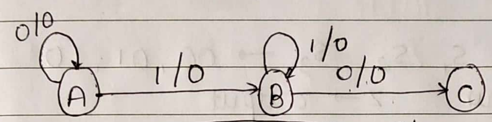
Step 5: 0/0

te

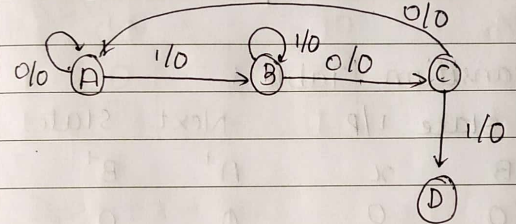


Step 1: A is the initial stage with input = 0 as soon as it detects high bit change that state from A to B

Step 2:

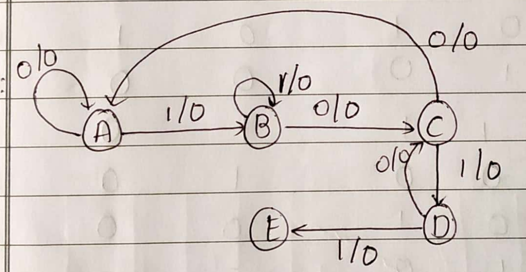


step 3:



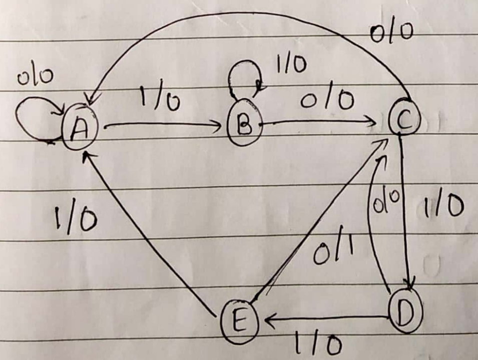
Z
0
0
0
0

Step4:



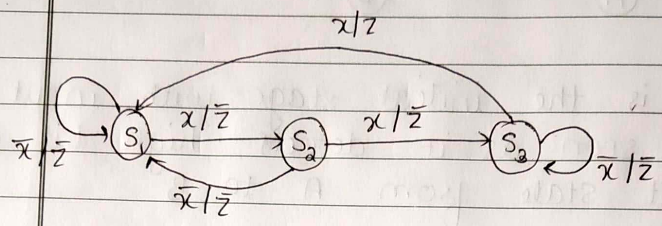
0110

Step 5:



tate

a system represented by
Realize ^ the foll state diagram using
i) D-flipflop. ii) JK F/F



3 states S_1 S_2 S_3 → 00, 01, 10
x → input z → output

State transition Table :

Present state		I/P	Next state		O/P
A	B	x	A^+	B^+	Z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	–	–	–
1	1	1	–	–	–

Excitation table :

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

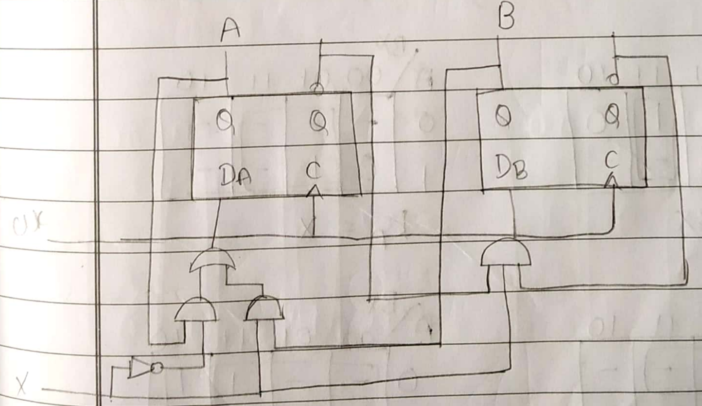
						F/F inputs	
A	B	x	A^+	B^+	Z	D_A	D_B
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	1	0	-	-	-	-	-
1	1	1	-	-	-	-	-

A \ BX	00	01	11	10
0	0	0	1	0
1	1	0	-	-

$D_A = Bx + A\bar{x}$

A \ BX	00	01	11	10
0	0	1	0	0
1	0	0	-	-

$D_B = \bar{A}\bar{B}X$



O/P
Z
0
0
0
0
0
1
-
-

Application table for JK

Q	Q^+	J	K
0	0	0	–
0	1	1	–
1	0	–	1
1	1	–	0

Excitation table :

A	B	X	A^+	B^+	Z	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	–	0	–
0	0	1	0	1	0	0	–	1	–
0	1	0	0	0	0	0	–	–	1
0	1	1	1	0	0	1	–	–	1
1	0	0	1	0	0	–	0	0	–
1	0	1	0	0	1	–	1	0	–
1	1	0	–	–	–	–	–	–	–
1	1	1	–	–	–	–	–	–	–

A \ BX	00	01	11	10
0	0	0	1	0
1	–	–	–	–

$J_A = BX$

A \ BX	00	01	11	10
0	–	–	–	–
1	0	1	–	–

$K_A = X$

A \ BX	00	01	11	10
0	0	1	–	–
1	0	0	–	–

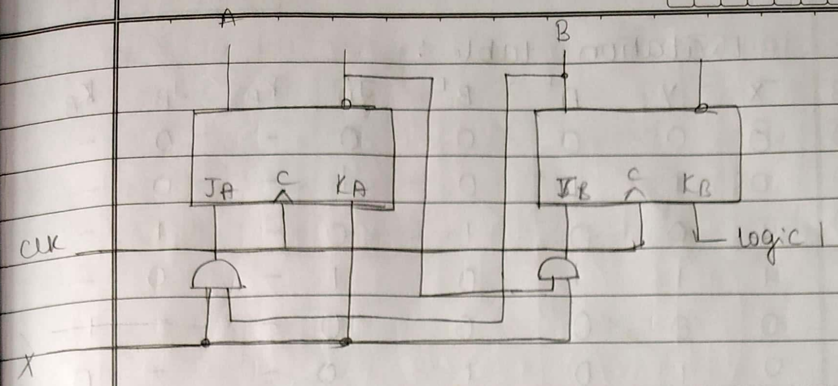
$J_B = \bar{A}X$

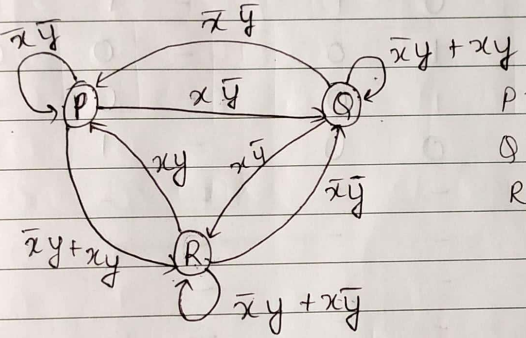
A \ BX	00	01	11	10
0	–	–	1	1
1	–	–	–	–

$K_B = 1$

clk

X





P - 00
Q - 01
R - 10

A	B	X	Y	A^+	B^+
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	0

1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Excitation table :

A	B	x	y	A^+	B^+	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	-	0	-
0	0	0	1	1	0	1	-	0	-
0	0	1	0	0	1	0	-	1	-
0	0	1	1	1	0	1	-	0	-
0	1	0	0	0	0	0	-	-	1
0	1	0	1	0	1	0	-	-	0
0	1	1	0	1	0	1	-	-	1
0	1	1	1	0	1	0	-	-	0
1	0	0	0	0	1	-	1	1	-
1	0	0	1	1	0	-	0	0	-
1	0	1	0	1	0	-	0	0	-
1	0	1	1	0	0	-	1	0	-
1	1	0	0	-	-	-	-	-	-
1	1	0	1	-	-	-	-	-	-
1	1	1	0	-	-	-	-	-	-
1	1	1	1	-	-	-	-	-	-

AB \ XY	00	01	11	10
00	0_0	1_1	1_3	0_2
01	0_4	0_5	0_7	1_6
11	$-_{12}$	$-_{13}$	$-_{15}$	$-_{14}$
10	$-_8$	$-_9$	$-_{11}$	$-_{10}$

AB \ XY	00	01	11	10
00	$-_0$	$-_1$	$-_3$	$-_2$
01	$-_4$	$-_5$	$-_7$	$-_6$
11	$-_{12}$	$-_{13}$	$-_{15}$	$-_{14}$
10	1_8	0_9	1_{11}	0_{10}

$J_A = \overline{B}Y + BX\overline{Y}$

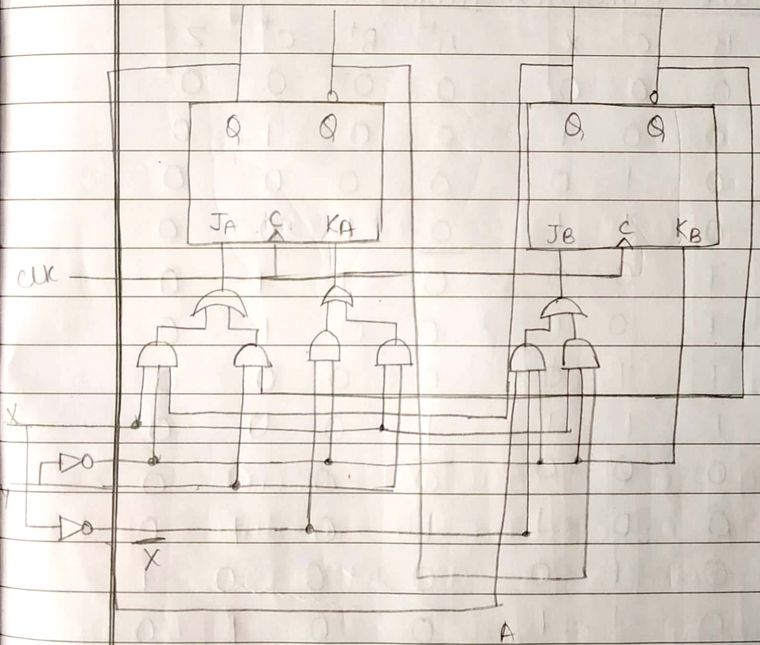
$K_A = \overline{X}\overline{Y} + XY$

AB \ XY	00	01	11	10
00	0_{0}	0_{1}	0_{3}	1_{2}
01	$-_{4}$	$-_{5}$	$-_{7}$	$-_{6}$
11	$-_{12}$	$-_{13}$	$-_{15}$	$-_{14}$
10	1_{8}	0_{9}	0_{11}	0_{10}

$J_B = A\overline{X}\overline{Y} + \overline{A}X\overline{Y}$

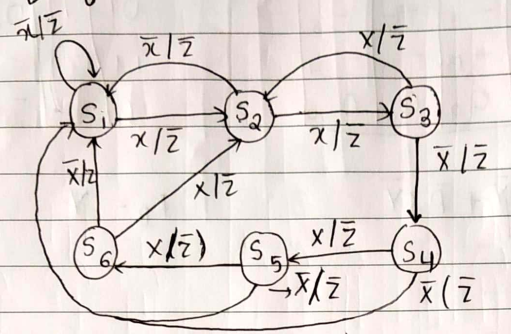
AB \ XY	00	01	11	10
00	$-_{0}$	$-_{1}$	$-_{3}$	$-_{2}$
01	1_{4}	0_{5}	0_{7}	1_{6}
11	$-_{12}$	$-_{13}$	$-_{15}$	$-_{14}$
10	$-_{8}$	$-_{9}$	$-_{11}$	$-_{10}$

$K_B = \overline{Y}$



Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

Implement state diagram show thar using T-flip flop.



$S_1 - 000$
$S_2 - 001$
$S_3 - 010$
$S_4 - 011$
$S_5 - 100$
$S_6 - 101$

<u>state transition table</u> :

A	B	C	X	A^+	B^+	C^+	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	1	1	0
0	1	0	1	0	0	1	0
0	1	1	0	0	0	0	0
0	1	1	1	1	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	-	-	-	-
1	1	0	1	-	-	-	-
1	1	1	0	-	-	-	-
1	1	1	1	-	-	-	-

Excita

A	B	C
0	0	0
0	0	0
0	0	1
0	0	1
0	1	0
0	1	0
0	1	1
0	1	1
1	0	0
1	0	0
1	0	1
1	0	1
1	1	0
1	1	0
1	1	1
1	1	1

AB \ CX	00
00	0
01	0
11	-
10	1

$T_A = A$

AB \
00
01
11
10

Excitation table :

A	B	C	X	A^+	B^+	C^+	T_A	T_B	T_C
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0	1
0	0	1	0	0	0	0	0	0	1
0	0	1	1	0	1	0	0	1	1
0	1	0	0	0	1	1	0	0	1
0	1	0	1	0	0	1	0	1	1
0	1	1	0	0	0	0	0	1	1
0	1	1	1	1	0	0	1	1	1
1	0	0	0	0	0	0	1	0	0
1	0	0	1	1	0	1	0	0	1
1	0	1	0	0	0	0	1	0	1
1	0	1	1	0	0	1	1	0	0
1	1	0	0	-	-	-	-	-	-
1	1	0	1	-	-	-	-	-	-
1	1	1	0	-	-	-	-	-	-
1	1	1	1	-	-	-	-	-	-

AB \ CX	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	-	-	-	-
10	1	0	1	1

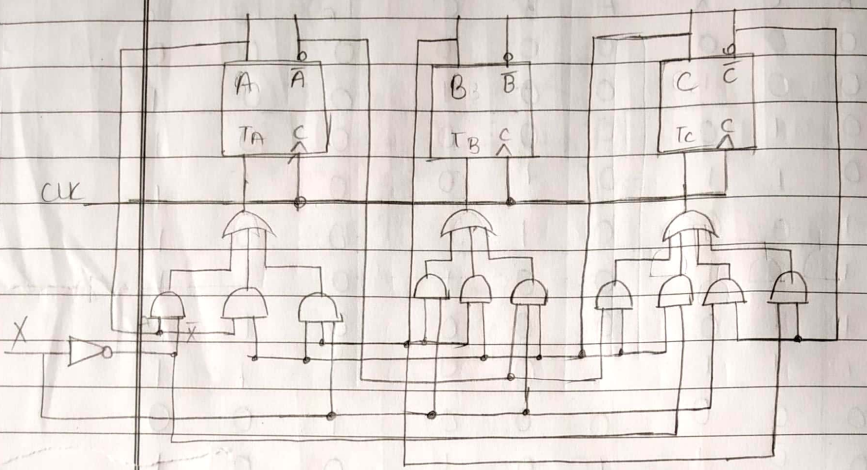
$T_A = A\bar{X} + AC + BCX$

AB \ CX	00	01	11	10
00	0	0	1	0
01	0	1	1	1
11	-	-	-	-
10	0	0	0	0

$T_B = BX + BC + \bar{A}CX$

AB \ CX	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	-	-	-	-
10	0	1	0	1

$T_C = \bar{A}C + C\bar{X} + \bar{C}X + B\bar{C}$



AB \ CX	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	-	-	-	-
10	0	0	0	1

$Z = \cancel{CX}\ AC\bar{X}$

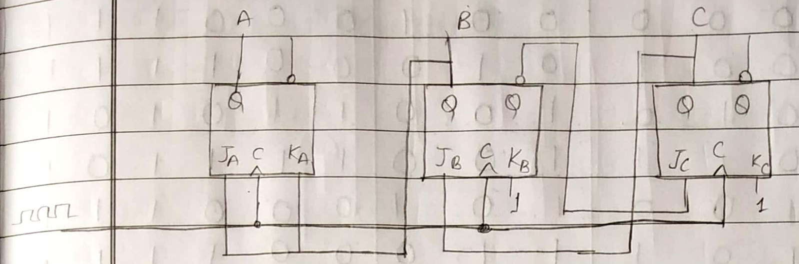
2/3 marks

Analysis of sequential circuits :

The procedure to analysis synchronous counter is as follows :

1. Identify the state variable (F/F outputs)
2. Identify F/F types
3. Write F/F input equations
4. Construct the K-map using the F/F equ^n
5. Fill the excitation table using the K-map & the ~~functioned~~ functional table of F/F.
6. Write ~~staty~~ state diagram from excitation table.

Analyse the foll synchronous sequential circuit.



State variable - A, B, C

F/F type - J K flip flop

F/F input equations :

$J_A = B$ $\quad K_A = B$

$J_B = C$ $\quad K_B = 1$

$J_C = \overline{B}$ $\quad K_C = 1$

K-map : J_A/K_A

A \ BC	00	01	11	10
0	0	0	1	1
1	0	0	1	1

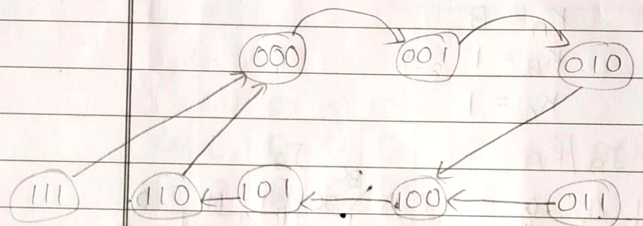
J_B

A \ BC	00	01	11	10
0	0	1	1	0
1	0	1	1	0

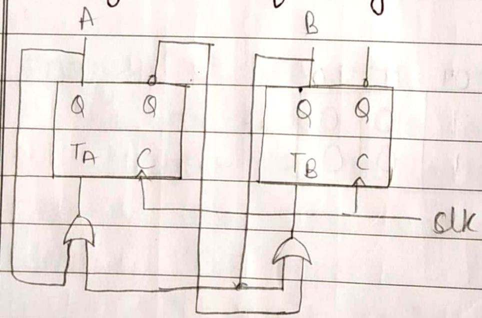
J_C

A \ BC	00	01	11	10
0	1	1	0	0
1	1	1	0	0

Present State			Next			J_A	K_A	J_B	K_B	J_C	K_C
A	B	C	A^+	B^+	C^+						
0	0	0	0	0	1	0	0	0	1	1	1
0	0	1	0	1	0	0	0	1	1	1	1
0	1	0	1	0	0	1	1	0	1	0	1
0	1	1	1	0	0	1	1	1	1	0	1
1	0	0	1	0	1	0	0	0	1	1	1
1	0	1	1	1	0	0	0	1	1	1	1
1	1	0	0	0	0	1	1	0	1	0	1
1	1	1	0	0	0	1	1	1	1	0	1



Analyse the foll synchronous circuit



state variables - A, B

F/F type - T F/F

F/F input equations :

$T_A = A + B$

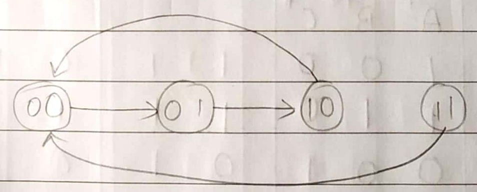
$T_B = B + \bar{A}$

A \ B	0	1
0	0	1
1	1	1

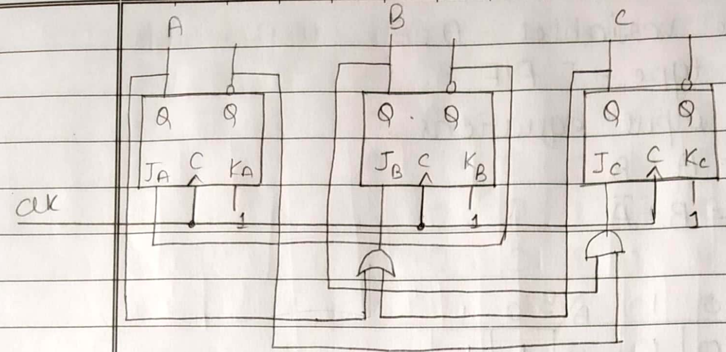
A \ B	0	1
0	1	1
1	0	1

Excitation table :

Present		Next		T_A	T_B
A	B	A^+	B^+		
0	0	0	1	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1



Analyse 4 bit synchronous sequential circuit.



State variable - A, B, C

F/F type - JK

F/F input equations

$J_A = \overline{B}$ $\quad K_A = K_B = K_C = 1$

$J_B = A + C$

$J_C = \overline{A}B$

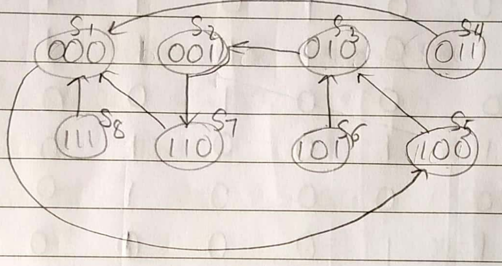
Excitation table

Present			Next			J_A	K_A	J_B	K_B	J_C	K_C
A	B	C	A^+	B^+	C^+						
0	0	0	1	0	0	1	1	0	1	0	1
0	0	1	1	1	0	1	1	1	1	0	1
0	1	0	0	0	1	0	1	0	1	1	1
0	1	1	0	0	0	0	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	0	1
1	0	1	0	1	0	1	1	1	1	0	1
1	1	0	0	0	0	0	1	1	1	0	1
1	1	1	0	0	0	0	1	1	1	0	1

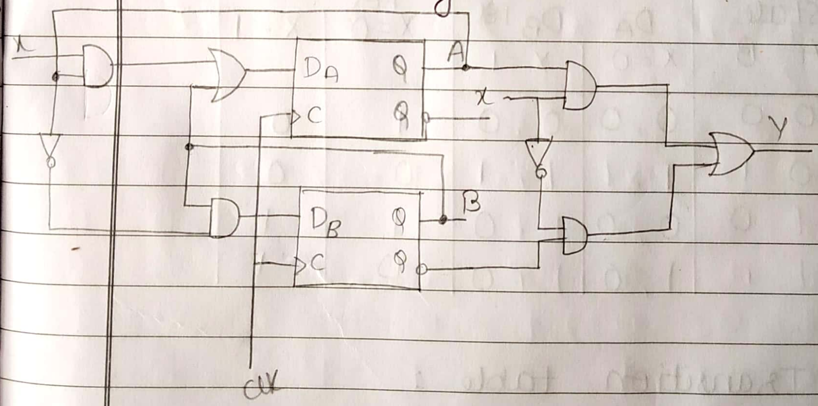
A \ BC	00	01	11	10
0	1_0	1_1	0_3	0_2
1	1_4	1_5	0_7	0_6

A \ BC	00	01	11	10
0	0	1	1	0
1	1	1	1	1

A \ BC	00	01	11	10
0	0	[illegible]	1	1
1	0	0	0	0



Analyse foll sequential circuit by writing input & output equations, state table and state diagram.



State variable - A B

F/F type - D

F/F input equ^n

$D_A = xA + B$

$D_B = \overline{A}B$

F/F output equ^n

$Y = Ax + \bar{B}\bar{x}$

A	B	X	xA	$\bar{A}B$	$\bar{B}\bar{x}$	D_A	D_B	Y
0	0	0	0	0	1	0	0	1
0	0	1	0	0	0	0	0	0
0	1	0	0	1	0	1	1	0
0	1	1	0	1	0	1	1	0
1	0	0	0	0	1	0	0	1
1	0	1	1	0	0	1	0	1
1	1	0	0	0	0	1	0	0
1	1	1	1	0	0	1	0	1

Excitation table :

Present State	Excitation D_A D_B For		Output Y For	
A B	X = 0	X = 1	X = 0	X = 1
0 0	0, 0	0, 0	1	0
0 1	1, 1	1, 1	0	0
1 0	0, 0	1, 0	1	1
1 1	1, 0	1, 0	0	1

Transition table :

Presen

A

0

0

1

1

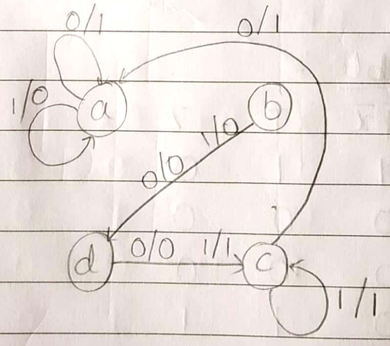
Present State		Next State A^+ B^+ for				Output Y for input	
A	B	$x=0$		$x=1$		$X=0$	$X=1$
0	0	0	0	0	0	1	0
0	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1
1	1	1	0	1	0	0	1

State ~~table~~ assignment

Assume 00 - a, 01 - b, 10 - c, 11 - d.

State table

Present State	Next State $X=0$	Next State $X=1$	Output $X=0$	Output $X=1$
a	a	a	1	0
b	d	d	0	0
c	a	c	1	1
d	c	c	0	1



Analyse foll sequential circuit shown in fig below and obtain

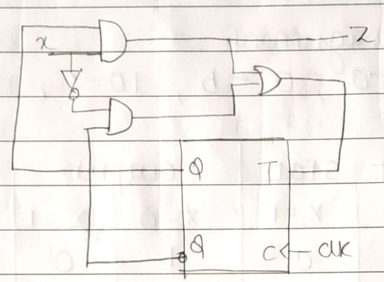
i) F/F input & output equ^n

ii) Transition equ^n

iii) Transition table

iv) State table

v) Draw state diagram



F/F equation

$T = \bar{x}\bar{Q} + Qx$

$Z = Qx$

Expression table :

Q	x	Qx	$\bar{Q}\bar{x}$	T	Z
0	0	0	1	1	0
0	1	0	0	0	0
1	0	0	0	0	0
1	1	1	0	1	1

in

Excitation Table :

Present Q	Excitation T for $x=0$	Excitation T for $x=1$	Output Z for $x=0$	Output Z for $x=1$
0	1	0	0	0
1	0	1	0	1

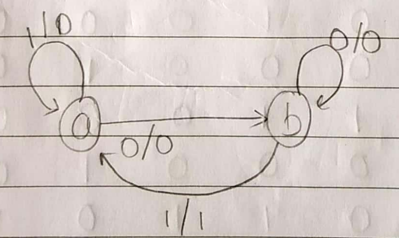
Transition table :

Present Q	Next Q^+ $x=0$	Next Q^+ $x=1$	Output z $x=0$	Output z $x=1$
0	1	0	0	0
1	1	0	0	1

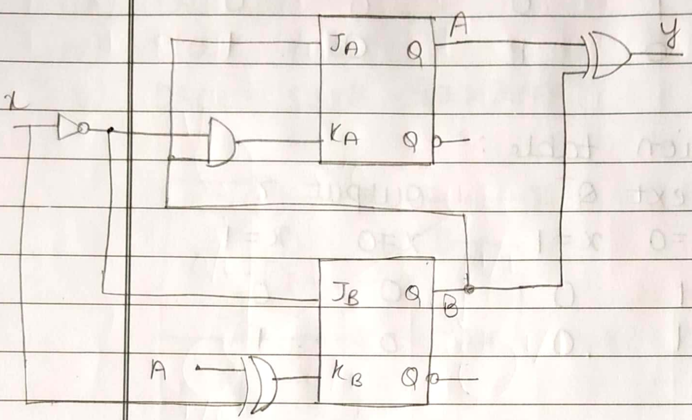
State assignment → $a = 0$ $b = 1$

State table

Present state	Next State $x=0$	Next State $x=1$	Output z $x=0$	Output z $x=1$
a	b	a	0	0
b	b	a	0	1



Construct the excitation table, transitio table state table & state diagram for a moore' sequential circuit shown



F/F equations

$J_A = B \qquad K_A = \bar{x}B$

$J_B = \bar{x} \qquad K_B = A \oplus x = A\bar{x} + \bar{A}x$

$Y = A \oplus B = A\bar{B} + \bar{A}B$

Expression table :

A	B	x	$\bar{x}B$	$\bar{x}$	$A\bar{x}$	$\bar{A}x$	$A\bar{B}$	$\bar{A}B$
0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	0	1
0	1	1	0	0	0	1	0	1
1	0	0	0	1	1	0	1	0
1	0	1	0	0	0	0	1	0
1	1	0	1	1	1	0	0	0
1	1	1	0	0	0	0	0	0

Present

A	B
0	0
0	1
1	0
1	1

Scanned by CamScanner

J_A	K_A	J_B	K_B	Y
0	0	1	0	0
0	0	0	1	0
1	1	1	0	1
1	0	0	1	1
0	0	1	1	1
0	0	0	0	1
1	1	1	1	0
1	0	0	0	0

Excitation table

Present		Excitation JK for		Output Y for	
A	B	X = 0	X = 1	X = 0	X = 1
0	0	00, 10	00, 01	0	0
0	1	11, 10	10, 01	1	1
1	0	00, 11	00, 00	1	1
1	1	11, 11	10, 00	0	0

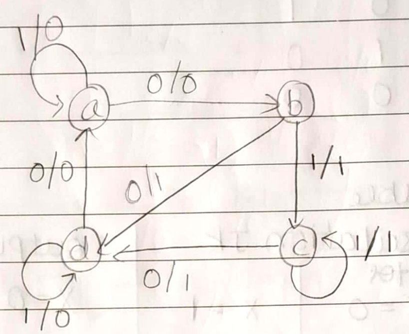
Transition table :

Present		~~Excitation~~ Next A^+ & B^+		Output Y	
A	B	X = 0	X = 1	X = 0	X = 1
0	0	0 1	0 0	0	0
0	1	1 1	1 0	1	1
1	0	1 1	1 0	1	1
1	1	0 0	1 1	0	0

State assignment → a → 00 b → 01
c → 10 d → 11

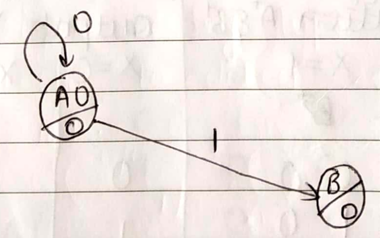
State diagram:

Present A	Present B		Next X=0	Next X=1	Output X=0	Output X=1
0	0	a	b	a	0	0
0	1	b	d	c	1	1
1	0	c	d	c	1	1
1	1	d	a	d	0	0

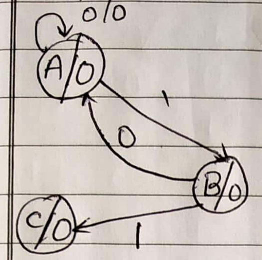


Draw a state diagram of a moore machine to output a one if the input has been 1 for 3 consequtive clock cycles.

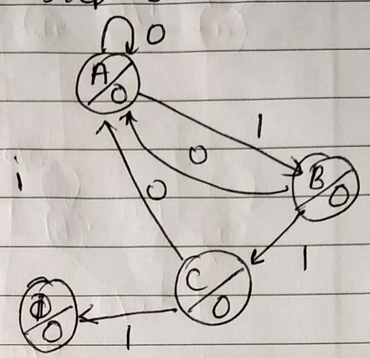
Step 1:



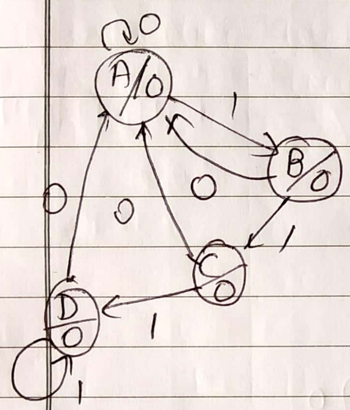
step 2 :



Step 3 :



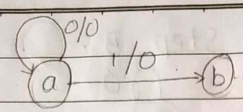
step 4 :

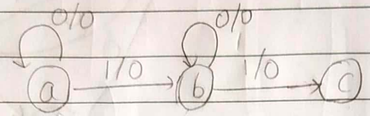


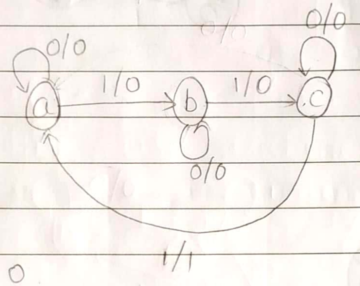
Draw state diagram of mealey machine whose o/P is 1 for every 3^{rd} i/P being 1 not necessarily consequetive but not overlapp.

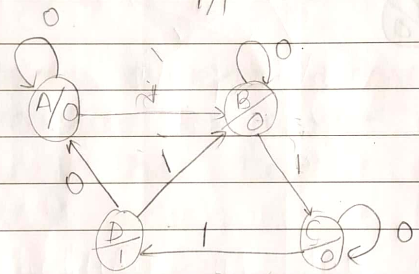
X = 0101011101011

0000010001000

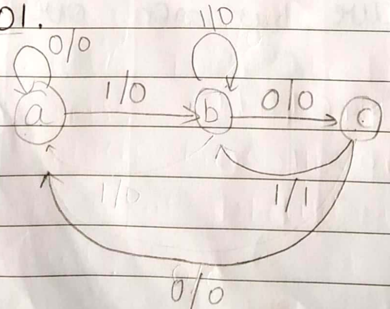








Design mealey type ~~desg~~ sequence detector to detect serial i/p sequence of 101.



a - 00
b - 01
c - 10
d - 11

State transition table :

Present state i/P Next state o/P

PS	NS x=0	NS x=1	O/P Z x=0	O/P Z x=1
A	A	B	0	0
B	C	B	0	0
C	A	B	0	1
~~B~~				

PS Q_1 Q_0	NS x=0	NS x=1	output Z x=0	output Z x=1
0 0	00	01	0	0
0 1	10	01	0	0
1 0	00	01	0	1

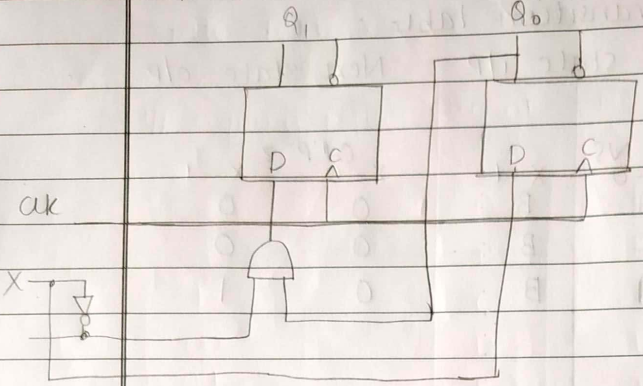
Q_1Q_0 \ X	0	1
00	0	0
01	1	0
11	-	-
10	0	0

Q_1Q_0 \ X	0	1
00	0	1
01	0	1
11	-	-
10	0	1

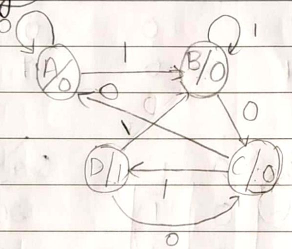
Q_1Q_0 \ X	0	1
00	0	0
01	0	0
11	-	-
10	0	1

$Q_1^+ = Q_0\bar{X}$ $Q_0^+ = X$ $Z = Q_1 X$

$D_A = Q_0\bar{X}$ $D_B = X$



Design moore machine for sequence 101.



Draw logic circuit

Guidelines for state assignment.

i) States which have in same next state for a given input should be given adjacent assignments.

ii) States which are the next stage of the same state should be given adjacent assignments.

iii) States which have the same output for a given input should be given adjacent assignment.

Assign a sequential circuit to convert BCD to excess 3 code.

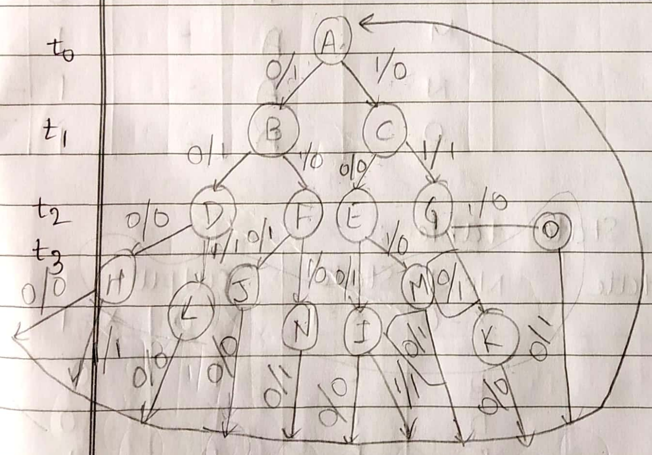
BCD				Excess - 3			
t_3	t_2	t_1	t_0	t_3	t_2	t_1	t_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	0	0	0

t_0

t_1

t_2

t_3



00 - D
01 - E
10 - F
11 - G
000 - H
001 - I
010 - J
~~000~~ - K
100 - L
M
N
O

H ≡ I ≡ J ≡ K ≡ L   E ≡ F ≡ G
M ≡ N ≡ O

State table :

Time	i/p sequence Recieved	Present State	Next State X = 0	Next State X = 1	Output X = 0	Output X = 1
t_0	reset	A	B	C	1	0
t_1	0	B	D	F	1	0
	1	C	E	G	0	1
t_2	00	D	H	L	0	1
	01	E	I	M	1	0
	10	F	J	N	1	0
	11	G	K	O	1	0
t_3	000	H	A	A	0	1
	001	I	A	A	0	1
	010	J	A	–	0	–
	011	K	A	–	0	–
	100	L	A	–	0	–
	101	M	A	–	1	–
	110	N	A	–	1	–
	111	O	A	–	1	–

Reduced State table :

Present State	Next State X = 0	Next State X = 1	Output X = 0	Output X = 1
A	B	C	1	0
B	D	E	1	0
C	E	E	0	1
D	H	H	0	1
E	H	M	1	0
H	A	A	0	1
M	A	–	1	–

Q_2Q_3 \ Q_1	0	1
00	A	B
01		C
11	H	D
10	M	E

State table :

Present state			Next state		Output	
Q_1	Q_2	Q_3	$Q_1^+ Q_2^+ Q_3^+$ $X=0$	$X=1$	$X=0$	$X=1$
0	0	0	1 0 0	1 0 1	1	0
1	0	0	1 1 1	1 1 0	1	0
1	0	1	1 1 0	1 1 0	0	1
1	1	1	0 1 1	0 1 1	0	1
1	1	0	0 1 1	0 1 0	1	0
0	1	1	0 0 0	0 0 0	0	1
0	1	0	0 0 0	- - -	1	-

Q_1Q_2 \ Q_3X	00	01	11	10
00	1	1	X	X
01	0	X	0	0
11	0	0	0	0
10	1	1	1	1

$Q_1^+ = \overline{Q_2}$

Q_1Q_2 \ Q_3X	00	01	11	10
00	0	0	X	X
01	0	X	0	0
11	1	1	1	1
10	1	1	1	1

$Q_2^+ = Q_1$

Q_1Q_2 \ Q_3X	00	01	11	10
00	0	1	X	X
01	0	X	0	0
11	1	0	1	1
10	1	0	0	0

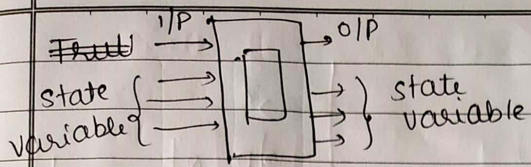
$Q_3^+ =$

Design sequential circuit to convert BCD to Excess-3 using ROM.

Truth table
state diagram
State table
Reduced state table

Transition table :

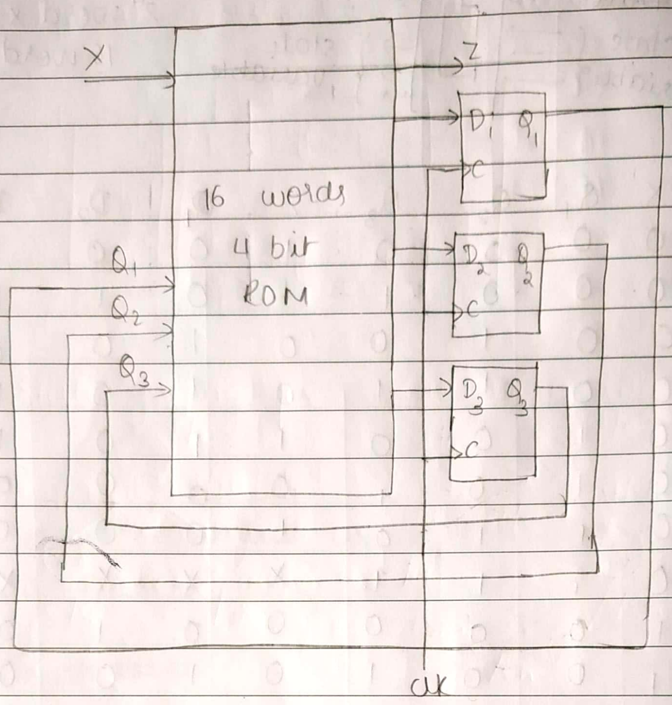
Present	Next state X = 0	Next state X = 1	O/P Z X = 0	O/P Z X = 1
A → 000	001	010	1	0
B → 001	011	100	1	0
C → 010	100	100	0	1
D → 011	101	101	0	1
E → 100	101	110	1	0
H → 101	000	000	0	1
M → 110	000	–	1	–



2^4 word x 4 bits

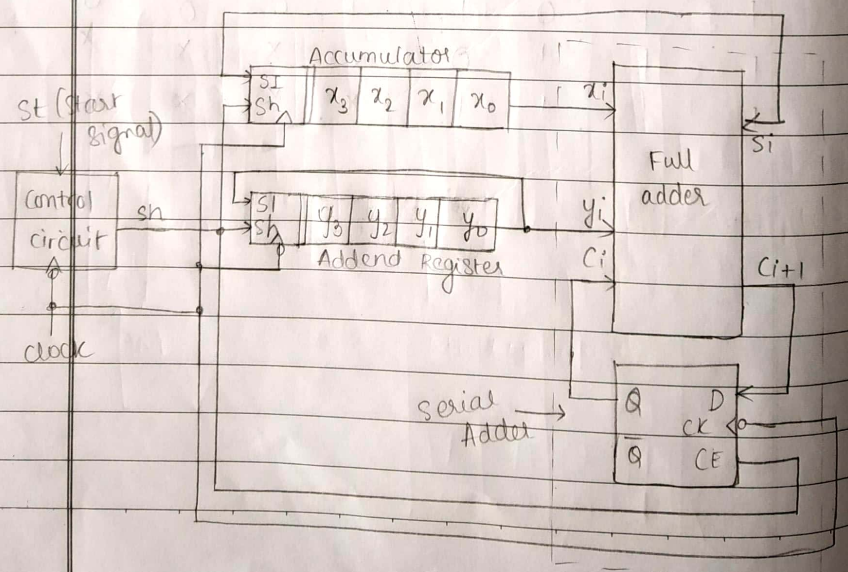
16 word x 4 bits

X	Q_1	Q_2	Q_3	Z	D_1	D_2	D_3
0	0	0	0	1	0	0	1
0	0	0	1	1	0	1	1
0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	1
0	1	0	0	1	1	0	1
0	1	0	1	0	0	0	0
0	1	1	0	1	0	0	0
0	1	1	1	X	X	X	X
1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	0	1	1	0
1	1	0	1	1	0	0	0
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X



Imp

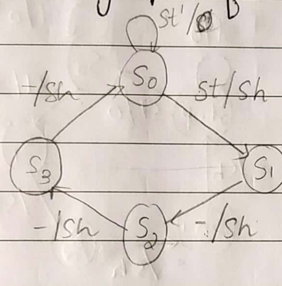
Block Diagram for serial Adder with Accumulator :



Operation of serial Adder :

	X	Y	C_i	S_i	C_i^+
t_0	0101	0111	0	0	1
t_1	0010	1011	1	0	1
t_2	0001	1101	1	1	1
t_3	1000	1110	1	1	0
t_4	1100	0111	0	(1)	(0)

State graph for serial Adder control :



Present	Next State St = 0	Next State St = 1	O/P (Sh) 0	O/P (Sh) 1
S_0	S_0	S_1	0	1
S_1	S_2	S_2	1	1
S_2	S_3	S_3	1	1
S_3	S_0	S_0	1	1

Derivations of control circuit Equations

	AB	A^+B^+ (St = 0)	A^+B^+ (St = 1)	Sh (0)	Sh (1)
S_0	00	00	01	0	1
S_1	01	10	10	1	1
S_2	10	11	11	1	1
S_3	11	00	00	1	1

AB \ St	0	1
00	0	0
01	1	1
11	0	0
10	1	1

$A^+ = \bar{A}B + A\bar{B}$

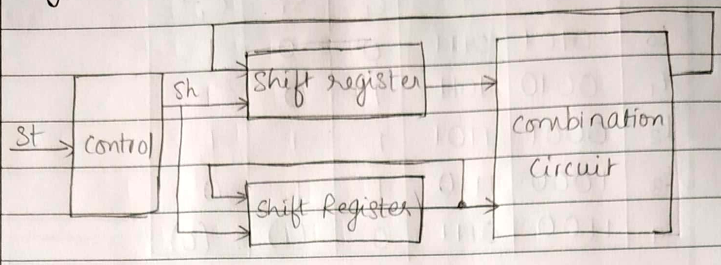
AB \ St	0	1
00	0	1
01	0	0
11	0	0
10	1	1

$B^+ = A\bar{B} + \bar{B}St$

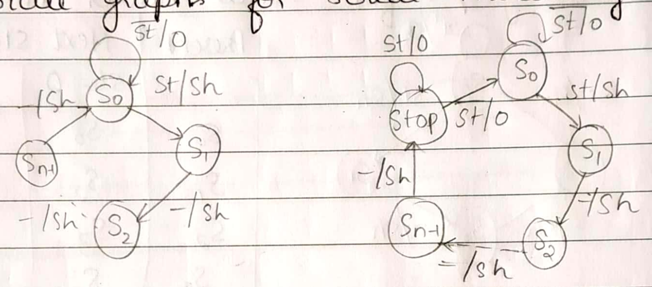
AB \ St	0	1
00	0	1
01	1	1
11	1	1
10	1	1

$Sh = St + B + A$

Typical serial Processing Unit :

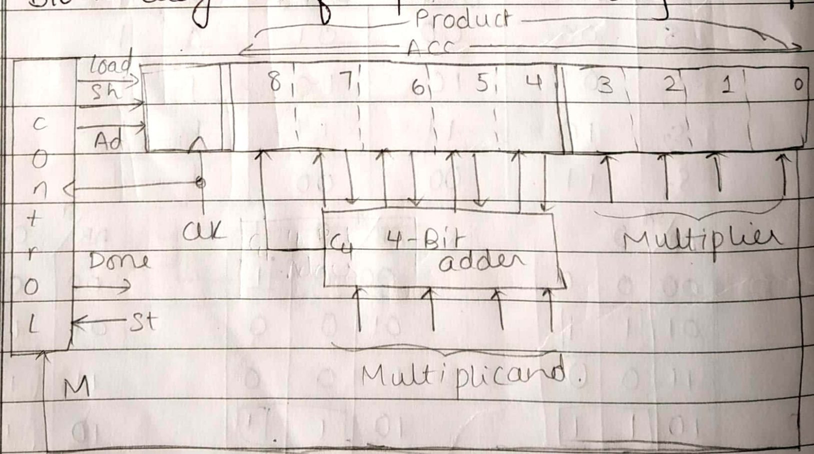


State graphs for serial Processing unit.



Design of Parallel Multiplier :

Block diagram for parallel Binary Multiplier



Eg :

1101 → Multiplier
1011 → Multiplicant

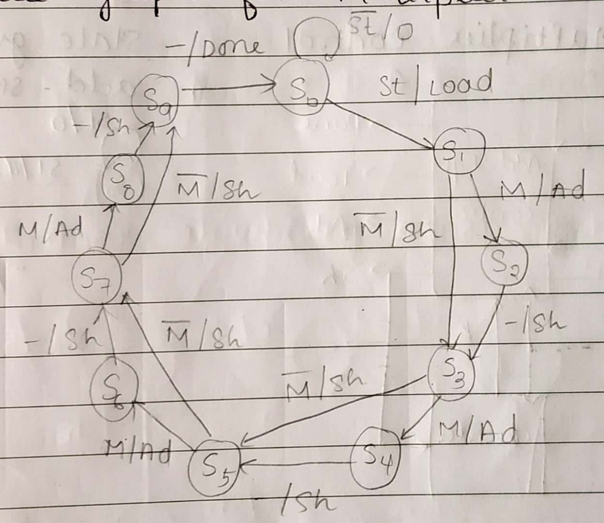
1101
1101

100111 → Partial Product
0000

100111
1101

$\boxed{0}$1000111 → Product

State graph for Multiplier control.



ACC → 000001011 → M=1
Multiplicant 1101

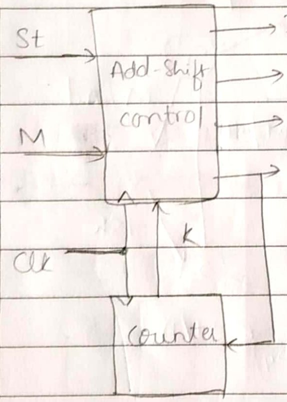
01101 → Add
011011011 shift
001101101 → M=1
1101

100111101 shift

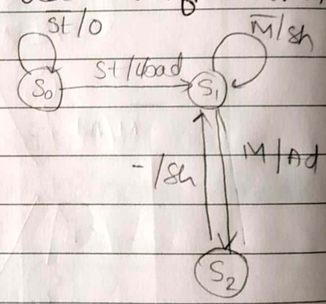
ACC	000001011	→ M=1
Multiplicand	1101	
	011011011	→ shift
	001101101	→ M=1
	1101	
	100111101	→ shift
	010011110	→ M=0 shift
	001001111	→ M=1
	1101	
	100011111	→ shift
Product →	010001111	

Time	Stat
t_0	S_0
t_1	S_0
t_2	S_1
t_3	S_2
t_4	S_1
t_5	S_2
t_6	S_1
t_7	S_1
t_8	S_2
t_9	S_2

Multiplier control



State graph for add - shift control



D

B

Operation of Multiplier Using a counter.

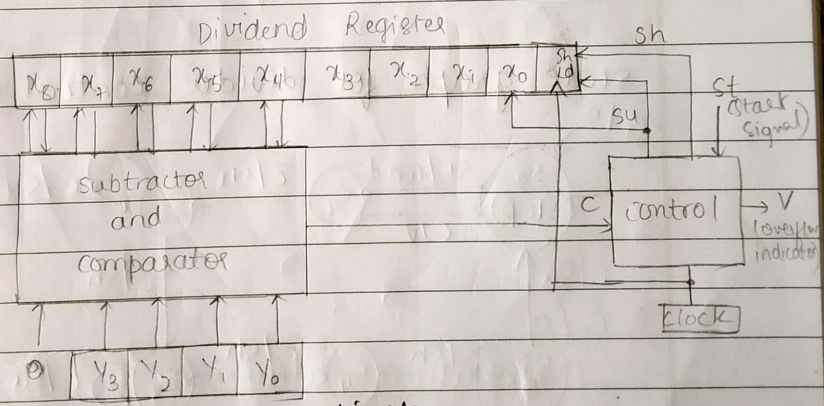
11

divisor

Time	State	Counter	Product Register	St	M	K	Load	Ad	Sh	Done
t_0	S_0	00	000000000	0	0	0	0	0	0	0
t_1	S_0	00	000000000	1	0	0	1	0	0	0
t_2	S_1	00	000001011	0	1	0	0	1	0	0
t_3	S_2	00	011011011	0	1	0	0	0	1	0
t_4	S_1	01	001101101	0	1	0	0	1	0	0
t_5	S_2	01	100111101	0	1	0	0	0	1	0
t_6	S_1	10	010011110	0	0	0	0	0	1	0
t_7	S_1	11	001001111	0	1	1	0	1	0	0
t_8	S_2	11	100011111	0	1	1	0	0	1	0
t_9	S_2	00	010001111	0	1	0	0	0	0	1

Design of a Binary divider :

Block diagram for parallel binary divider



1010 → quotient

1101) 10000111 ← divisor

1001

001111

1101

00101

00000

00101 → Remainder

$x_8\ x_7\ x_6\ x_5\ x_4\ x_3\ x_2\ x_1\ x_0$

0 1 0 0 0 0 1 1 ; 1

0 1 1 0 1 ; C = 0

1 0 0 0 0 1 1 1 ; 0 shift Sh = 1

0 1 1 0 1 ; C = 1

0 0 0 1 1 1 1 1 1 1 shift Sh = 1

0 1 1 0 1

0 0 1 1 1 1 1 1 ; 0 C = 0 shift

0 1 1 0 1

0 1 1 1 1 1 1 0 ; 0 C = 0 shift

0 1 1 0 1

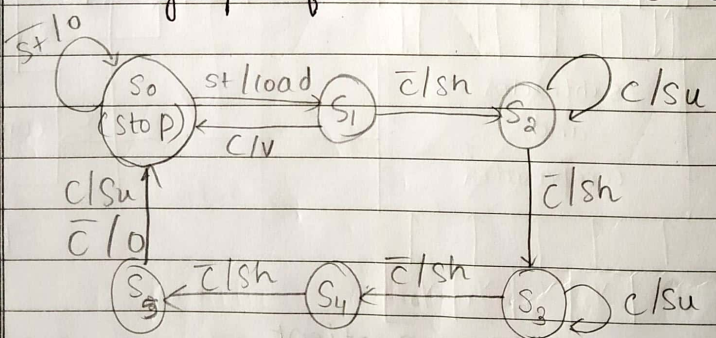
0 0 0 1 0 1 1 0 ; 0

0 1 1 0 1 C = 0 shift

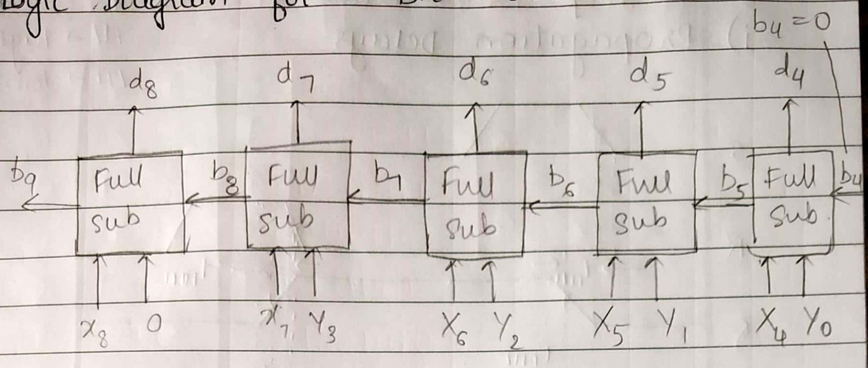
0 0 0 0 0 ; 1 0 0 0

Remainder quotient

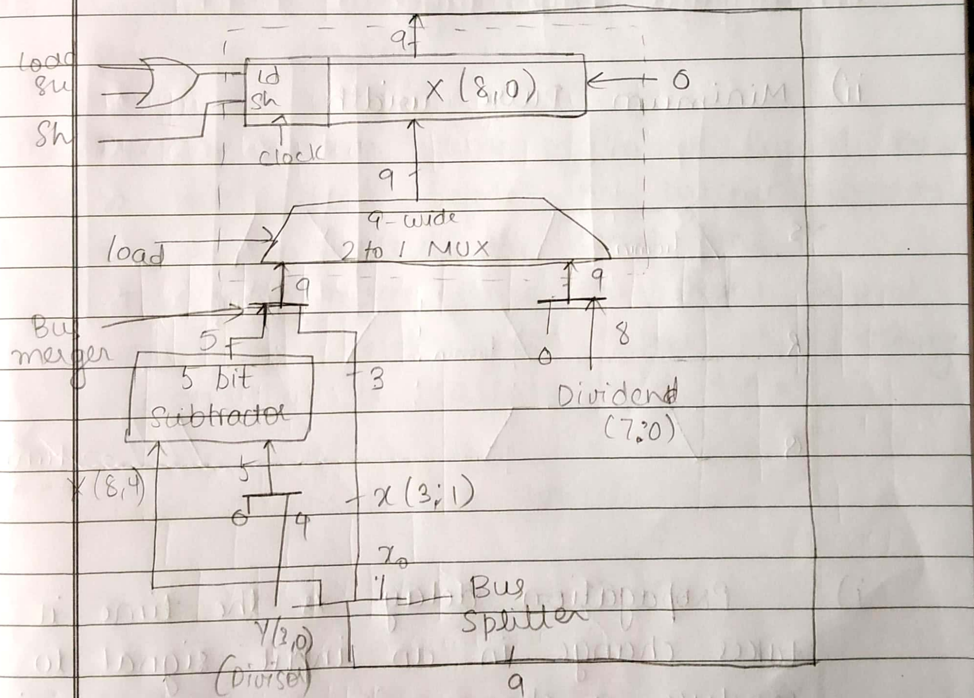
state graph for divider control circuit



Logic Diagram for 5-Bit Subtractor



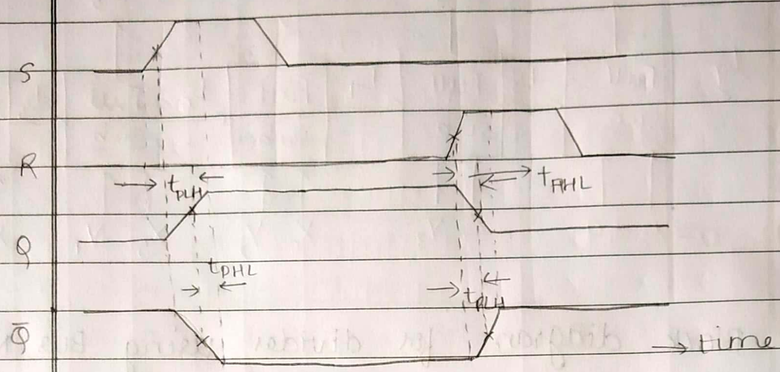
Block diagram for divider Using Bus Notation



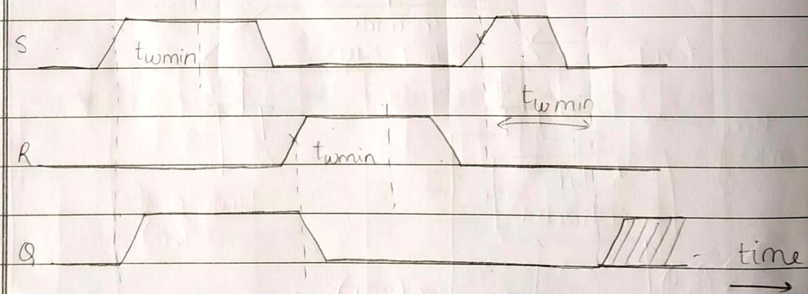
Timing considerations

i) Propagation Delays

HL → high to low
LH → low to high



ii) Minimum Pulse width



i) Propagation delay is the time it takes change in an input signal to produce a change in an output signal

C

D

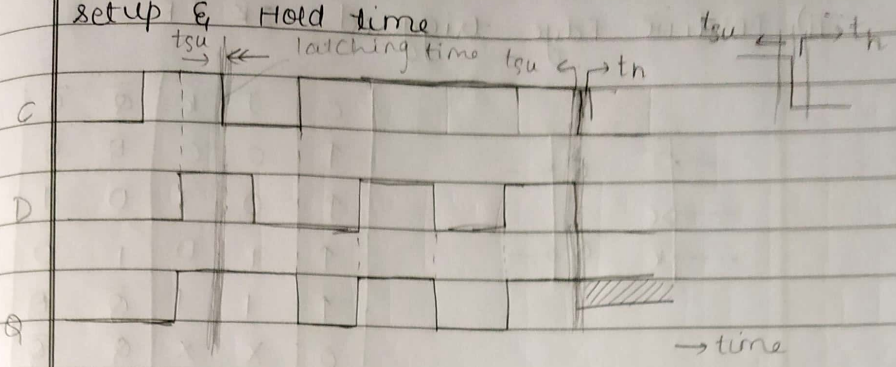
Q

ii)

iii)

i)

Setup & Hold time

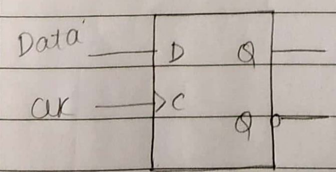


ii) It is a minimum amount of time a signal must be applied in order to produce desired result.

iii) The minimum time of input signal must be held fixed before the latching action ~~the~~ t_{su} is called the setup time.
The minimum time the input signal must be held fixed after the latching action t_H is called Hold time.

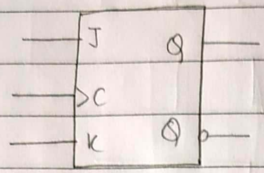
Edge triggered flip flop.

i) Positive Edge - triggered D - FF



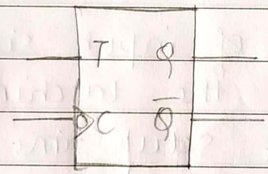
C	D	Q	$\bar{Q}$
↑	0	0	1
↑	1	1	0
0	X	Q	$\bar{Q}$
1	X	Q	$\bar{Q}$

ii) Positive Edge triggered JK FF



C	J	K	Q	$\bar{Q}$
↑	0	0	Q	$\bar{Q}$
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	$\bar{Q}$	Q
0	X	X	Q	$\bar{Q}$
1	X	X	Q	$\bar{Q}$

iii) Negative Edge triggered T FF



C	T	Q	$\bar{Q}$
↓	0	Q	$\bar{Q}$
↓	1	$\bar{Q}$	Q
0	X	Q	$\bar{Q}$
1	X	Q	$\bar{Q}$