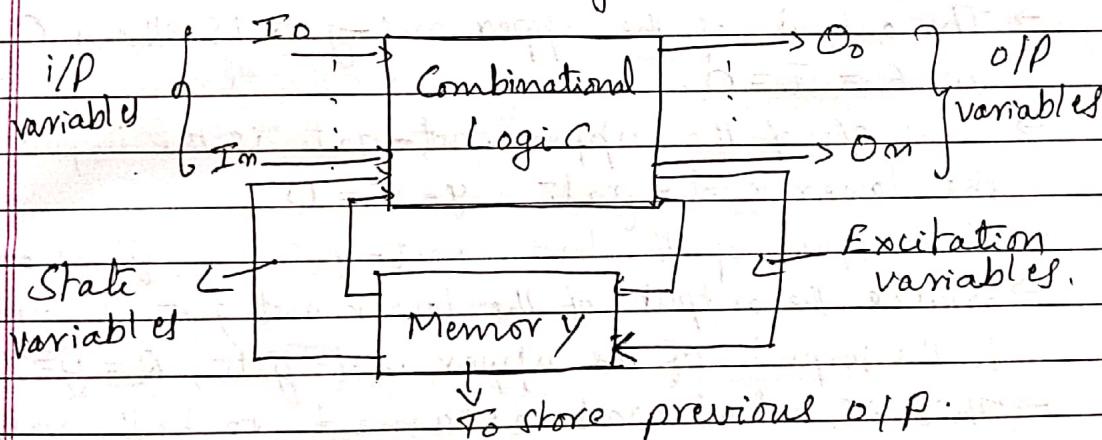


Flip-Flops & its applications:-Sequential Circuits:-

A sequential n/w is defined as a 2-valued n/w in which the outputs at any instant are dependent not only upon the inputs present at that instant but also upon the past history (or sequence) of inputs. To preserve past history of inputs, sequential n/w are said to have memory.

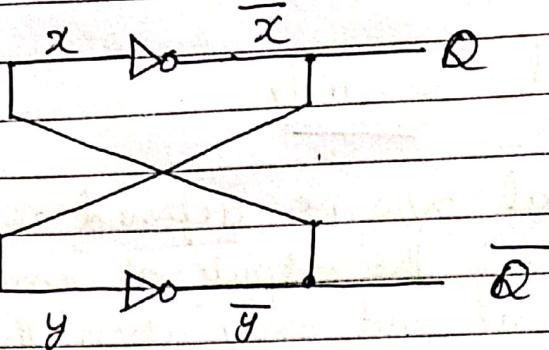
The 2 main components of sequential ckt are : combinational logic & Memory

2 Types :-

- i) Synchronous Sequential n/w : - is one in which its behaviour is determined by the values of the signals at only discrete instant of time. Controlled by a master clock. The i/p to the d/l is sampled at discrete instances of these clock pulses which determine the lkt operation.

- ii) Asynchronous Sequential n/w : - are those whose behaviour is immediately affected by the input signal changes.

6.1 Basic Bistable Element



- The basic bistable element is a ckt having 2 stable conditions (or states).
- It has 2 outputs Q & \bar{Q} .
- Assume that when power is switched on to the ckt, X is at 1.
- The output of the upper not-gate is then 0 i.e., $Q = \bar{Q} = 0$.
- Since o/p of the upper not-gate is the input to the lower not-gate $y = \bar{x} = 0$.
- The output of the lower not-gate i.e., \bar{y} is 1.
- Since the output of the lower not-gate is connected to the input of the upper not-gate, $\bar{Q} = \bar{y} = x = 1$.
- This is what was assumed to be the value of x .
- The ckt is stable with $\bar{Q} = x = \bar{y} = 1$ & $Q = \bar{x} = y = 0$.
- If $x = 0$ when power is switched on,
 $\bar{x} = 1 \Rightarrow Q = 1$
 $y = 1 \Rightarrow \bar{y} = 0 \Rightarrow \bar{Q} = 0$
- The basic bistable element is used to store binary symbols.
- When the o/p line ~~is~~ Q is 1, the element is said to be storing a ~~is~~ 1.
- When the o/p line Q is 0, the element is said to be storing a 0.
- The 2 o/p's Q & \bar{Q} are complementary.

- The binary symbol (0 or 1) stored in the basic bistable element is called the state of the element.
- Besides the two stable states, the bistable element can also be in Mesastable state which happens when both the o/p's are midway between 0 & 1 in terms of voltages.
- The bistable elements has no inputs. When power is applied, it becomes stable in one of the 2 stable states.
- It remains in this state until the power is removed.
- A flip-flop is a bistable device, with inputs, that remains in a given state as long as power is applied & until input signals are applied to cause its o/p to change.
- The process of storing a 1 into a flip-flop is called setting or prettting the flip-flop.
- The process of storing a 0 into a flip-flop is called resetting or clearing the flip-flop.

2 Types :-

- i) Asynchronous :- is one in which a signal change of sufficient magnitude & duration essentially produce an immediate change in the state of the flip-flop.
- ii) Synchronous :- is one which does not immediately affect the state of the flip-flop, but rather affects the state of the flip-flop only when some control signal also occurs.

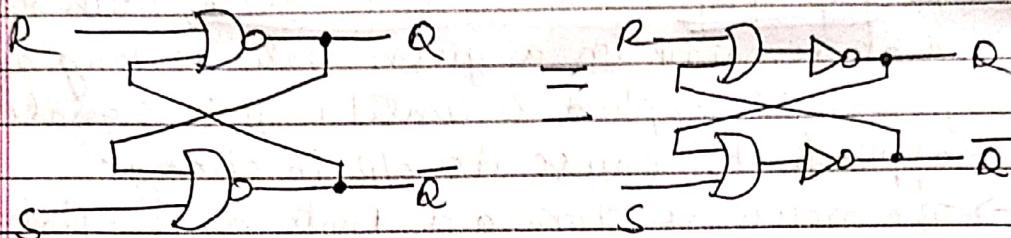
6.2 Latches :- are storage devices.

→ The output responds immediately to changes on the input lines.

6.2.1 i) The SR latch :-

→ The set-reset (SR) latch consists of 2 cross-coupled NOR gates.

→ It has 2 inputs, S & R referred to as the set & reset inputs & 2 outputs: Q & \bar{Q} .



$$\begin{array}{|c|c|} \hline S & Q \\ \hline R & \bar{Q} \\ \hline \end{array} = \begin{array}{|c|c|} \hline S & Q \\ \hline R & \bar{Q} \\ \hline \end{array}$$

Inputs	Outputs
S R	Q^+ \bar{Q}^+
0 0	Q \bar{Q}
0 1	0 1
1 0	1 0
1 1	0* 0*

Q denote present state of the latch

Q^+ denote next state of the latch.

→ For $S=R=0$, Q^+ & \bar{Q}^+ are same as Q & \bar{Q} respectively. i.e., the next state of the device is same as its present state. No change in its output.

→ When $S=0$ & $R=1$, the output of Q must be 0. This output is fed back to the lower NOR gate along with 0 on the S i/p, causes O/P of lower NOR gate \bar{Q} to become 1.

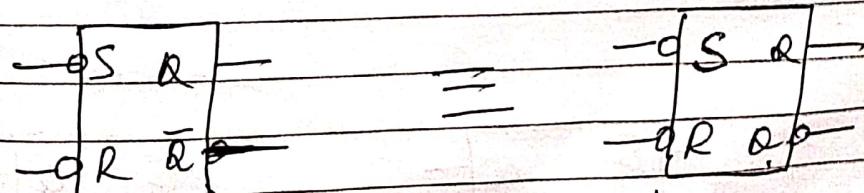
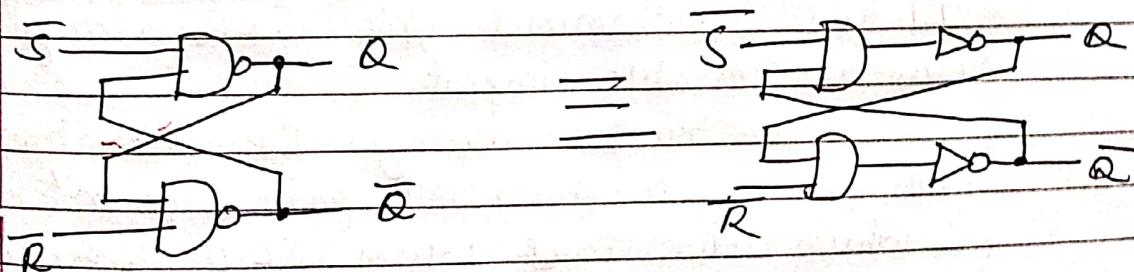
→ When $S=1$ & $R=0$, $Q=1$ & $\bar{Q}=0$

→ When $S=R=1$, the output of both NOR gates become 0 & they are not complementary outputs.

→ When both inputs return to 0 simultaneously the device may enter metastable state, which should be avoided.

→ A 1 serves as the activation signal of a device, i.e., a 1 on either the S or R i/p terminal causes the device to set or reset, respectively

6.2.3(i) The $\bar{S}\bar{R}$ Latch :- is constructed by cross-coupling two NAND-gates.



Logic Symbol:

\bar{S}	\bar{R}	Q^+	\bar{Q}^+
0	0	1*	1*
0	1	1	0
1	0	0	1
1	1	Q	\bar{Q}

→ When $\bar{S} = \bar{R} = 1$, the logic diagram functions as a basic bistable element. Thus the device has 2 stable states.

→ With $\bar{S} = \bar{R} = 0$ is forbidden state as this makes both Q & \bar{Q} to be at logic 1

→ With $\bar{S} = 0$ & $\bar{R} = 1$, Q will be 0 & $\bar{Q} = 1$, set the latch.

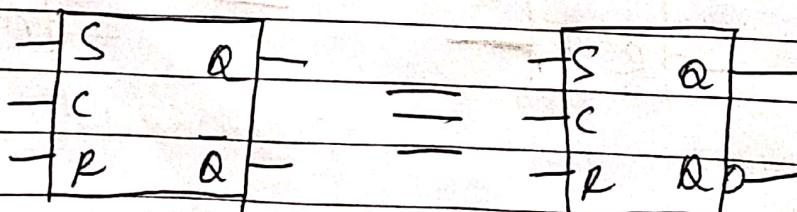
→ With $\bar{S} = 1$ & $\bar{R} = 0$, $Q = 0$ & $\bar{Q} = 1$, the latch resets.

6.2.4 iii) The Gated SR Latch

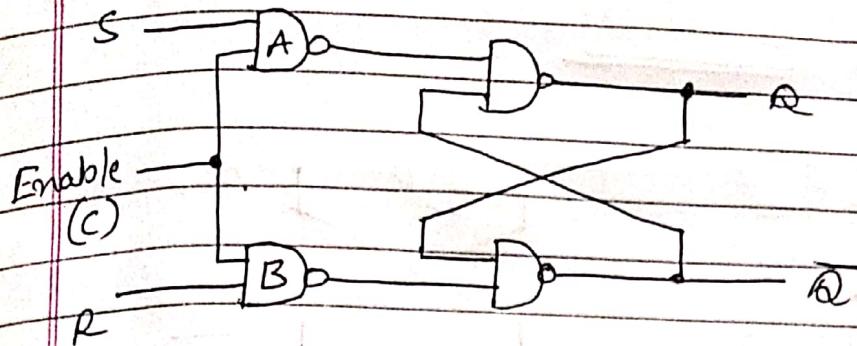
→ It is also called an SR latch with enable.

→ It has synchronous i/p's S & R along with an enable input C.

→ It is constructed using $\bar{S}\bar{R}$ latch together with 2 additional NAND gate & control input C which determines when S & R i/p's becomes effective.



Logic Symbols

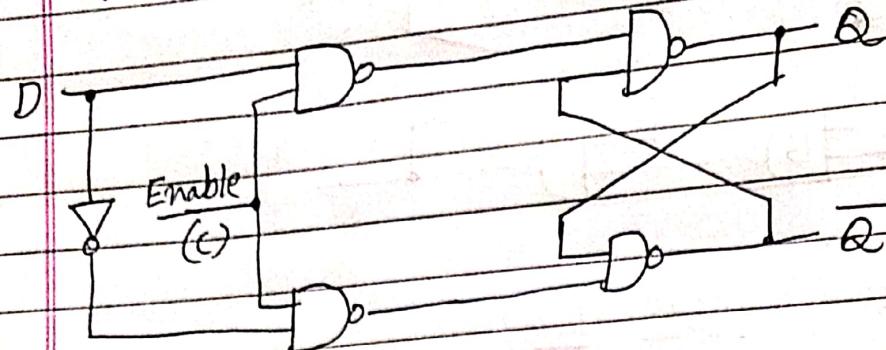
Logic Diagram

Inputs	Output	State
S R C	Q^+ \bar{Q}^+	
0 0 1	0 0	No Change.
0 1 1	0 1	Reset
1 0 1	1 0	Set
1 1 1	1* 1*	Unpredictable
x x 0	Q \bar{Q}	No change.

Function Table

- When $C=0$, D/p of NAND gate A & B are 1, which makes $\bar{S}=\bar{R}=1$, keeping $\bar{S}\bar{R}$ latch in its current stable state.
- When $C=1$, latch is enabled. NAND gates A & B invert the signals S & R & is given to cross coupled NAND gates A causes the latch to be Set or reset.

6.2.5 iv) Gated D-latch:



logic Diagram

$$\begin{array}{c|cc} \overline{D} & Q = & \overline{Q} \\ \overline{C} & \overline{Q} = & \overline{C} \overline{Q} \end{array}$$

logic Symbol

<u>Inputs</u>	<u>Outputs</u>
C D	$Q^+ \overline{Q}^+$
1 0	0 1
1 1	1 0
0 x	0 \overline{Q}

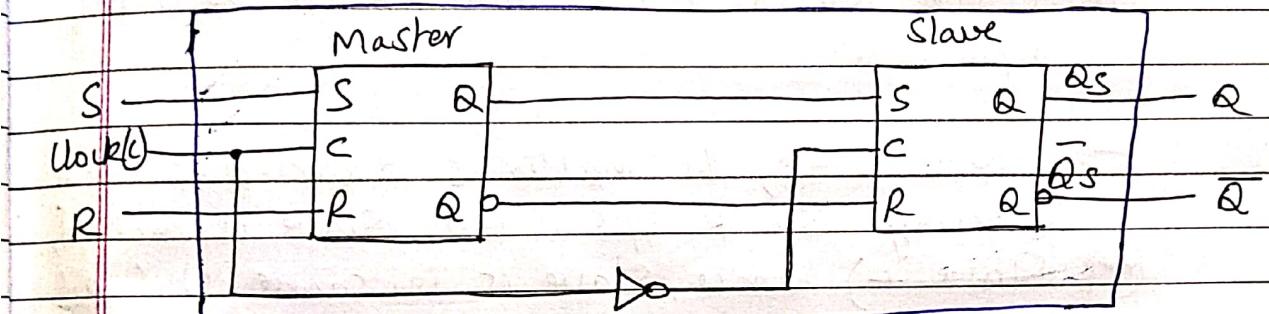
- This latch avoids the $S=R=1$ condition of the SR latch.
- It is a gated SR latch in which a not-gate is connected between the S & R terminals.
- The latch consists of single input D that determines its next state & enable input C determines when the D input is effective.
- When the latch is enabled with $C=1$, the signal at the D input appears at the Q output.
- The output follows the inputs.
- When latch is disabled with $C=0$, the off retains its previous state.

6.4 Master Slave Flip-Flops (Pulse-Triggered Flip-Flops)

Date / / 20

- A master-slave flip-flop consists of two cascaded sections, each capable of storing a binary symbol.
- The first section is referred to as the master & the second section as the slave.
- Information is entered into the master on one level of a control signal & is transferred to the slave on the next level of the control signal.

6.4.1) Master-Slave SR Flip-Flop :-



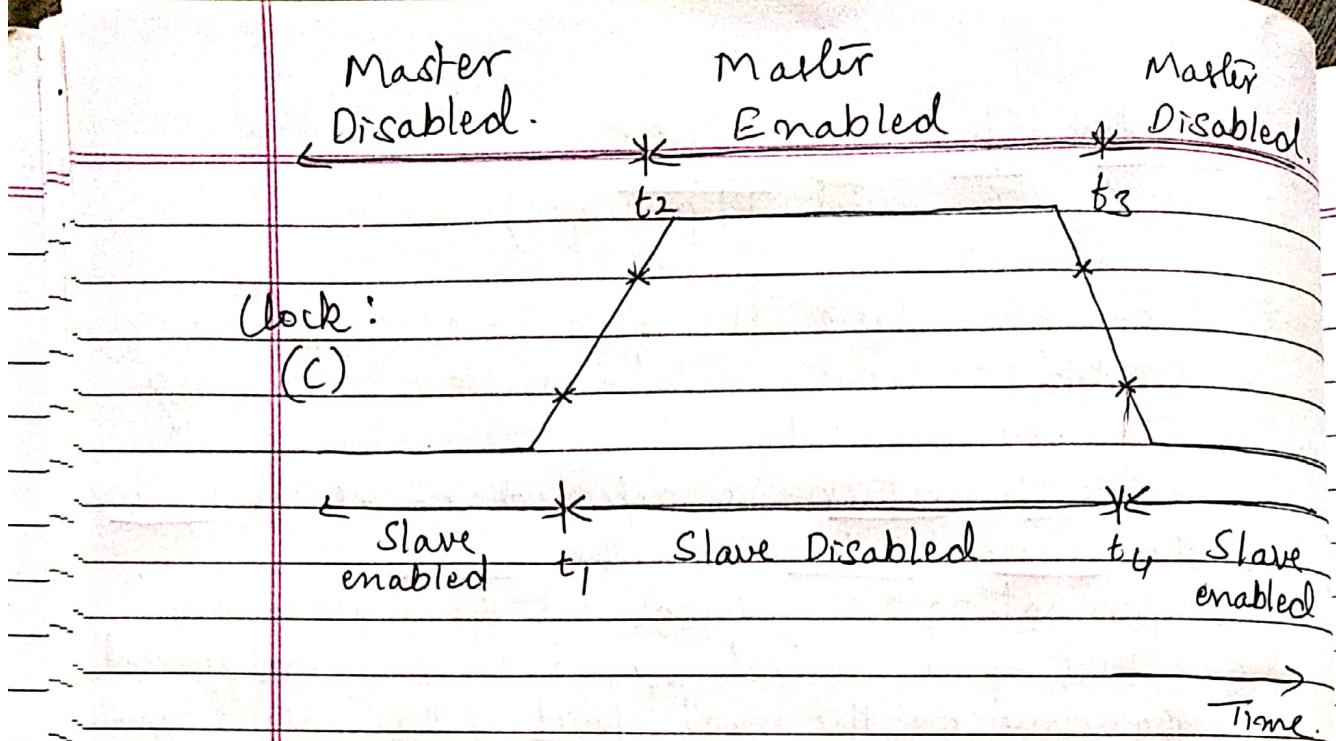
Logic Diagram

$S \rightarrow Q$		$S \rightarrow Q$
C	or	C
$R \rightarrow \bar{Q}$		$R \rightarrow Q$

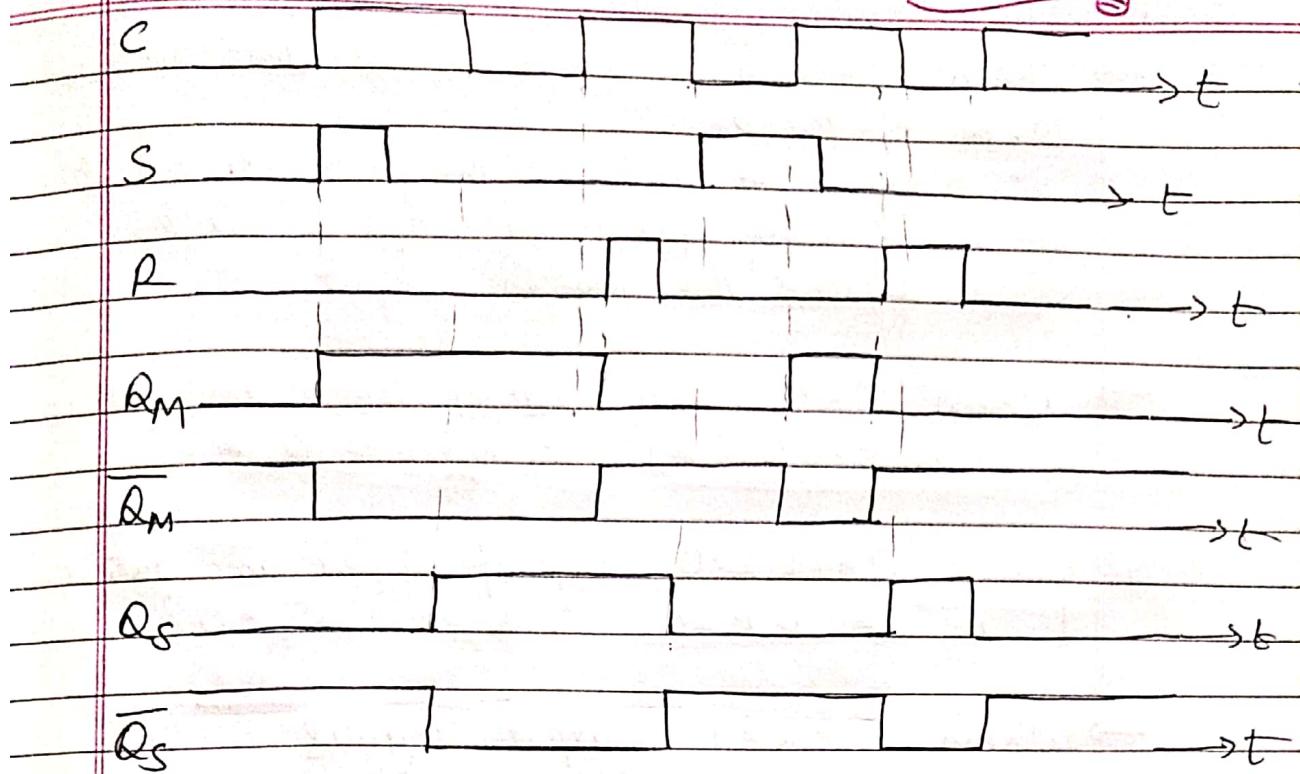
Logic Symbol

Inputs	Outputs
$C \ S \ R$	$Q^t \ \bar{Q}^t$
$0 \ 0 \ 0$	$Q \ \bar{Q}$
$0 \ 1$	$0 \ 1$
$1 \ 0$	$1 \ 0$
$1 \ 1$	Undefined
$0 \ X \ X$	$Q \ \bar{Q}$

Function Table / Truth Table

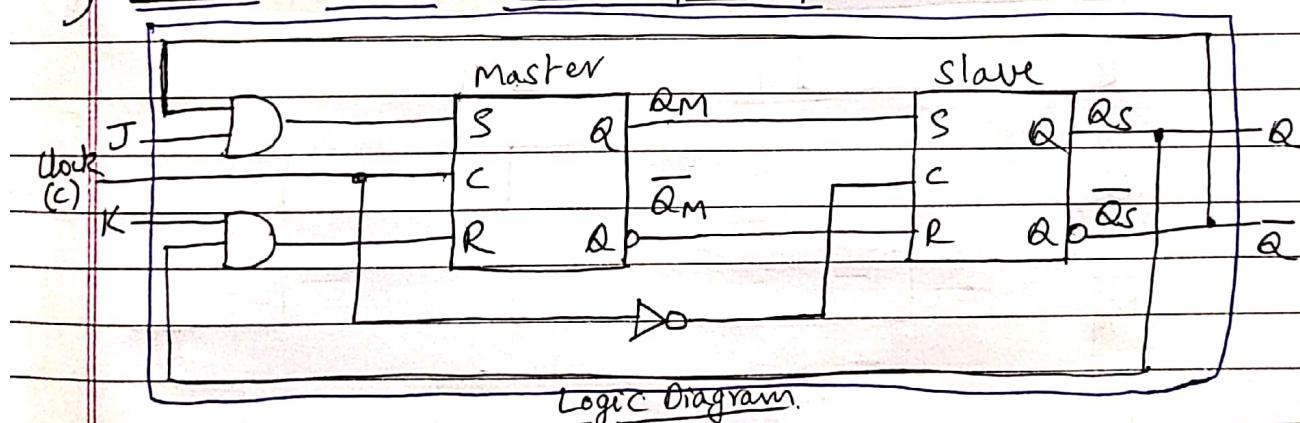


- The information input lines S & R are used to set & reset the flip-flop.
- A clock signal C_1 is applied to the control input line.
- When $C=0$, the master is disabled thereby ignoring S & R ips. But slave is enabled, hence slave is in same state as that of master because Q_M & \bar{Q}_M are connected to S & R of slave.
- When $C=1$, master is enabled & slave is disabled. Master responds to ips on S&R lines, but this changes are not reflected by the slave.



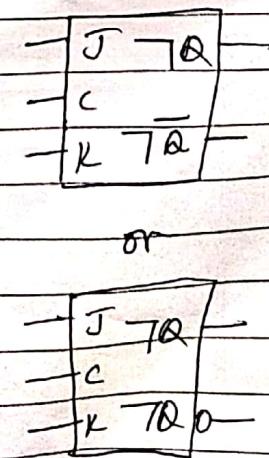
Timing Diagram for a Master-Slave SR FF

Sub. ii) Master Slave JK Flip-Flop :-



Inputs	Outputs
C J K	Q ⁺ Q̄ ⁺
0 0 0	Q Q̄
0 1 1	0 1
1 0 1	1 0
1 1 0	Q Q̄
0 x x	Q Q̄

Function Table



Logic Symbol

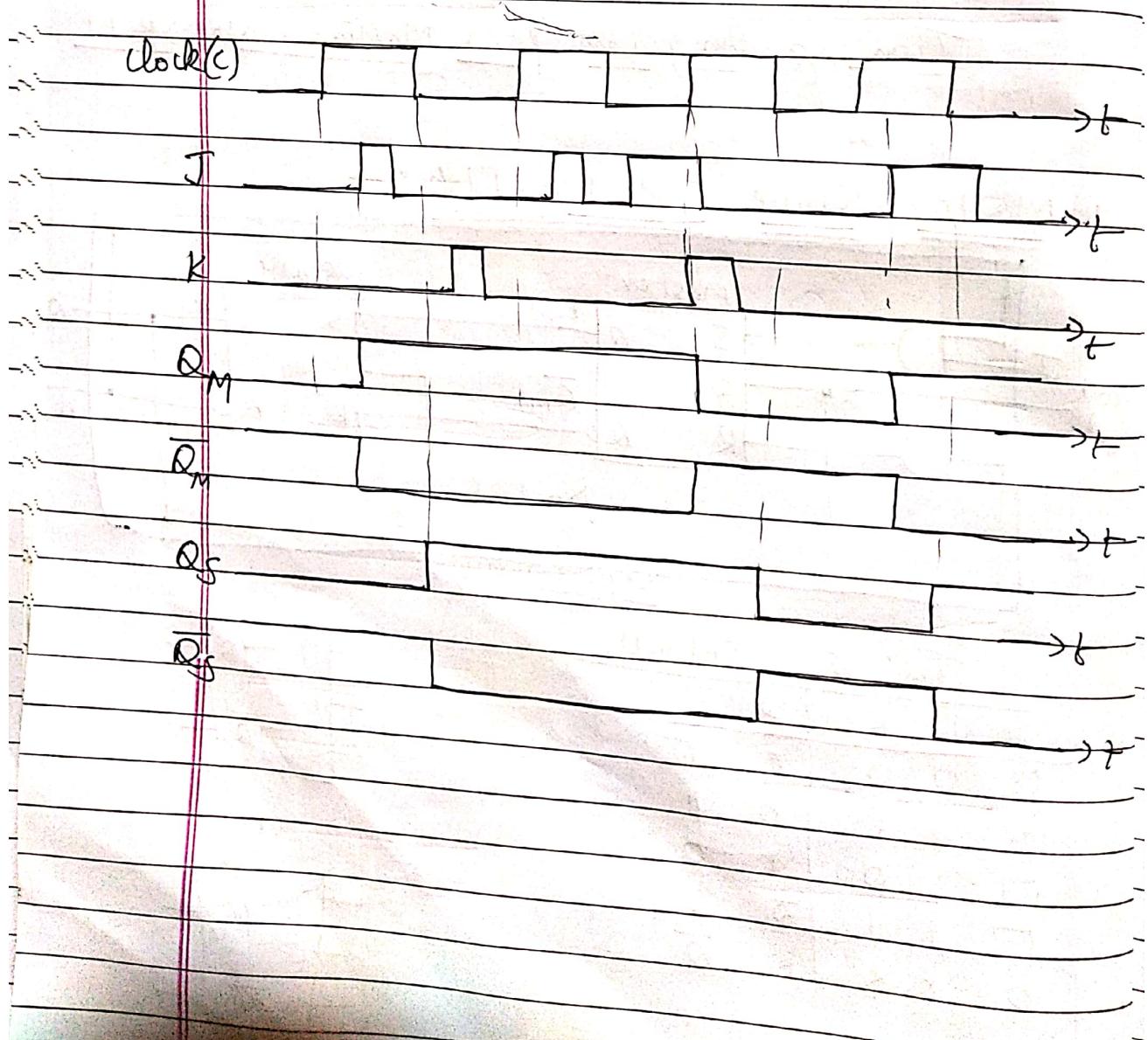
→ When $C=1$ & $J=K=0$, o/p of and-gate is 0. & $S=R=0$.

∴ Master retains the previous output value. On the falling edge of clock, Slave follows the master output.

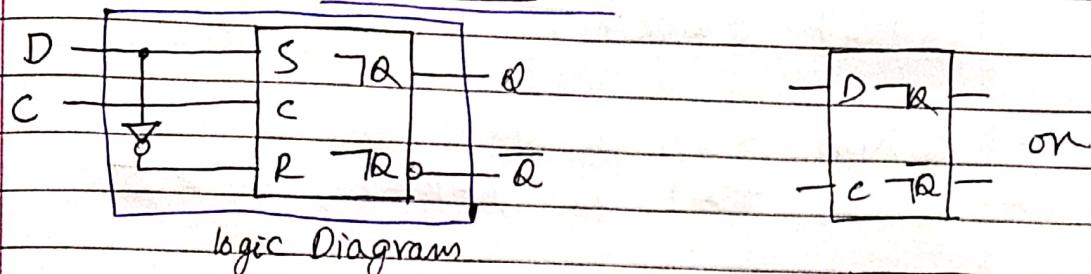
→ When $J=0$ & $K=1$, o/p of lower and-gate is 1, i.e., $S=0$ & $R=1$ ∴ $Q_M=1$ & $\bar{Q}_M=0$

→ When $J=1$ & $K=0$, o/p of upper and-gate is 1, i.e., $S=1$ & $R=0$. ∴ $Q_M=0$ & $\bar{Q}_M=1$

→ When $J=K=1$ Output Toggles.



iii) Master-Slave D-FF :-



C	D	Q^+	\bar{Q}^+	D-72
0	0	0	1	\bar{Q}
1	1	1	0	Q
0	X	Q	\bar{Q}	

Function Table

Logic Symbol.

- When $C=1$, master saves the D i/p.
- At the falling edge of the clock the state of the master is transferred to the slave.

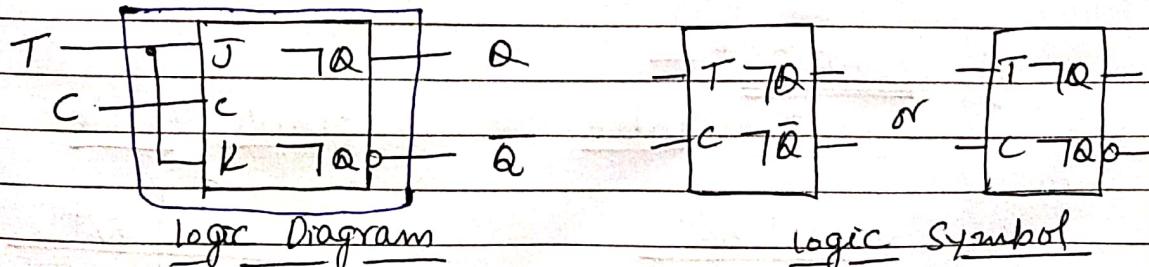
clock | | | | | → t

D | | | | | → t

Q_M | | | | | → t

Q_S | | | | | → t

iv) Master-Slave T-FF :-



Logic Symbol

C	T	Q^+	\bar{Q}^+
0	0	Q	\bar{Q}
1	1	\bar{Q}	Q
0	X	Q	\bar{Q}

→ J & K input terminals are tied together so that $J = K = T$.

→ When $T=0$ i.e., $J=K=0$, $Q^+ = Q$

→ When $T=1$ i.e., $J=K=1$, $Q^+ = \bar{Q}$

6.6. Characteristic Equations

i) SR-PF :-

Function Table

SR	Q^+
0 0	Q
0 1	0
1 0	1
1 1	-

Truth Table

S	R	Q	Q^+
0	0	0	0
0	1	1	1
1	0	0	0
1	1	0	1
		1	1
		0	0

K-map:

S	R	Q	Q ⁺
0	0	0	0
1	0	1	1

$$Q^+ = S + \bar{R}Q$$

ii) D-PF :-

Function Table

D	Q^+
0	0
1	1

Truth Table

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

K-map

D	\bar{Q}	Q	1
0	0	0	0
1	1	1	D

$$Q^+ = D$$

iii) JK - FF :-Function Table

J	K	Q	Q ⁺
0	0	0	Q
0	1	0	0
1	0	1	1
1	1	1	Q

Truth Table

J	K	Q	Q ⁺
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

K-map

J	Q	00	01	11	10
0	0	0	1	0	0
1	1	1	1	0	1

$$Q^+ = \bar{J}\bar{Q} + \bar{K}Q$$

iv) T - FF :-Function Table

T	Q	Q ⁺
0	Q	Q
1	Q	Q

Truth Table

T	Q	Q ⁺
0	0	0
0	1	1
1	0	1
1	1	0

K-map

T	Q	00	01
0	0	0	1
1	1	1	0

$$Q^+ = \bar{T}Q + T\bar{Q}$$

$$Q^+ = T \oplus Q$$

6.7 Registers

- A register is simply a collection of flip-flops taken as an entity.
- Registers holds information within a digital system so as to make it available to the logic elements during the computing process.
- The 0-1 combinations are known as the state or content of the register.
- Registers that are capable of moving information positionwise upon the occurrence of a clock signal are called shift registers.

Classification :-

- Based on the way they can move the information in one or two directions registers can be unidirectional or bidirectional.
- The manner in which information is entered into or outputted from a register is another way of categorization: SISO, SIPD, PISO, PIPO.

i) Serial-in Serial-out shift register : SISO

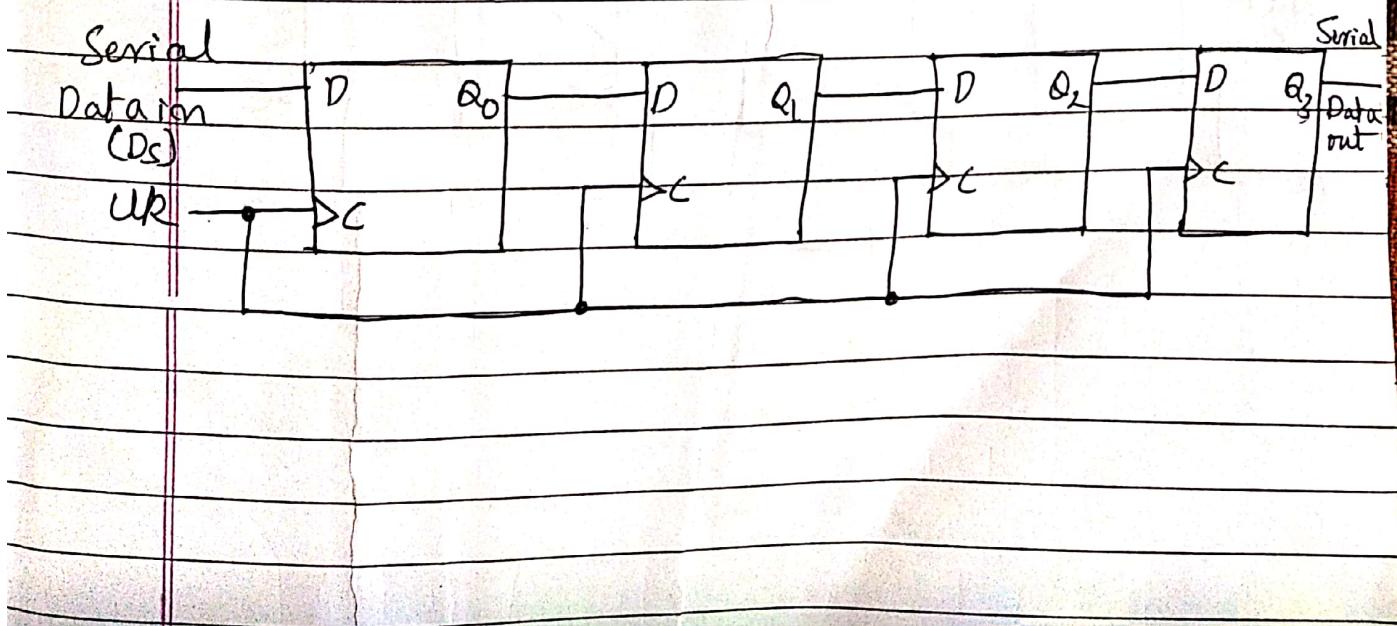
- It is a unidirectional shift register.
- SISO is constructed using positive-edge-triggered D flip-flops.
- The Q output of each flip-flop is connected to the D input of the flip-flop to its right.

→ The control inputs of all the flip-flops are connected together to a common synchronizing signal called the clock.

→ Upon the occurrence of a positive edge of the clock signal, the content of each flip-flop is shifted one position to the right.

Eg:- Let the initial content be $Q_0 Q_1 Q_2 Q_3 = 0000$.
Let us shift the data ~~(000)~~ 0011 serially into SISO.

clock pulses	UK	Serial data in (D _s)	$Q_0 \ Q_1 \ Q_2 \ Q_3$
-	-	-	0 0 0 0
1	↑	1 (LSB)	1 0 0 0
2	↑	1	1 1 0 0
3	↑	0	0 1 1 0
4	↑	0	0 0 1 1
5	↑	x	x 0 0 1
6	↑	x	x x 0 0
7	↑	x	x x x 0
SISO			



ii) Serial-in Parallel-out shift register (SIP)

→ It is a unidirectional shift register

→ outputs are provided from each flip-flop.

→ Once information is shifted into the register, the information is available as a single entity i.e., parallel out.

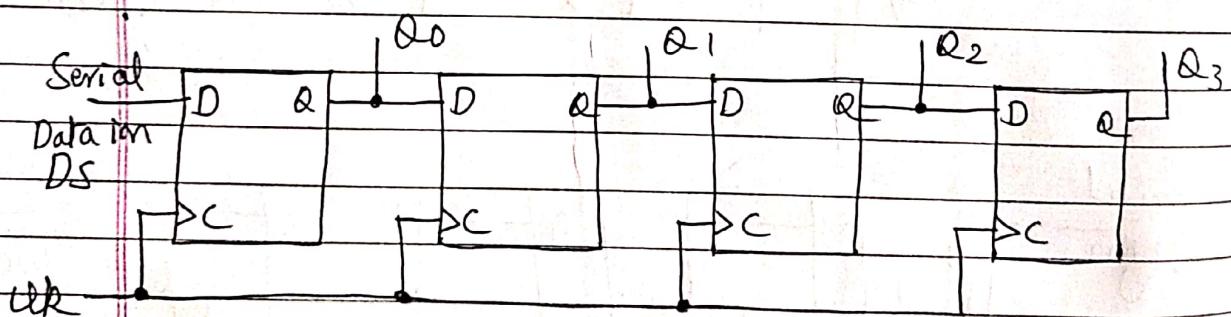
Ex:-

Eg:- Let the initial value be $Q_0 Q_1 Q_2 Q_3 = 0000$

Let us shift the data 0011 serially into SIP.

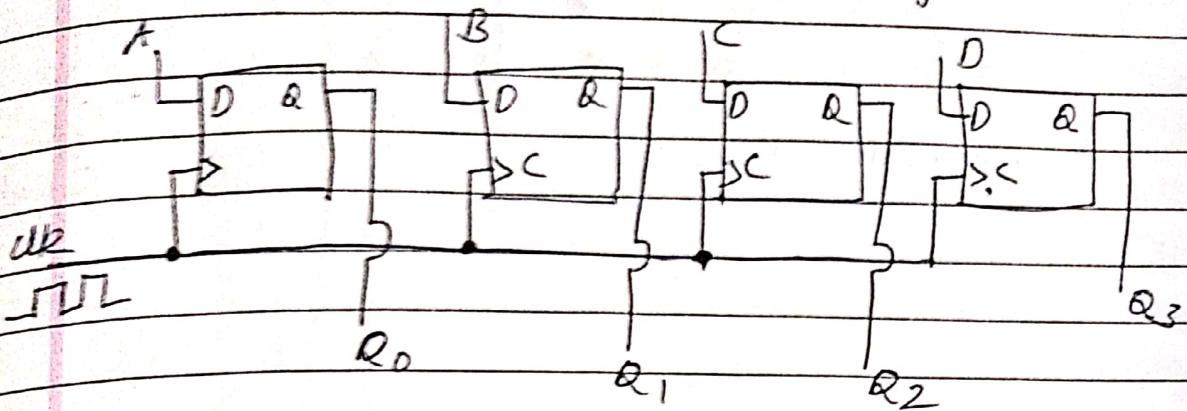
clock pulses	Clk	D ₅	Q ₀ Q ₁ Q ₂ Q ₃
-	-	-	0 0 0 0
1	↑	1	1 0 0 0
2	↑	1	1 1 0 0
3	↑	0	0 1 1 0
4	↑	0	0 0 1 1

Serial-in parallel-out



iii) Parallel-in Parallel-out shift register (PIPO)

→ It is a unidirectional shift register



→ A B C D are parallel-in data

→ Q₀, Q₁, Q₂, Q₃ are parallel-out data

Eg:- Let initial values be Q₀, Q₁, Q₂, Q₃ = 1100 & A B C D = 0011

Unit pulse	clk	Q ₀ Q ₁ Q ₂ Q ₃	parallel-in
-	-	1 1 0 0	
1	↑	0 0 1 1	parallel-out

iv) Parallel-in unidirectional shift register :-

→ The operation of the register is controlled by the Load/Shift line.

→ When Load/shift = 0 → The signals on the parallel-data-in lines T_AT_BT_CT_D are transferred into the register upon the occurrence of a positive edge clock signal.

→ When Load/shift = 1 → It functions as a unidirectional shift register with serial data-in.

→ It can function as PIPO & PISO register.

U_k	I_A	I_B	I_C	I_D	Q_A	Q_B	Q_C	Q_D
1	1	1	0	1	1	1	0	1
↑	x	x	x	x	x	1	1	0
↑	x	x	x	x	x	x	1	1
↑	x	x	x	x	x	x	x	1

parallel-in

serial-out

parallel-out

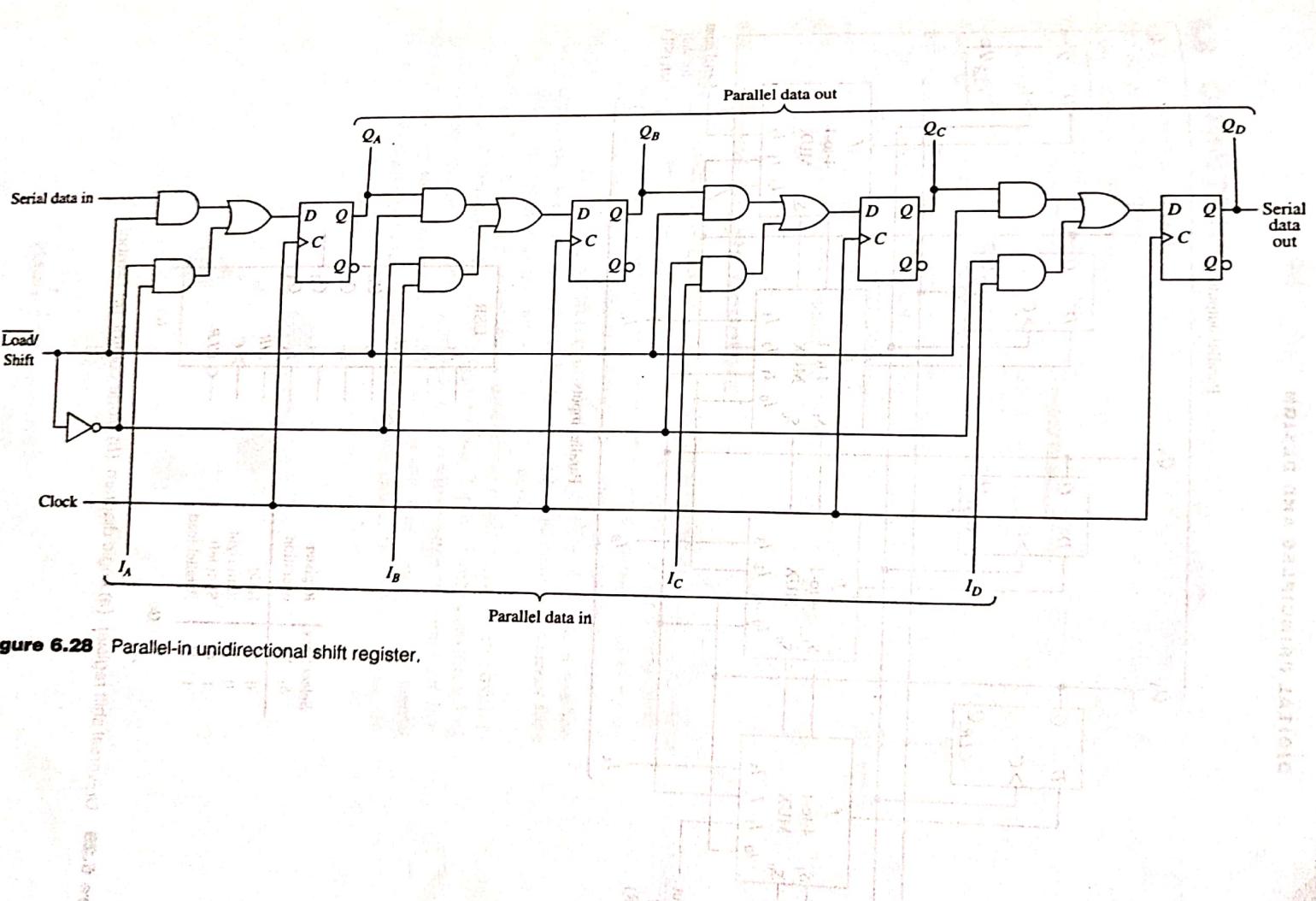


Figure 6.28 Parallel-in unidirectional shift register.

6.8 Counters

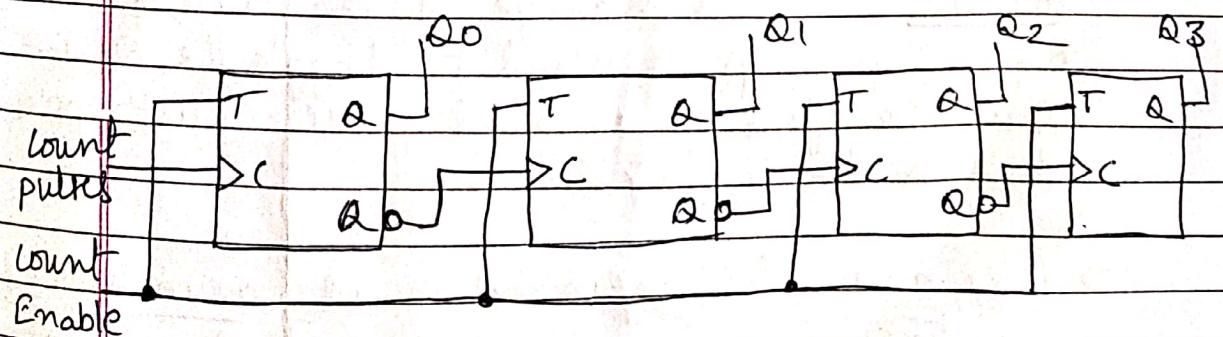
Date / / 120

- Its primary function is to produce a specified output pattern sequence.
- It is also a pattern generator.
- Each of the 0-1 combinations that are stored in the collection of flip-flops that comprise the counter is known as a state of the counter.
- The total number of states is called its modulus.
- If a counter has 'm' distinct states, then it is called a modulus-m counter or mod-m counter.
- The order in which the states appear is referred to as its counting sequence.
- The counting sequence is often depicted by a directed graph called a state diagram.

6.8.1 i) Binary Ripple Counter (mod-16 counter) :-

- counters whose counting sequence corresponds to that of the binary numbers are called binary counters.
- The modulus of a binary counter is 2^n , where n is the number of flip-flops in the counter.

Eg:- 4-bit binary up-counter (mod-16 counter)



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
<hr/>			
0	0	0	0

count
pulse

Q_0

Q_1

Q_2

Q_3

→ The binary counter is known as a ripple counter since a change in the state of the Q_{i-1} flip-flop is used to toggle the Q_i FF. Thus the effect of a count pulse must ripple through the counter.

→ They are also referred to as asynchronous counters.

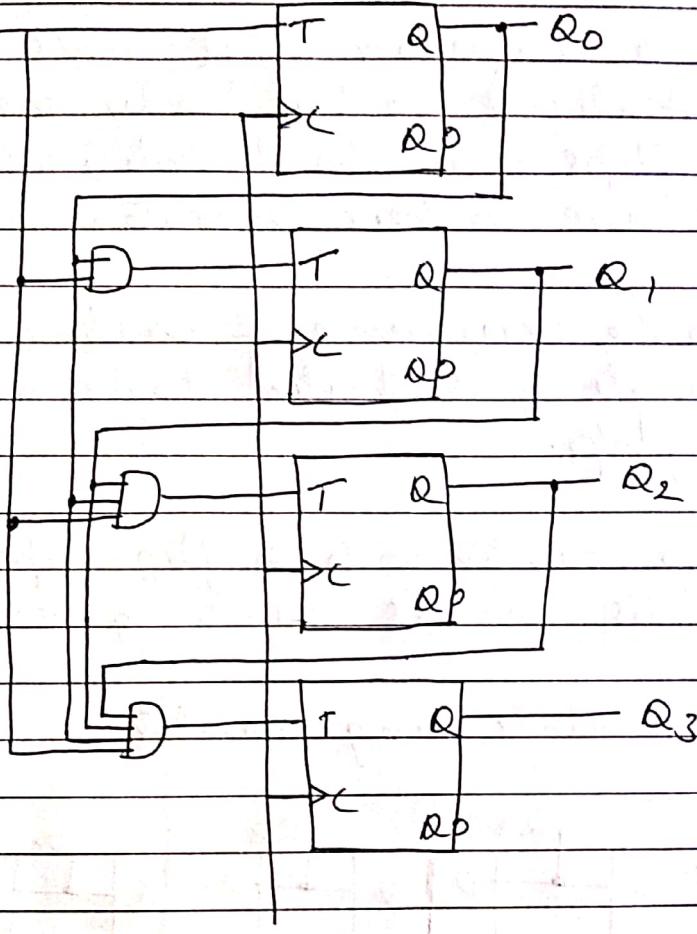
6.2 ii) Synchronous Binary Counter :-

→ The count pulses are applied directly to the control inputs, C, of all the clocked flip-flops.

Eg:- 4-bit synchronous binary up counter

Count

Enable



Q₃ Q₂ Q₁ Q₀

0 0 0 0

0 0 0 1

0 0 1 0

0 0 1 1

0 1 0 0

0 1 0 1

0 1 1 0

1 0 0 0

1 0 0 1

1 0 1 0

1 0 1 1

1 1 0 0

1 1 0 1

1 1 1 0

1 1 1 1

6.8.3 Counters Based on Shift Registers:

→ Types of non-binary counters are:
ring counter & switch-tail counter.

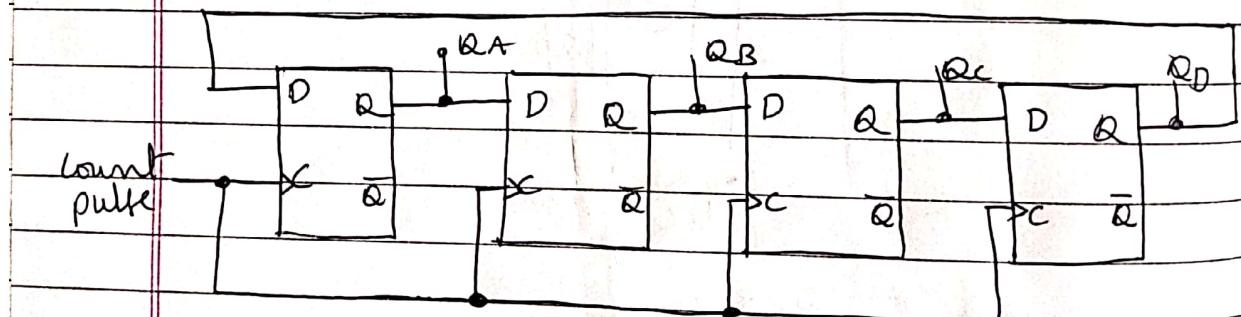
i) Ring Counter :-

→ It is a circular shift register which is initialized so that only one of its flip-flops is in the 1-state; while the others are in their 0-state.

→ Upon the occurrence of each count pulse, the single 1 is shifted to its adjacent flip-flop.

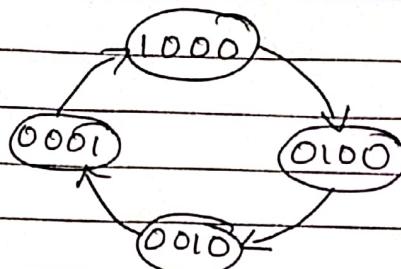
→ A ring counter with n flip-flops has only n -states in its counting sequence.

Eg:- Mod-4 ring counter



count pulse	Q _A	Q _B	Q _C	Q _D
↑	1	0	0	0
↑	0	1	0	0
↑	0	0	1	0
↑ -	-	0	0	1
	-	1	0	0

Truth Table



State Diagram

ii) Switch-tail counter

→ Also known as the twisted-ring counter or Johnson counter.

→ It has 2^n states where $n = \text{no. of FF}$

