MODULE-5b. Fabrication

SYLLABUS

Fabrication of p-n junctions Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, metallization. (Text 1: 5.1)

Text Books: 1. Ben. G. Streetman, Sanjay Kumar Banergee, "Solid State Electronic Devices", 7thEdition, Pearson Education, 2016, ISBN 978-93-325-5508-2.

Contents

1. Fabrication of p-n junctions

The basic P-N Junction fabrication steps will be described in the following sections. Some of these steps may be carried out many times, in different combinations and/or processing conditions during a complete fabrication run.

1.1. Oxidation

- In **oxidation**, silicon reacts with oxygen to form silicon dioxide (SiO2). To speed up this chemical reaction, it is necessary to carry out the oxidation at high temperatures (e.g., 1000–1200°C) and inside ultraclean furnaces.

$$Si + O_2 \rightarrow SiO_2 \text{ (dry oxidation)}$$

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \text{ (wet oxidation)}$$

- To avoid the introduction of even small quantities of contaminants (which could significantly alter the electrical properties of the silicon), it is necessary to operate in a **clean room**.
- Particle filters are used to ensure that the airflow in the processing area is free from dust. All personnel must protect the clean-room environment by wearing special lint-free clothing that covers a person from head to toe.
- The oxygen used in the reaction can be introduced either as a high-purity gas (referred to as a "**dry oxidation**") or as steam (forming a "**wet oxidation**").

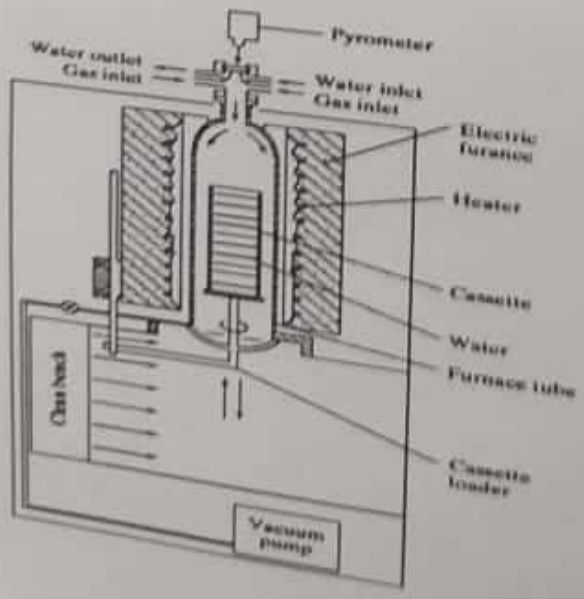


Figure 5–1b Vertical furnace for large Si wafers. The silica wafer holder is loaded with Si wafers and moved into the furnace above for oxidation, diffusion, or deposition operations.

- In general, wet oxidation has a faster growth rate, but dry oxidation gives better electrical characteristics.
- The thermally grown oxide layer has excellent electrical insulation properties. can be used to form excellent MOS capacitors.
- Silicon dioxide can also serve as an effective mask against many impurities, allowing the introduction of dopants into the silicon only in regions that are not covered with oxide.
- Silicon dioxide is a transparent film, and the silicon surface is highly reflective. If white light is shone on an oxidized wafer, constructive and destructive interference will cause certain colors to be reflected.
- The wavelengths of the reflected light depend on the thickness of the oxide layer. In fact, by categorizing the color of the wafer surface, one can deduce the thickness of the oxide layer.

1.2. Diffusion

- **Diffusion** is a process by which atoms move from a high-concentration region to a low- concentration region.
- This is very much like a drop of ink dispersing through a glass of water except that it occurs much more slowly in solids.
- In VLSI fabrication, this is a method to introduce impurity atoms (dopants) into silicon to change its resistivity.
- The rate at which dopants diffuse in silicon is a strong function of temperature.
- Diffusion of impurities is usually carried out at high temperatures (1000–1200°C) to obtain the desired doping profile.
- When the wafer is cooled to room temperature, the impurities are essentially "frozen" in position.
- The diffusion process is performed in furnaces similar to those used for oxidation. The depth to which the impurities diffuse depends on both the temperature and the processing time.
- The most common impurities used as dopants are boron, phosphorus, and arsenic. Boron is a p-type dopant, while phosphorus and arsenic are n-type dopants.
- These dopants can be effectively masked by thin silicon dioxide layers. By diffusing boron into an n-type sub- strate, a pn junction is formed (diode).
- if the dopant atoms are supplied
- continuously, such that the concentration at the surface is maintained at a constant value, the distribution follows what is called a **complementary error function.**

- Common impurity source materials for diffusions in Si are B_2O_3, BBr_3, and BCl_3 for boron; phosphorus sources include PH_3, $P2O_5$, and $POCl_3$

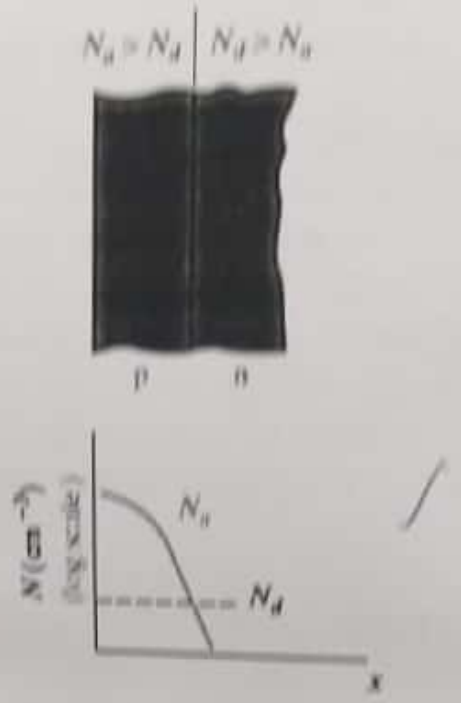


Figure 5-2 Impurity concentration profile for fabricating a p-n junction by diffusion.

1.3. Rapid Thermal Processing

- Rapid thermal processing (RTP) is a semiconductor manufacturing process which heats silicon wafers to high temperatures (over 1,000 °C) on a timescale of several seconds or less. During cooling, however, wafer temperatures must be brought down slowly to prevent dislocations and wafer breakage due to thermal shock.
- Such rapid heating rates are often attained by high intensity lamps or lasers. These processes are used for a wide variety of applications in semiconductor manufacturing including dopant activation, thermal oxidation, metal reflow and chemical vapor deposition

3 types of Heat Flow Mechanisms:

1.) Conduction: Flow of heat between two bodies in intimate contact.Heat flow per unit area in a solid is expressed in terms of a solids thermal conductivity

2.) Convection: Flow of heat between two bodies through an intermediate medium (a gas in our case)For a gas with effective heat transfer coefficient

3.) Radiation: Flow of heat between two bodies through radiation and absorption of light. use the spectral radiant exitance= the radiated power per area per unit wavelength,

3 Type of Process

1) rapid thermal oxidation,
2) annealing of ion implantation,
3) chemical vapor deposition,

- a single wafer is held (face down to minimize particulates) on low-thermal-mass quartz pins, surrounded by a bank of high-intensity (tens of kW) tungsten– halogen infrared lamps, with gold-plated reflectors around them.
- By turning on the lamps, the high-intensity infrared radiation shines through the quartz chamber and is absorbed by the wafer, causing its temperature to rise very rapidly (~50-100°C>s).
- The processing temperature can be reached quickly, after the gas flows have been stabilized in the chamber.
- At the end of the process, the lamps are turned off, allowing the wafer temperature to drop rapidly, once again because of the much lower thermal mass of an RTP system compared to a furnace.
- In RTP, therefore, temperature is essentially used as a "switch" to start or quench the reaction. Two critical aspects of RTP are ensuring temperature uniformity across large wafers
- ,RTP operates at higher temperatures (~1000°C) but does so for only a few seconds (compared to minutes or hours in a furnace).

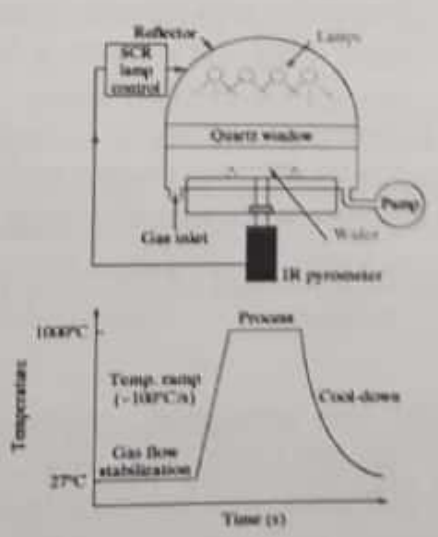


Figure 5-3 Schematic diagram of a rapid thermal processor and typical time-temperature profile.

1.4. Ion Implantation

- **Ion implantation** is another method used to introduce impurities into the semiconductor crystal. An ion implanter produces ions of the desired dopant, accelerates them by an electric field, and allows them to strike the semiconductor surface.
- Ion implantation can be used to form a deep region of doping using a **two step** procedure.
  - A high concentration of dopant is deposited near the surface in the **predeposition** or predep stage
  - The dopant source is then removed and the wafer heated to cause redistribution of the dopant via diffusion in the **drive-in stage**

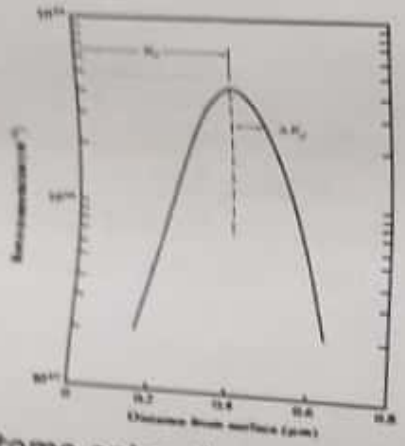


Figure 5–4 Distribution of implanted impurities: gaussian distribution of boron atoms about a projected range R_p (in this example, a dose of 10^{14} B atoms/cm² implanted at 140 keV).

- As the impurity atoms enter the crystal, they give up their energy to the lattice in collisions and finally come to rest at some average penetration depth, called the **projected range R_p.**
- Depending on the impurity and its implantation energy, the range in a given semiconductor may vary from a few hundred angstroms to about 1 μm.
- For most implantations the ions come to rest distributed almost evenly about the projected range R_p, as shown in Fig. 5–4. An implanted dose of h ions>cm2 is distributed approximately by a gaussian formula.

$$N(x) = \frac{\phi}{\sqrt{2\pi}\Delta R_p} \exp\left[-\frac{1}{2}\left(\frac{x - R_p}{\Delta R_p}\right)^2\right] \qquad (5\text{–}1a)$$

- where ΔRp, called the **straggle**, measures the half-width of the distribution at $e^{-1/2}$ of the peak (Fig. 5–4).
- Both Rp and ΔRp increase with increasing implantation energy. These parameters are shown as a function of energy

- This control over doping level, along with the uniformity of the implant over the wafer surface, make ion implantation particularly attractive for the fabrication of Si integrated circuits.

Disadvantage

- One problem with this doping method is the lattice damage which results from collisions between the ions and the lattice atoms.
- most of this damage can be removed in Si by heating the crystal after the implantation. This process is called **annealing**.
- Although Si can be heated to temperatures in excess of 1000°C without difficulty, GaAs and some other compounds tend to dissociate at high temperatures.
- For example, As evaporation from the surface of GaAs during annealing damages the sample. Therefore, it is common to encapsulate the GaAs with a thin layer of silicon nitride during the anneal.
- Another approach to annealing either Si or compounds is to heat the sample only briefly (e.g., 10 s) using RTP, rather than a conventional furnace. Annealing leads to some unintended diffusion of the implanted species.
- It is desirable to minimize this diffusion by optimizing the annealing time and temperature. The profile after annealing is given by

$$N(x) = \frac{\phi}{\sqrt{2\pi}(\Delta R_p^2 + 2Dt)^{1/2}} \exp\left[-\frac{1}{2}\left(\frac{(x - R_p)^2}{\Delta R_p^2 + 2Dt}\right)\right] \quad (5\text{–}16)$$

1.5. Chemical vapor deposition (CVD)

- Chemical vapor deposition (CVD) is a process by which gases or vapors are chemically reacted, leading to the formation of solids on a substrate.
- CVD can be used to deposit various materials on a silicon substrate including SiO2, Si3N4, polysilicon, and so on.
- The properties of the CVD oxide layer are not as good as those of a thermally grown oxide, but they are sufficient to allow the layer to act as an electrical insulator.
- SiO2 films can also be formed by **low pressure chemical vapor deposition** (LPCVD) (Fig. 5–6) or **plasma enhanced CVD** (PECVD). The key differences are that thermal oxidation.

- consumes Si from the substrate, and very high temperatures are required whereas CVD of SiO2 does not consume Si from the substrate and can be done at much lower temperatures.
- The CVD process reacts a Si-containing gas such as SiH4 with an oxygen-containing precursor, causing a chemical reaction, leading to the deposition of SiO2 on the substrate.

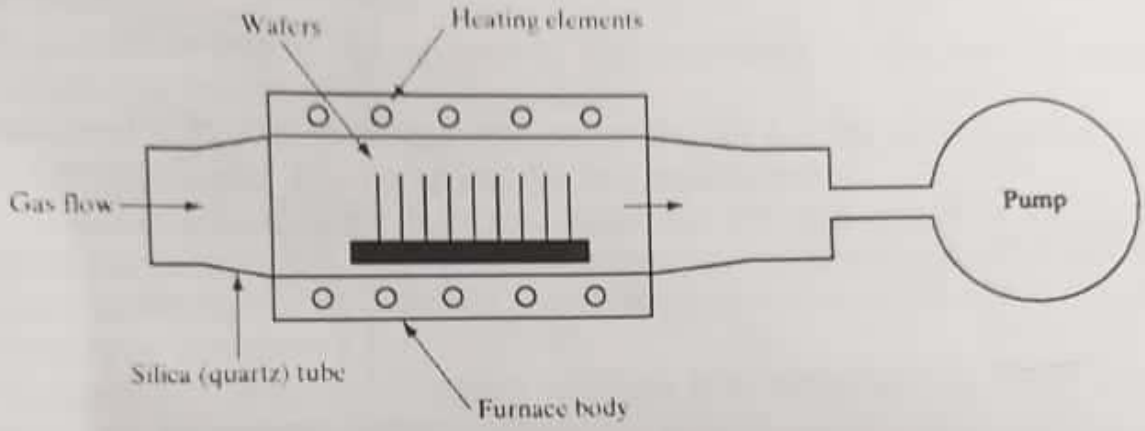


Figure 5–6
Low-pressure chemical vapor deposition (LPCVD) reactor.

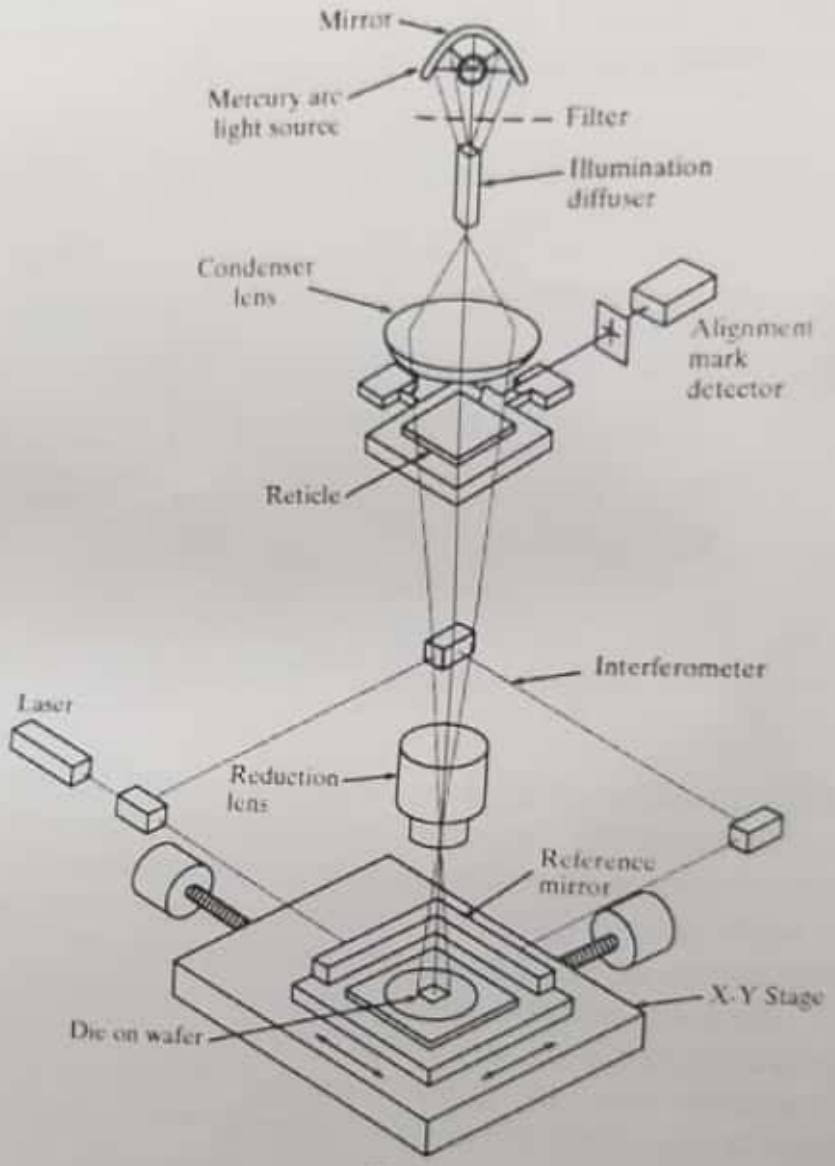
- As a complicated device structure is built up, the Si substrate may not be available for reaction, or there may be metallization on the wafer that cannot withstand very high temperatures.
- In such cases, CVD is a necessary alternative. Although we have used deposition of SiO2 as an important example, LPCVD is also widely used to deposit other dielectrics such as silicon nitride (Si3N4), and polycrystalline or amorphous Si.
- It should also be clear that the VPE of Si or MOCVD of compound semiconductors is really a special, more challenging example of CVD where not only must a film be deposited, but single-crystal growth must also be maintained.

1.6. Photolithography

- Lithography refers to the transfer of an image onto paper using a plate and ink-soluble grease.
- Photolithography is the transfer of an image using photographic techniques) Photolithography transfers designer generated information (device placement and interconnections).

- **First step** in photolithography is to coat the surface with approx. 1 μm of **photoresist** (PR) PR will be the medium whereby the required image is transferred to the surface.

Figure 5-7b Schematic diagram of an optical stepper.



•PR is often applied to the center of the wafer, which is then spun to force the PR over the entire surface
• the PR is approx. 1 μm thick while the wafer is 1000 μm thick. The PR is then **exposed to UV (ultraviolet)** radiation through a mask
• The masks generated from information about device placement and connection
• The UV radiation causes a chemical change in the PR

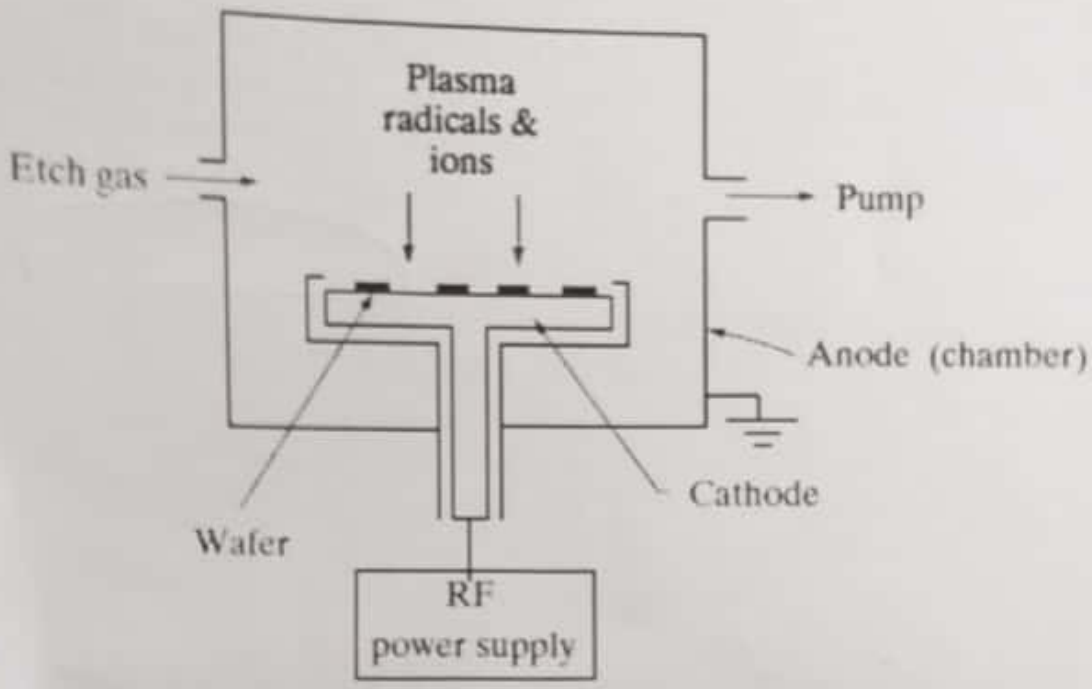
- As the name implies, the **planarizing process** is partly chemical in nature (using a basic solution), and partly mechanical grinding of the layers using an abrasive slurry.
- CMP can be achieved using a slurry of fine SiO2 particles in an NaOH solution. The expression for diffraction-limited geometry [Eq. (5–2a)] explains why there is interest in electron beam lithography. The de Broglie relation states that the wavelength of a particle varies inversely with its momentum:

$$\lambda = \frac{h}{p} \qquad (5\text{–}2c)$$

Thus, more massive or energetic particles have shorter wavelengths. Electron beams are easily generated, focused, and deflected. Since a 10-keV electron has a wavelength of about 0.1 Å, the linewidth limits become the size of the focused beam and its interaction with the photoresist layer.

1.7. Etching

- To permanently imprint the photographic patterns onto the wafer, chemical (**wet**) etching or RIE **dry etching** procedures can be used.
- Chemical etching is usually referred to as **wet etching**.
- Different chemical solutions can be used to remove different layers. For example, hydrofluoric (HF) acid can be used to etch SiO2, potassium hydroxide (KOH) for silicon, phosphoric acid for aluminum, and so on.
- Two most important issues in etching are **selectivity** and **anisotropy**.
- – **Selectivity** refers to the ability of an etchant to remove one material on the surface while leaving another intact.
- – **Isotropic** refers to the tendency of the etching to proceed laterally as well as downward
- The patterned photoresist layer can be used as an effective masking layer to protect materials below from wet chemical **etching** or **reactive ion etching** (RIE).
- Silicon dioxide, silicon nitride, polysilicon, and metal layers can be selectively removed using the appropriate etching methods.
- In wet etching, the chemical usually attacks the exposed regions that are not protected by the photoresist layer in all directions (**isotropic etching**).



- Depending on the thickness of the layer to be etched, a certain amount of undercut will occur. Therefore, the dimension of the actual pattern will differ slightly from the original pattern.
- If exact dimension is critical, RIE **dry etching** can be used.
- This method is essentially a directional bombardment of the exposed surface using a corrosive gas (or ions).
- The cross section of the etched layer is usually highly directional (**anisotropic etching**) and has the same dimension as the photoresist pattern. A comparison between isotropic and anisotropic etching is given in Fig. A.3.

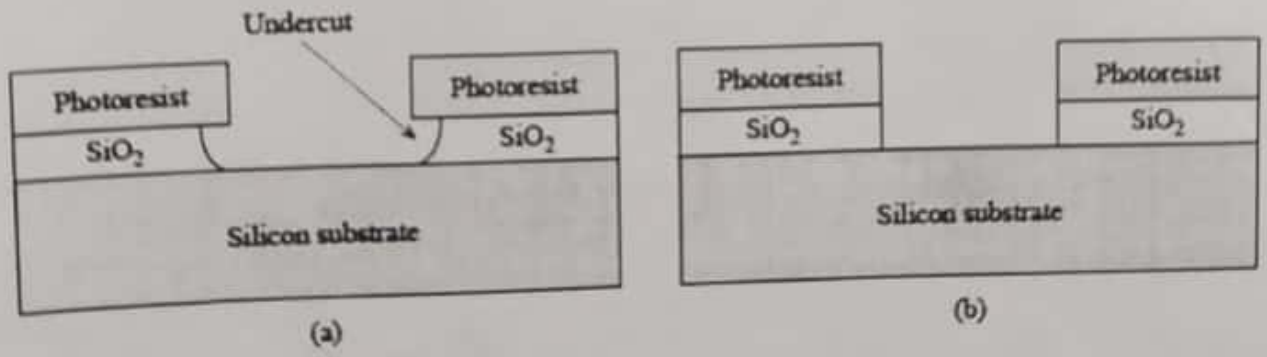


Figure A.3 (**a**) Cross-sectional view of an isotropic oxide etch with severe undercut beneath the photoresist layer. (**b**) Anisotropic etching, which usually produces a cross section with no undercut.

1.8. Metallization

- The purpose of metallization is to interconnect the various components (transistors, capacitors, etc.) to form the desired integrated circuit.
- Metallization involves the deposition of a metal over the entire surface of the silicon. The required interconnection pattern is then selectively etched.
- The metal layer is normally deposited via a sputtering process. A pure metal disk (e.g., 99.99% aluminum target) is placed under an Ar (argon) ion gun inside a vacuum chamber.
- The wafers are also mounted inside the chamber above the target. The Ar ions will not react with the metal, since argon is a noble gas. However, the ions are made to physically bombard the target and literally knock metal atoms out of the target.
- These metal atoms will then coat all the surface inside the chamber, including the wafers.
- The thickness of the metal film can be controlled by the length of the sputtering time, which is normally in the range of 1 to 2 minutes. The metal interconnects can then be defined using photolithography and etching steps.

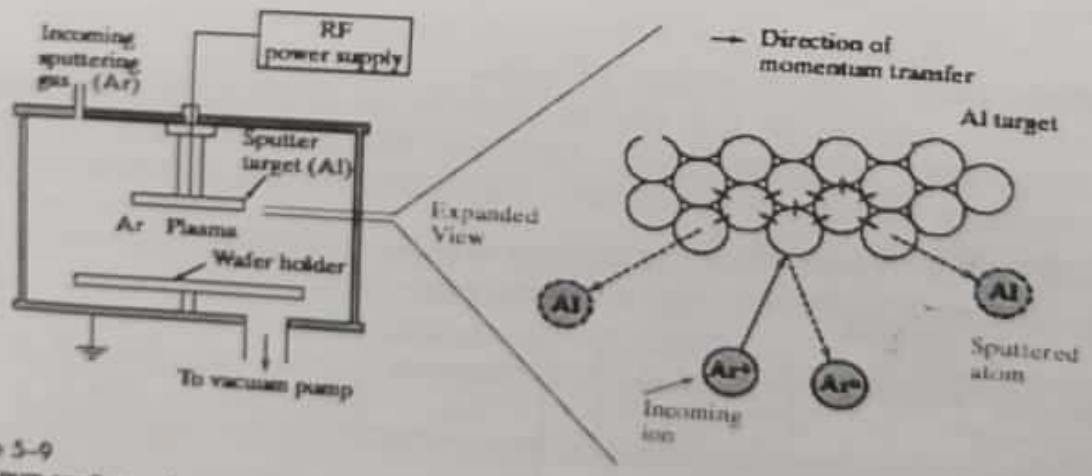


Figure 5–9
Aluminum sputtering by Ar^+ ions. The Ar^+ ions with energies of ~1–3 keV physically dislodge Al atoms which end up depositing on the Si wafers held in close proximity. The chamber pressures are kept low such that the mean free path of the ejected Al atoms is long compared to the target-to-wafer separation.