

**Third Semester B.E. Degree Examination, June/July 2019
Computer Organization**

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing
ONE full question from each module.

Module-1

1. a. Write the basic performance equation. Explain the role of each of the parameters in the equation of the performance of the computer. (04 Marks)
b. Draw and explain the connections between the processor and the main memory. (08 Marks)
c. Write a program to evaluate the arithmetic statement $Y = (A + B) * (C + D)$ using three – address, two-adders, one adderss and zero – address instructions. (08 Marks)

OR

2. a. What is an addressing mode? Explain any four addressing modes with examples. (08 Marks)
b. Explain the concept of stack frames, when subroutines are nested. (06 Marks)
c. Explain the shift and rotate operations with examples. (06 Marks)

Module-2

3. a. Give comparison between memory mapped I/O and I/O mapped I/O. (04 Marks)
b. Explain the following methods of handling interrupts from multiple devices.
i) Interrupt nesting /priority structure
ii) Daisy chain method. (08 Marks)
c. What is bus arbitration? Explain distributed arbitration with a neat diagram. (08 Marks)

OR

4. a. Draw neat timing diagrams and explain
i) Multicycle synchronous bus transfer for a read operation.
ii) Asynchronous bus transfer for a write operation. (12 Marks)
b. Explain the following with respect to USB.
i) USB architecture
ii) USB addressing. (08 Marks)

Module-3

5. a. With a neat diagram, explain the internal organization of a $2M \times 8$ dynamic memory chip. (08 Marks)
b. Distinguish between SRAM and DRAM. (04 Marks)
c. Describe any two mapping functions in cache. (08 Marks)

OR

6. a. What is virtual memory? With a diagram, explain how virtual memory address is translated? (08 Marks)
b. Define the following :
i) Memory latency ii) Memory bandwidth iii) Hit-rate iv) Miss-penalty. (04 Marks)
c. Describe the working principle of a typical magnetic disk. (08 Marks)

Module-4

- 7 a. Convert the following pairs of decimal numbers to 5-bit signed 2's complement numbers and add them. State whether overflow has occurred.
i) -5 and 7 ii) -10 and -13 iii) -14 and 11.
b. Draw 4-bit carry-look ahead adder and explain.
c. Explain Booth's algorithm, multiply +15 and -6 using Booth's multiplication.

OR

- 8 a. Explain the concept of carry-save addition for the multiplication operation $M \times 0$ 4-bit operands, with diagram and suitable example.
b. Explain IEEE standard for floating – point numbers.
c. Perform the non-restoring division for $8 \div 3$ by showing all the steps.

Module-5

- 9 a. Draw and explain multiple bus organization of CPU. And write the control sequence instruction Add-R₄, R₅, B₆ for the multiple bus organization.
b. Explain with block diagram the basic organization of a micro programmed controller.

OR

- 10 a. With block diagram, explain the working of a microwave oven.
b. Explain the structure of general-purpose multiprocessors with diagrams.

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Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Computer Organization

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain with a neat diagram the connection between the processor and the computer memory. (05 Marks)
 b. Explain the Basic Instruction types with example. (05 Marks)
 c. Define Addressing mode, explain the various addressing modes with example. (10 Marks)

OR

- 2 a. Write an assembly program that reads a line of characters and display it. (05 Marks)
 b. What are assembler directives? Point out and explain the various directives with example. (05 Marks)
 c. Point out various shifts and rotate instruction and example with a neat diagram and example. (10 Marks)

Module-2

- 3 a. Define interrupt. Point out and explain the various ways of enabling and disabling interrupts. (07 Marks)
 b. What are Exceptions? Point out and explain the different kinds of exceptions. (05 Marks)
 c. What is interrupt nesting, explain with a neat diagram the implementation of interrupt priority, using individual interrupt request and acknowledge lines. (08 Marks)

OR

- 4 a. What is Bus Arbitration? Explain centralized and distributed arbitration. With a neat diagram. (10 Marks)
 b. Explain Universal serial Bus tree structure and split bus operation with a neat diagram. (10 Marks)

Module-3

- 5 a. Explain synchronous DRAMS with a block diagram. (05 Marks)
 b. Define ROM ; point out and explain various types of ROMS. (05 Marks)
 c. Define cache memory, explain various types of it with a neat block diagram. (10 Marks)

OR

- 6 a. What is Virtual memory? Explain virtual memory organization. (07 Marks)
 b. Explain the optical disk organization with a neat diagram. (10 Marks)
 c. Define Hit rate and miss penalty. (03 Marks)

Module-4

- 7 a. Draw 4-bit carry-look ahead adder and explain. (10 Marks)
 b. Perform multiplication for -13 and $+9$ using Booth's Algorithm and explain Booth's Algorithm process. (10 Marks)

OR

- 8 a. Explain with a neat figure the circuit arrangement for binary division.
b. Explain IEEE standard for floating point number.

Module-5

- 9 a. Explain three – bus organization of the datapath with a neat block diagrams.
b. Explain Hard Wired Control Unit Organization in a processing unit.
c. Write the control sequence for execution of the Instruction. Add (R_3), R_1 in the executing a complete instruction.
- 10 a. Explain briefly the block diagram of a digital camera.
b. With a neat block diagram, explain the working of microwave oven in an embedded system.

OR

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CBCS SCHEME

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15CS34

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019 Computer Organization

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing
ONE full question from each module.

Module-1

- 1 a. Define the functions of following processor registers :
i) MAR ii) MDR iii) IP iv) IR. (04 Marks)
b. How to measure the performance of a computer? Explain. (05 Marks)
c. Compute the content of 8 bit register namely R1 and R2 containing a value of $-17_{(10)}$ and $+98_{(10)}$ with initial carry bit as 1 after performing following shift or rotate operations by 2 times. i) SHR R1, 2 ii) SAR R1, 2 [Arithmetic shift]
iii) ROR R2, 2 iv) RCR R2, 2 [Rotate right with carry]. (07 Marks)

OR

- 2 a. What is the need of processor stack? Explain a commonly used layout for information in a subroutine stack frame. (06 Marks)
b. With relevant examples briefly explain about any 2 encoding types of machine instruction. (05 Marks)
c. With a memory layout starting at address 'i' represent how "ABCD" data is stored in big endian and little endian assignment scheme in a system of word length 16 bits. (05 Marks)

Module-2

- 3 a. Explain how simultaneous interrupt requests from several I/O devices can be handled by processor through a single INTR line. (06 Marks)
b. What is bus arbitration? With neat diagram explain about distributed arbitration process. (06 Marks)
c. With a neat diagram, explain about how data is read in asynchronous bus scheme. (04 Marks)

OR

- 4 a. Explain with a neat block diagram, the hardware components needed for connecting a keyboard to a processor. (08 Marks)
b. With a neat sequence diagram explain the process of, how output operation is carried between processor and output device connected to host through USB hub. (08 Marks)

Module-3

- 5 a. With a neat diagram, explain the design of $2M \times 32$ memory module using $1M \times 8$ memory chips. (07 Marks)
b. Consider a cache consisting of 256 blocks of 16 words each, for a total of 4096 words and assume main memory is addressable by 16 bit address and it consists of 4K blocks. How many bits are there in each of Tag, block/set and word fields for different mapping techniques? (09 Marks)

OR

- 6 a. Explain the process of address translation with a neat diagram. (06 Mar)
 b. With a neat diagram discuss about organization of magnetic disk. (06 Mar)
 c. Calculate the average access time experienced by processor if miss penalty is 17 cycles and Miss rate is 10% and cache access time is 1 clock cycle. (04 Mar)

Module-4

- 7 a. Design and explain the working of 16 bit carry look ahead adder built from 8 bit carry look ahead adder. Compare its performance with 16 bit ripple carry adder built from 8 bit ripple carry adder. (10 Marks)
 b. Calculate the product of $-2_{(10)}X + 14_{(10)}$ using bit pair recording multiplier method. Why bit pair method is better than Booth algorithm? (06 Marks)

OR

- 8 a. Perform the non-restoring division for the given binary numbers where dividend is 1011_2 and divisor is 0101_2 with all cycles. (08 Marks)
 b. Represent $0.0625_{(10)}$ in double precision format and calculate the decimal value of A floating point number represented in single precision format as $44900000H$. (08 Marks)

Module-5

- 9 a. Write and discuss about micro-routine for complete execution of instruction Add (R1), R2 in single bus organization. (08 Marks)
 b. With a detailed block diagram explain about hardwired control unit. (08 Marks)

OR

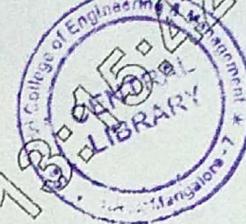
- 10 a. With a block diagram explain briefly about an embedded processor. (06 Marks)
 b. Explain briefly about different ways of implementing multiprocessor system with supportive diagrams. (06 Marks)
 c. Write the control sequence for instruction Add R4, R5, R6 for 3 bus organization. (04 Marks)

CBCS SCHEME

USN

Third Semester B.E. Degree Examination, June/July 2018 Computer Organization

15CS34



Max. Marks: 80

Time: 3 hrs.

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

- 1 a. Define Addressing Mode. Give the details of different addressing modes. (08 Marks)
b. Describe the basic operational concepts between the processor and memory. (08 Marks)

OR

- 2 a. What is Subroutine? How to pass parameters to subroutines? Illustrate with an example. (08 Marks)
b. How to encode assembly instructions into 32-bit words? Explain with examples. (08 Marks)

Module-2

- 3 a. Define Bus Arbitration. With diagrams, explain the centralized bus arbitration mechanism. (08 Marks)
b. With the help of timing diagram, briefly discuss the main phases of SCSI bus involved in its operation. (08 Marks)

OR

- 4 a. With neat diagrams, explain how to interface printer to the processor. (08 Marks)
b. Explain the following methods of handling interrupts from multiple devices.
i) Interrupt nesting/priority structure ii) Daisy chain method. (08 Marks)

Module-3

- 5 a. Describe how to translate virtual address into physical address with diagram. (08 Marks)
b. Draw and explain the internal organisation of $2M \times 8$ asynchronous DRAM chip. (08 Marks)

OR

- 6 a. Describe any two mapping functions in cache. (08 Marks)
b. Describe the principles of magnetic disk. (08 Marks)

Module-4

- 7 a. Perform the operations on 5 - bit signed numbers using 2's complement system. Also indicate whether overflow has occurred. (06 Marks)
i) $(-10) + (-13)$ ii) $(-10) - (-13)$ iii) $(-2) + (-9)$.
b. Perform the multiplication of 13 and -6 using Booth algorithm and Bit - pair recoding method. (10 Marks)

OR

- 8 a. Perform the restoring division for $8 \div 3$ by showing all the steps. (06 Marks)
b. Explain the logic diagram of 4 - bit carry look ahead adder and its operations. (10 Marks)

Module-5

- 9 a. Draw and explain multiple bus organization along with its advantages. (10 Marks)
b. Write down the control sequence for the instruction Add (R_3), R_1 for single bus organization. (06 Marks)

OR

- 10 a. With block diagram, explain the general requirements and working of digital camera. (10 Marks)
b. Write the control sequence for an unconditional branch instruction. (06 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg. $42+8 = 50$, will be treated as malpractice.



CBCS Scheme

USN

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15CS34

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018 Computer Organization

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

- 1 a. List the steps needed to execute the machine instruction Add LOCA, RO in terms of transfers between the processor and the memory along with some simple control commands. Assume that the instruction itself is stored in the memory at location INSTR and that this address is initially in register PC. The first two steps might be expressed as:
- Transfer the contents of Register PC to register MAR.
 - Issue a Read command to the memory and then wait until it has transferred the requested word into register MDR.
- Remember to include the steps needed to update the contents of PC from INSTR to INSTR+1 so that the next instruction can be fetched. (08 Marks)
- b. What is performance measurement? Explain the overall SPEC rating for the computer in a program suit. (08 Marks)

OR

- 2 a. With relevant figure define the little Endian and big Endian assignments. (04 Marks)
- b. Consider a computer that has a byte addressable memory organized in 32 bit words according to the big Endian scheme. A program reads ASCII characters entered at a keyboard and store them in successive byte location starting at location 1000. Show the contents of the two memory words at locations 1000 and 1004 after the name "Johnson" has been entered. (ASCII codes J = 4 AH, o = 6 FH, h = 68 H, n = 6 EH, S = 73 H) (04 Marks)
- c. Write about shift and rotate instruction with neat diagram and example of each. (08 Marks)

Module-2

- 3 a. With supporting diagram, explain the following with respect to interrupts:
i) Vectored interrupts
ii) Interrupt Nesting
iii) Simultaneous requests. (06 Marks)
- b. Three devices A, B and C are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt requests from C may be accepted while either A or B is being serviced. Suggest different ways in which this can be accomplished in each of the following cases:
i) The computer has one interrupt request line.
ii) Two interrupt request line, INTR1 and INTR2 are available with INTR1 having higher priority. Specify when and how interrupts are enabled and disable in each case. (06 Marks)
- c. Illustrate the tree structure of USB with diagram. (04 Marks)

OR

- 4 a. With a neat diagram, explain the centralized arbitration and distributed bus arbitration scheme. (08 Marks)
- b. With neat timing diagram illustrate the asynchronous bus data transfer during an input operation. Use handshake scheme. (08 Marks)

Module-3

- 5 a. Draw a diagram and explain the working of 16 Megabit DRAM chip configured as $2M \times 32$ memory using $512K \times 8$ memory chips.
 b. Describe organization of an $2M \times 32$ memory using $512K \times 8$ memory chips.

OR

- 6 a. Discuss in detail the working of set associative mapped cache with two blocks per set with relevant diagram.
 b. Define the following with respect to cache memory: (i) Valid bit, (ii) Dirty bit, (iii) Stale data, (iv) Flush the cache.
 c. A block-set associative cache consists of a total of 64 blocks divided into 4-blocks sets. main memory contains 4096 blocks, each consisting of 128 words.
 i) How many bits are there in a main memory address?
 ii) How many bits are there in each of the TAG, SET and WORD fields?

Module-4

- 7 a. Convert the following pairs of decimal numbers to 5-bit signed 2's complement numbers and add them. State whether or not overflow occurs in each case.
 i) 5 and 10 ii) -14 and 11 iii) -5 and 7 iv) -10 and -13
 b. Design the 16 bit carry look ahead adder using 4-bit adder. Also unite the expression for C_{l+1} .
 c. Draw the two n-bit number x and y to perform addition/subtraction.

OR

- 8 a. With an example explain the Booth's algorithm to multiply two signed operands.
 b. Multiply each of the following pairs of signed 2's complement number using the Booth's algorithm. (A = multiplicand and B = multiplier).
 i) A = 010111 and B = 110110
 ii) A = 110011 and B = 101100
 iii) A = 110101 and B = 011011
 iv) A = 001111 and B = 001111

Module-5

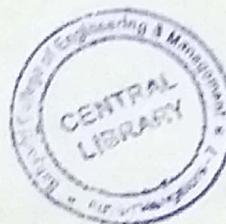
- 9 a. Discuss with neat diagram, the single bus organization of the data path inside a processor.
 b. Write the sequence of control steps required for single bus structure for each of the following instructions.
 i) Add the contents of memory location NUM to register R1.
 ii) Add the contents of memory location whose address is at memory location register R1.

OR

- 10 a. Discuss the microwave oven with neat block diagram.
 b. Discuss the digital camera with neat block diagram.

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CBCS Scheme



15CS34

USN

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Third Semester B.E. Degree Examination, June/July 2017

Computer Organization

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

- 1 a. With a neat block diagram discuss the basic operational concept of a computer. (06 Marks)
b. Explain the methods to improve the performance of computer. (04 Marks)
c. Explain Big-Endian, little Endian and assignment byte addressability. (06 Marks)

OR

- 2 a. What are addressing modes? Explain the different 4 types addressing modes with example. (08 Marks)
b. Write the use of Rotate and shift instruction with example. (04 Marks)
c. What is stack and queue? Write the line of code to implement the same. (04 Marks)

Module-2

- 3 a. Define bus arbitration? Explain detail any one approach of bus arbitration. (08 Marks)
b. What are priority interrupts? Explain any one interrupt priority scheme. (04 Marks)
c. Write a note on register in DMA interface. (04 Marks)

OR

- 4 a. With a block diagram explain how the printer interfaced to processor. (08 Marks)
b. Explain the following with respect to U.S.B
 i) U.S.B Architecture
 ii) U.S.B protocols. (08 Marks)

Module-3

- 5 a. Define :
 i) Memory Latency
 ii) Memory bandwidth
 iii) Hit-rate
 iv) Miss-penalty. (04 Marks)
b. With a neat diagram explain the internal organization of a $2M \times 8$ dynamic memory chip. (06 Marks)
c. Explain Associative mapping technique and set Associative mapping technique. (06 Marks)

OR

- 6 a. What is virtual memory? With a diagram explain how virtual memory address is translated. (08 Marks)
b. Write a note on :
 i) Magnetic tape system
 ii) Flash memory. (08 Marks)

Module-4

- 7 a. Perform following operations on the 5-bit signed numbers using 2's complement representation system. Also indicate whether overflow has occurred.
 i) $(-9) + (-7)$ ii) $(+7) - (-8)$.
- b. Explain with a neat block diagram, 4 bit carry lookahead adder.
- c. Explain the concept of carry save addition for the multiplication operation, $M \times Q = ?$ 4-bit operands with diagram and suitable example.

OR

- 8 a. Multiply the following signed 2's complement numbers using Booth's algorithm
 multiplicand = $(010111)_2$, multiplier = $(110110)_2$.
- b. Perform division operation on the following unsigned numbers using the restoring method
 Dividend = $(10101)_2$ Divisor = $(00100)_2$,
- c. With a neat diagram, explain the floating point addition/subtraction unit.

Module-5

- 9 a. Draw and explain multiple bus organization of CPU. And write the control sequence for instruction Add R4, R5, R6 for the multiple bus organization.
 b. Explain with neat diagram, micro-programmed control method for design of control unit write the micro-routine for the instruction Branch < 0.

OR

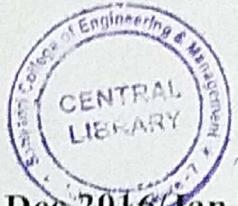
- 10 a. With block diagram, explain the working of microwave oven in an embedded system.
 b. With block diagram, explain parallel I/O interface.

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CBCS Scheme

USN

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15CS34

Third Semester B.E. Degree Examination, Dec 2016/Jan.2017 Computer Organization

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

- 1 a. With a neat diagram, explain basic operational concept of computer. (06 Marks)
b. What is performance measurement? Explain overall SPEC rating for computer. (04 Marks)
c. Draw single bus structure, discuss about memory mapped I/O. (06 Marks)

OR

- 2 a. What is an addressing mode? Explain any three addressing modes with example. (10 Marks)
b. Explain BIG-ENDIAN and LITTLE-ENDIAN methods of byte addressing with proper example. (06 Marks)

Module-2

- 3 a. What is an Interrupt? With example illustrate concept of interrupt. (06 Marks)
b. Define Exception. Explain 2 kinds of exception. (04 Marks)
c. With a neat diagram explain DMA controller. (06 Marks)

OR

- 4 a. Explain PCI bus. (05 Marks)
b. List SCSI bus signal with their functionalities. (05 Marks)
c. Explain the tree structure of USB with split bus operation. (06 Marks)

Module-3

- 5 a. Briefly explain any two mapping function used in cache memory. (08 Marks)
b. With a neat diagram explain the internal organization of memory chip ($2M \times 8$ and dynamic memory chip). (08 Marks)

OR

- 6 a. Explain the following :
i) Hit Rate and Miss penalty ii) Virtual memory organization. (08 Marks)
b. With diagram explain how virtual memory translation take place. (08 Marks)

Module-4

- 7 a. Draw 4-bit carry-look ahead adder and explain. (06 Marks)
b. Perform multiplication for -13 and +09 using Booth's Algorithm. (06 Marks)
c. Design a logic circuit to perform addition/subtraction of 'n' bit number X and Y. (04 Marks)

OR

- 8 a. Explain IEEE standard for floating point number. (06 Marks)
b. With figure explain circuit arrangement for binary division. (10 Marks)

Module-5

- 9 a. With a figure explain single bus organization of datapath inside a processor. (08 Marks)
b. What are the actions required to Execute a complete instruction Add (R3), R₁. (02 Marks)
c. Give the control sequence for execution of instruction ADD (R3), R₁. (06 Marks)

OR

- 10 a. Briefly explain the block diagram of camera. (08 Marks)
b. Explain multiprocessors. Justify how time is reduced. (08 Marks)

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Third Semester B.E. Degree Examination, June/July 2019 Computer Organization

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

- 1 a. Explain the connection between processor and memory with neat diagram and show how to add A + B to form C with the help of the same diagram. (08 Marks)
b. Write short notes on :
(i) Performance equation (ii) SPEC Rating (08 Marks)

OR

- 2 a. What do you mean by addressing mode? Explain different types of addressing modes with example. (10 Marks)
b. Explain shift and rotate instructions with example. (06 Marks)

Module-2

- 3 Write short notes on :
(i) Daisy chain (ii) Subroutine (iii) Interrupt hardware (iv) Exception (16 Marks)

OR

- 4 a. Explain how DMA (with register) is taking place in a system with necessary diagram. (08 Marks)
b. Define Bus arbitration. Discuss different types of Bus Arbitration methods with diagram. (08 Marks)

Module-3

- 5 a. With diagram, describe the internal organization of a 128×8 memory chip. (08 Marks)
b. With the diagram of basic SRAM (Static RAM) and DRAM (Asynchronous DRAM) chip (cell), explain the read and write operations on each of them. (08 Marks)

OR

- 6 a. Describe different types of cache mapping techniques (between memory to cache memory) with diagram. (10 Marks)
b. Calculate the total capacity of a 4.8 inch disk having the following parameters:
(i) 100 data recording surfaces (ii) 100000 tracks per surface (iii) 100 sectors per track
(iv) Each track contains 512 bytes of data. (03 Marks)
c. In a given system (i) hit rate (n) = 0.5 (ii) Miss penalty (M) = 100 ns (iii) Time to access cache memory (c) = 100 ns. Calculate the average access time (t_{ave}) experienced by the processor. (03 Marks)

Module-4

- 7 a. Write down the steps of Booth's multiplication algorithm. (02 Marks)
b. Perform Booth's multiplication between $(+13) \times (-6)$. (08 Marks)
c. Explain generation and propagation functions used in Carry-Look-Ahead Adder. (06 Marks)

OR

- 8 a. Explain Bit-Pair Recording / Fast multiplication with example.
b. Write down the steps of restoring division algorithm. Apply Restoring division algorithm
 $1000/11$.

Module-5

- 9 a. Describe Multiple Bus Organization (with diagram).
b. Write down the control sequence for execution of the instruction Add (R_3), R_1

OR

- 10 a. What do you mean by micro-instruction? Design Basic organization of a microprogram control unit with diagram.
b. Describe a simple microcontroller with diagram. Also mention parallel and serial I/O ports.

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