MODULE-4b. MOSFET

SYLLABUS

MOSFET Two terminal MOS structure- Energy band diagram, Ideal Capacitance – Voltage Characteristics and Frequency Effects, Basic MOSFET Operation- MOSFET structure, Current-Voltage Characteristics. (Text 2: 9.1.1, 9.4, 9.6.1, 9.6.2, 9.7.1, 9.7.2, 9.8.1,9.8.2).

Text Books: 2. Donald A Neamen, Dhrubes Biswas, "Semiconductor Physics and Devices", 4th Edition, MCGraw Hill Education, 2012, ISBN 978-0-07-107010-2.

Contents

1. THE TWO-TERMINAL MOS STRUCTURE

The heart of the MOSFET is the MOS capacitor shown in Figure 10.1. The metal may be aluminum or some other type of metal, although in many cases, it is actually a high-conductivity polycrystalline silicon that has been deposited on the oxide; however, the term metal is usually still used. The parameter t_{ox} in the figure is the thickness of the oxide and $_{ox}$ is the permittivity of the oxide.

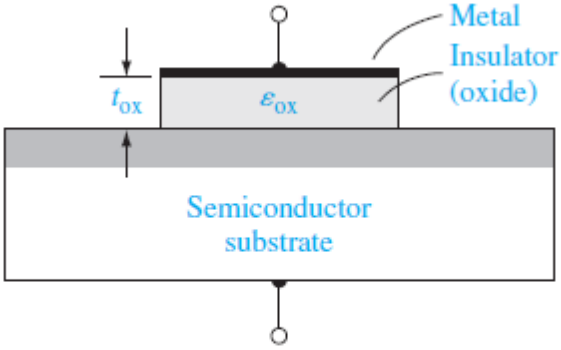


Figure 10.1 | The basic MOS capacitor structure.

1.1. Plate Capacitor Electric Field And Conductor Charges

- Figure 10.2a shows a parallel-plate capacitor with the top plate at a negative voltage with respect to the bottom plate.
- An insulator material separates the two plates. With this bias, a negative charge exists on the top plate, a positive charge exists on the bottom plate, and an electric field is induced between the two plates as shown.
- The capacitance per unit area for this geometry is

$$C' = \frac{\epsilon}{d} \tag{10.1}$$

where ϵ is the permittivity of the insulator and d is the distance between the two plates. The magnitude of the charge per unit area on either plate is

$$Q' = C'V \tag{10.2}$$

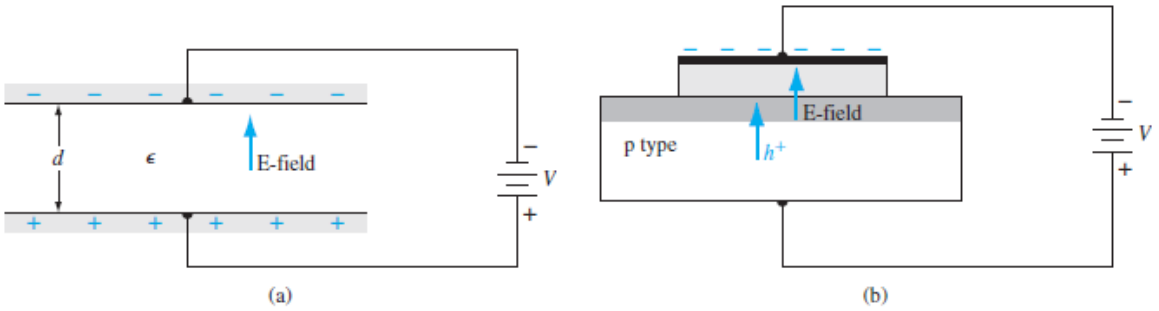


Figure 10.2 | (a) A parallel-plate capacitor showing the electric field and conductor charges. (b) A corresponding MOS capacitor with a negative gate bias showing the electric field and charge flow.

where the prime indicates charge or capacitance per unit area. The magnitude of the electric field is

$$E=\frac{V}{d}$$

- Figure 10.2b shows a MOS capacitor with a p-type semiconductor substrate.
- The top metal gate is at a negative voltage with respect to the semiconductor substrate.
- From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced with the direction shown in the figure.
- If the electric field were to penetrate into the semiconductor, the majority carrier holes would experience a force toward the oxide– semiconductor interface.

2. Modes of operation

- the capacitance value of a capacitor doesn't change with values of voltage applied across its terminals. However, this is not the case with MOS capacitor.
- the capacitance of MOS capacitor changes its value with the variation in Gate voltage. This is because application of gate voltage results in band bending in silicon substrate and hence variation in charge concentration at **Si-SiO2** interface.

2.1. Case 1 Equilibrium (No voltage)

- MOS capacitor is an equilibrium device i.e. when the external voltage is not applied to the device the Fermi level of metal and semiconductor are at same level.

- When external voltage is applied to device it behaves according to the voltage applied with respect to flat band voltage and threshold voltage.
- Flat band voltage is defined as a work function difference between the gate metal and the semiconductor when no charge is present in oxide-semiconductor interface.
- Threshold voltage is defined as the minimum gate-to-source voltage required to induce or create a conducting channel. This can be divided into three types

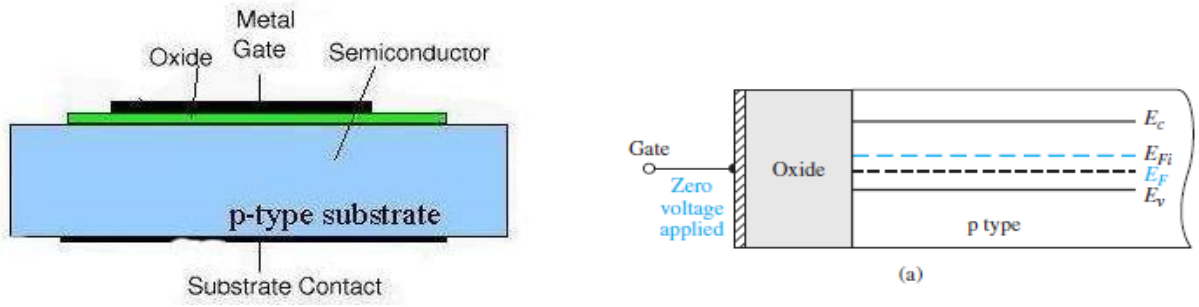


Figure 10.3. The diagram of a MOS capacitor with a p-type substrate for (a) diagram of a MOS capacitor for energy-band a zero applied gate bias showing the *ideal* case,

2.2. Case 2- Accumulation layer: (negative voltage)

- In this case, applied voltage (V_g) is less than flat band voltage. Voltage applied to gate(on metal side) is negative.

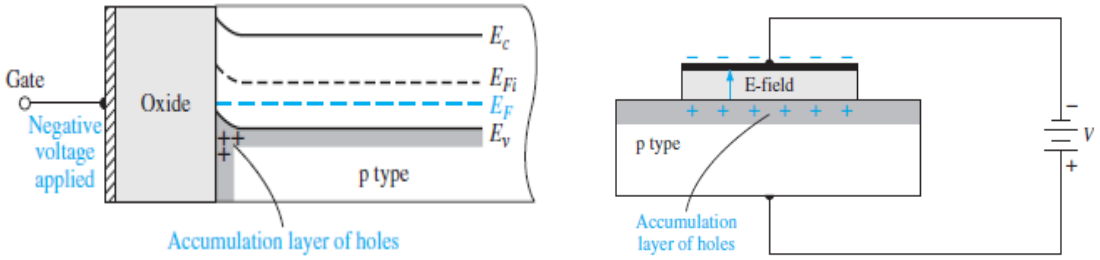


Figure 10.4. The diagram of a The MOS capacitor with an accumulation layer of holes.

Where

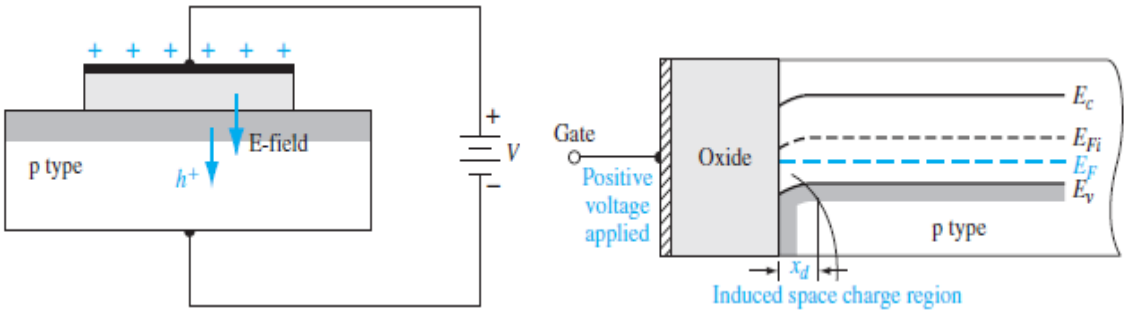
E_C= conduction band energy level
E_F= Fermi energy level
E_V= valance band energy level
E_i = intrinsic energy level
Q = charge of electron

V_g=voltage applied on gate

- When voltage is applied, MOSFET no longer remain in equilibrium condition. The Fermi energy level of metal changes by charge of electron multiplied by applied voltage. Voltage applied is negative and hence rise in Fermi level of metal takes place while Fermi level of semiconductor remain constant
- Voltage applied to the gate is negative hence negative charge develops near metal-oxide junction thus positively charged hole travel towards the oxide junction thus creating positive charge near the oxide-semiconductor junction.
- Due to accumulation of positive charge, surface voltage is developed near oxide-semiconductor junction due to this energy band bending takes place and the value is charge of electron multiplied by surface voltage.
- Energy band bending is changes in energy offset (level) of semiconductor's band structure near junction due to space charge.

2.3. Case 3- Depletion layer: (small positive voltage)

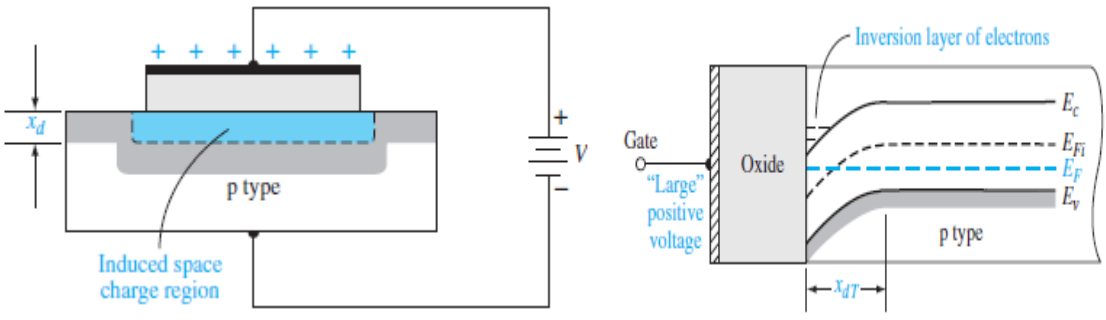
- In depletion region, voltage applied to gate is greater than flat band voltage and less than threshold voltage.



- In this case, voltage applied to gate is positive hence there is fall in Fermi energy level of metal while rise in Fermi energy level of semiconductor.
- Since voltage applied to positive and hence positive charge develops near metal-oxide junction thus the electrons travel towards the gate creating negative charge near oxide-semiconductor junction.
- Electrons recombine with holes present near oxide creating depletion region.
- Surface voltage develops in depletion region and effect of this we have energy band bending in depletion region.

2.4. Case 4 - Inversion layer: (Large Positive Charge)

- In inversion layer, applied voltage is greater than threshold voltage.
- The reason it is called as inversion layer as the surface is inverted from p-type to n-type near the junction.
- Voltage applied is very high hence Fermi level of metal goes down further
- Since voltage applied is positive to gate, electrons travel towards the gate and accumulates near semiconductor-oxide junction resulting development of surface potential. Due to surface potential energy band bending takes place.
- From the diagram p type substrate near semiconductor-oxide junction has intrinsic energy level below Fermi energy level and this part of substrate behave as n-type semiconductor and part above the Fermi level behave as p-type semiconductor. This happen due to concentration of electrons exceeds concentration of holes near semiconductor-oxide junction and the event is called as **surface inversion**.
- N-type semiconductor acts as a channel for current and current can flow through this channel on application of positive drain-source voltage.



- Accumulation
  - $V_G > V_{FB}$
  - Electrons accumulate at surface
- Depletion
  - $V_G < V_{FB}$
  - Electrons repelled from surface
- Inversion
  - $V_G < V_T$
  - Surface becomes p-type

(this diagram just for understanding purpose)

3. Ideal *C–V* Characteristics

- the ideal *C–V* characteristics of the MOS capacitor and then discuss some of the deviations that occur from these idealized results.
- there is zero charge trapped in the oxide and also that there is no charge trapped at the oxide–semiconductor interface.

3.1. Case 1 accumulation layer (negative voltage)

- Figure 10.23a shows the energy-band diagram of a MOS capacitor with a p-type substrate for the case when a negative voltage is applied to the gate, inducing an accumulation layer of holes in the semiconductor at the oxide–semiconductor interface.
- A small differential change in voltage across the MOS structure will cause a differential change in charge on the metal gate and also in the hole accumulation charge, as shown in Figure 10.23b.
- The differential changes in charge density occur at the edges of the oxide, as in a parallel-plate capacitor.

$$C'(\text{acc}) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \qquad (10.35)$$

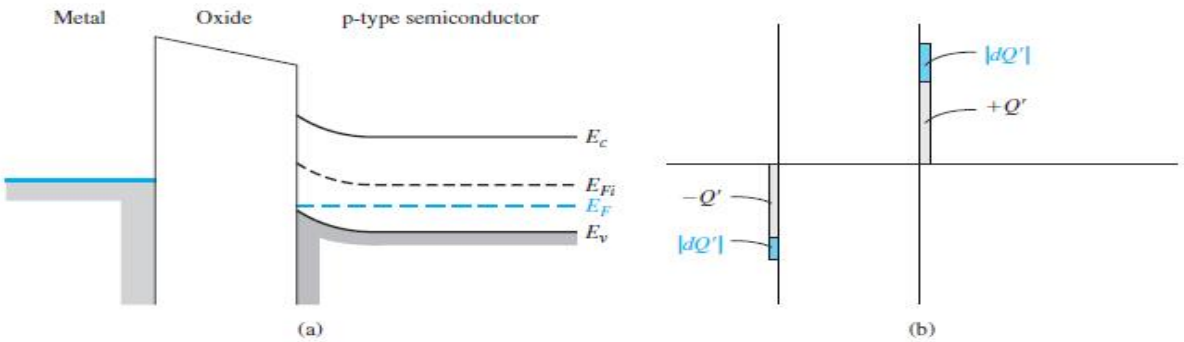


Figure 10.23 | (a) Energy-band diagram through a MOS capacitor for the accumulation mode. (b) Differential charge distribution at accumulation for a differential change in gate voltage.

Figure 10.23 | (a) Energy-band diagram through a MOS capacitor for the accumulation mode. (b) Differential charge distribution at accumulation for a differential change in gate voltage.

3.2. Case 2 depletion region (small positive voltage)

- Figure 10.24a shows the energy-band diagram of the MOS device when a small positive voltage is applied to the gate, inducing a space charge region in the semiconductor;
- Figure 10.24b shows the charge distribution through the device for this condition. The oxide capacitance and the capacitance of the depletion region are in series.
- A small differential change in voltage across the capacitor will cause a differential change in the space charge width. The corresponding differential changes in charge densities are shown in the figure.
- The total capacitance of the series combination is

$$\frac{1}{C'(\text{depl})} = \frac{1}{C_{ox}} + \frac{1}{C'_{SD}} \tag{10.36a}$$

or

$$C'(\text{depl}) = \frac{C_{ox}C'_{SD}}{C_{ox} + C'_{SD}} \tag{10.36b}$$

Since $C_{ox} = \epsilon_{ox}/t_{ox}$ and $C'_{SD} = \epsilon_s/x_d$, Equation (10.36b) can be written as

$$C'(\text{depl}) = \frac{C_{ox}}{1 + \dfrac{C_{ox}}{C'_{SD}}} = \frac{\epsilon_{ox}}{t_{ox} + \left(\dfrac{\epsilon_{ox}}{\epsilon_s}\right)x_d} \tag{10.37}$$

As the space charge width increases, the total capacitance $C'(\text{depl})$ decreases.

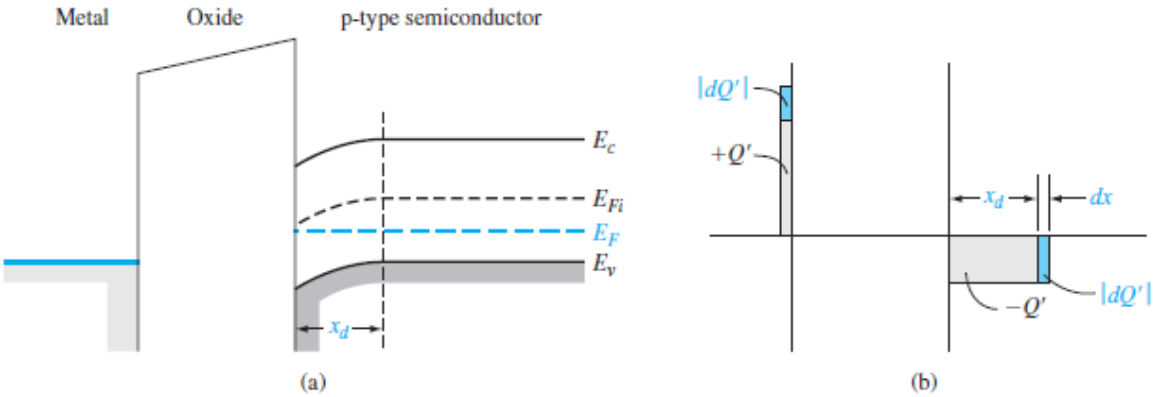


Figure 10.24 | (a) Energy-band diagram through a MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gate voltage.

3.3. Case 3: inversion layer (Large Positive Charge)

- Figure 10.25a shows the energy-band diagram of this MOS device for the inversion condition.
- In the ideal case, a small incremental change in the voltage across the MOS capacitor will cause a differential change in the inversion layer charge density. The space charge width does not change.
- If the inversion charge can respond to the change in capacitor voltage as indicated in Figure 10.25b, then the capacitance is again just the oxide capacitance,

$$C'_{\text{min}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}} + \left(\frac{\epsilon_{\text{ox}}}{\epsilon_s}\right) x_{dT}} \qquad (10.38)$$

$$C'(\text{inv}) = C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} \qquad (10.39)$$

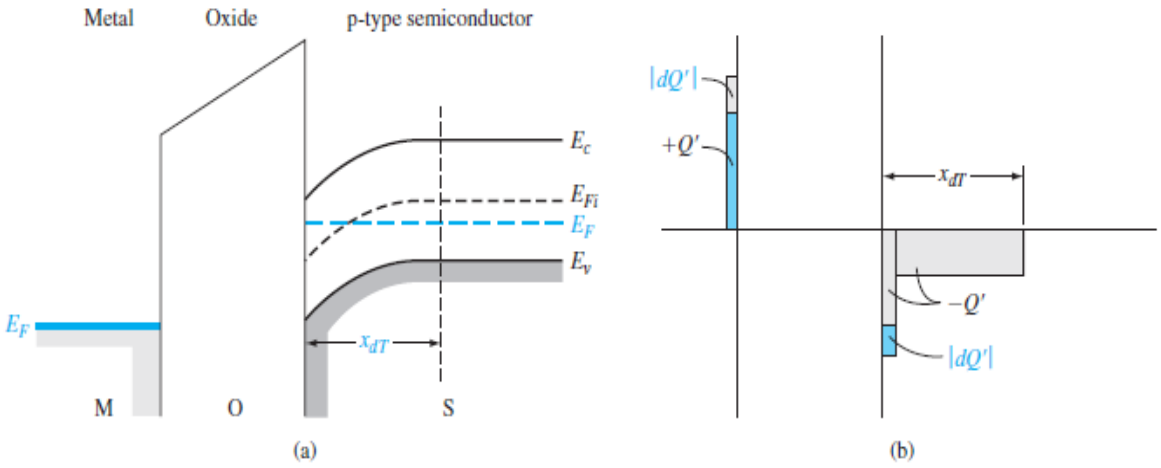


Figure 10.25 | (a) Energy-band diagram through a MOS capacitor for the inversion mode. (b) Differential charge distribution at inversion for a low-frequency differential change in gate voltage.

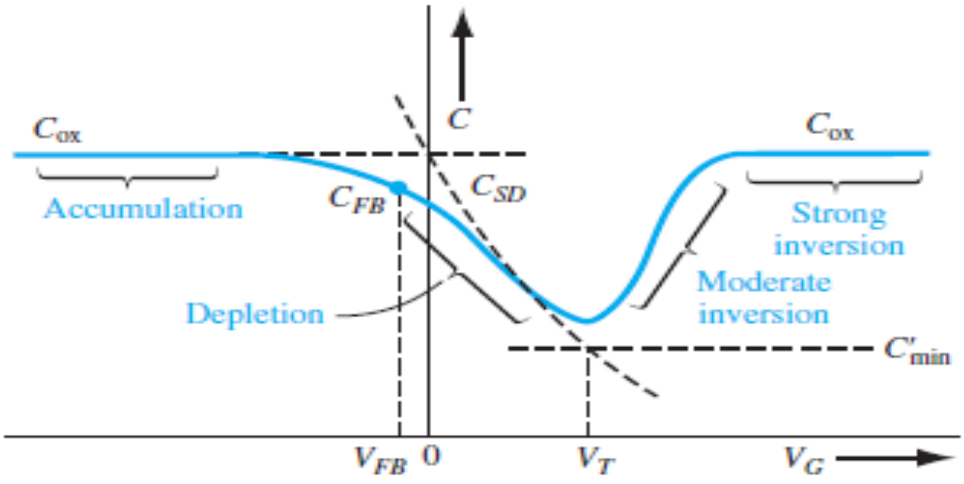
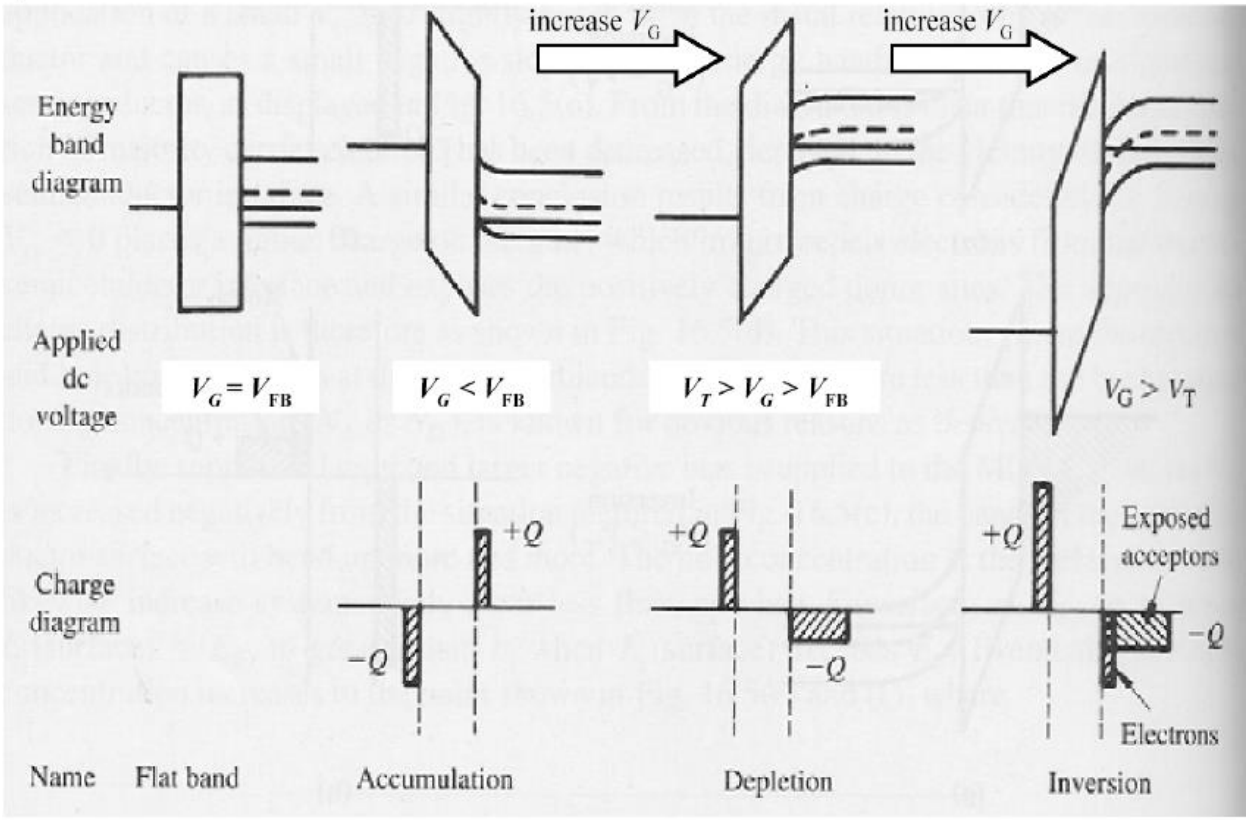


Figure 10.26 | Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate. Individual capacitance components are also shown.

- Figure 10.26 shows the ideal capacitance versus gate voltage, or *C–V*, characteristics of the MOS capacitor with a p-type substrate.
- The three dashed segments correspond to the three components C_{ox}, C_{SD} and C_{min}. The solid curve is the ideal net capacitance of the MOS capacitor.
- Moderate inversion, which is indicated in the figure, is the transition region between the point when only the space charge density changes with gate voltage and when only the inversion charge density changes with gate voltage.
- The point on the curve that corresponds to the **flat-band** condition is of interest. The flat-band condition occurs between the accumulation and depletion conditions.
- The capacitance at flat band is given by

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\left(\frac{kT}{e}\right)\left(\frac{\epsilon_s}{eN_a}\right)}} \qquad (10.40)$$



(this is just for understanding purpose)

Objective: Calculate C_{ox}, C'_{min}, and C'_{FB} for a MOS capacitor.

Consider a p-type silicon substrate at $T = 300$ K doped to $N_a = 10^{16}$ cm^{-3}.

The oxide is silicon dioxide with a thickness of $t_{ox} = 18$ nm $= 180$ Å, and the gate is aluminum.

■ **Solution**

The oxide capacitance is

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{180 \times 10^{-8}} = 1.9175 \times 10^{-7}\ \text{F/cm}^2$$

To find the minimum capacitance, we need to calculate

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259) \ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.3473\ \text{V}$$

and

$$x_{dT} = \left\{\frac{4\epsilon_s \phi_{fp}}{eN_a}\right\}^{1/2} = \left\{\frac{4(11.7)(8.85 \times 10^{-14})(0.3473)}{(1.6 \times 10^{-19})(10^{16})}\right\}^{1/2}$$

$$\cong 0.30 \times 10^{-4} \text{ cm}$$

Then

$$C'_{\min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)x_{dT}} = \frac{(3.9)(8.85 \times 10^{-14})}{180 \times 10^{-8} + \left(\frac{3.9}{11.7}\right)(0.30 \times 10^{-4})}$$

$$= 2.925 \times 10^{-8} \text{ F/cm}^2$$

We may note that

$$\frac{C'_{\min}}{C_{ox}} = \frac{2.925 \times 10^{-8}}{1.9175 \times 10^{-7}} = 0.1525$$

The flat-band capacitance is

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\frac{V_t \epsilon_s}{eN_a}}}$$

$$= \frac{(3.9)(8.85 \times 10^{-14})}{180 \times 10^{-8} + \left(\frac{3.9}{11.7}\right)\sqrt{\frac{(0.0259)(11.7)(8.85 \times 10^{-14})}{(1.6 \times 10^{-19})(10^{16})}}}$$

$$= 1.091 \times 10^{-7} \text{ F/cm}^2$$

We also note that

$$\frac{C'_{FB}}{C_{ox}} = \frac{1.091 \times 10^{-7}}{1.9175 \times 10^{-7}} = 0.569$$

4. C-V Characteristics Frequency Effects

The low frequency and high frequency C-V characteristics curves of a MOS capacitor are shown in fig 10.29

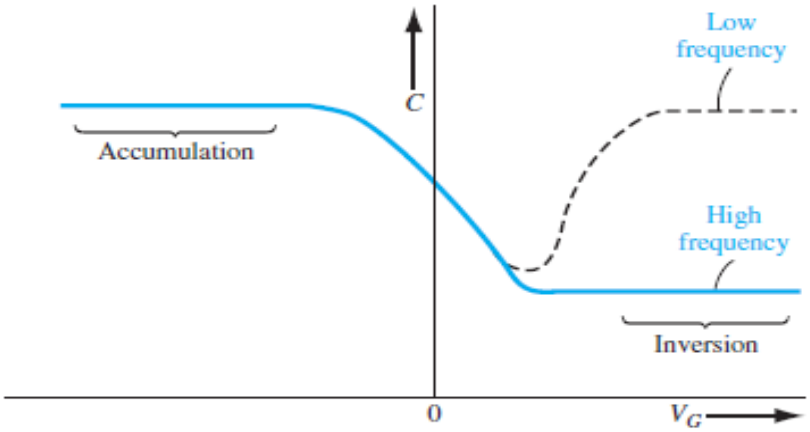


Figure 10.29 | Low-frequency and high-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate.

- The **low frequency** or quasi-static measurement maintains thermal equilibrium at all times. This capacitance is the ratio of the change in charge to the change in gate voltage, measured while the capacitor is in equilibrium. A typical measurement is performed with an electrometer, which measures the charge added per unit time as one slowly varies the applied gate voltage. low frequency corresponds to values in the range of **5 to 100 Hz.**
- The **high frequency** capacitance is obtained from a small-signal capacitance measurement at high frequency. The bias voltage on the gate is varied slowly to obtain the capacitance versus voltage. Under such conditions, one finds that the charge in the inversion layer does not change from the equilibrium value corresponding to the applied DC voltage. The high frequency capacitance therefore reflects only the charge variation in the depletion layer and the (rather small) movement of the inversion layer charge. high frequency corresponds to a value on the order of **1 MHz**
- The high-frequency and low-frequency limits of the C–V characteristics are shown in Figure 10.29.

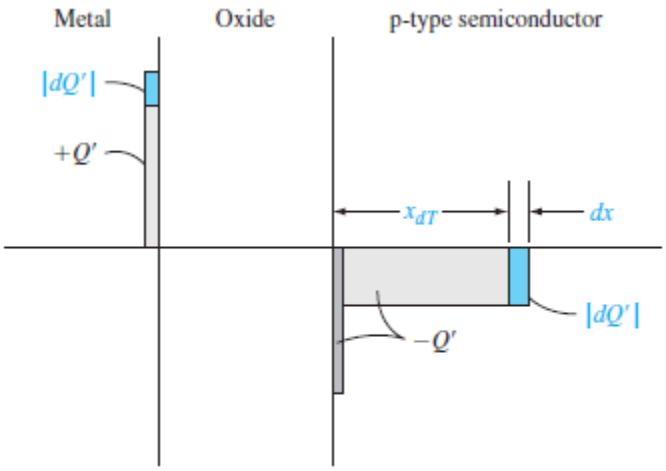


Figure 10.28 | Differential charge distribution at inversion for a high-frequency differential change in gate voltage.