4.8 IC553 Timer

The component parts are as follows:

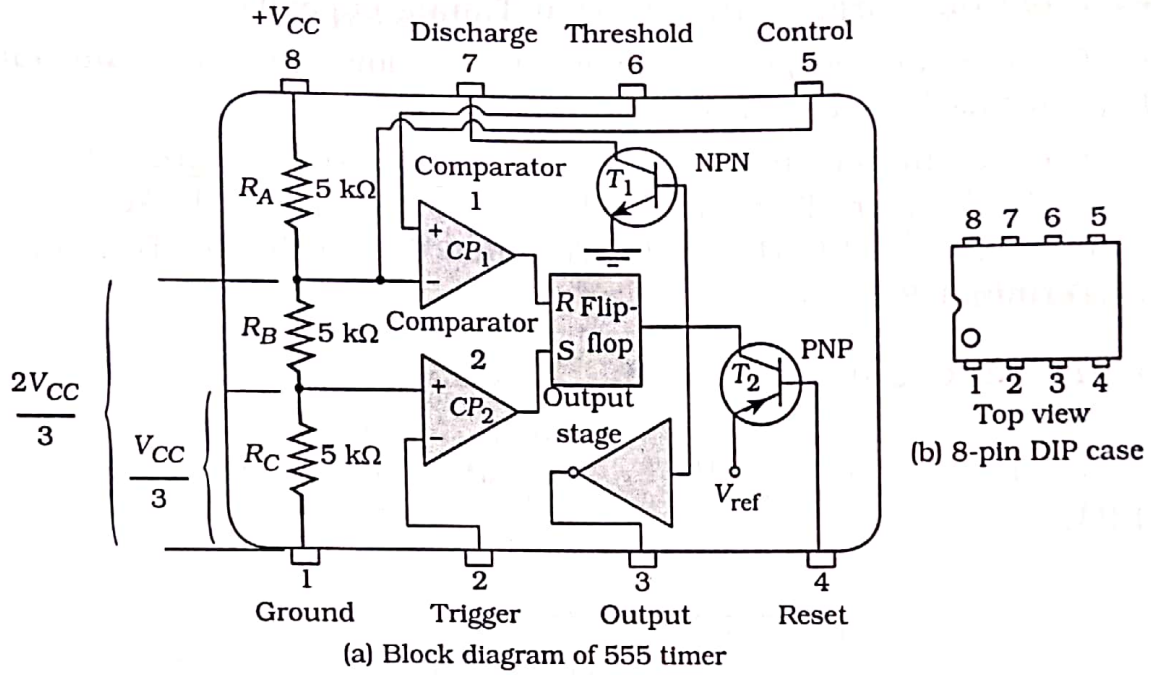

Fig. 4.23(a): Block diagram of 555 timer

a) Voltage comparator 1 (CP_1)

b) Voltage comparator 2 (CP_2)

c) RS Flip Flop

d) Output stage

e) Transistor T_1

f) Transistor T_2

The Supply voltage V_{CC} is given to one end of the voltage divider at terminal 8, while the other end is grounded at Terminal 1.

Voltage comparators compare the voltages at their inverting and non-inverting inputs. The resistive voltage divider is used to set the voltage comparator levels. All three resistors are of equal value; therefore, the upper comparator has a reference of $\frac{2}{3}V_{CC}$, and the lower comparator has a reference of $\frac{1}{3}V_{CC}$. When the trigger voltage goes below $\frac{1}{3}V_{CC}$, the flop-flop sets and the flop flop jumps to its high level. The threshold input is normally connected to an external RC timing circuit. When the external capacitor voltage exceeds $\frac{2}{3}V_{CC}$, the upper comparator resets the flip-flop,

which in turn switches the output back to its low level. When the device output is low, the discharge transistor T_1 is turned on and provides a path for the rapid discharge of the external Timing capacitor.

The flip - flop output is applied to the low-impedance output stage, which performs like a voltage follower.

The different terminals of the Timer 555 are designated as *Ground* (Terminal 1), *Trigger* (Terminal - 2), *Output* (Terminal 3), *Reset* (Terminal 4), *control* (Terminal 5), *Threshold* (Terminal 6), *Discharge* (Terminal 7) and + V_{CC} (Terminal 8).

4.8.1 Astable Oscillator using IC 555

A 555 Timer connected to operate in the **astable** mode as a free - running Relaxation Oscillator (**Astable Multivibrator**) is shown in Fig. 4.24.

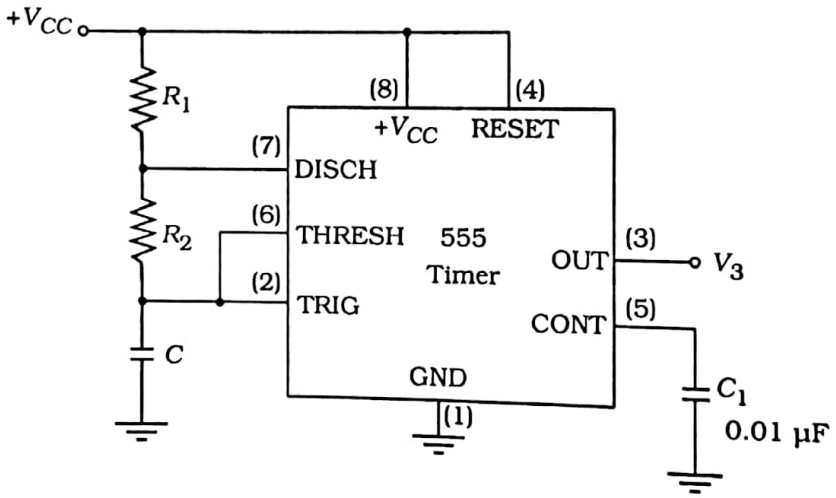

Fig: 4.24: 555 Timer connected as an Astable Multivibrator

It may be pointed out that the threshold input (THRESH) is now connected to the trigger input (TRIG). The external components R_1, R_2 and C form the timing circuit that sets the frequency of oscillation. The 0.01 μF capacitor connected to control (CONT) is for decoupling and does not affect the operation of the device.

Initially, capacitor C is uncharged, so the trigger voltage (pin 2) is at 0V, causing the output of the lower comparator to be high and the output of the upper comparator to be low, forcing the output of the flip-flop, and so the base of transistor T_1 low and keeping the transistor off.

Next, when the power is switched ON, the capacitor C begins to change from the dc source + V_{CC} through R_1 and R_2. When the capacitor

voltage reaches $\frac{1}{3}V_{CC}$, the lower comparator switches to its low output state, and when the capacitor voltage reaches $\frac{2}{3}V_{CC}$, the upper comparator switches to its high output state. This resets the flip-flop, causing the base of T_1 to go high, and turns ON the transistor. Now, a discharge path is created for the capacitor through R_2 and the transistor. At the point where the capacitor discharges down to $\frac{1}{3}V_{CC}$, the lower comparator switches HIGH, setting the flip-flop, which makes the base of the transistor T_1 (Discharge transistor) LOW and turns OFF the transistor. Another charging cycle begins and the process is repeated. The result is a rectangular wave whose duty cycle depends on the values of R_1 and R_2.

The capacitor charging through $(R_1 + R_2)$ is shown by the exponential curve AB and its discharging through R_2 is shown by the exponential curve BC, as shown in R_2 is shown by the exponential curve BC, as shown in Fig. 4.25. Also shown is the output waveform.

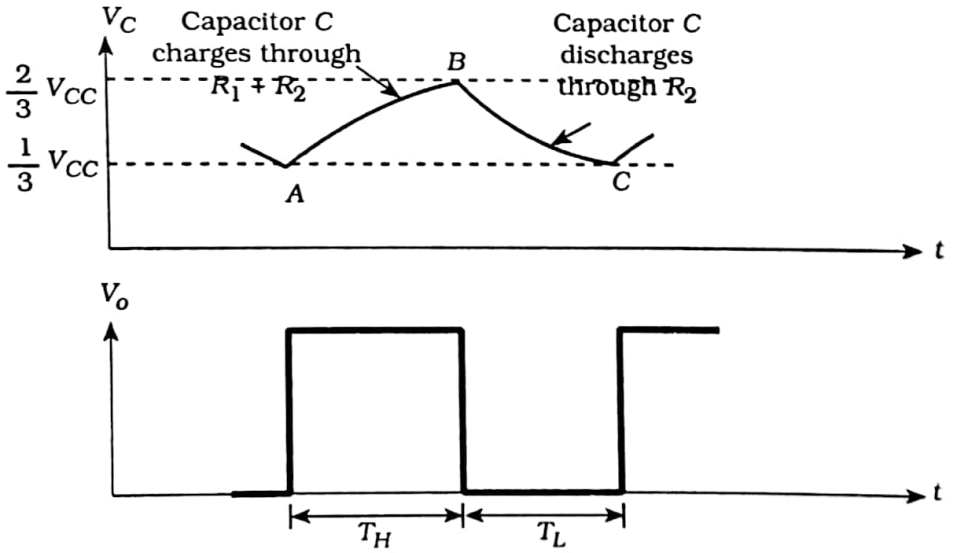

Fig. 4.25: Capacitor Charging and Discharging Cycle and Output Waveform

The frequency of oscillation is given by the following equation.

$$f = \frac{1.44}{(R_1 + 2R_2)C} \qquad \text{...(4.23)}$$

A formula to calculate the duty cycle is developed as follows. The time that the output is high (T_H) is how long it takes C to charge from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$. It is expressed as

$$t_H = 0.694\ (R_1 + R_2)\ C \qquad \ldots(4.$$

The time that the output is low (T_L) is how long it takes C to discha from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$. It is expressed as

$$t_L = 0.694\ R_2\ C \qquad \ldots(4.$$

The period T of the output waveform (which is the reciprocal o given in eqn (4.23), is given by

$$\therefore\ T = t_H + T_L = 0.694\ (R_1 + 2R_2)\ C$$

The percent duty cycle is

$$\text{Duty cycle} = \left(\frac{T_H}{T}\right)100\% = \left(\frac{T_H}{T_H + T_L}\right)100\%$$

$$\textbf{Duty Cycle} = \left(\frac{\mathbf{R_1 + R_2}}{\mathbf{R_1 + 2R_2}}\right)\mathbf{100\%}$$

4.9 Review Questions

1. Explain the basic transistor amplifier with a circuit diagram a waveforms.
2. Explain, with the help of neat sketches how a BJT can be used as switch.
3. With the help of a neat circuit diagram show how a transistor can b used to switch ON/OFF an LED in a power circuit using a relay.
4. a) List out the advantages of a Negative Feedback Amplifier.
   b) Write a note on the stabilisation of voltage gain of a series - volta negative feedback amplifier.
5. Draw a diagram to show the principle of series voltage negative feedba & briefly explain. Also list the major effects of negative feedback on a amplifier.
6. Derive an equation for the input impedance of an amplifier that use voltage negative feedback.
7. Derive an equation for the output impedance of an amplifier that use series voltage negative feedback.
8. With the help of diagrams, explain the effect of negative feedback on th bandwidth of an amplifier.
9. With the help of diagrams explain the phenomenon of harmonic distortio