A Report on

Designing a CMOS OP-AMP

By

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Submitted in partial fulfillment of the course

EEE F313/ INSTR F313 - Analog and Digital VLSI Design

Under the guidance of

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Acknowledgement

We would like to express our sincere gratitude towards Dr. Anu Gupta, Prof. Karri Babu Ravi Teja and the entire ADVD faculty along with the EEE department for their constant guidance and support in the project work.

We are also thankful to our batchmates and TAs for their help with software related issues and helping us understand the various steps, protocols and how to proceed with our project.

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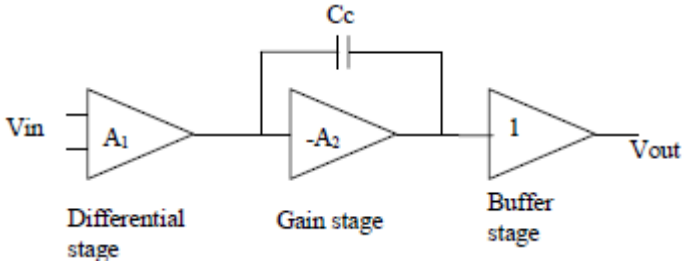
Problem Statement

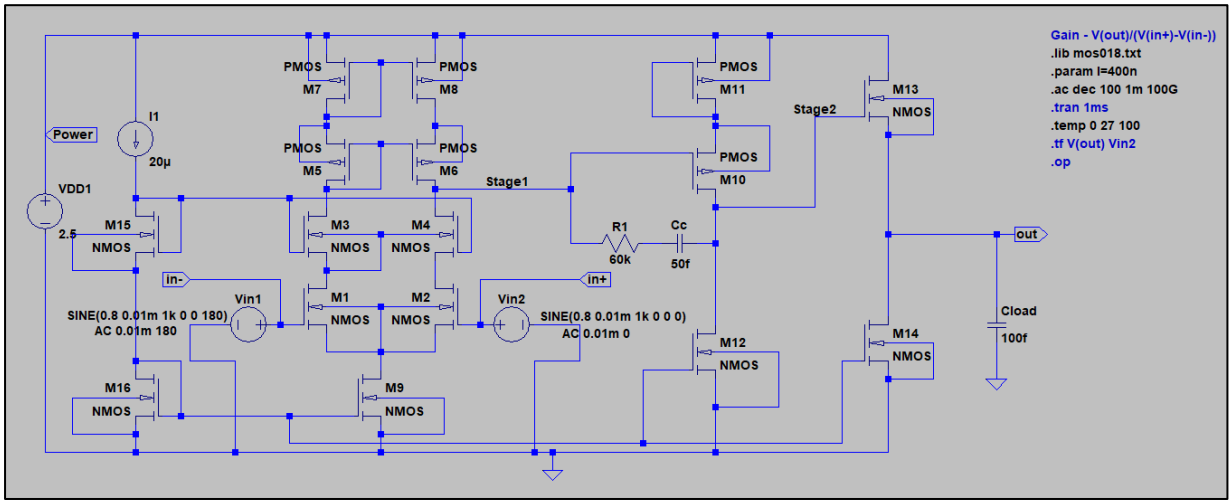
Design a CMOS OPAMP.



a) Analog schematic of the model shown alongside.
b) Analysis of all the equations of your design, with systematic derivations of all transistor W/L ratios and spectre simulations of circuit for the following simulations.
   i. Gain >= 100 dB
   ii. Setting time <= 20 ns
   iii. UGB >= 200 MHz
   iv. Slew Rate <= 20 V/µs
c) STB analysis to calculate the closed loop gain and phase margin for the OPAMP.
d) Calculate and plot the following parameters for your OPAMP: DC Gain, Bode Plot for AC Gain and Phase, CMRR plot, ICMR plot, slew rate, settling time, output voltage swing (dc + transient), power consumption, and input and output offset voltage.

1. CHOOSING THE SCHEMATIC:

The schematic was designed based on the specifications provided in the question.

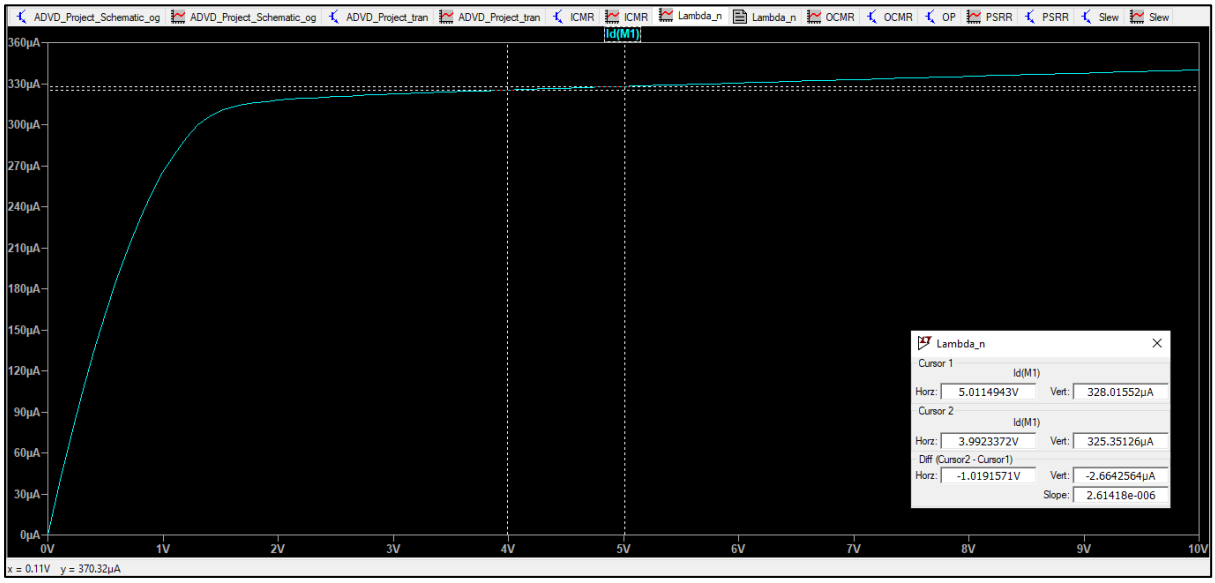


As shown in the schematic below, the first stage is the Differential stage, the second stage is the Gain stage, and the 3rd stage is a Buffer.

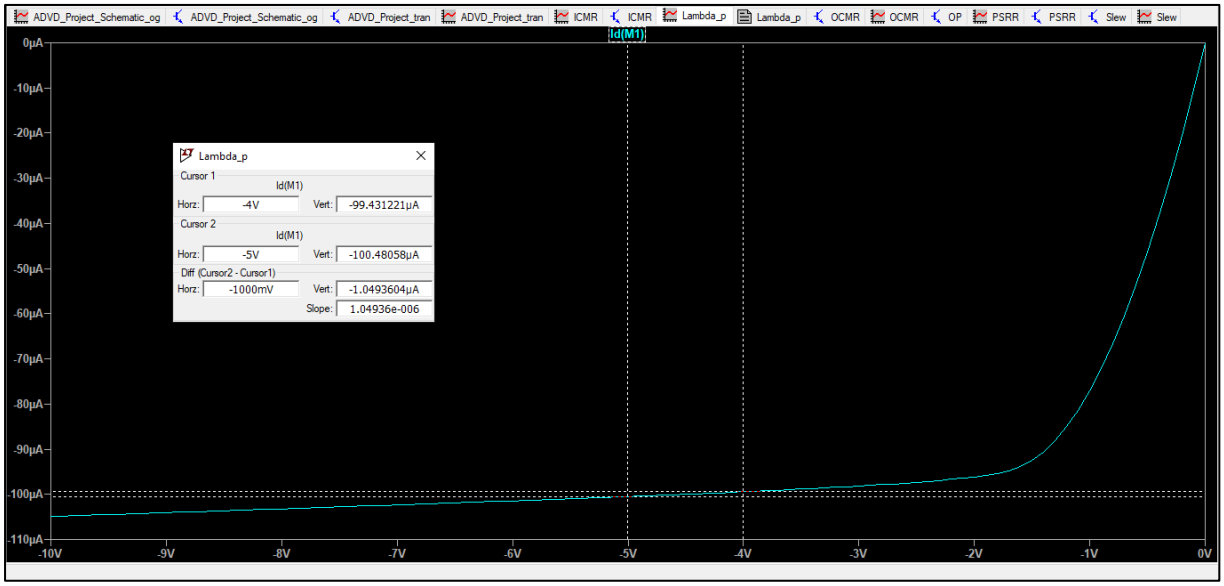
2. CALCULATIONS:

Determining the channel length modulation parameters for NMOS and PMOS models given to us.

NMOS



PMOS



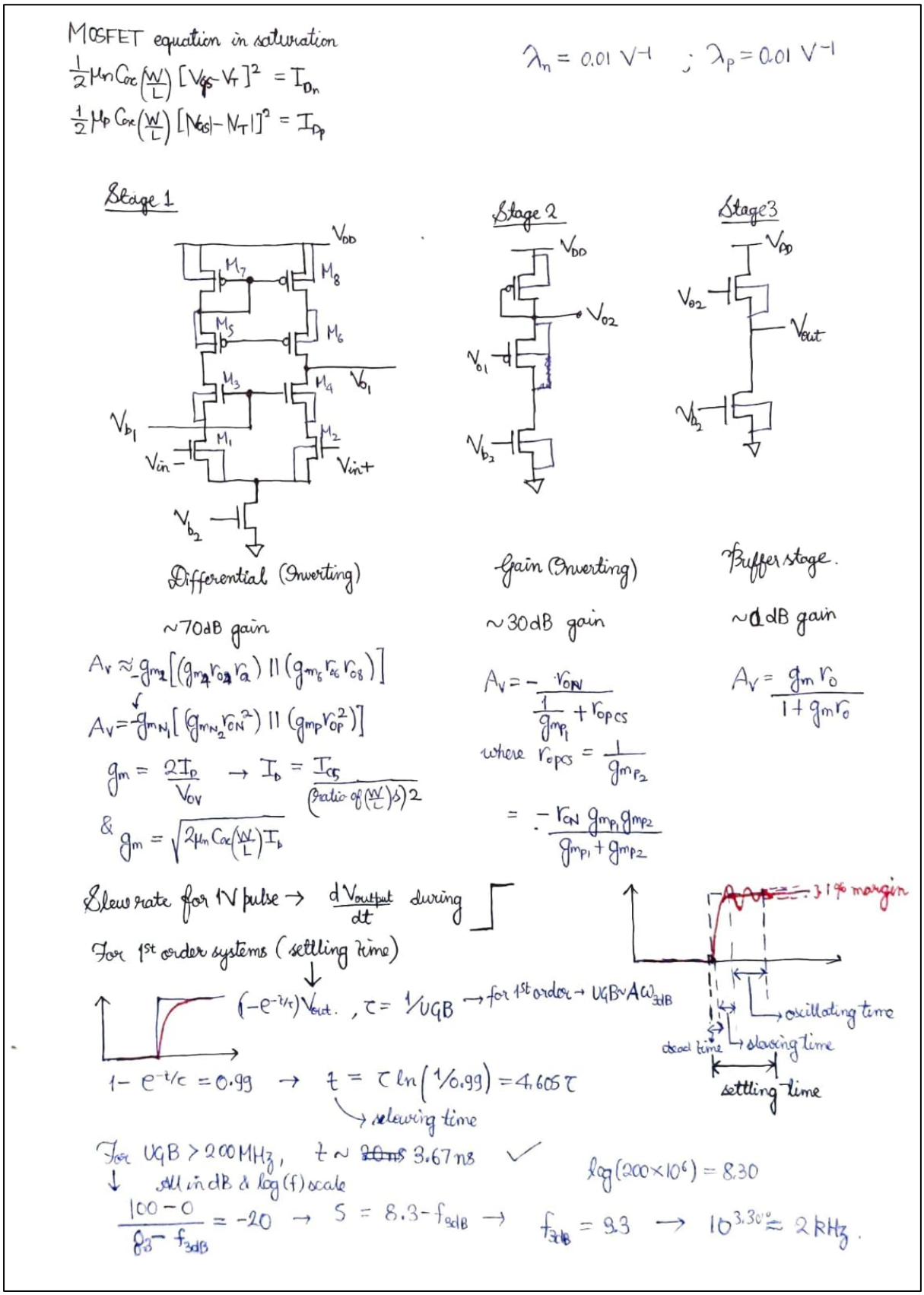
Value for λ was calculated by plotting I_d vs V_{ds} plot for a particular V_{gs}

$$\lambda = \frac{\text{slope}}{\text{constant current value}}$$

$\boldsymbol{\lambda_{pmos} = 0.01\ V^{-1}}$

$\boldsymbol{\lambda_{nmos} = 0.01\ V^{-1}}$

Rough visualisation of how the approximate calculations should be carried out:



3. RESULTS (all at 27°C):

3.1. Gain and Phase Plot:

Observed Values:

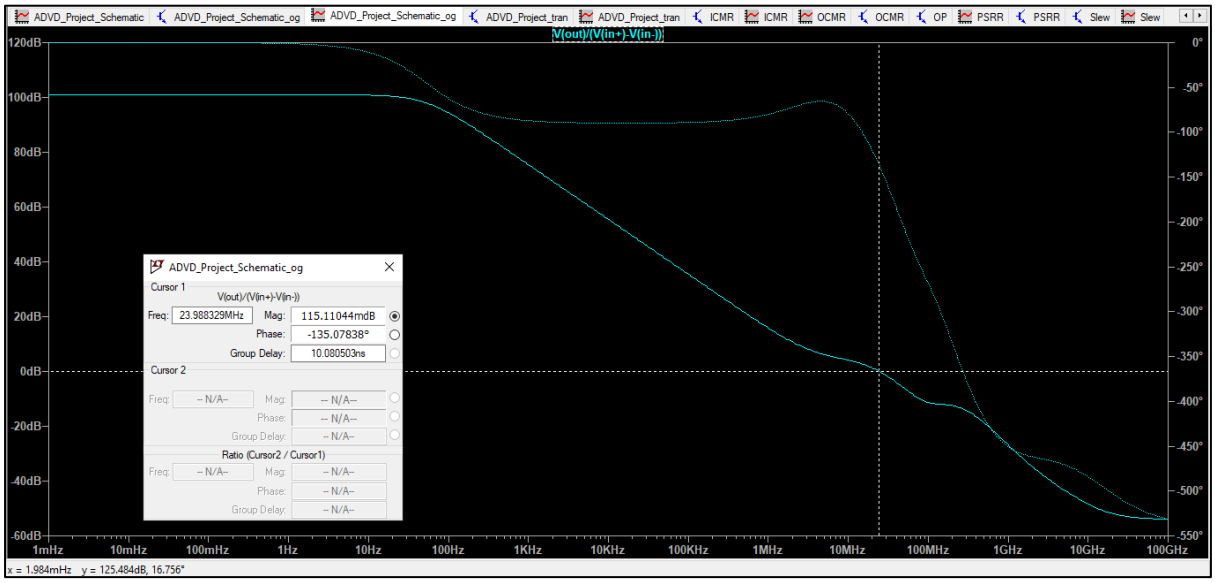
Gain = 102.09 dB

Gain Margin = 5.155 dB

Phase Margin = 52.35°

UGB = 213.79 MHz

3dB frequency = 701.57 Hz



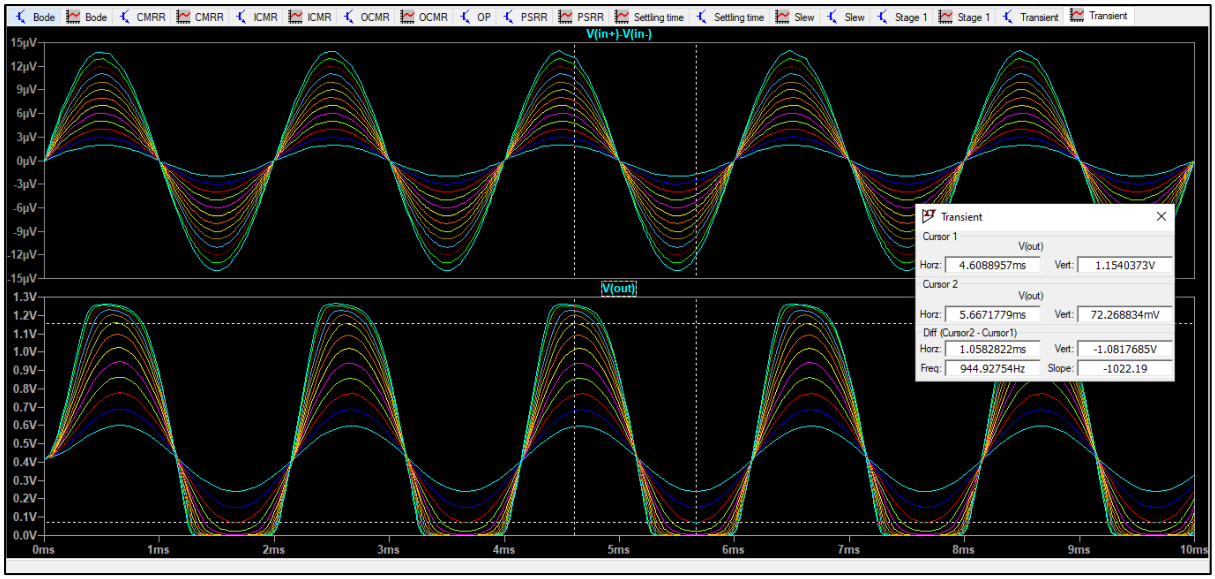
3.2. Output Voltage Swing:

Observed Values:

V_{max} = 1.154 V

V_{min} = 41.29 mV

Swing = $V_{max} - V_{min}$ = 1.154 – 0.072 V = **1.082 V**



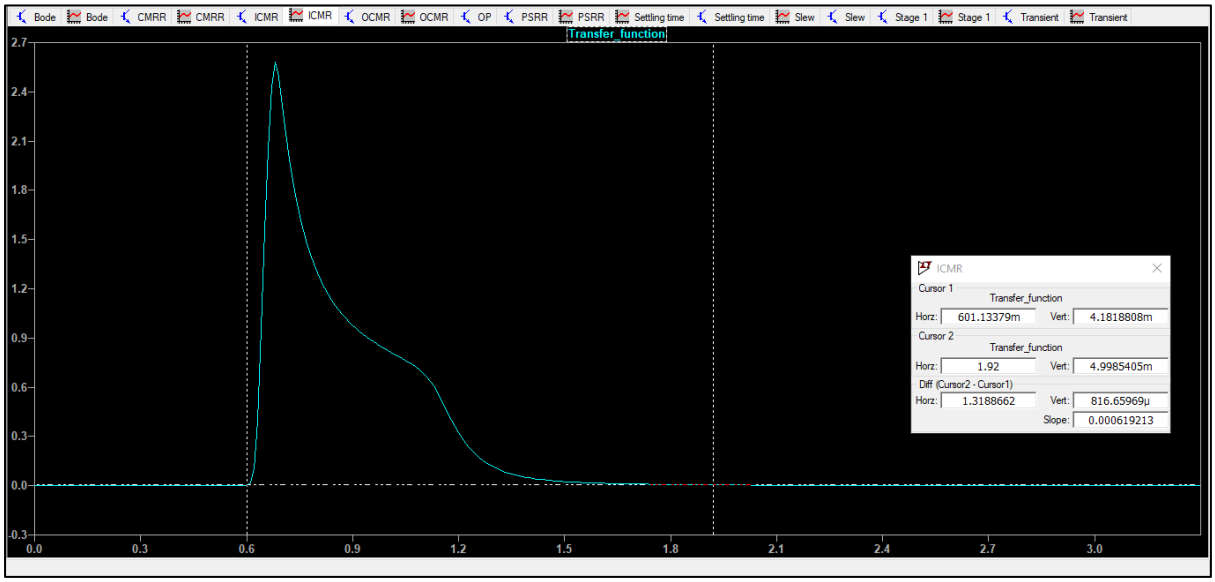
3.3. ICMR:

Observed Values:

$V_{in,min}$ = 601.13 mV

$V_{in,max}$ = 1.92 V

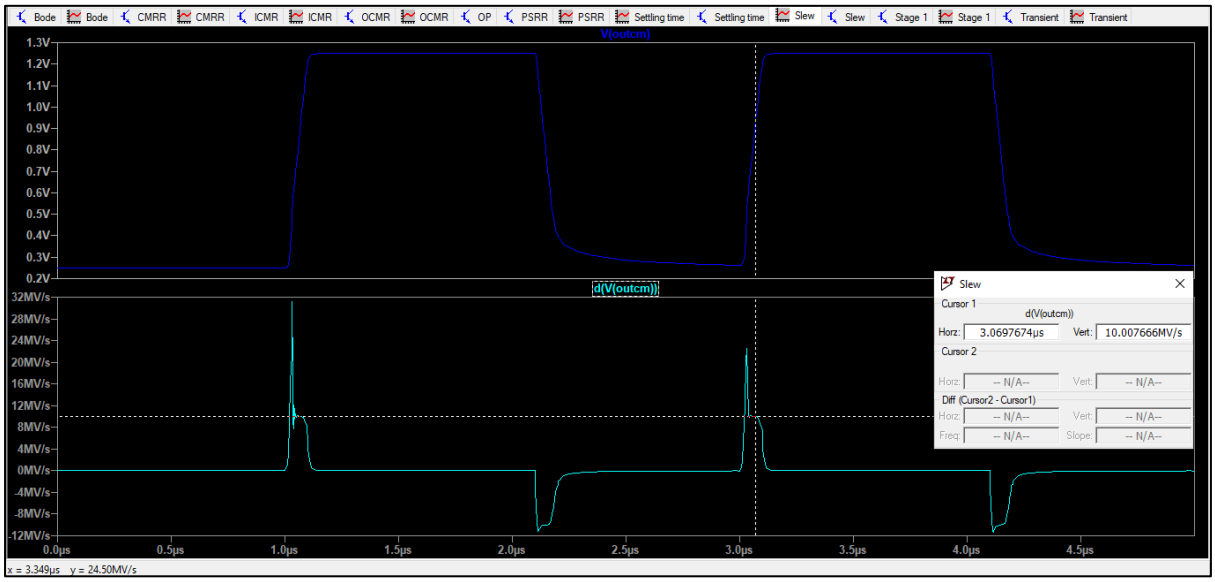
ICMR = $V_{in,max} - V_{in,min}$ = 1.92 V – 0.601 V = **1.89 V**



3.4. Slew Rate:

Observed Values: (for a 1V unit step pulse)

Slope = 10 V/µsec



3.5. Settling Time:

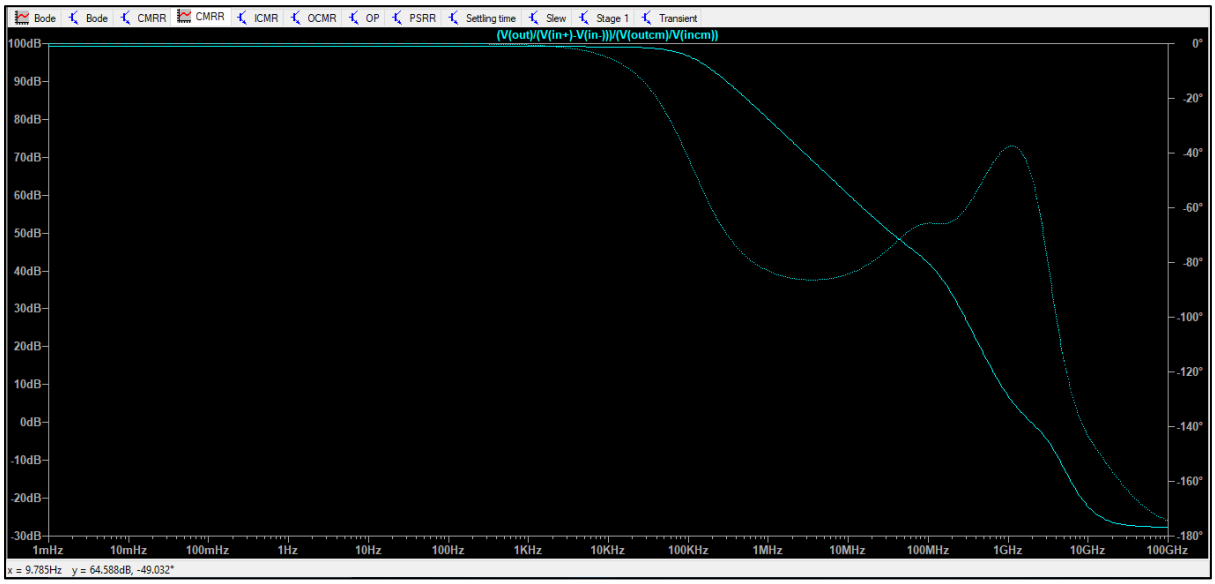
Observed Value (1mV small signal used for settling time measurement):

Settling Time = 12.135 ns

3.6. CMRR Plot:

Observed Value:

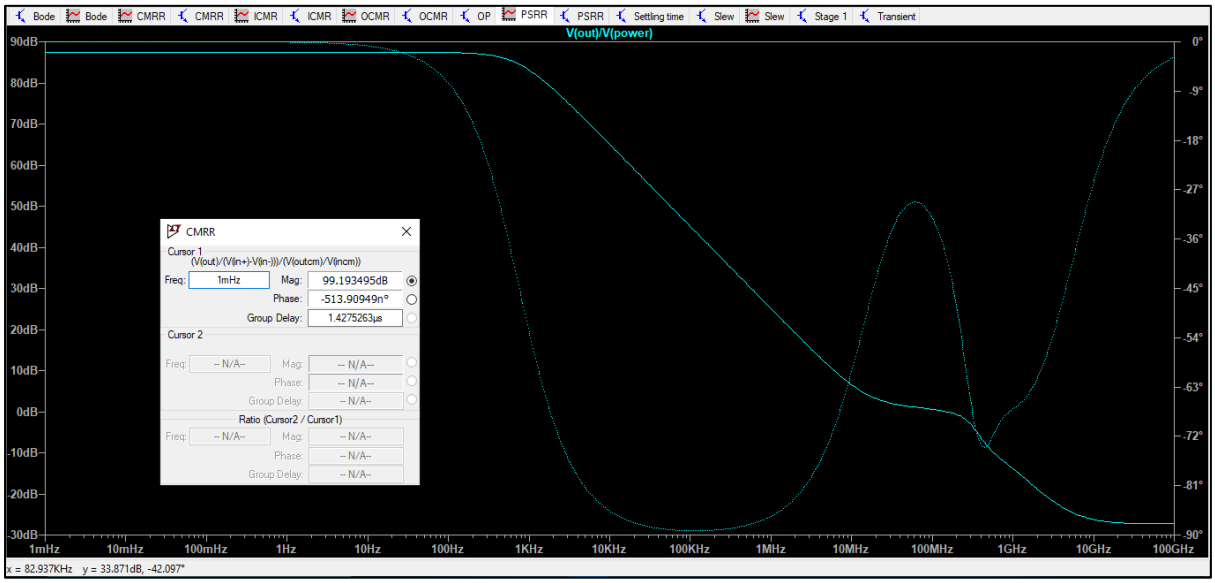
CMRR = 99.19 dB



3.7. PSRR Plot:

Observed Value:

PSRR = 87.464 dB



3.8. Operating Point:

Power Consumption(total) $= V_{DD} \times I(V_{DD})$

$= 2.5 \times 9.3631 \times 10^{-5}$ W

Power Consumption(total) = 0.2409 mW

```
--- Operating Point ---
V(power):       2.5             voltage
V(stage2):      0.855464        voltage
V(out):         0.307116        voltage
V(n006):        0.520373        voltage
V(n007):        0.672094        voltage
V(in-):         0.8             voltage
V(n010):        0.256584        voltage
V(n009):        0.672092        voltage
V(in+):         0.8             voltage
V(n001):        1.95881         voltage
V(n003):        1.95881         voltage
V(n005):        1.21214         voltage
V(stage1):      1.36744         voltage
V(n004):        1.36763         voltage
V(n008):        1.36744         voltage
V(n002):        1.96551         voltage
Id(M16):        -1.24487e-005   device_current
Ig(M16):        -0              device_current
Ib(M16):        1.12005e-011    device_current
Is(M16):        1.24487e-005    device_current
Id(M15):        -1.24487e-005   device_current
Ig(M15):        -0              device_current
Ib(M15):        1.36122e-011    device_current
Is(M15):        1.24487e-005    device_current
Id(M14):        -2.00872e-006   device_current
Ig(M14):        -0              device_current
Ib(M14):        6.01177e-013    device_current
Is(M14):        2.00872e-006    device_current
```

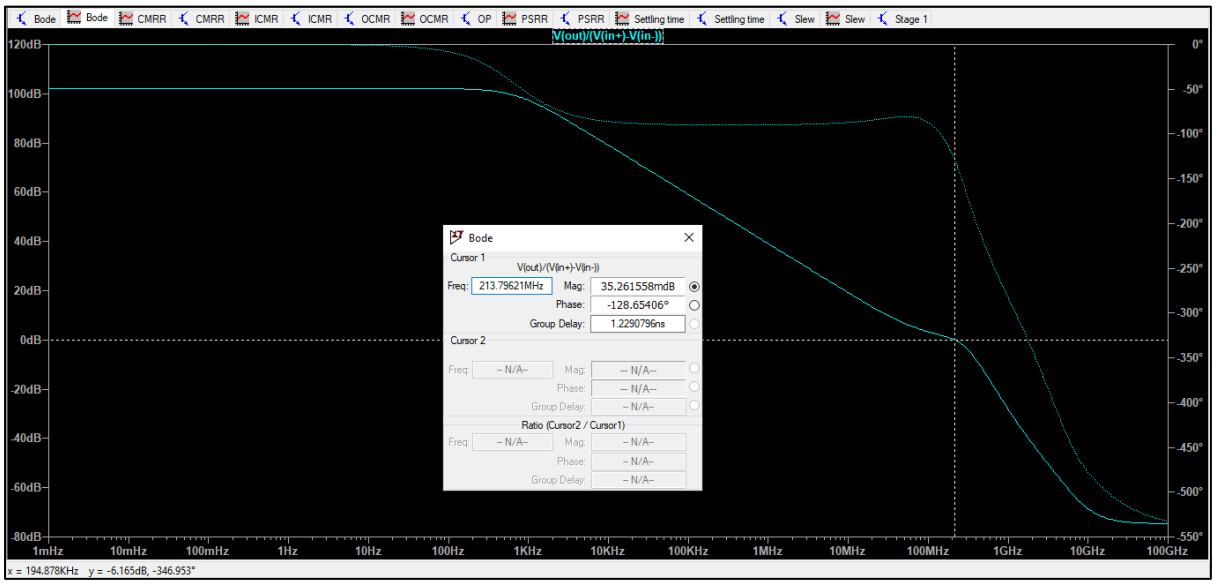
```
Id(M13):        -2.00872e-006 device_current
Ig(M13):        -0            device_current
Ib(M13):        6.01362e-013  device_current
Is(M13):        2.00872e-006  device_current
Id(M6):         -2.00872e-006 device_current
Ig(M6):         -0            device_current
Ib(M6):         1.10239e-012  device_current
Is(M6):         2.00872e-006  device_current
Id(M5):         -2.00872e-006 device_current
Ig(M5):         -0            device_current
Ib(M5):         1.10238e-012  device_current
Is(M5):         2.00872e-006  device_current
Id(M12):        2e-005        device_current
Ig(M12):        0             device_current
Ib(M12):        -7.01766e-013 device_current
Is(M12):        -2e-005       device_current
Id(M11):        1.24487e-005  device_current
Ig(M11):        0             device_current
Ib(M11):        -4.32732e-012 device_current
Is(M11):        -1.24487e-005 device_current
Id(M10):        2.00872e-006  device_current
Ig(M10):        0             device_current
Ib(M10):        -7.05538e-013 device_current
Is(M10):        -2.00872e-006 device_current
Id(M9):         2.00872e-006  device_current
Ig(M9):         0             device_current
Ib(M9):         -7.05348e-013 device_current
Is(M9):         -2.00872e-006 device_current
Id(M8):         2e-005        device_current
Ig(M8):         0             device_current
Ib(M8):         -5.30373e-013 device_current
Is(M8):         -2e-005       device_current
Id(M7):         4.01743e-006  device_current
Ig(M7):         0             device_current
Ib(M7):         -2.66584e-013 device_current
Is(M7):         -4.01743e-006 device_current
Id(M4):         2.00872e-006  device_current
Ig(M4):         0             device_current
Ib(M4):         -4.25508e-013 device_current
Is(M4):         -2.00872e-006 device_current
Id(M3):         2.00872e-006  device_current
Ig(M3):         0             device_current
Ib(M3):         -4.25509e-013 device_current
Is(M3):         -2.00872e-006 device_current
Id(M2):         5.71649e-005  device_current
Ig(M2):         0             device_current
Ib(M2):         -9.51347e-013 device_current
Is(M2):         -5.71649e-005 device_current
Id(M1):         5.71649e-005  device_current
Ig(M1):         0             device_current
Ib(M1):         -4.40577e-011 device_current
Is(M1):         -5.71649e-005 device_current
I(C2):          3.07116e-026  device_current
I(C1):          -2.5599e-026  device_current
I(I1):          2e-005        device_current
I(R1):          0             device_current
I(Vin2):        0             device_current
I(Vin1):        0             device_current
I(Vdd1):        -9.36311e-005 device_current
```

Output Offset Voltage (Operating point) = **0.2436 V**
Input Offset Voltage (Operating point) = **0.8 V > 0.26+0.36 V{ = V_{gs} -V_T; to ensure operation in saturation}**

3.9. Stability Analysis:

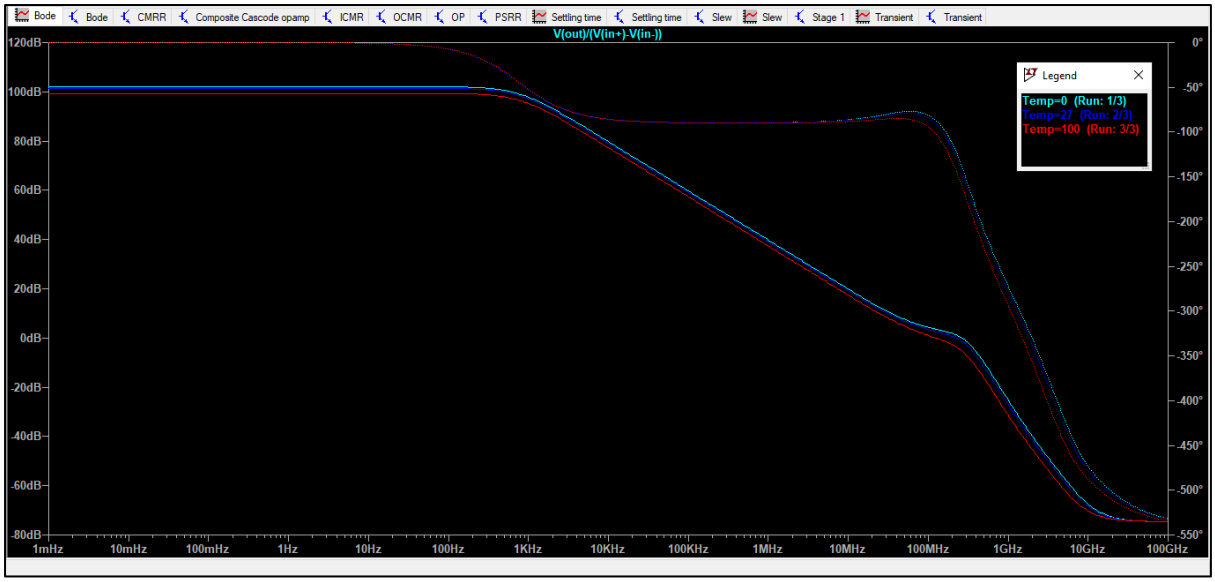
Observed Values:
Gain = 102.09 dB
Gain Margin = 5.155 dB
Phase Margin = 52.35^O
UGB = 213.79 MHz
3dB frequency = 701.57 Hz

The designed system is stable because the Phase Margin is high (greater than 45^O) and so is the Gain Margin.



4. ANALYSIS AT DIFFERENT TEMPERATURES (0 and 100º C):

4.1. Bode Plots:



Temperature 0ºC – DC gain – 102.75 dB
Temperature 100ºC – DC gain – 100.14 dB

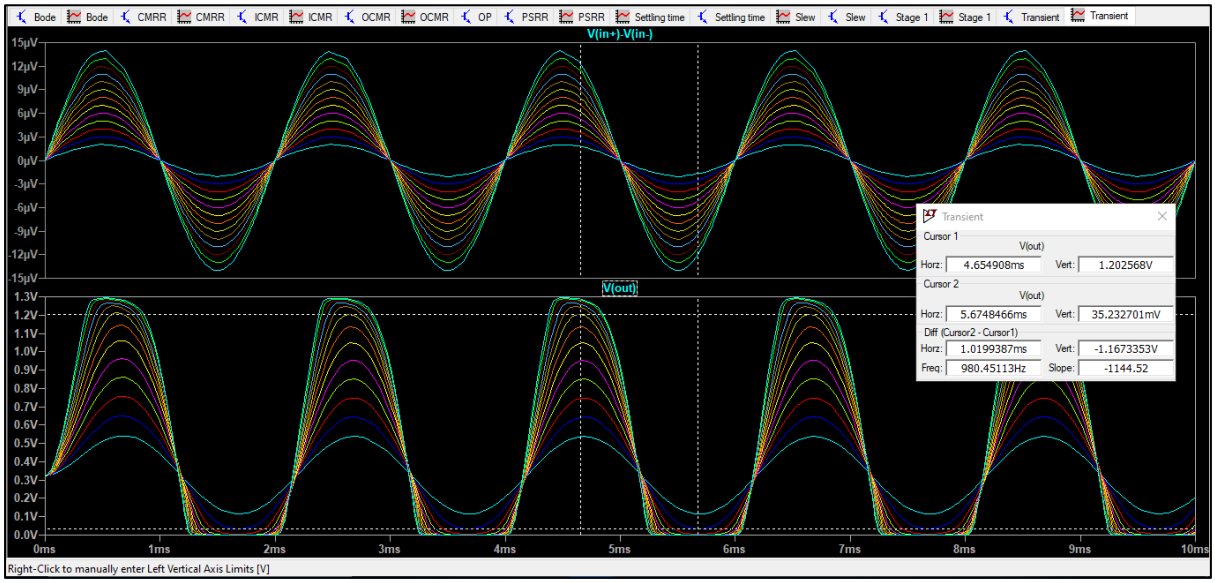
4.2. Output Swing:

Temperature – 0° C

V_{max} = 1.202 V

V_{min} = 35.23 mV

Swing = $V_{max} - V_{min}$ = 1.202 – 0.035 V = **1.166 V**

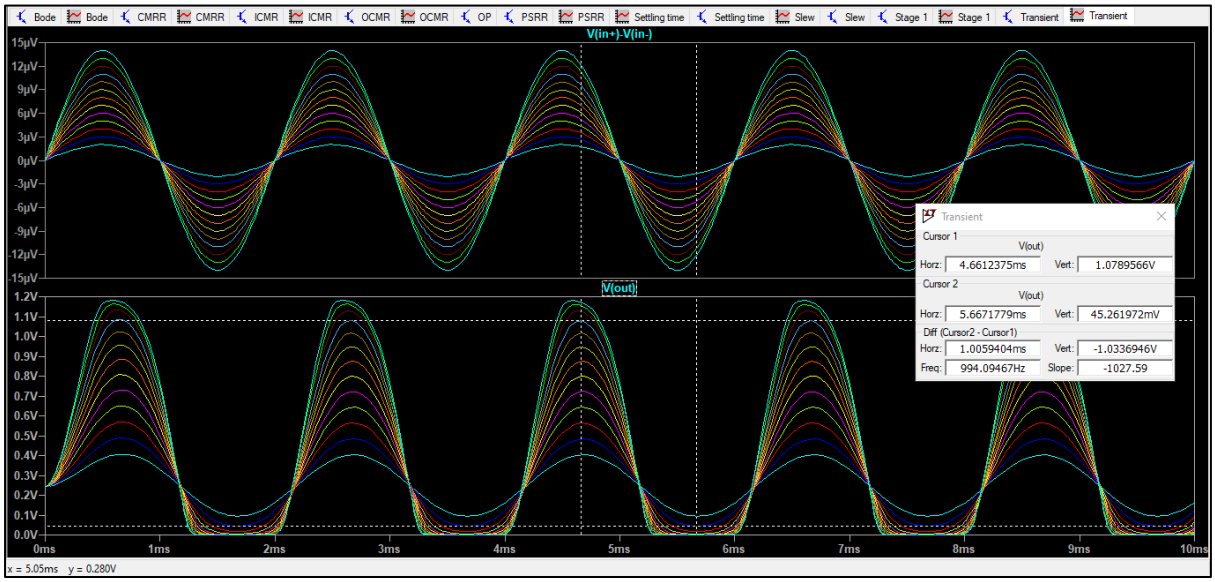


Temperature – 100° C

V_{max} = 1.079 V

V_{min} = 45.26 mV

Swing = $V_{max} - V_{min}$ = 1.079 – 0.045 V = **1.034 V**



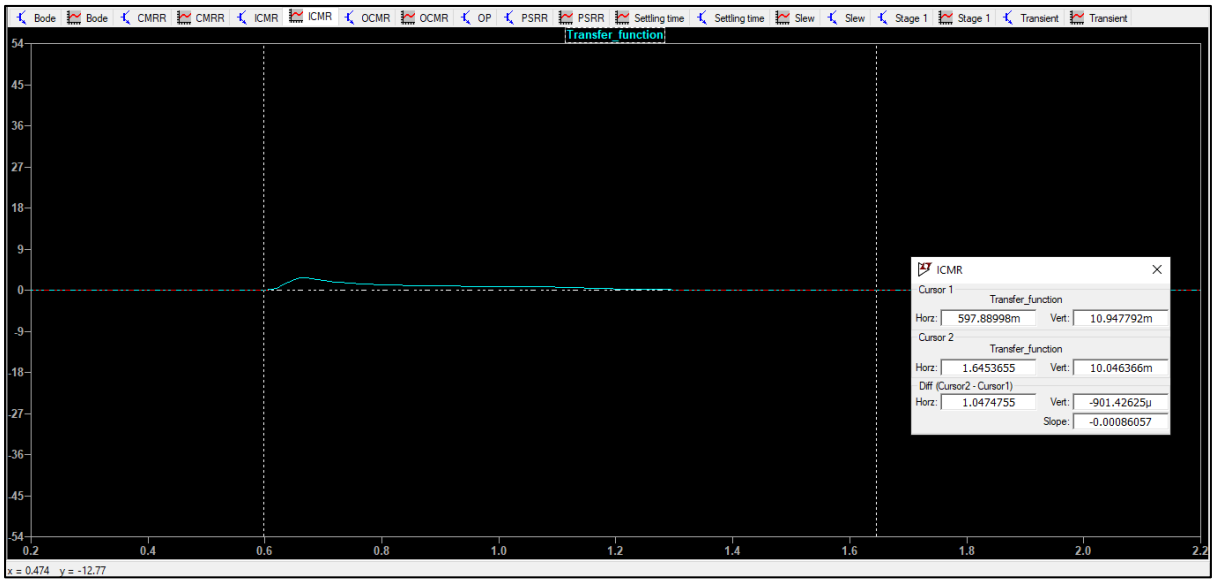
4.3. ICMR

Temperature – 0º Celsius

$V_{in,min}$ = 597.89 mV

$V_{in,max}$ = 1.645 V

ICMR = $V_{in,max} - V_{in,min}$ = 1.645 V – 0.597 V = **1.047 V**

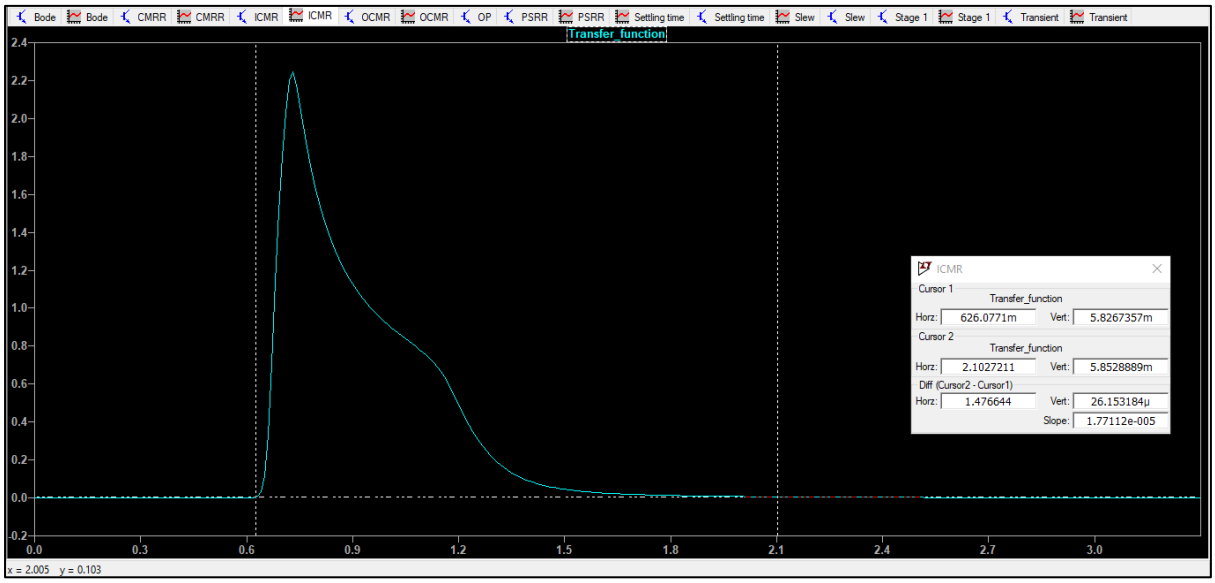


Temperature – 100º Celsius

$V_{in,min}$ = 626.07 mV

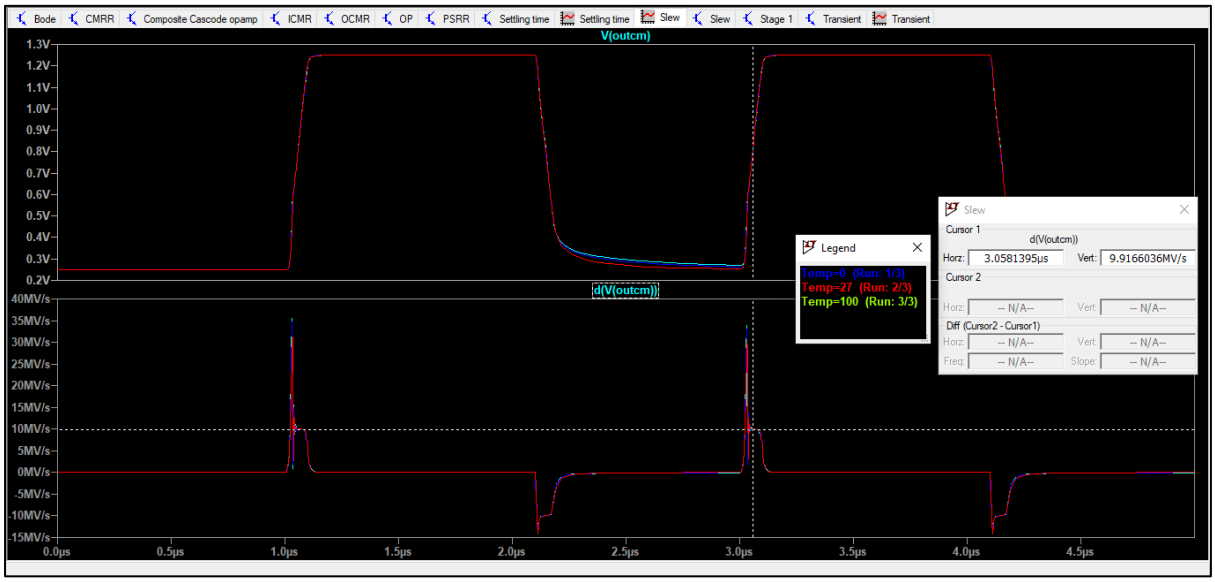
$V_{in,max}$ = 2.102 V

ICMR = $V_{in,max} - V_{in,min}$ = 2.102 V – 0.626 V = **1.476V**



4.4. Slew Rate:

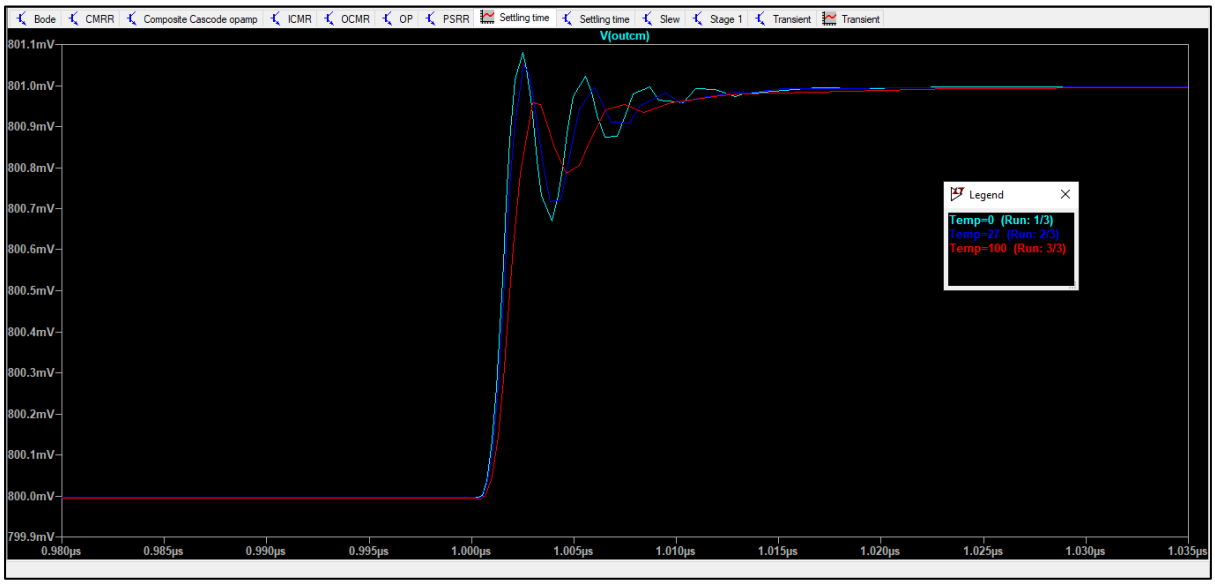
The Slew Rates for both positive and negative pulse for all Temperatures (0, 27 and 100 ºC)



4.5. Settling Time

Temperature 0º C - **Settling Time = 8.704 ns**

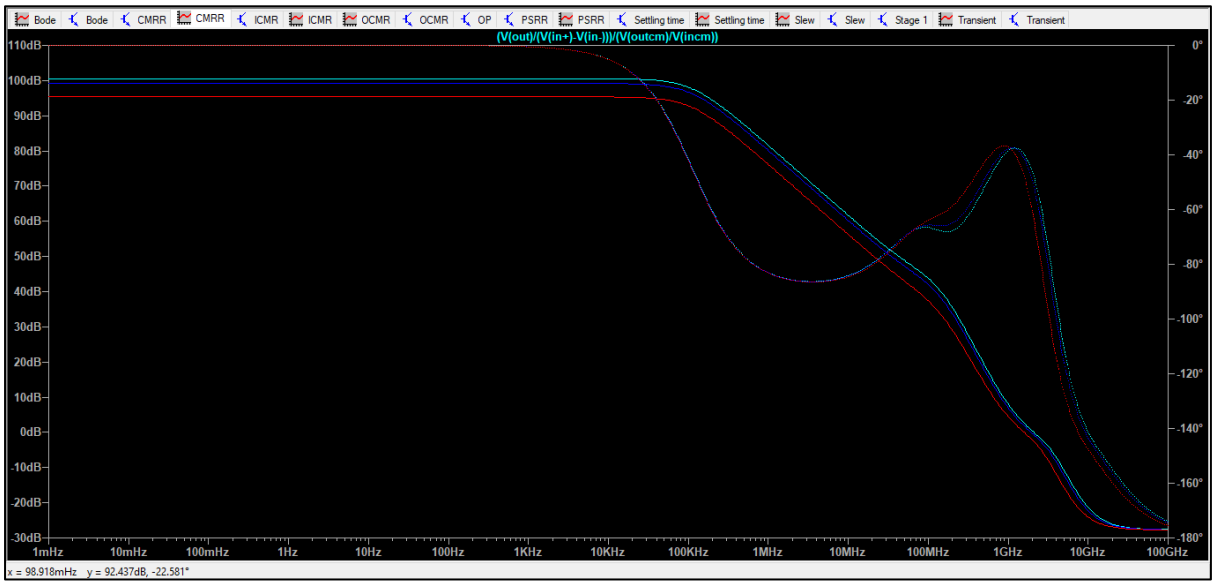
Temperature 100º C - **Settling Time = 17.870 ns**



4.6. CMRR Plot

Temperature 0ºC – DC gain – 100.52 dB

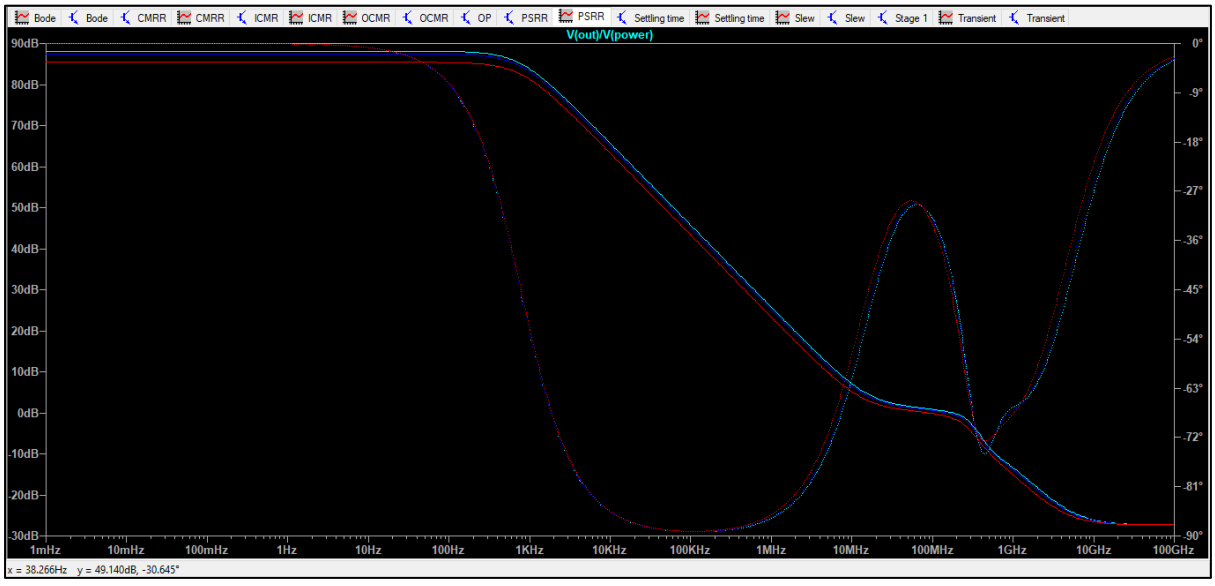
Temperature 100ºC – DC gain – 95.33 dB



4.7. PSRR Plot:

Temperature 0ºC – DC gain – 100.52 dB

Temperature 100ºC – DC gain – 95.33 dB



5. Summary of Results:

The final W/L ratios used for simulation in LTSpice were as follows: Where $\mathbf{l_{min}}$ was taken as **400 nm**.

MOSFET	W/L RATIOS
M1	10/0.4
M2	30/0.4
M3	12.5/0.4
M4	5/0.8
M5	5/0.4
M6	2/0.4
M7	0.5/0.4
M8	0.5/0.4
M9	0.5/0.4
M10	0.5/0.4
M11	1/0.4
M12	1/0.4
M13	1/0.4 (m=2)
M14	1/0.4 (m=2)
M15	1/0.4
M16	10/0.4

Table 1: W/L Ratio values for all MOSFETs (in μm, 'm' is the number of parallel devices)

Sr.no.	Quantity	Value	Required
1	DC Gain	102.09 dB	>= 100 dB
2	Output Voltage Swing	1.082 V	-
3	ICMR	1.89 V	-
4	Slew Rate	10 V/ μsec	<= 20 V/μsec
5	Phase Margin	52.35^{O}	$\sim 60^{O}$
6	Power Dissipation	0.2409 mW	<= 3 mW
7	Output Offset Voltage	0.2436 V	-
8	Input Offset Voltage	0.8 V	-
9	CMRR	99.19 dB	-
10	PSRR	87.464 dB	-
11	-3dB	701.57 Hz	-
12	UGB	213.79 MHz	-
13	Settling Time	12.135 ns	-

Table 2: Summary of Results found and required values

6. Problems faced during designing:

- The MOS018.CIR file which was shared with us had errors and it took us significant amount of time to realize that. Therefore, its contents were corrected and copied into a .txt file and that file was used to simulate using LTSpice.

- The knowledge required for attempting and solving the problem asked in this assignment was neither taught in the lectures nor was it completely covered in the TA sessions.

- It was very challenging to meet all the specifications given in the problem statement simultaneously. Several trade-offs were employed to satisfy most of the constraints mentioned in the problem.

- All the constraints cannot be satisfied simultaneously, without proper guidelines, for example, the Settling time cannot be within 20ns for a large signal (~1V), with a slew rate < 20MV/sec and nothing is mentioned about finding settling time.

7. Design Tips to Start

- Choose the design schematic as per the gain requirements.
- Preferably keep the currents low for the high gain stages, such that the W/L values are not very large, and hence the poles and zeroes that occur are not at a very low frequency. (Low intrinsic capacitance values help in increasing the pole and zero frequencies)
- For the buffer stage, keep the $g_m r_o$ values of the buffer MOSFET as high as possible. (In case the buffer is made of a source follower)
- Use Miller compensation wherever required, keeping the values of the order of tens to of pF to tens of fF.
- Keep the number of stages <= the number of stages specified.
- With the given instructions, only one kind of NMOS CM or PMOS current mirror biasing is possible, stick to whatever you choose throughout the design.
- Input offset voltage is very important, it is often neglected, and the circuits don’t work.