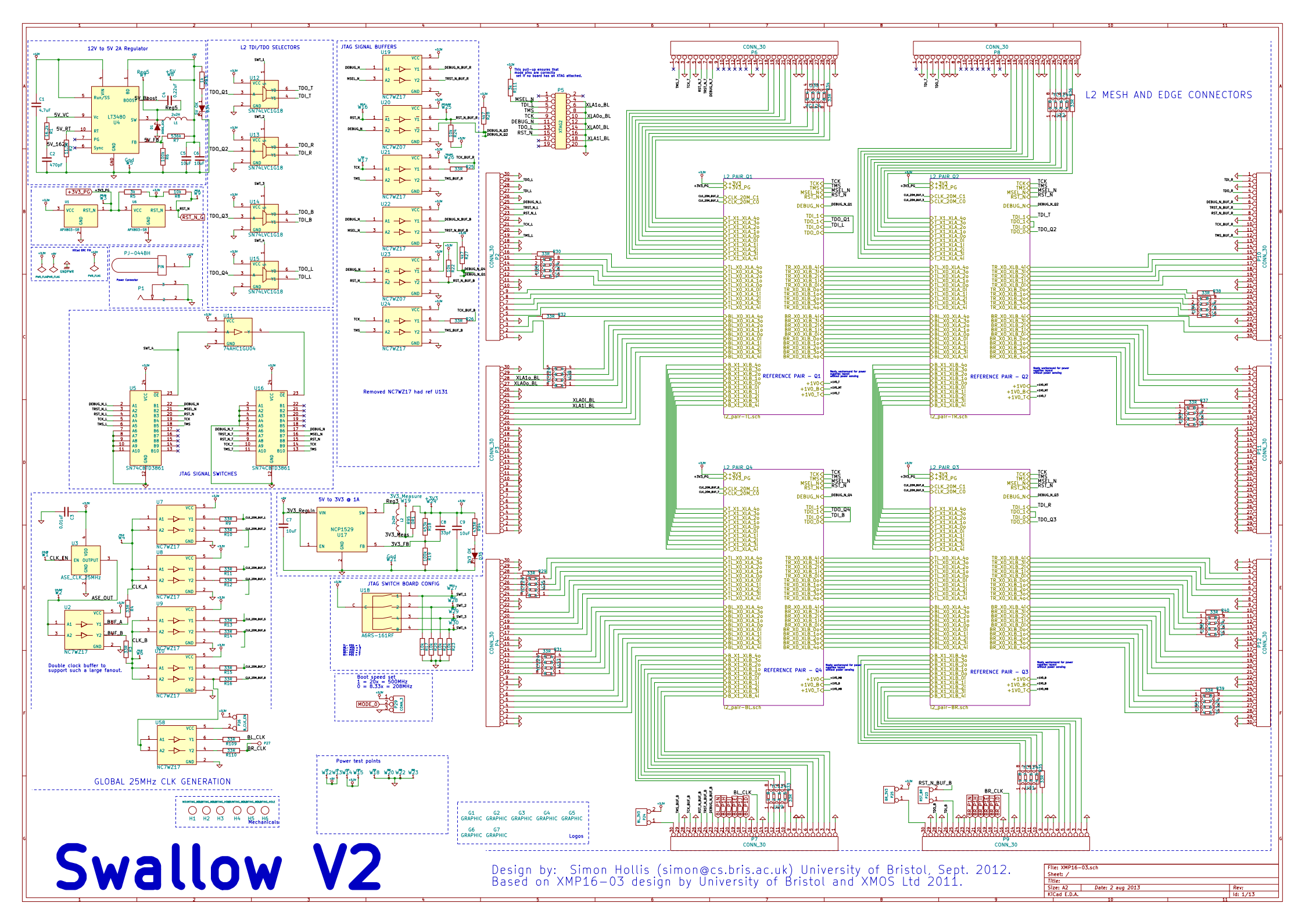
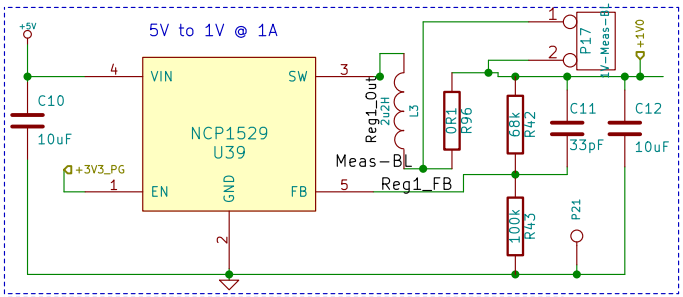
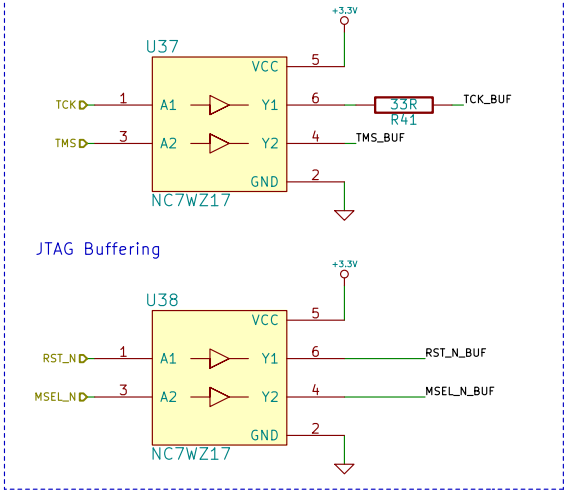
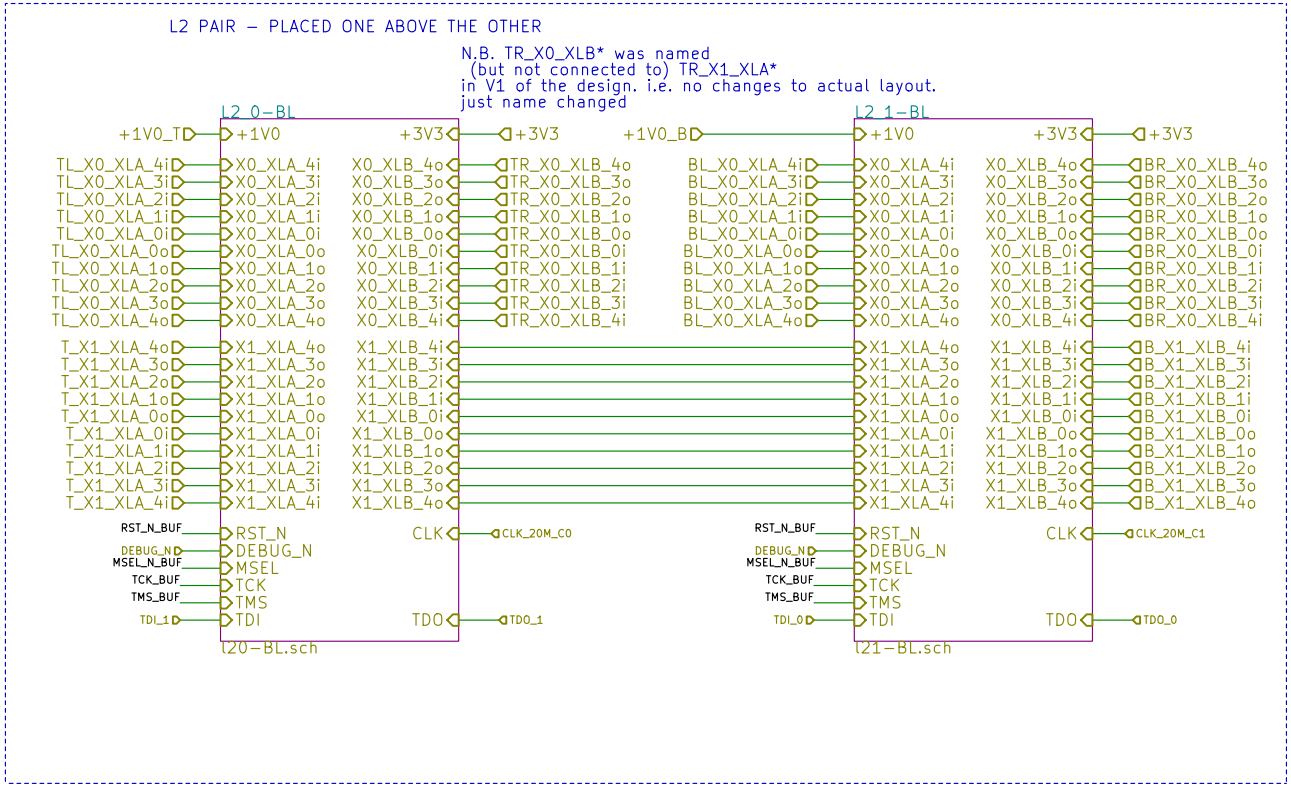

12V to 5V 2A Regulator
L2 TDI/TDO SELECTORS
JTAG SIGNAL BUFFERS
L2 MESH AND EDGE CONNECTORS
JTAG SIGNAL SWITCHES
GLOBAL 25MHz CLK GENERATION
5V to 3V3 @ 1A
JTAG SWITCH BOARD CONFIG
Power test points
Boot speed set
1 = 20x = 500MHz
0 = 8.33x = 208MHz
Double clock buffer to
support such a large fanout.
Removed NC7WZ17 had ref U131
L2_pair-TL.sch
L2_pair-TR.sch
L2_pair-BL.sch
L2_pair-BR.sch
Mechanicals
Logos
Swallow V2
Design by: Simon Hollis (simon@cs.bris.ac.uk) University of Bristol, Sept. 2012.
Based on XMP16-03 design by University of Bristol and XMOS Ltd 2011.
File: XMP16-03.sch
Sheet: /
Title:
Size: A2
Date: 2 aug 2013
Rev:
KiCad E.D.A.
Id: 1/13







File: l2_pair-BL.sch		
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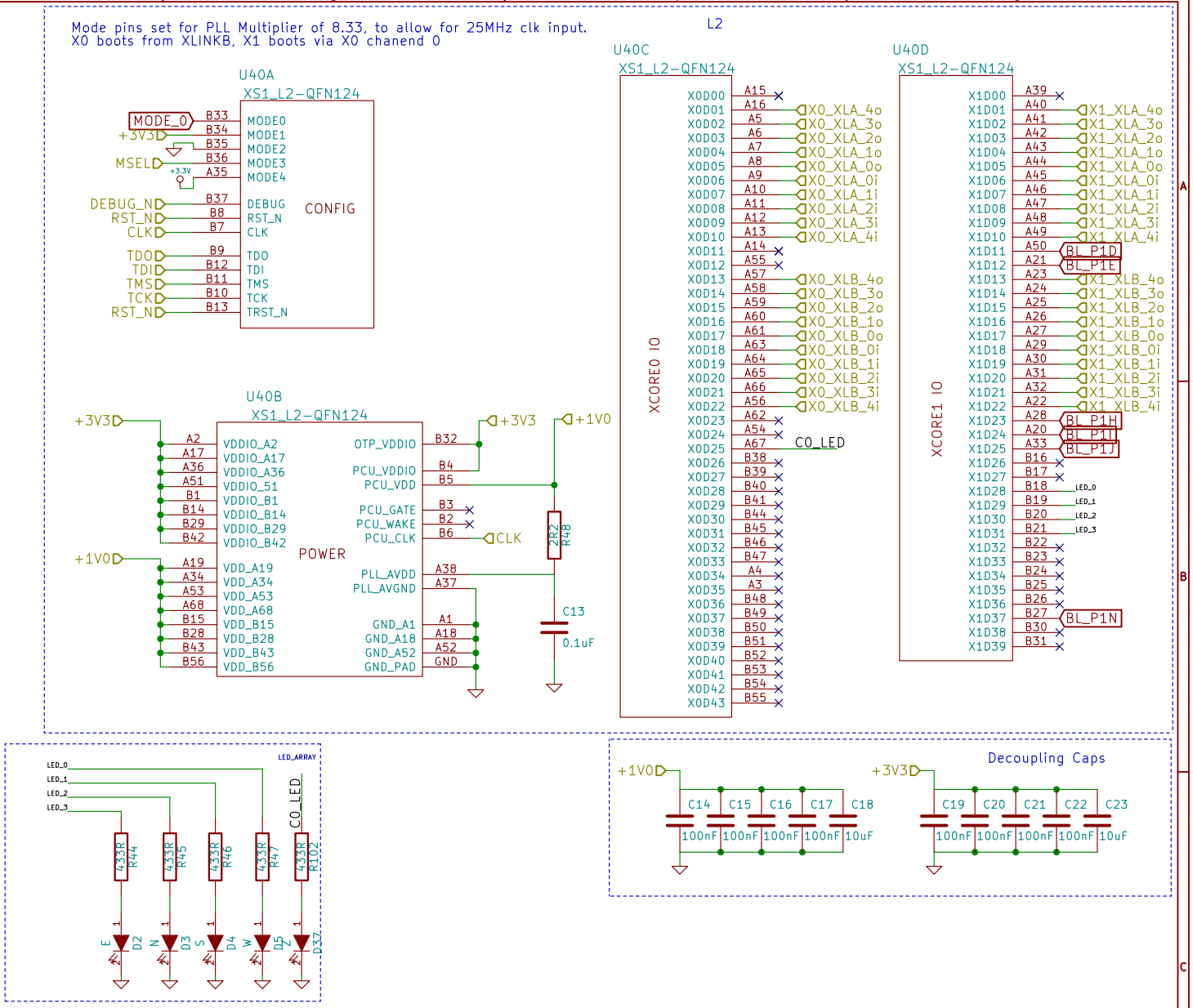
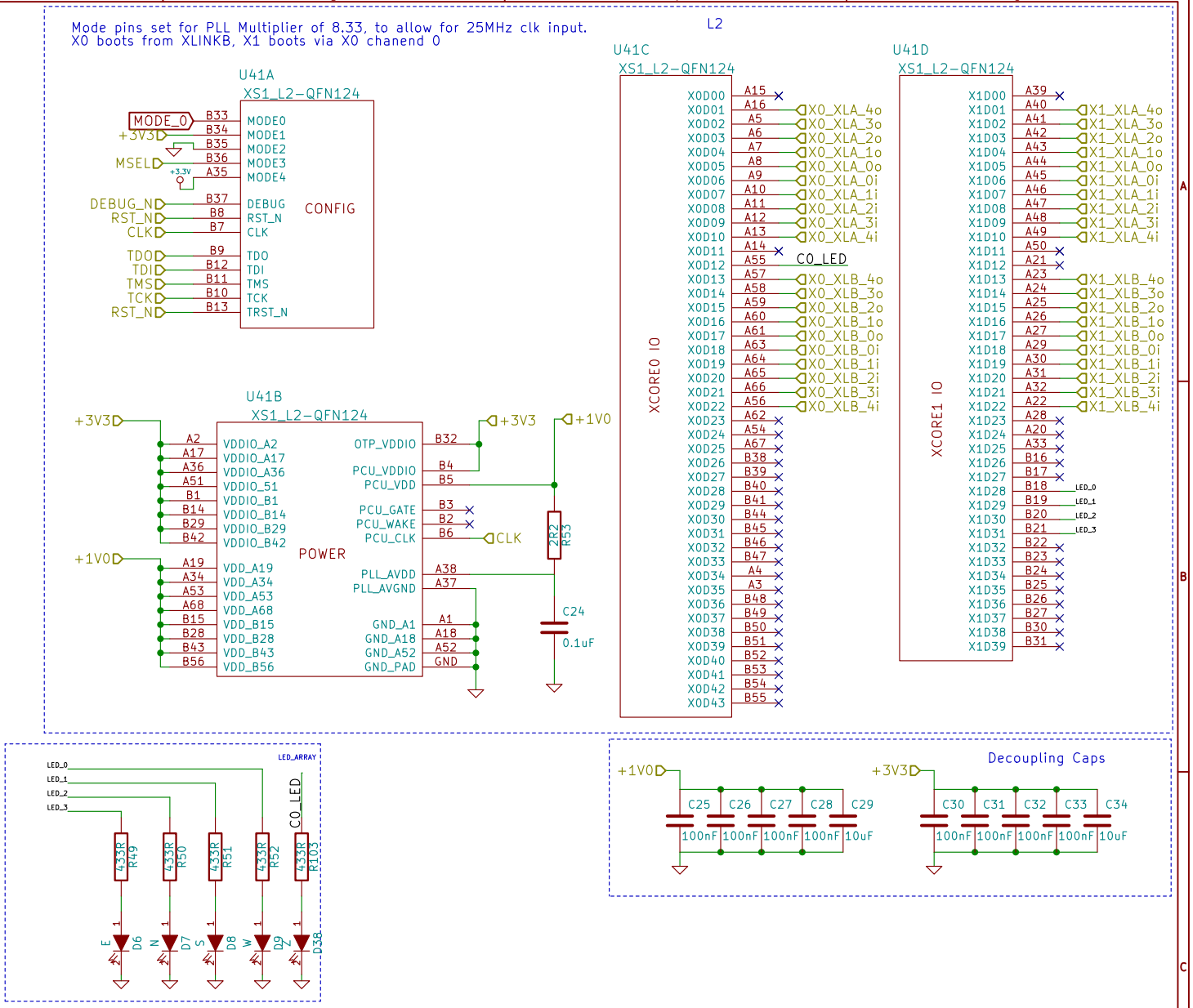
Size: A4	*Date: 2 aug 2013*	*Rev:*
KiCad E.D.A.		Id: 2/13


Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0
L2
U40A
XS1_L2-QFN124
MODE_0
+3V3
MSEL
DEBUG_N
RST_N
CLK
TDO
TDI
TMS
TCK
RST_N
MODE0
MODE1
MODE2
MODE3
MODE4
DEBUG
RST_N
CLK
TDO
TDI
TMS
TCK
TRST_N
CONFIG
U40B
XS1_L2-QFN124
+3V3
+1V0
VDDIO_A2
VDDIO_A17
VDDIO_A36
VDDIO_51
VDDIO_B1
VDDIO_B14
VDDIO_B29
VDDIO_B42
VDD_A19
VDD_A34
VDD_A53
VDD_A68
VDD_B15
VDD_B28
VDD_B43
VDD_B56
POWER
OTP_VDDIO
PCU_VDDIO
PCU_VDD
PCU_GATE
PCU_WAKE
PCU_CLK
PLL_AVDD
PLL_AVGND
GND_A1
GND_A18
GND_A52
GND
CLK
2R2
R48
C13
0.1uF
U40C
XS1_L2-QFN124
XCORE0 IO
X0D00
X0D01
X0D02
X0D03
X0D04
X0D05
X0D06
X0D07
X0D08
X0D09
X0D10
X0D11
X0D12
X0D13
X0D14
X0D15
X0D16
X0D17
X0D18
X0D19
X0D20
X0D21
X0D22
X0D23
X0D24
X0D25
X0D26
X0D27
X0D28
X0D29
X0D30
X0D31
X0D32
X0D33
X0D34
X0D35
X0D36
X0D37
X0D38
X0D39
X0D40
X0D41
X0D42
X0D43
X0_XLA_4o
X0_XLA_3o
X0_XLA_2o
X0_XLA_1o
X0_XLA_0o
X0_XLA_0i
X0_XLA_1i
X0_XLA_2i
X0_XLA_3i
X0_XLA_4i
X0_XLB_4o
X0_XLB_3o
X0_XLB_2o
X0_XLB_1o
X0_XLB_0o
X0_XLB_0i
X0_XLB_1i
X0_XLB_2i
X0_XLB_3i
X0_XLB_4i
C0_LED
U40D
XS1_L2-QFN124
XCORE1 IO
X1D00
X1D01
X1D02
X1D03
X1D04
X1D05
X1D06
X1D07
X1D08
X1D09
X1D10
X1D11
X1D12
X1D13
X1D14
X1D15
X1D16
X1D17
X1D18
X1D19
X1D20
X1D21
X1D22
X1D23
X1D24
X1D25
X1D26
X1D27
X1D28
X1D29
X1D30
X1D31
X1D32
X1D33
X1D34
X1D35
X1D36
X1D37
X1D38
X1D39
X1_XLA_4o
X1_XLA_3o
X1_XLA_2o
X1_XLA_1o
X1_XLA_0o
X1_XLA_0i
X1_XLA_1i
X1_XLA_2i
X1_XLA_3i
X1_XLA_4i
BL_P1D
BL_P1E
X1_XLB_4o
X1_XLB_3o
X1_XLB_2o
X1_XLB_1o
X1_XLB_0o
X1_XLB_0i
X1_XLB_1i
X1_XLB_2i
X1_XLB_3i
X1_XLB_4i
BL_P1H
BL_P1I
BL_P1J
BL_P1N
LED_0
LED_1
LED_2
LED_3
LED_ARRAY
C0_LED
433R
R44
R45
R46
R47
R102
D2
D3
D4
D5
D37
Decoupling Caps
+1V0
+3V3
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
100nF
10uF
File: l21-BL.sch
Sheet: /L2_PAIR_Q4/L2_1-BL/
Title:
Size: A4
Date: 2 aug 2013
Rev:
KiCad E.D.A.
Id: 3/13



File: l20-BL.sch		
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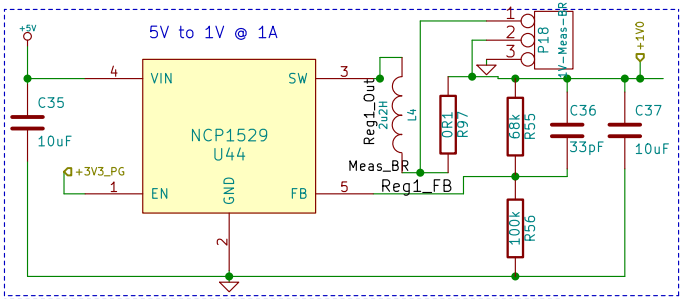
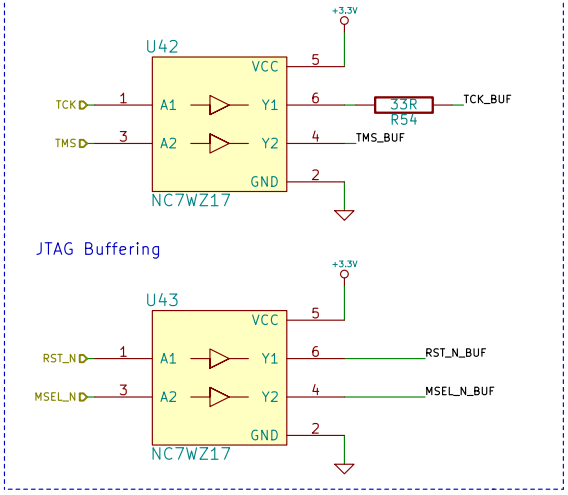
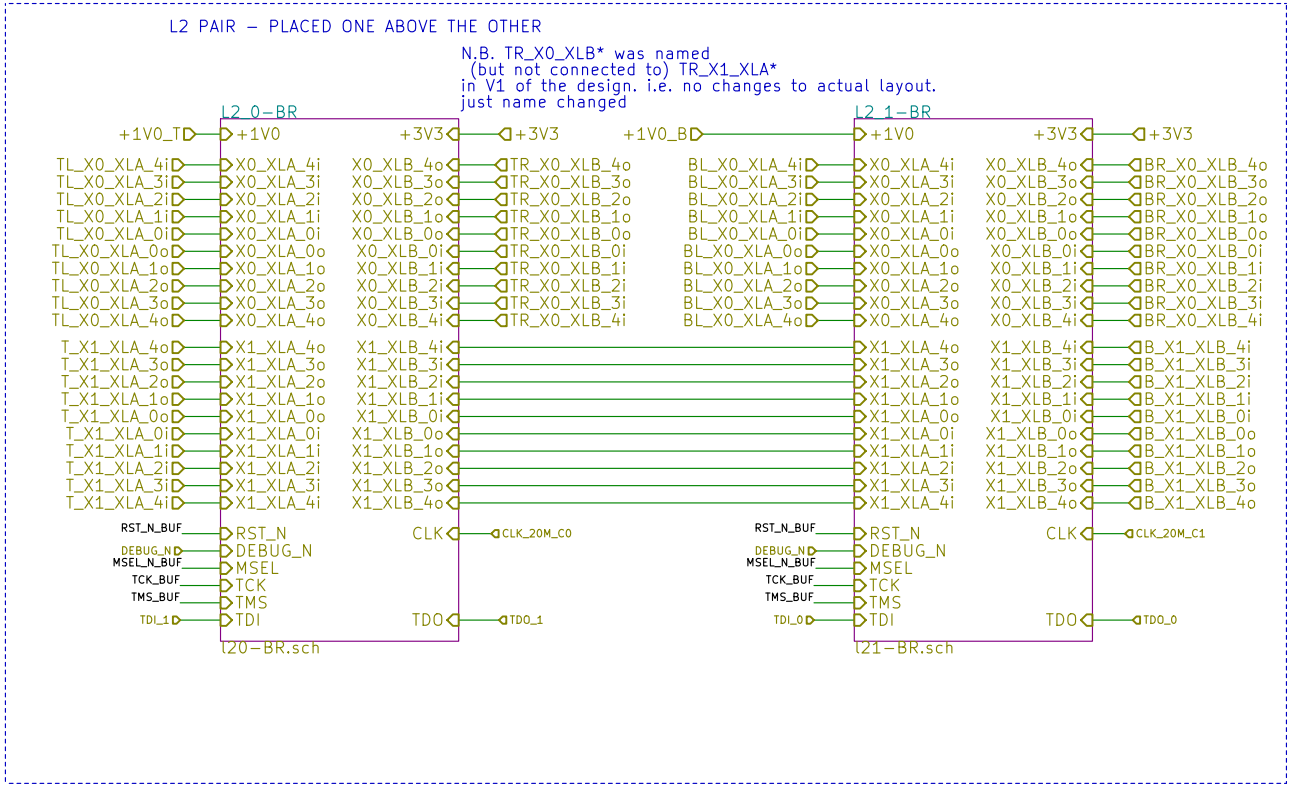
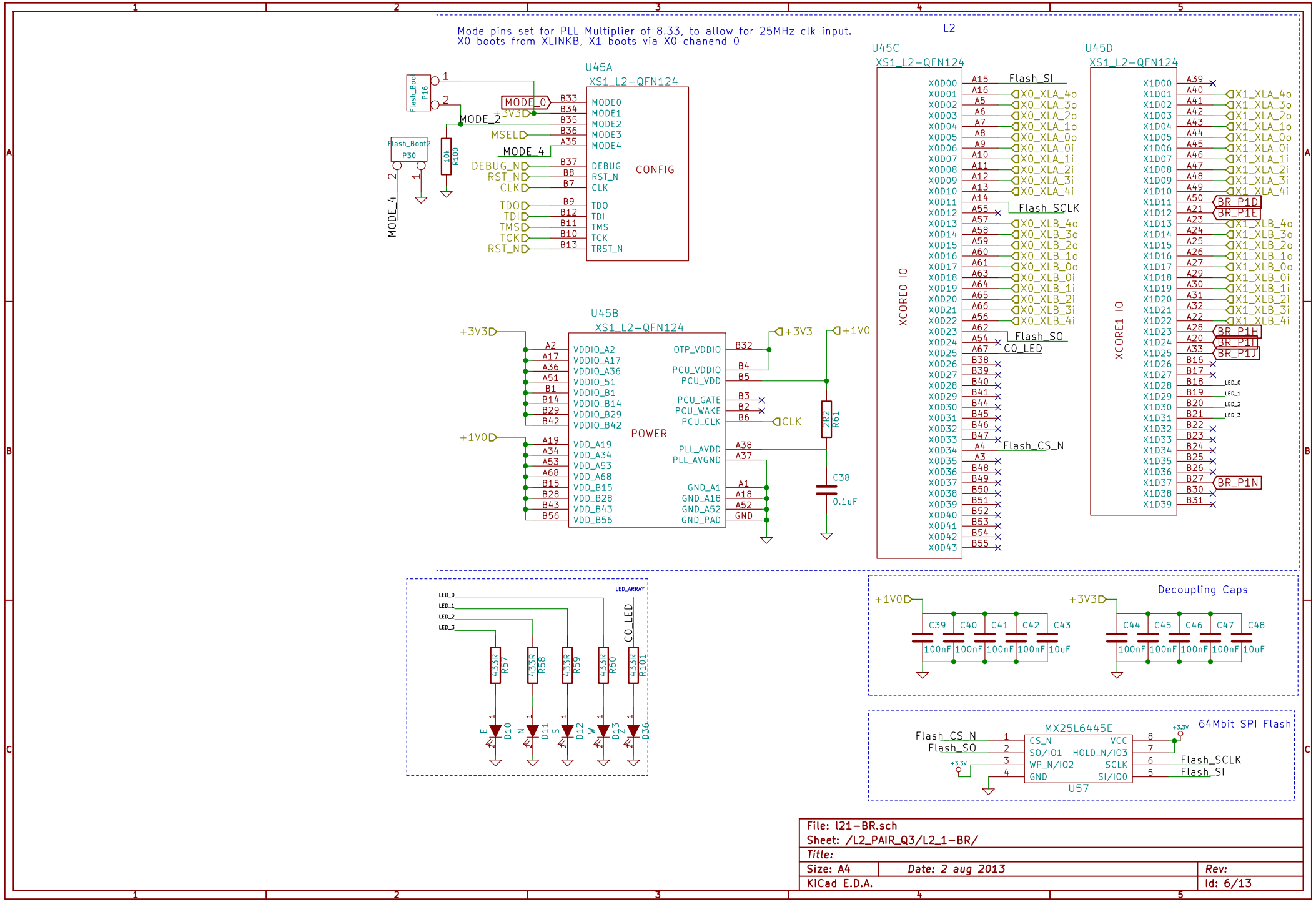
Title:		
Size: A4	*Date: 2 aug 2013*	*Rev:*
KiCad E.D.A.		Id: 4/13

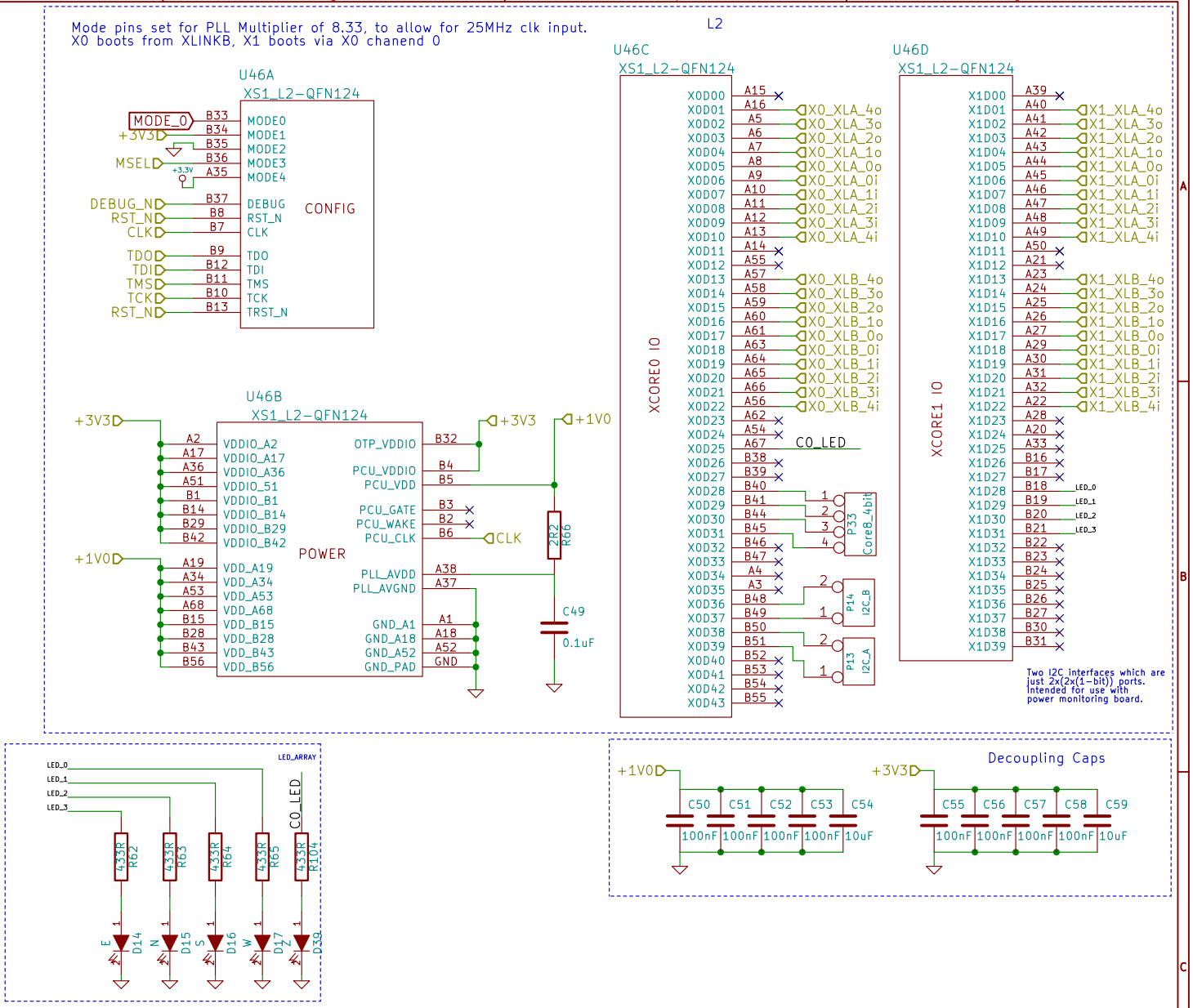




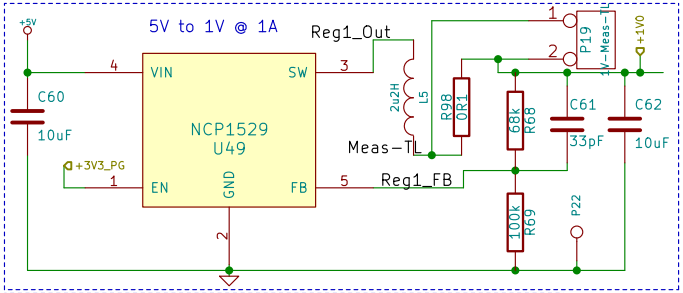


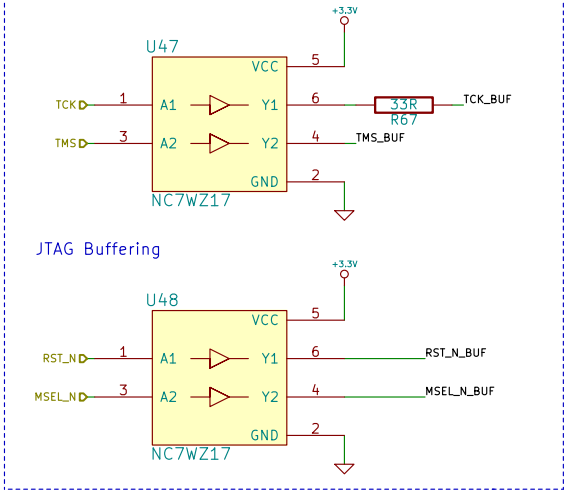
File: l2_pair-BR.sch		
Sheet: /L2_PAIR_Q3/		
Title:		
Size: A4	Date: 2 aug 2013	Rev:
KiCad E.D.A.		Id: 5/13

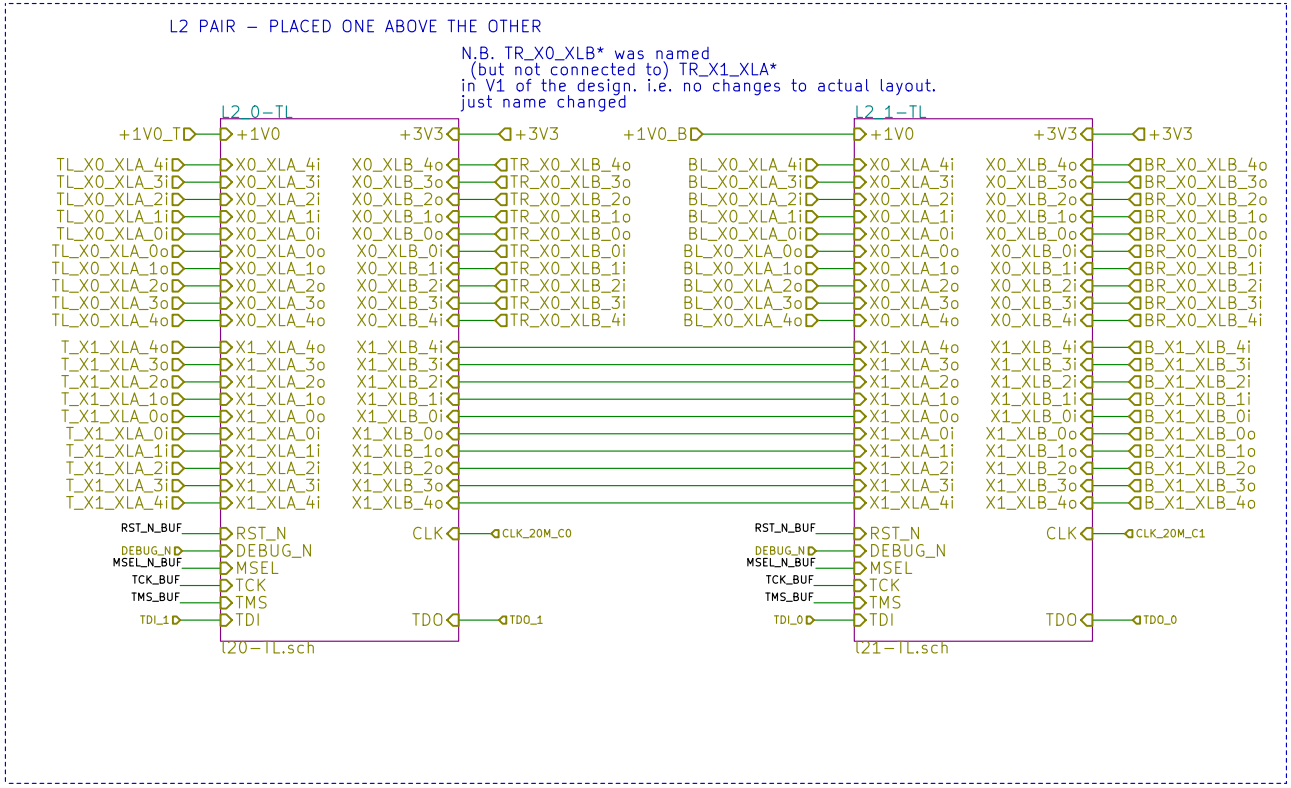

Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0
L2
U45A
XS1_L2-QFN124
Flash_Boot
P16
Flash_Boot2
P30
MODE_0
MODE_2
MODE_4
+3V3
10k
R100
MSEL
DEBUG_N
RST_N
CLK
TDO
TDI
TMS
TCK
TRST_N
MODE0
MODE1
MODE2
MODE3
MODE4
DEBUG
CONFIG
U45B
XS1_L2-QFN124
+1V0
VDDIO_A2
VDDIO_A17
VDDIO_A36
VDDIO_51
VDDIO_B1
VDDIO_B14
VDDIO_B29
VDDIO_B42
VDD_A19
VDD_A34
VDD_A53
VDD_A68
VDD_B15
VDD_B28
VDD_B43
VDD_B56
POWER
OTP_VDDIO
PCU_VDDIO
PCU_VDD
PCU_GATE
PCU_WAKE
PCU_CLK
PLL_AVDD
PLL_AVGND
GND_A1
GND_A18
GND_A52
GND_PAD
2R2
R61
C38
0.1uF
U45C
XS1_L2-QFN124
XCORE0 IO
U45D
XS1_L2-QFN124
XCORE1 IO
Flash_SI
Flash_SCLK
Flash_SO
C0_LED
Flash_CS_N
LED_ARRAY
LED_0
LED_1
LED_2
LED_3
C0_LED
433R
R57
R58
R59
R60
R101
D10
D11
D12
D13
D36
Decoupling Caps
C39
C40
C41
C42
C43
C44
C45
C46
C47
C48
100nF
10uF
MX25L6445E
64Mbit SPI Flash
U57
CS_N
SO/IO1
WP_N/IO2
GND
VCC
HOLD_N/IO3
SCLK
SI/IO0
File: l21-BR.sch
Sheet: /L2_PAIR_Q3/L2_1-BR/
Title:
Size: A4
Date: 2 aug 2013
Rev:
KiCad E.D.A.
Id: 6/13



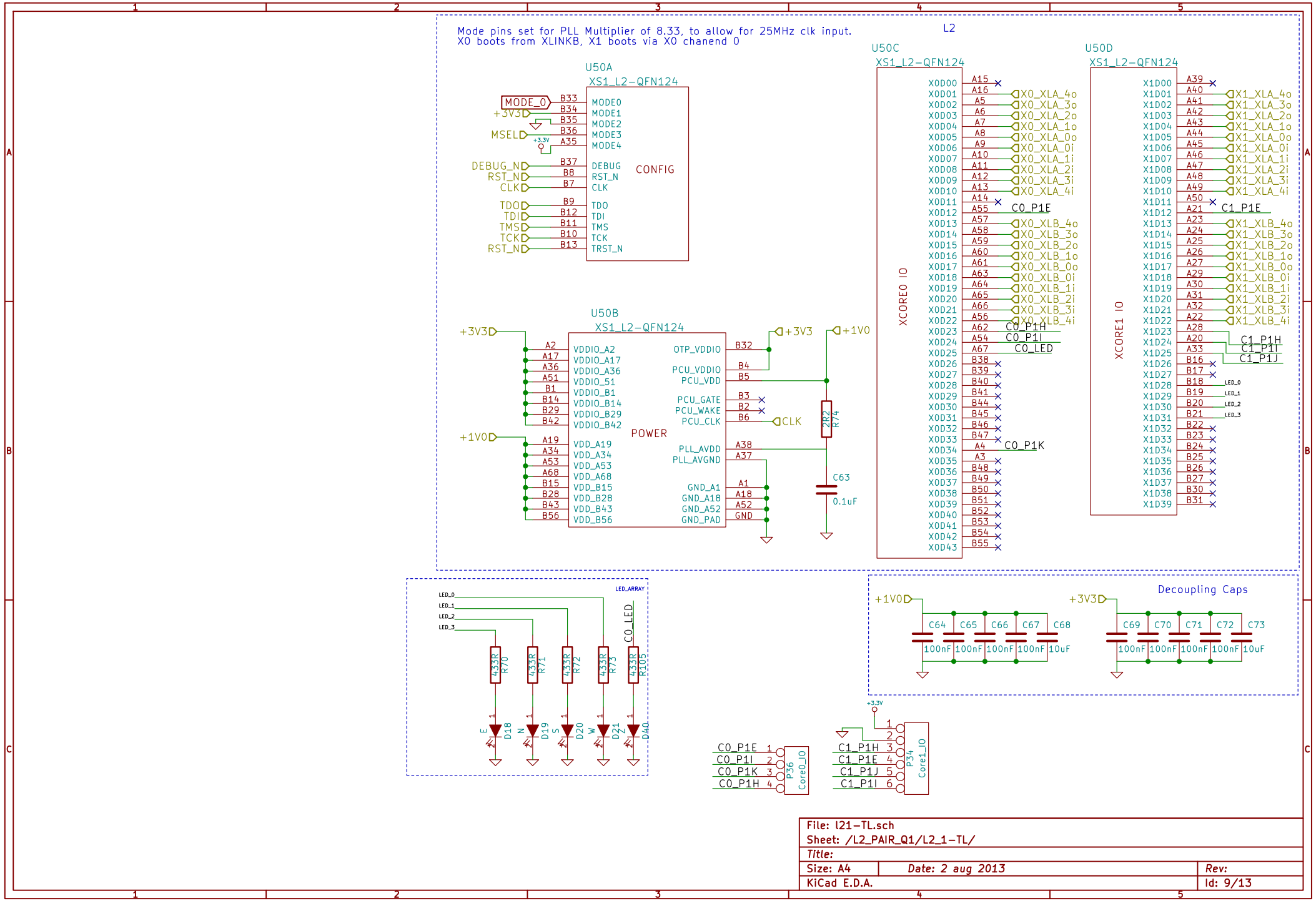
File: l20-BR.sch		
Sheet: /L2_PAIR_Q3/L2_0-BR/		
Title:		
Size: A4	Date: 2 aug 2013	Rev:
KiCad E.D.A.		Id: 7/13

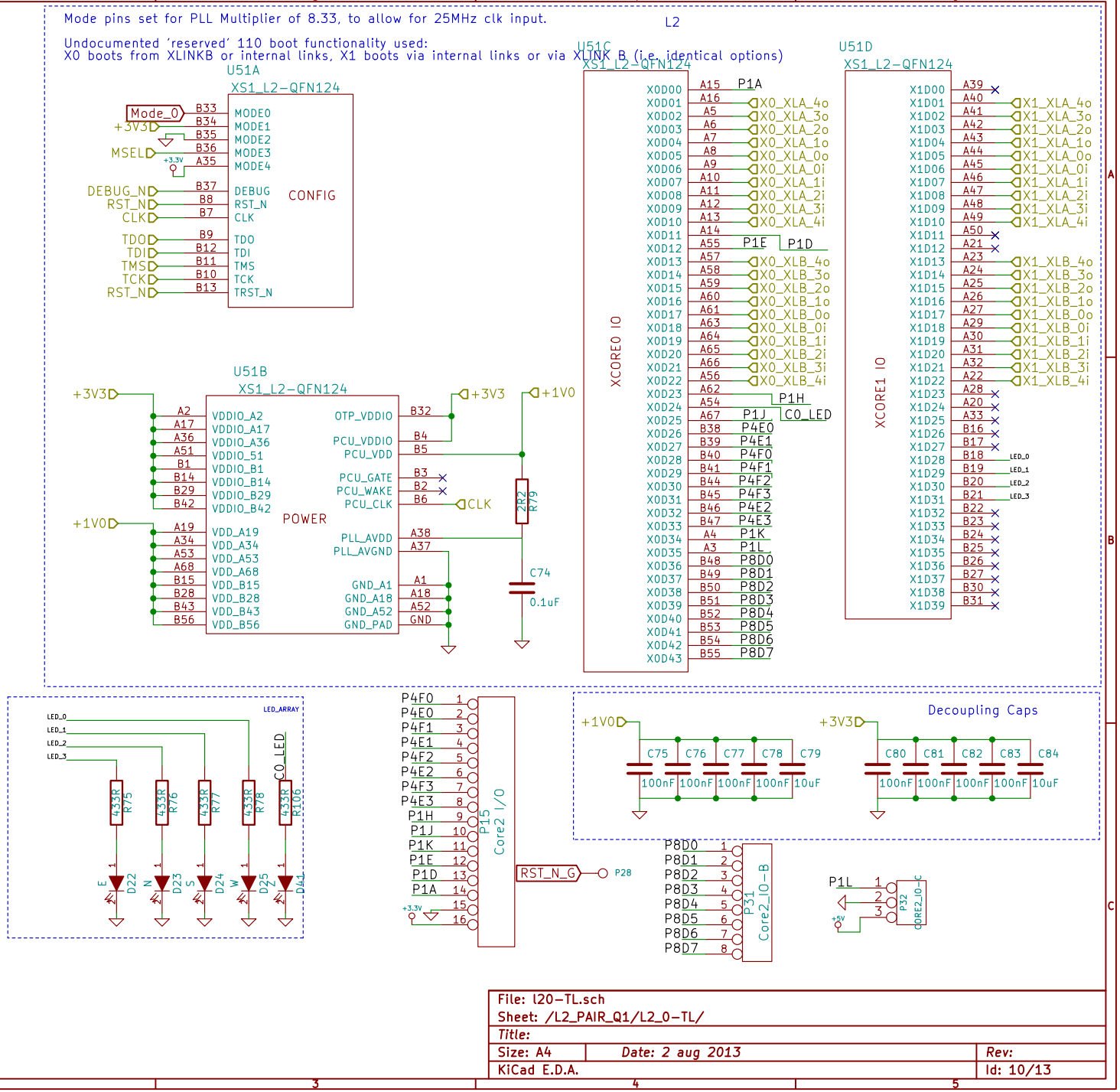


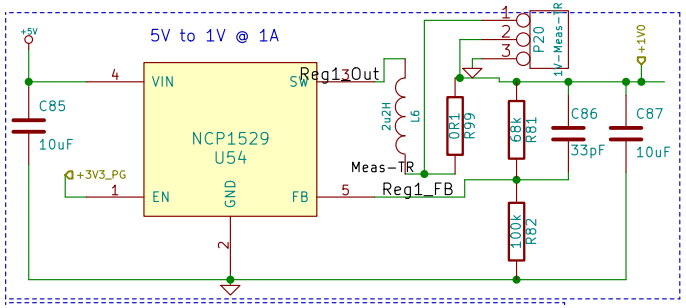


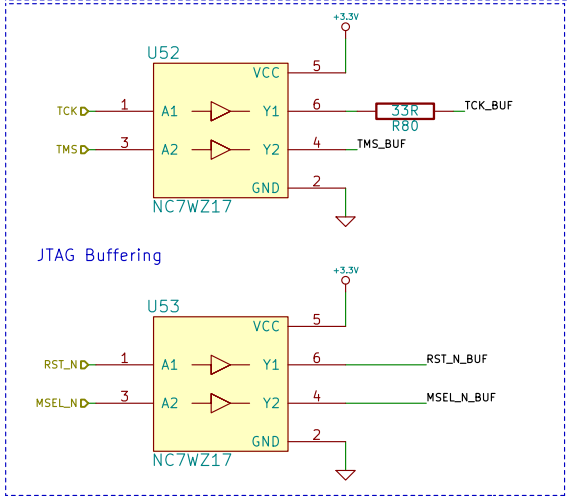


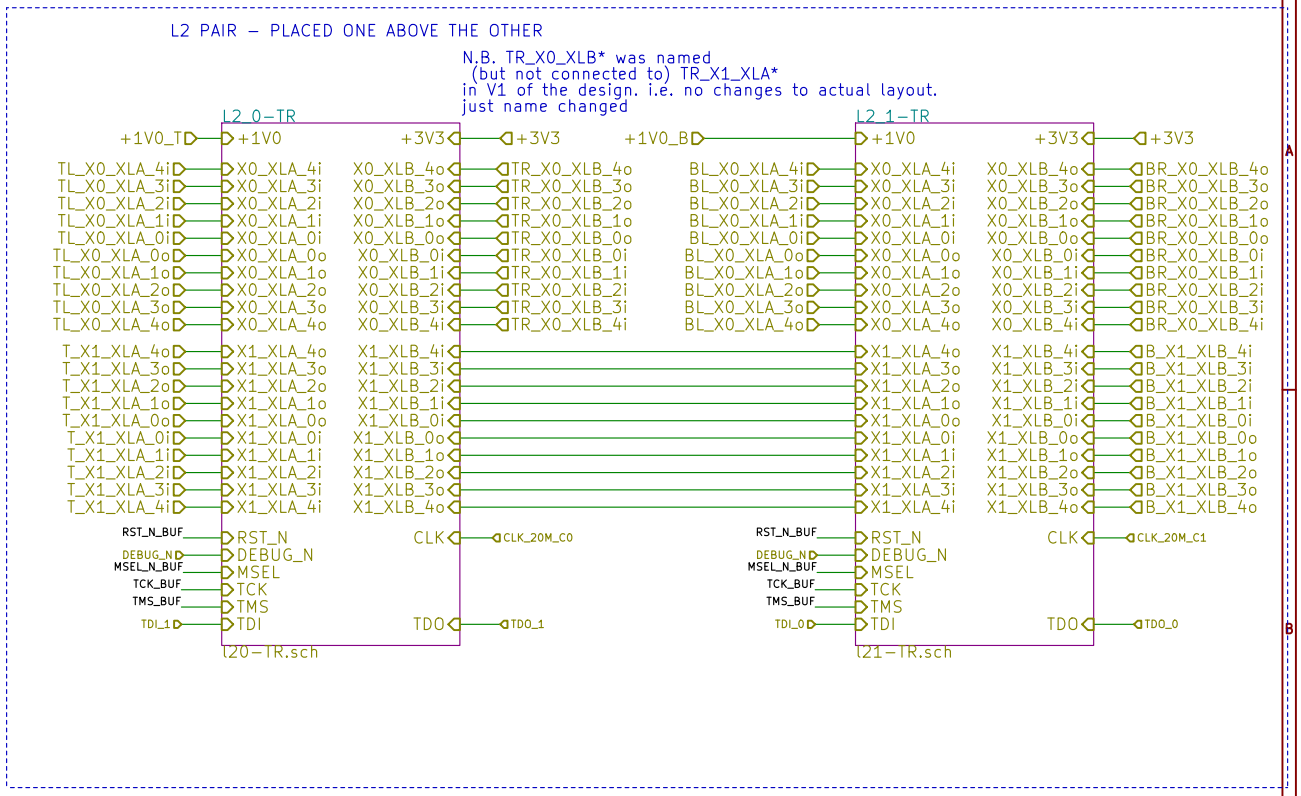
File: l2_pair-TL.sch		
Sheet: /L2_PAIR_Q1/		
Title:		
Size: A4	Date: 2 aug 2013	Rev:
KiCad E.D.A.		Id: 8/13


Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0
L2
U50A
XS1_L2-QFN124
MODE_0
+3V3
MSEL
DEBUG_N
RST_N
CLK
TDO
TDI
TMS
TCK
RST_N
CONFIG
U50B
XS1_L2-QFN124
POWER
+3V3
+1V0
CLK
2R2
R74
C63
0.1uF
U50C
XS1_L2-QFN124
XCORE0 IO
C0_P1E
C0_P1H
C0_P1I
C0_P1K
C0_LED
U50D
XS1_L2-QFN124
XCORE1 IO
C1_P1E
C1_P1H
C1_P1I
C1_P1J
LED_ARRAY
C0_LED
433R
Decoupling Caps
C64
C65
C66
C67
C68
C69
C70
C71
C72
C73
100nF
10uF
P36
Core0_IO
P34
Core1_IO
File: l21-TL.sch
Sheet: /L2_PAIR_Q1/L2_1-TL/
Title:
Size: A4
Date: 2 aug 2013
Rev:
KiCad E.D.A.
Id: 9/13

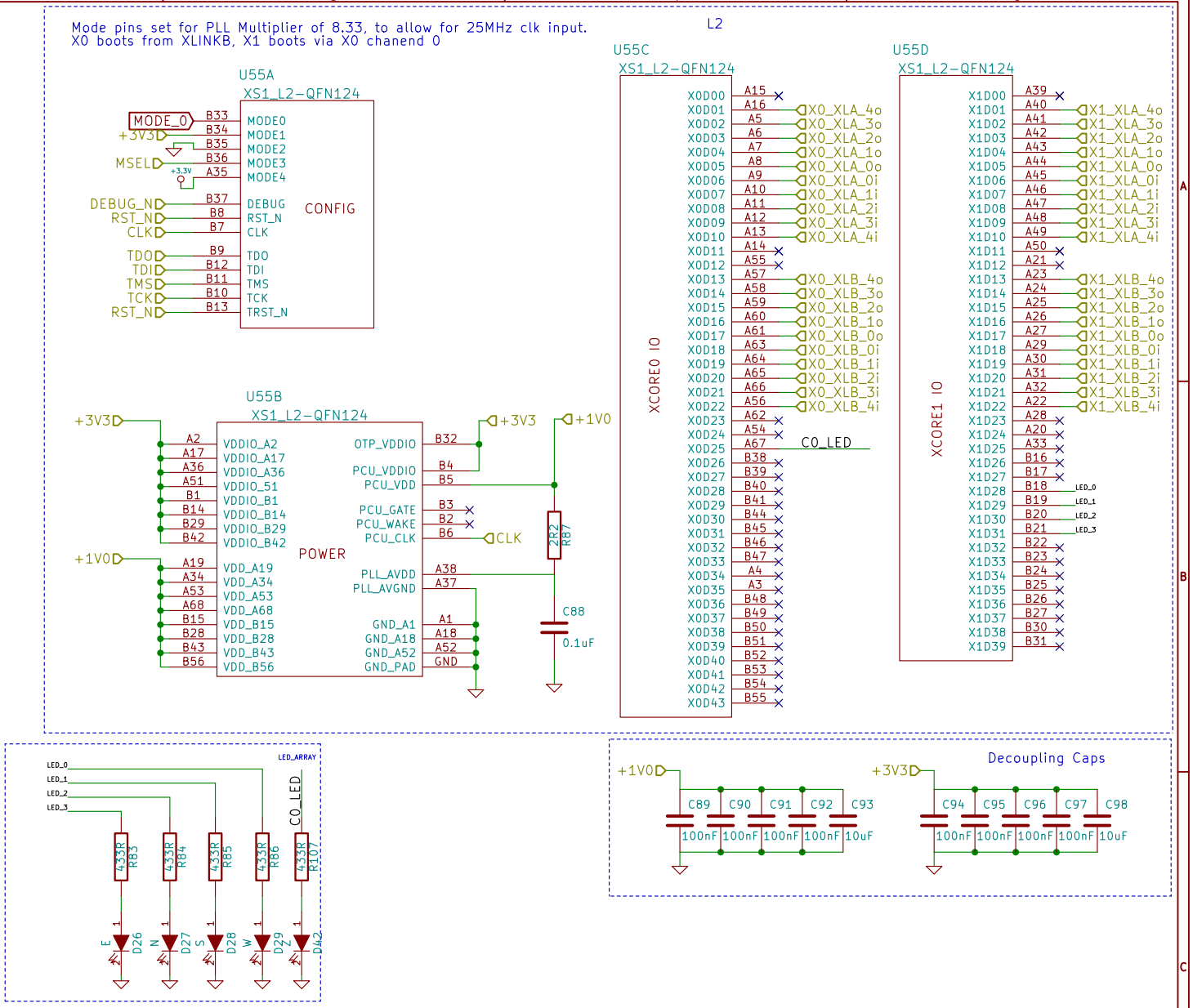

Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
Undocumented 'reserved' 110 boot functionality used:
X0 boots from XLINKB or internal links, X1 boots via internal links or via XLINK B (i.e. identical options)
L2
U51A
XS1_L2-QFN124
Mode_0
+3V3
MSEL
DEBUG_N
RST_N
CLK
TDO
TDI
TMS
TCK
RST_N
MODE0
MODE1
MODE2
MODE3
MODE4
DEBUG
RST_N
CLK
TDO
TDI
TMS
TCK
TRST_N
CONFIG
U51B
XS1_L2-QFN124
+3V3
+1V0
VDDIO_A2
VDDIO_A17
VDDIO_A36
VDDIO_51
VDDIO_B1
VDDIO_B14
VDDIO_B29
VDDIO_B42
VDD_A19
VDD_A34
VDD_A53
VDD_A68
VDD_B15
VDD_B28
VDD_B43
VDD_B56
OTP_VDDIO
PCU_VDDIO
PCU_VDD
PCU_GATE
PCU_WAKE
PCU_CLK
PLL_AVDD
PLL_AVGND
GND_A1
GND_A18
GND_A52
GND_PAD
POWER
CLK
2R2
R79
C74
0.1uF
U51C
XS1_L2-QFN124
XCORE0 IO
U51D
XS1_L2-QFN124
XCORE1 IO
P1A
P1E
P1D
P1H
P1J
C0_LED
P4E0
P4E1
P4F0
P4F1
P4F2
P4F3
P4E2
P4E3
P1K
P1L
P8D0
P8D1
P8D2
P8D3
P8D4
P8D5
P8D6
P8D7
X0_XLA_4o
X0_XLA_3o
X0_XLA_2o
X0_XLA_1o
X0_XLA_0o
X0_XLA_0i
X0_XLA_1i
X0_XLA_2i
X0_XLA_3i
X0_XLA_4i
X0_XLB_4o
X0_XLB_3o
X0_XLB_2o
X0_XLB_1o
X0_XLB_0o
X0_XLB_0i
X0_XLB_1i
X0_XLB_2i
X0_XLB_3i
X0_XLB_4i
X1_XLA_4o
X1_XLA_3o
X1_XLA_2o
X1_XLA_1o
X1_XLA_0o
X1_XLA_0i
X1_XLA_1i
X1_XLA_2i
X1_XLA_3i
X1_XLA_4i
X1_XLB_4o
X1_XLB_3o
X1_XLB_2o
X1_XLB_1o
X1_XLB_0o
X1_XLB_0i
X1_XLB_1i
X1_XLB_2i
X1_XLB_3i
X1_XLB_4i
LED_0
LED_1
LED_2
LED_3
LED_ARRAY
C0_LED
433R
R75
R76
R77
R78
R106
D22
D23
D24
D25
D41
P15
Core2 I/O
RST_N_G
P28
P31
Core2_IO-B
P32
CORE2_IO-C
Decoupling Caps
C75
C76
C77
C78
C79
C80
C81
C82
C83
C84
100nF
10uF
File: l20-TL.sch
Sheet: /L2_PAIR_Q1/L2_0-TL/
Title:
Size: A4
Date: 2 aug 2013
Rev:
KiCad E.D.A.
Id: 10/13







File: l2_pair-TR.sch		
Sheet: /L2_PAIR_Q2/		
Title:		
Size: A4	*Date: 2 aug 2013*	*Rev:*
KiCad E.D.A.		Id: 11/13


Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0
L2
U55A
XS1_L2-QFN124
MODE_0
+3V3
MSEL
DEBUG_N
RST_N
CLK
TDO
TDI
TMS
TCK
RST_N
MODE0
MODE1
MODE2
MODE3
MODE4
DEBUG
RST_N
CLK
TDO
TDI
TMS
TCK
TRST_N
CONFIG
U55B
XS1_L2-QFN124
VDDIO_A2
VDDIO_A17
VDDIO_A36
VDDIO_51
VDDIO_B1
VDDIO_B14
VDDIO_B29
VDDIO_B42
VDD_A19
VDD_A34
VDD_A53
VDD_A68
VDD_B15
VDD_B28
VDD_B43
VDD_B56
OTP_VDDIO
PCU_VDDIO
PCU_VDD
PCU_GATE
PCU_WAKE
PCU_CLK
PLL_AVDD
PLL_AVGND
GND_A1
GND_A18
GND_A52
GND_PAD
POWER
+3V3
+1V0
CLK
2R2
R87
C88
0.1uF
U55C
XS1_L2-QFN124
XCORE0 IO
C0_LED
U55D
XS1_L2-QFN124
XCORE1 IO
LED_ARRAY
LED_0
LED_1
LED_2
LED_3
C0_LED
433R
R83
R84
R85
R86
R107
D26
D27
D28
D29
D42
E
N
S
W
Decoupling Caps
+1V0
+3V3
C89
C90
C91
C92
C93
C94
C95
C96
C97
C98
100nF
10uF
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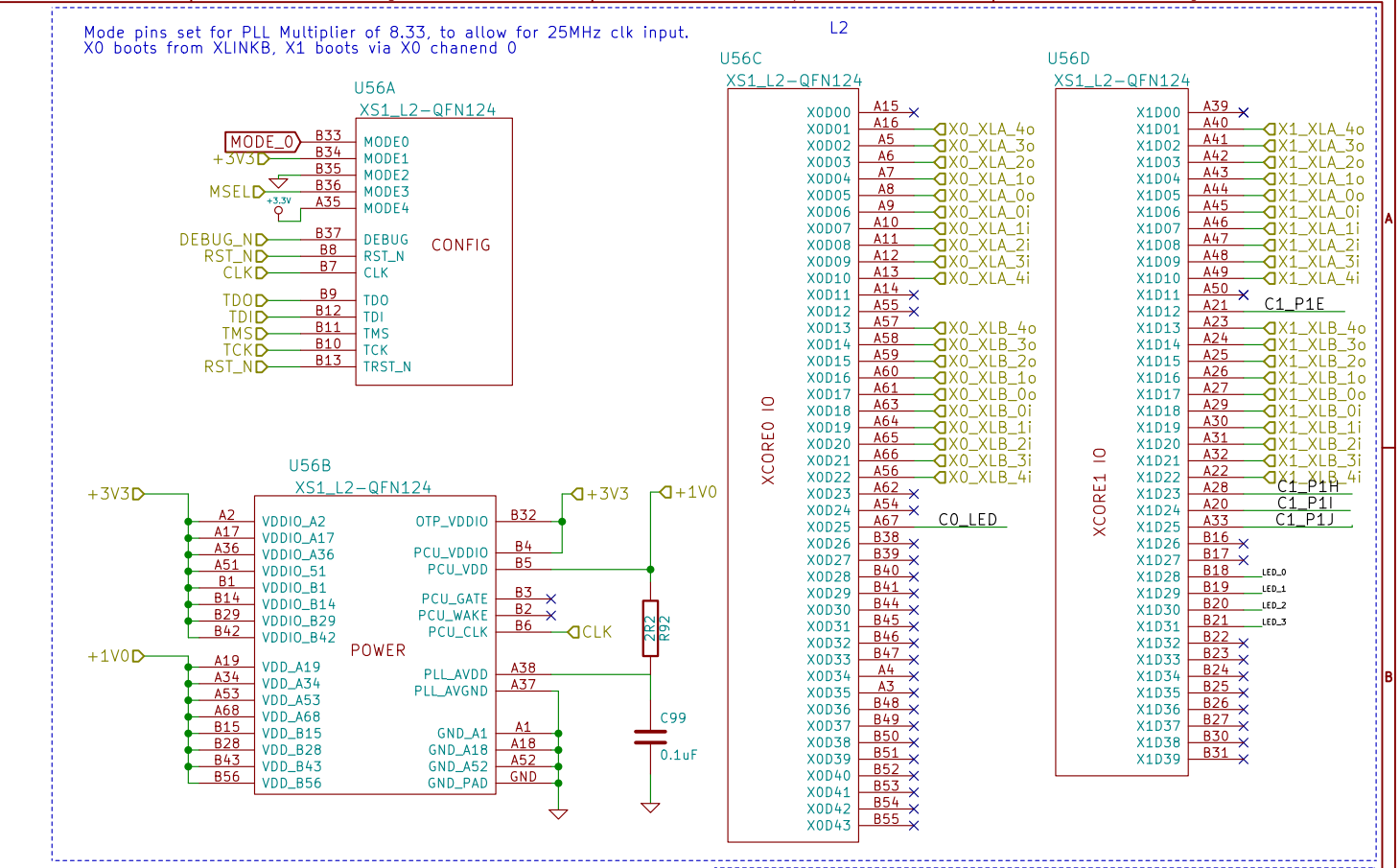
Date: 2 aug 2013
Rev:
KiCad E.D.A.
Id: 12/13



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