12V to 5V 2A Regulator

L2 TDI/TDO SELECTORS

JTAG SIGNAL BUFFERS

Removed NC7WZ17 had ref U131

This pull-up ensures that mode pins are correctly set if no board has an XTAG attached.

L2 MESH AND EDGE CONNECTORS

JTAG SIGNAL SWITCHES

5V to 3V3 @ 1A

JTAG SWITCH BOARD CONFIG

Boot speed set
1 = 20x = 500MHz
0 = 8.33x = 208MHz

Double clock buffer to support such a large fanout.

GLOBAL 25MHz CLK GENERATION

Power test points

Mechanicals

REFERENCE PAIR – Q1

REFERENCE PAIR – Q2

REFERENCE PAIR – Q3

REFERENCE PAIR – Q4

Nasty workaround for power supplies layout without power sensing

Swallow V2

Design by: Simon Hollis (simon@cs.bris.ac.uk) University of Bristol, Sept. 2012.
Based on XMP16-03 design by University of Bristol and XMOS Ltd 2011.

File: XMP16-03.sch	
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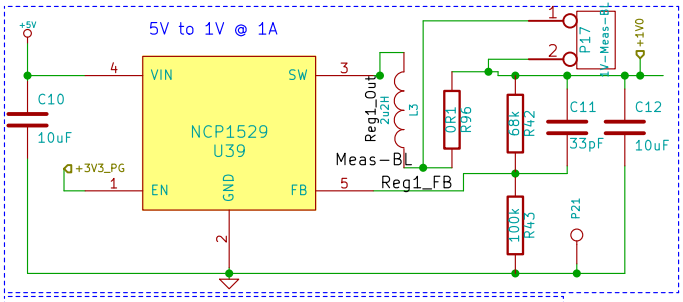
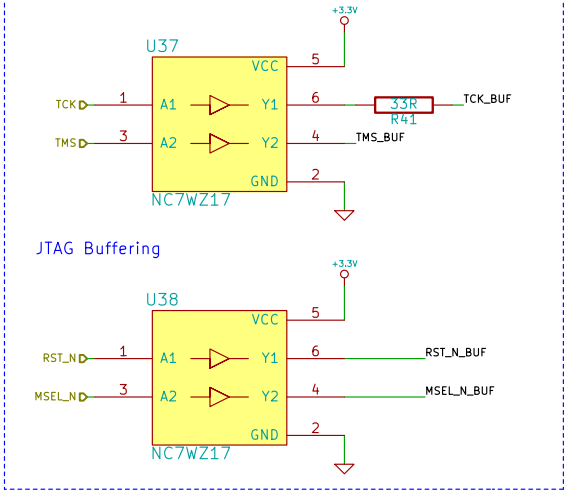
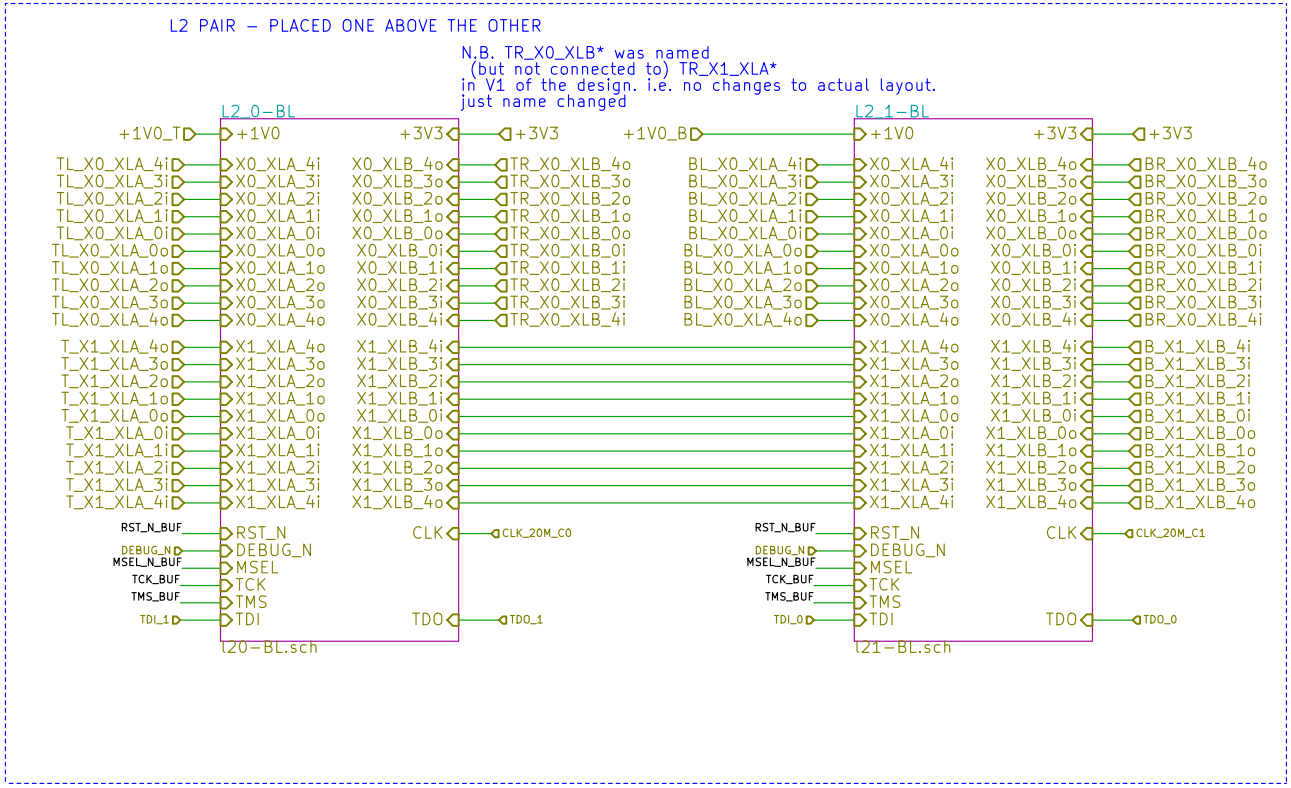
Title:	
Size: A2	Date: 28 oct 2012
KiCad E.D.A.	Id: 1/13







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KiCad E.D.A.		Id: 2/13

Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0

L2

U40A
XS1_L2-QFN124

MODE_0 B33 MODE0
+3V3 B34 MODE1
B35 MODE2
MSEL B36 MODE3
+3.3V A35 MODE4
CONFIG
DEBUG_N B37 DEBUG
RST_N B8 RST_N
CLK B7 CLK
TDO B9 TDO
TDI B12 TDI
TMS B11 TMS
TCK B10 TCK
RST_N B13 TRST_N

U40B
XS1_L2-QFN124

+3V3 A2 VDDIO_A2
A17 VDDIO_A17
A36 VDDIO_A36
A51 VDDIO_51
B1 VDDIO_B1
B14 VDDIO_B14
B29 VDDIO_B29
B42 VDDIO_B42
+1V0 A19 VDD_A19
A34 VDD_A34
A53 VDD_A53
A68 VDD_A68
B15 VDD_B15
B28 VDD_B28
B43 VDD_B43
B56 VDD_B56
POWER
OTP_VDDIO B32
PCU_VDDIO B4
PCU_VDD B5
PCU_GATE B3
PCU_WAKE B2
PCU_CLK B6
PLL_AVDD A38
PLL_AVGND A37
GND_A1 A1
GND_A18 A18
GND_A52 A52
GND_PAD GND
+3V3
+1V0
CLK
2R2 R48
C13 0.1uF

U40C
XS1_L2-QFN124
XCORE0 IO

X0D00 A15
X0D01 A16 X0_XLA_4o
X0D02 A5 X0_XLA_3o
X0D03 A6 X0_XLA_2o
X0D04 A7 X0_XLA_1o
X0D05 A8 X0_XLA_0o
X0D06 A9 X0_XLA_0i
X0D07 A10 X0_XLA_1i
X0D08 A11 X0_XLA_2i
X0D09 A12 X0_XLA_3i
X0D10 A13 X0_XLA_4i
X0D11 A14
X0D12 A55
X0D13 A57 X0_XLB_4o
X0D14 A58 X0_XLB_3o
X0D15 A59 X0_XLB_2o
X0D16 A60 X0_XLB_1o
X0D17 A61 X0_XLB_0o
X0D18 A63 X0_XLB_0i
X0D19 A64 X0_XLB_1i
X0D20 A65 X0_XLB_2i
X0D21 A66 X0_XLB_3i
X0D22 A56 X0_XLB_4i
X0D23 A62
X0D24 A54
X0D25 A67 C0_LED
X0D26 B38
X0D27 B39
X0D28 B40
X0D29 B41
X0D30 B44
X0D31 B45
X0D32 B46
X0D33 B47
X0D34 A4
X0D35 A3
X0D36 B48
X0D37 B49
X0D38 B50
X0D39 B51
X0D40 B52
X0D41 B53
X0D42 B54
X0D43 B55

U40D
XS1_L2-QFN124
XCORE1 IO

X1D00 A39
X1D01 A40 X1_XLA_4o
X1D02 A41 X1_XLA_3o
X1D03 A42 X1_XLA_2o
X1D04 A43 X1_XLA_1o
X1D05 A44 X1_XLA_0o
X1D06 A45 X1_XLA_0i
X1D07 A46 X1_XLA_1i
X1D08 A47 X1_XLA_2i
X1D09 A48 X1_XLA_3i
X1D10 A49 X1_XLA_4i
X1D11 A50 BL_P1D
X1D12 A21 BL_P1E
X1D13 A23 X1_XLB_4o
X1D14 A24 X1_XLB_3o
X1D15 A25 X1_XLB_2o
X1D16 A26 X1_XLB_1o
X1D17 A27 X1_XLB_0o
X1D18 A29 X1_XLB_0i
X1D19 A30 X1_XLB_1i
X1D20 A31 X1_XLB_2i
X1D21 A32 X1_XLB_3i
X1D22 A22 X1_XLB_4i
X1D23 A28 BL_P1H
X1D24 A20 BL_P1I
X1D25 A33 BL_P1J
X1D26 B16
X1D27 B17
X1D28 B18 LED_0
X1D29 B19 LED_1
X1D30 B20 LED_2
X1D31 B21 LED_3
X1D32 B22
X1D33 B23
X1D34 B24
X1D35 B25
X1D36 B26
X1D37 B27 BL_P1N
X1D38 B30
X1D39 B31

LED_ARRAY
LED_0
LED_1
LED_2
LED_3
C0_LED
433R R44 E D2
433R R45 N D3
433R R46 S D4
433R R47 W D5
433R R102 D37

Decoupling Caps
+1V0
C14 100nF
C15 100nF
C16 100nF
C17 100nF
C18 10uF
+3V3
C19 100nF
C20 100nF
C21 100nF
C22 100nF
C23 10uF

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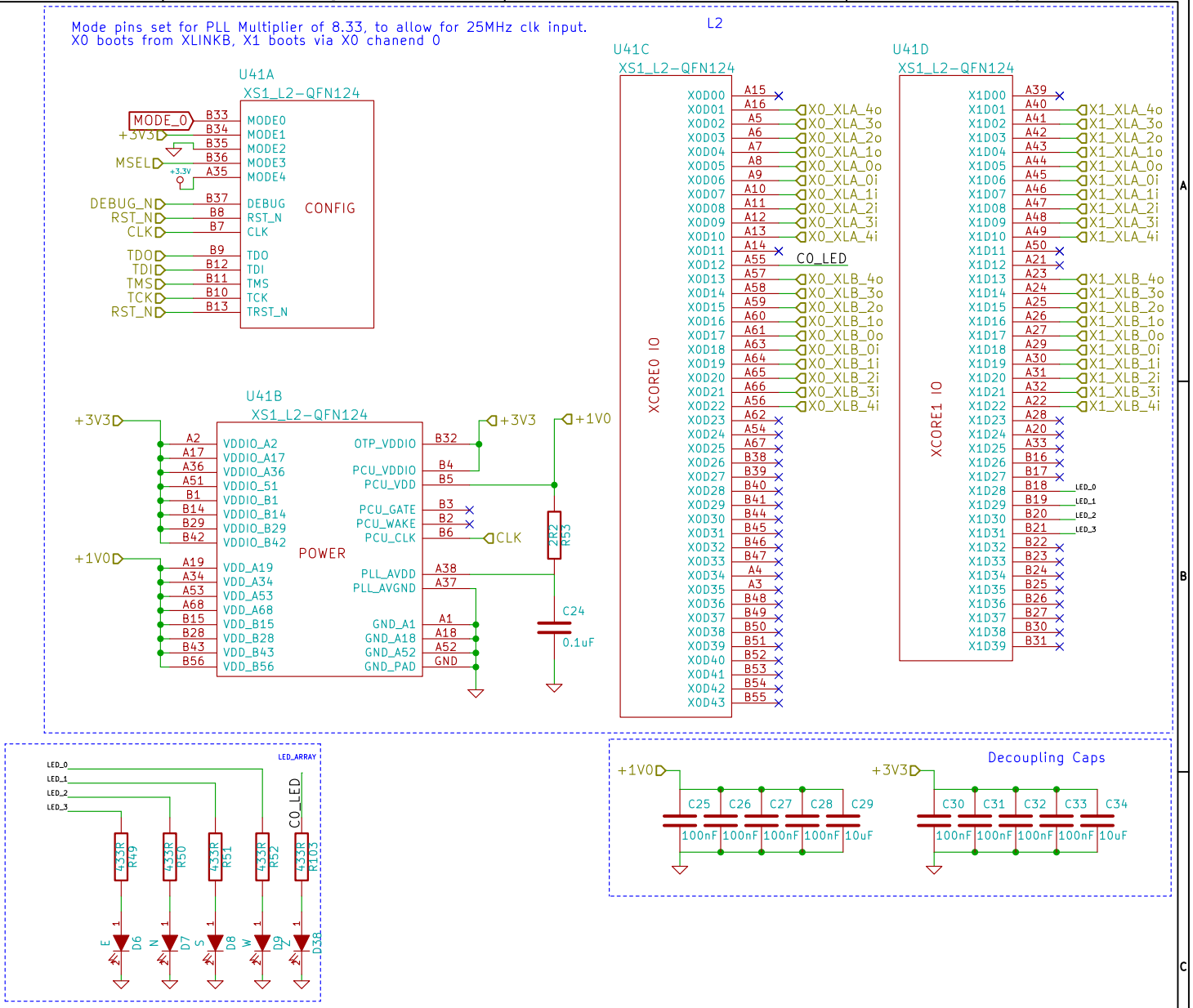
Size: A4	Date: 28 oct 2012	Rev:
KiCad E.D.A.		Id: 3/13



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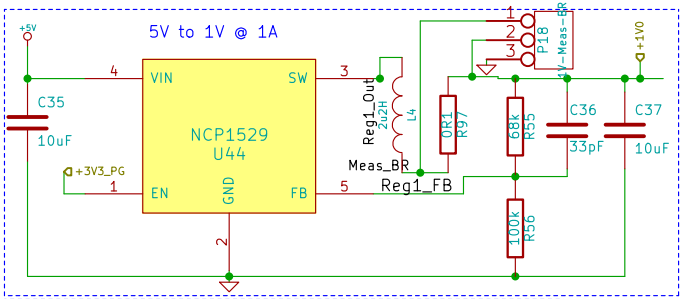
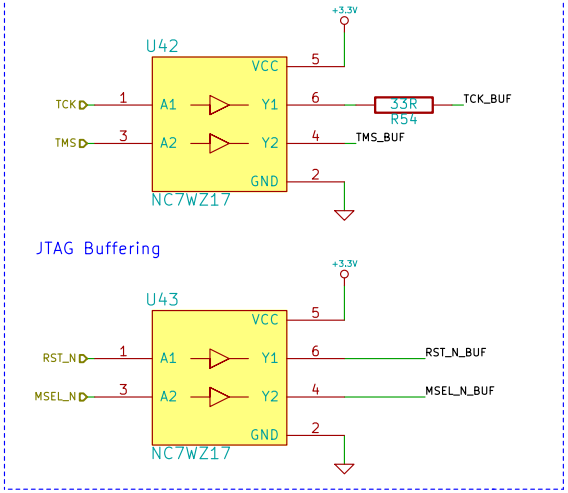
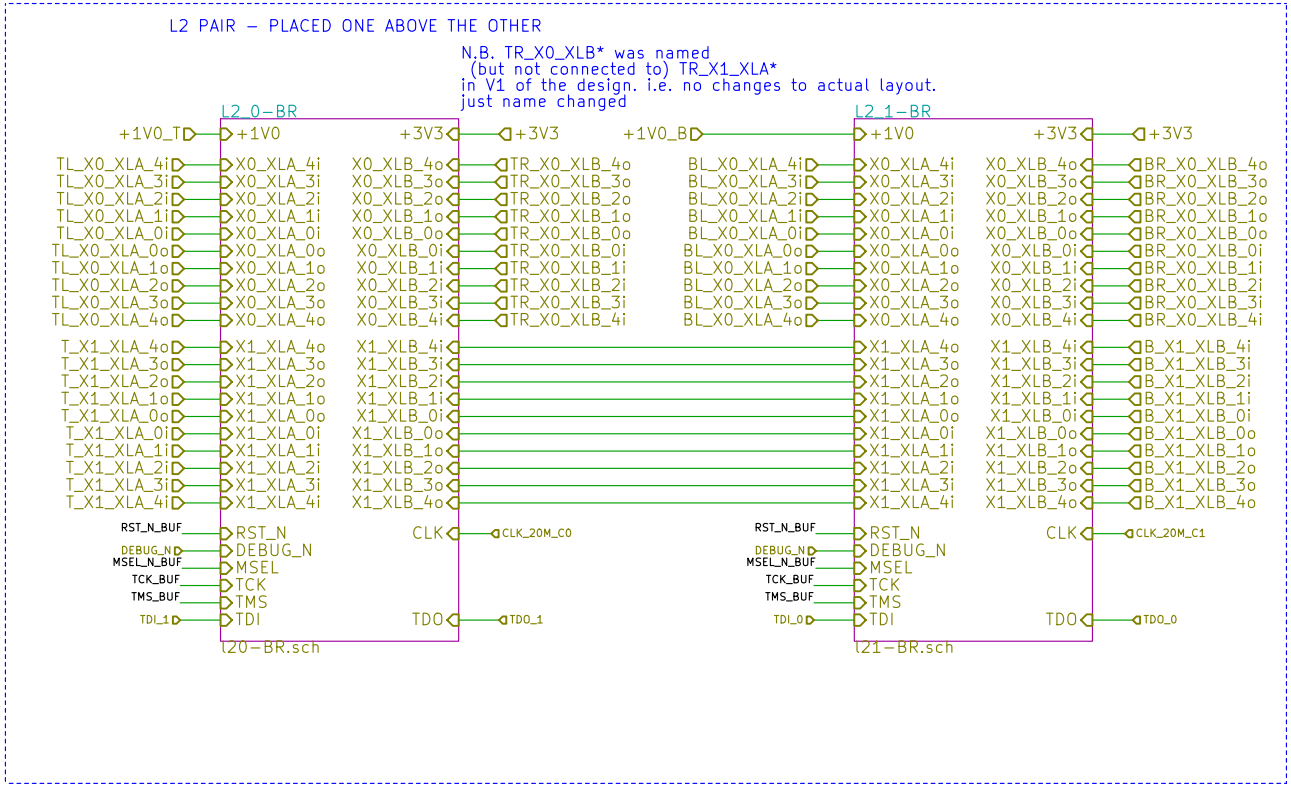
KiCad E.D.A.		Id: 4/13







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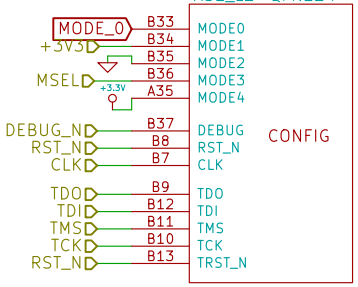
KiCad E.D.A.		Id: 5/13

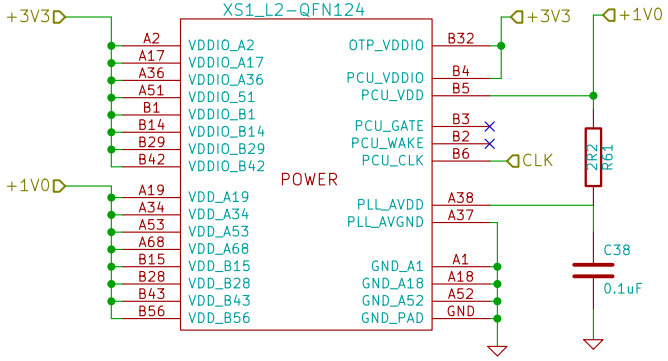
Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0

L2

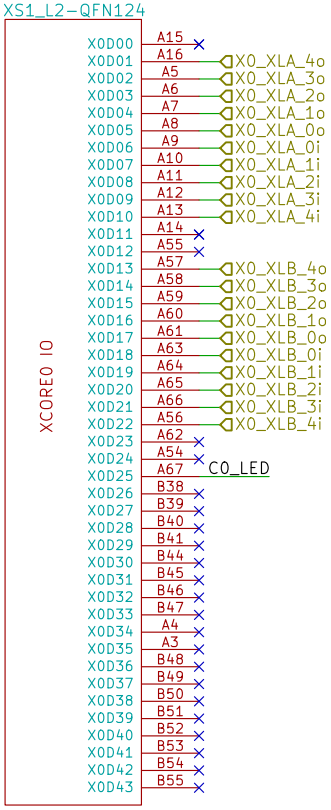
U45A
XS1_L2-QFN124



U45B
XS1_L2-QFN124



U45C
XS1_L2-QFN124



U45D
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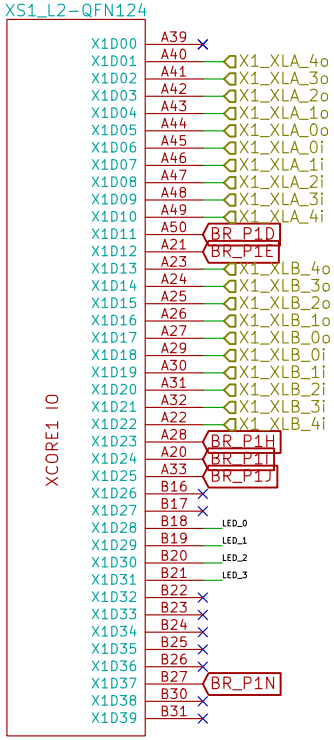

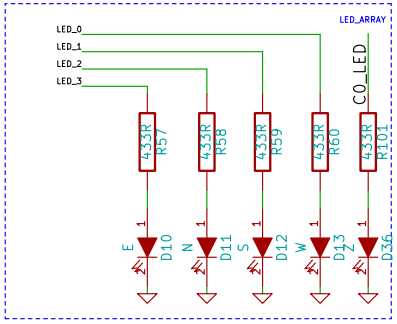

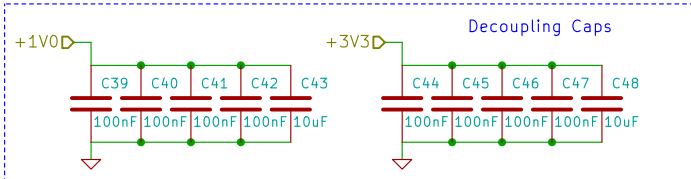

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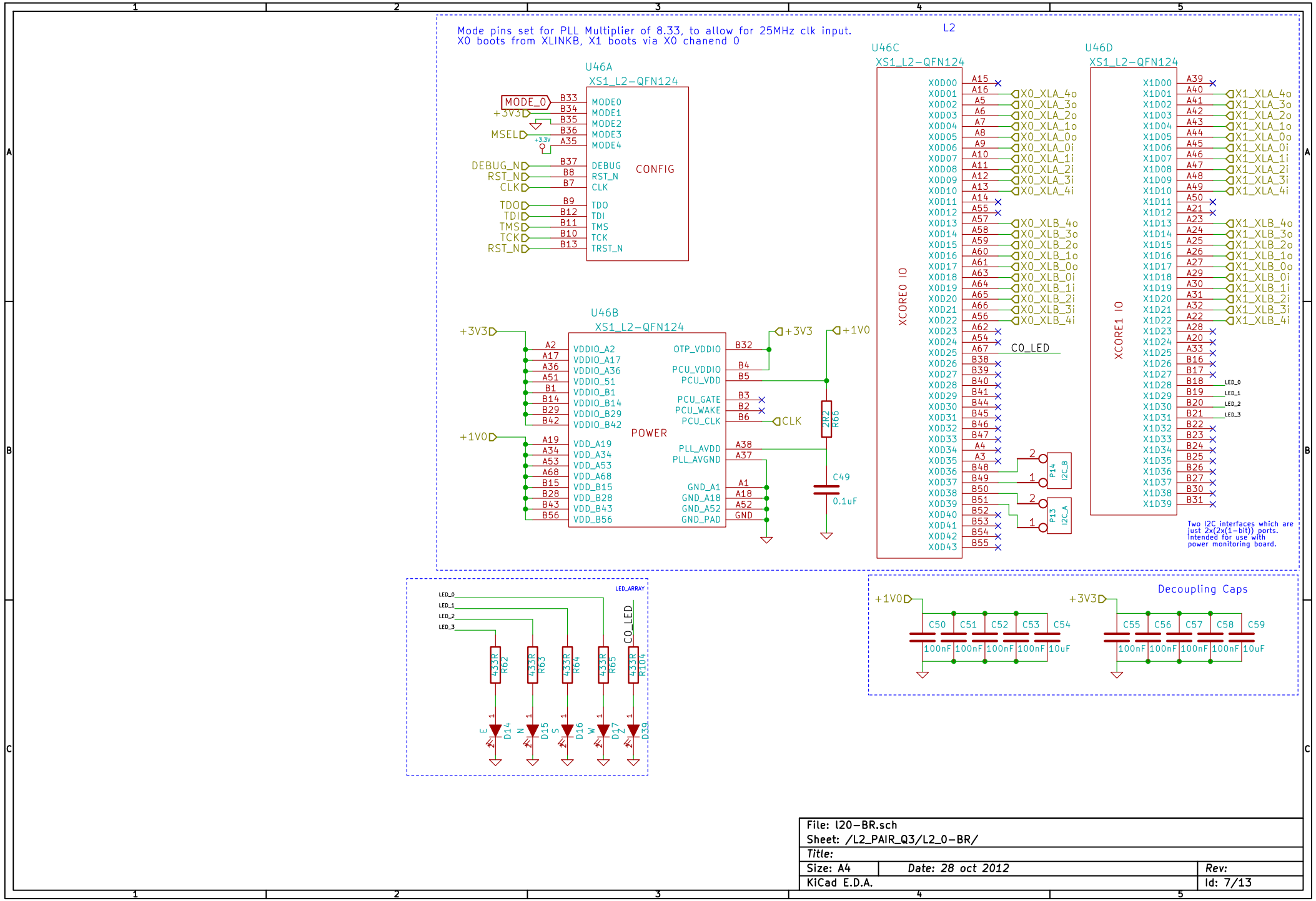

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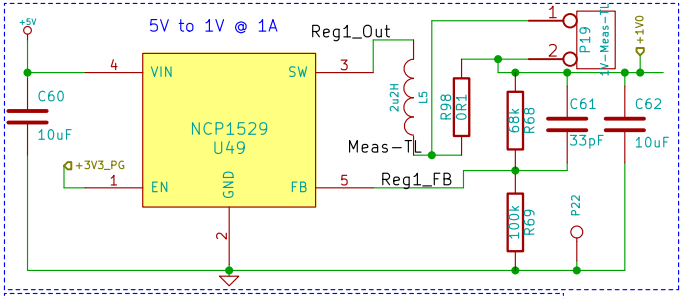
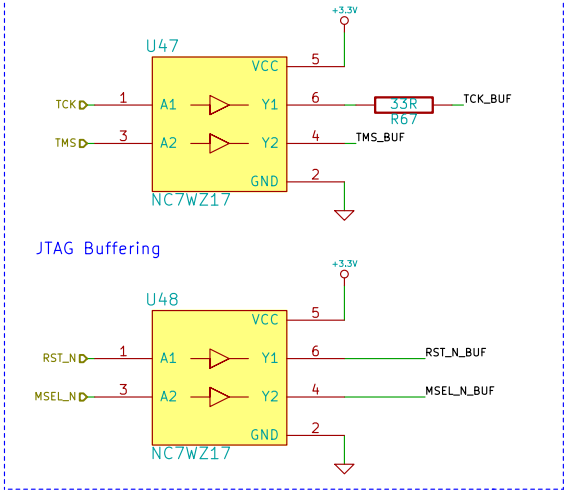
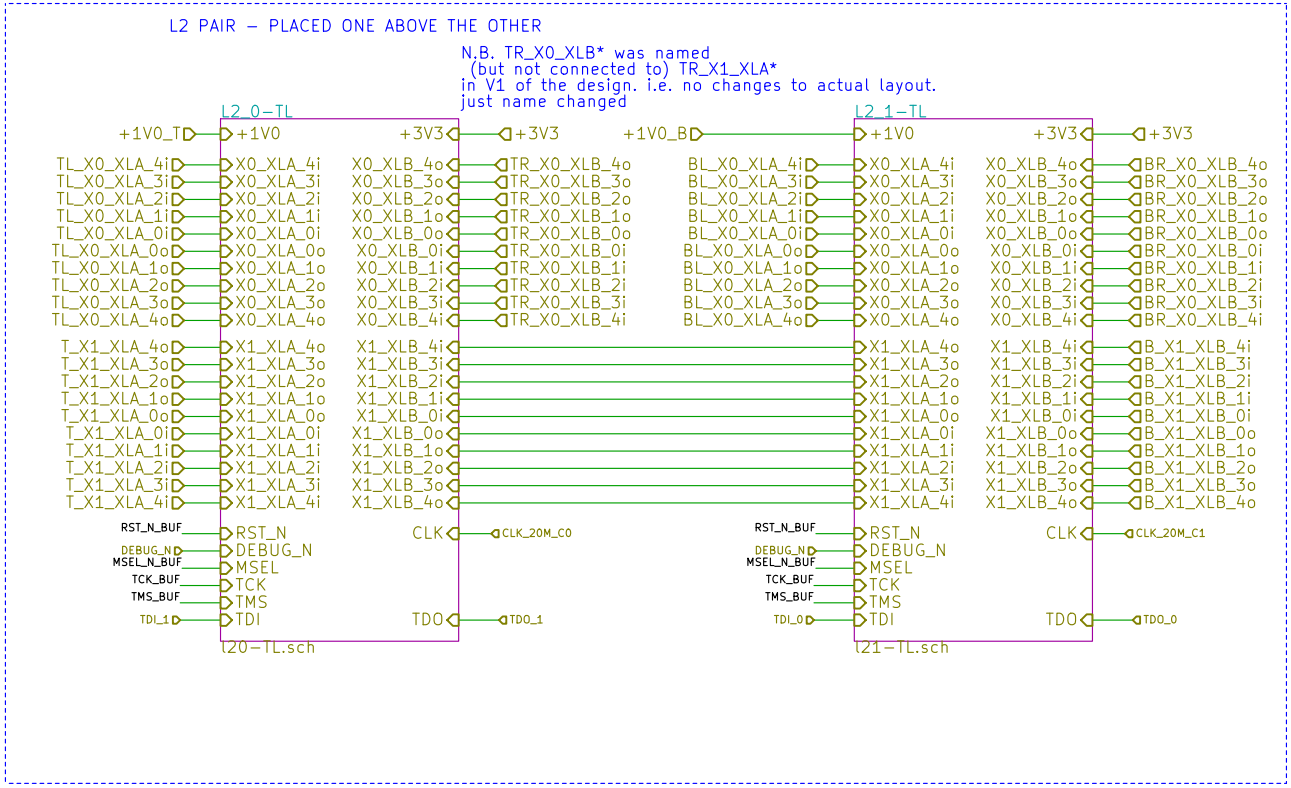
KiCad E.D.A.		Id: 7/13







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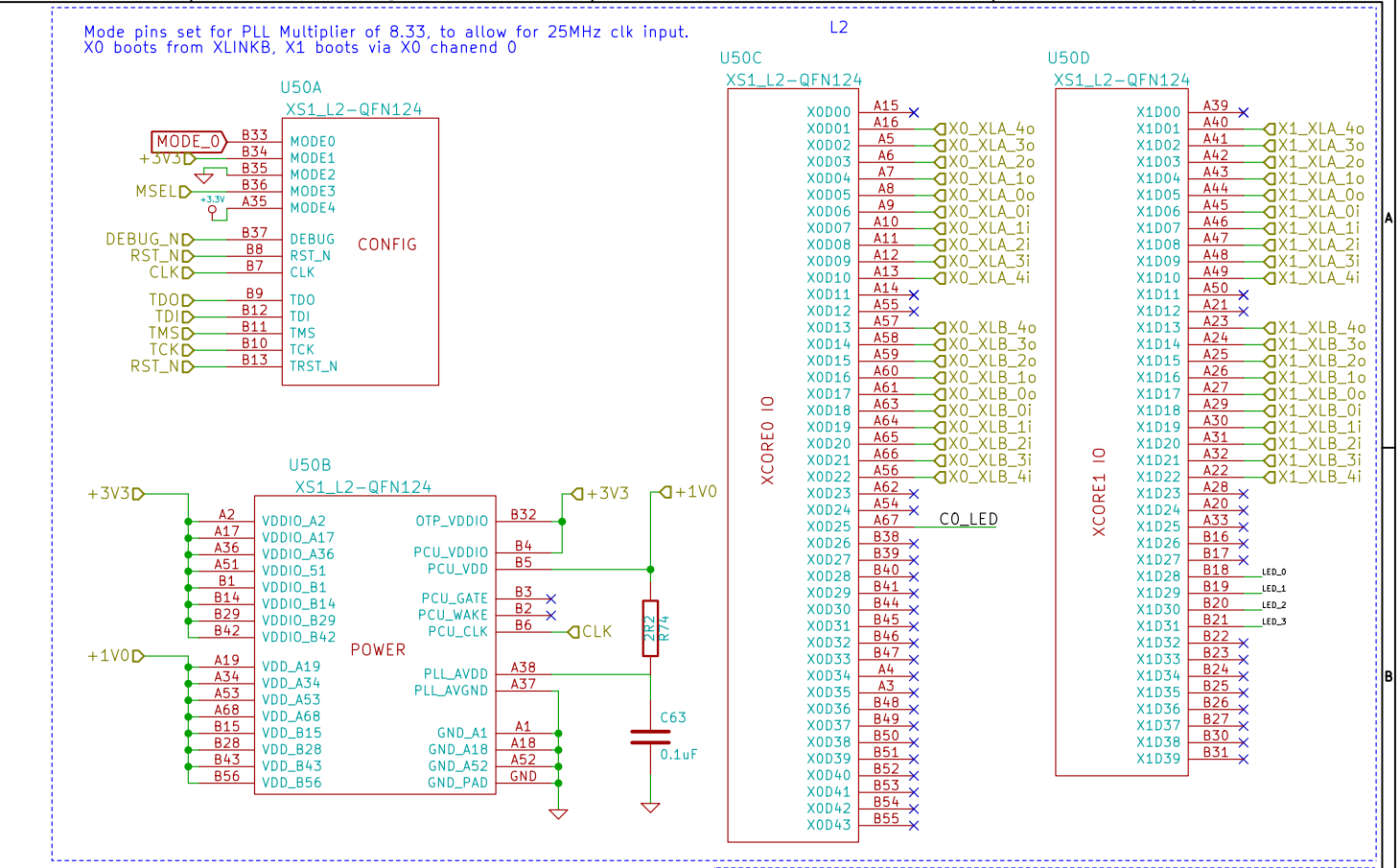

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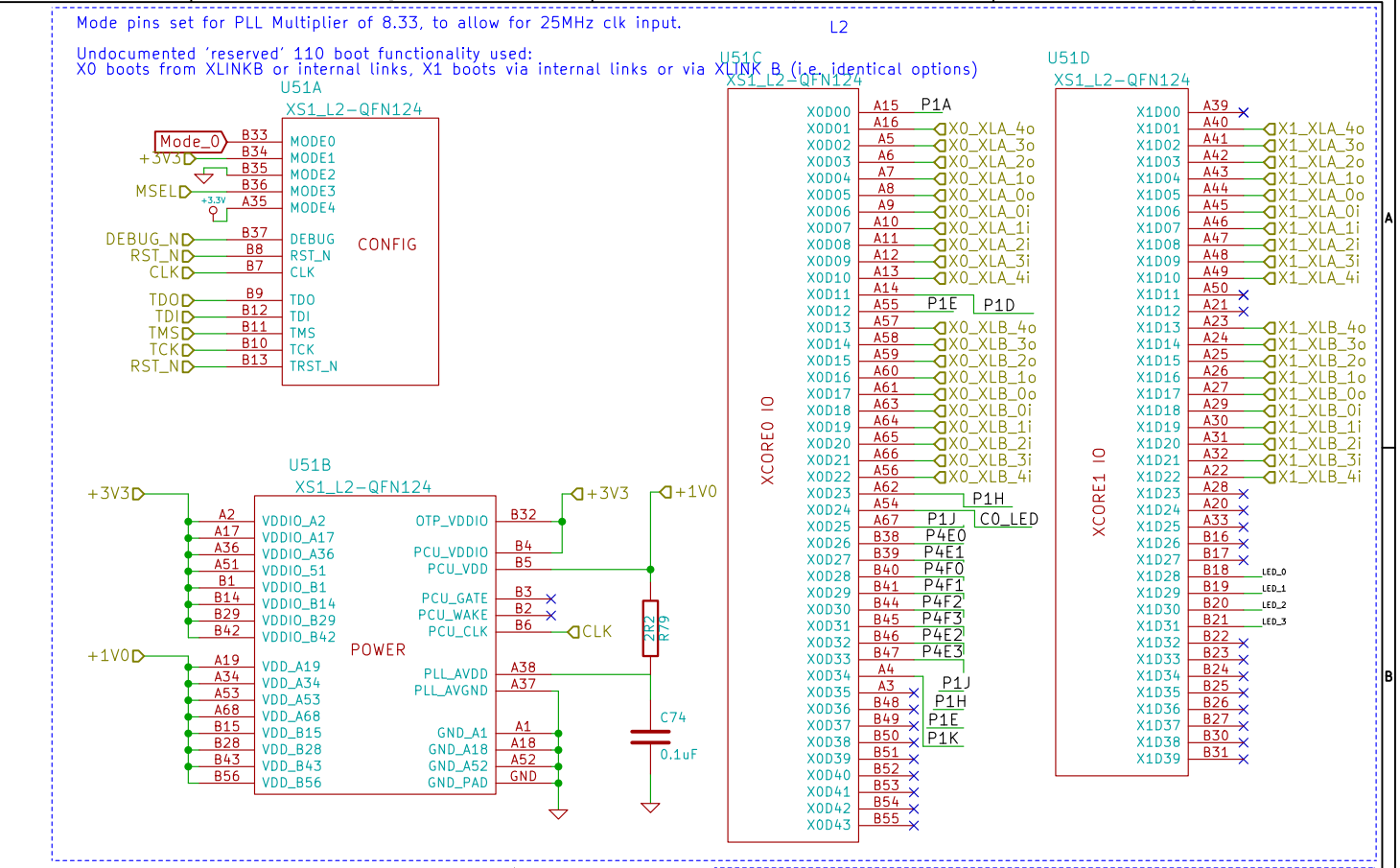
KiCad E.D.A.		Id: 9/13



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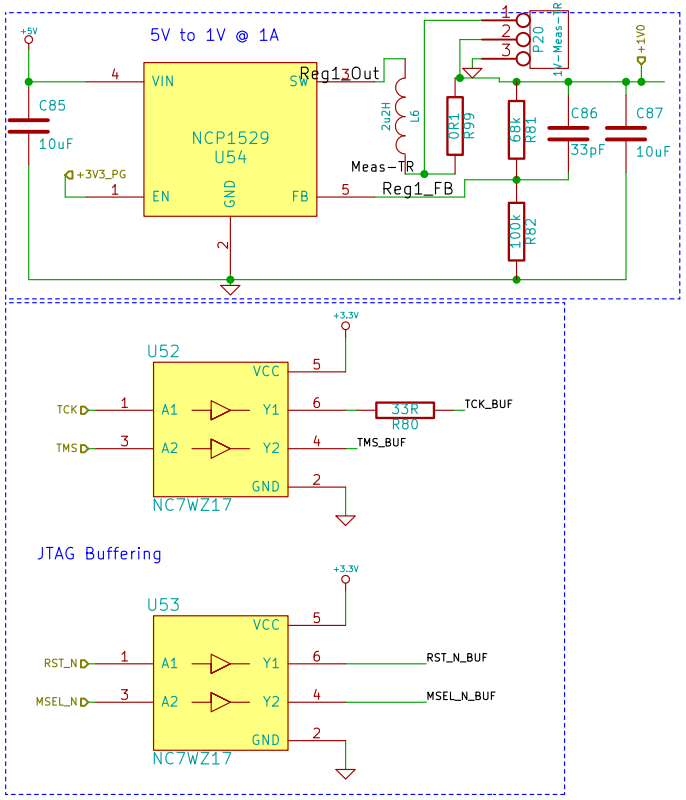

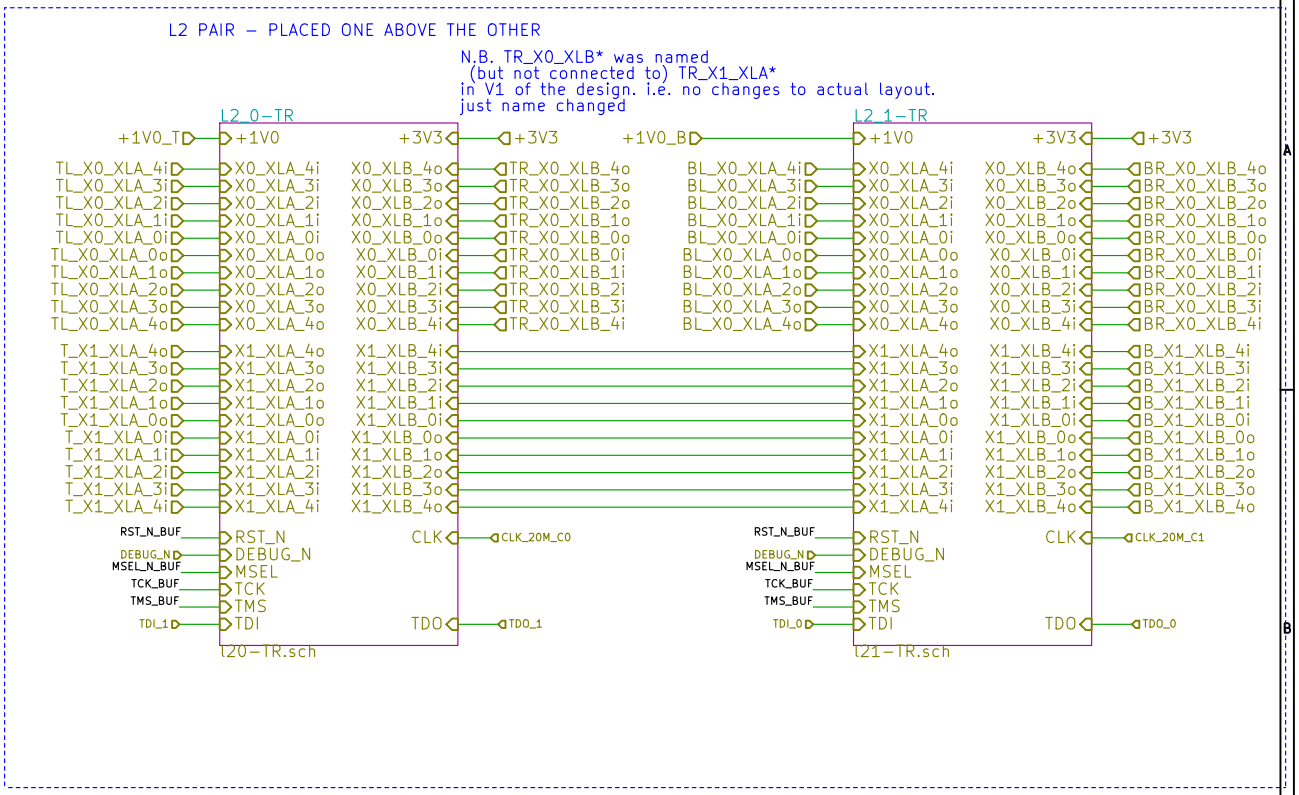

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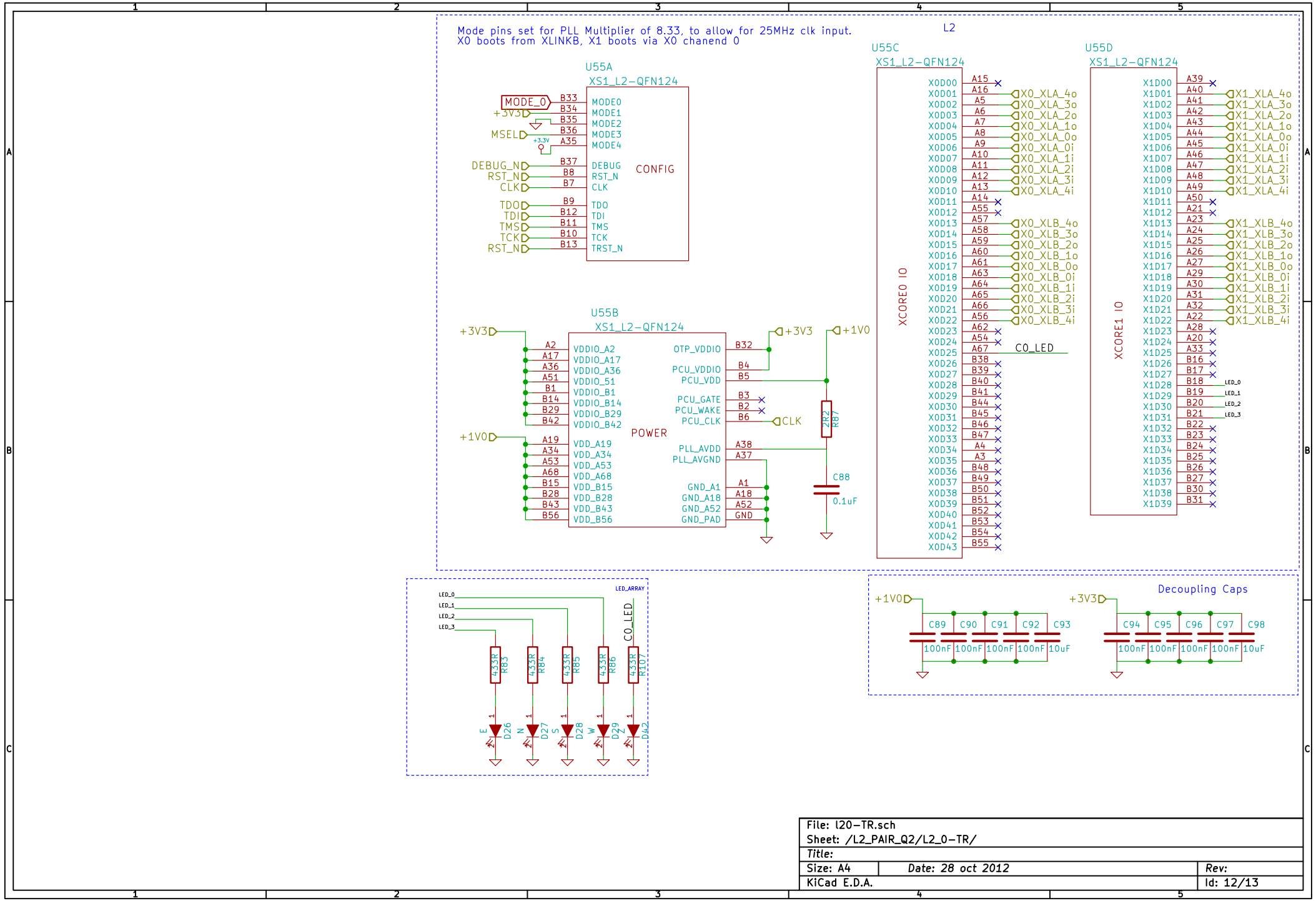

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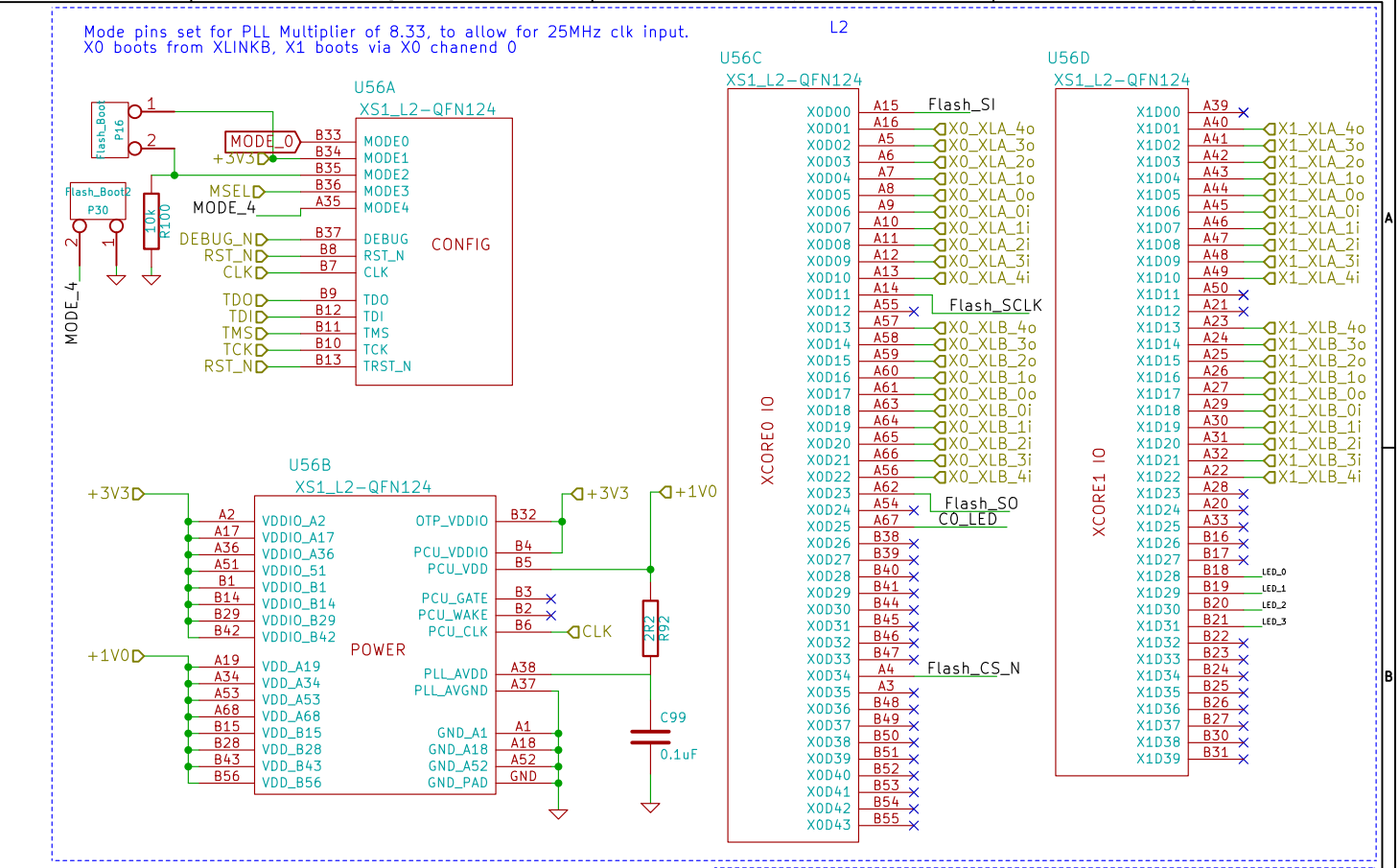

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