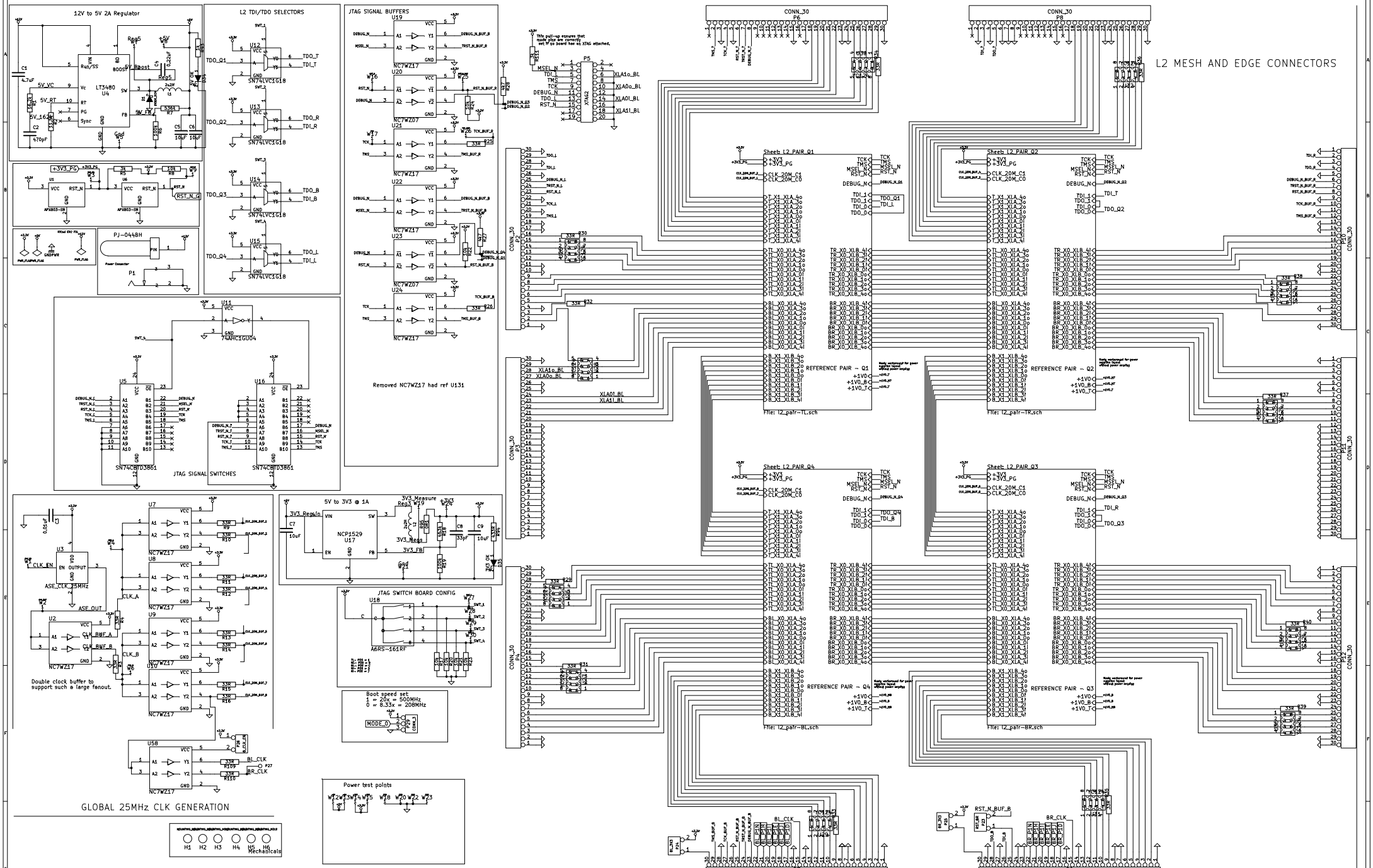
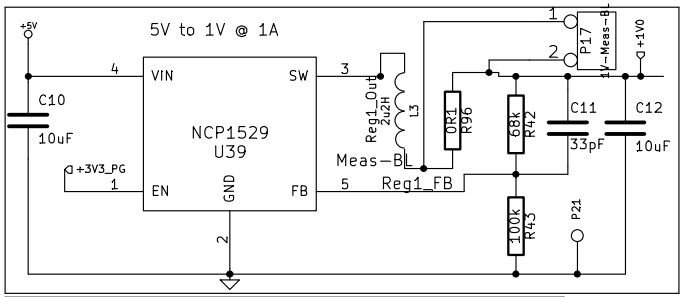
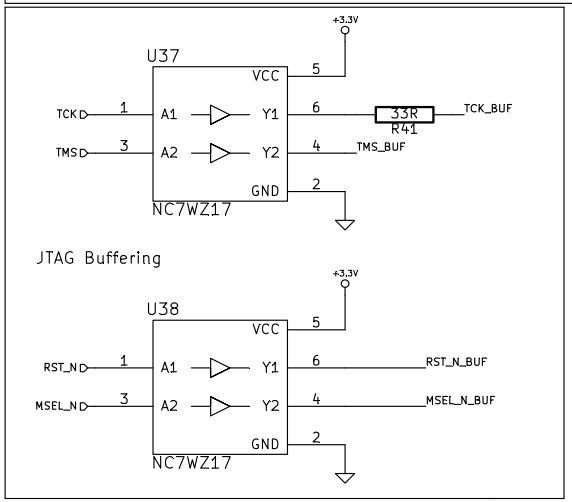
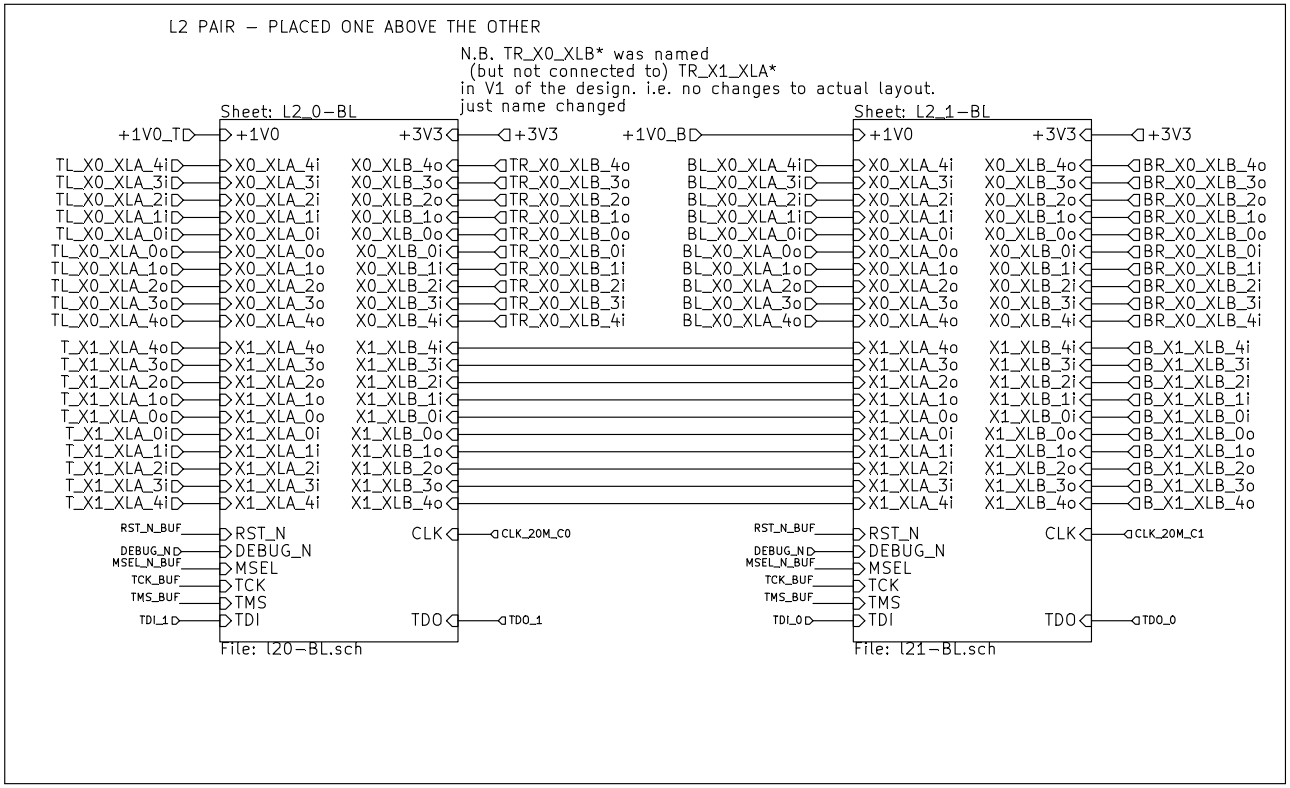
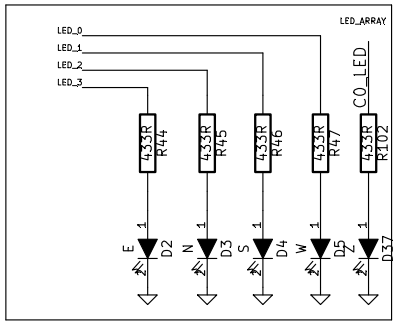

12V to 5V 2A Regulator
L2 TDI/TDO SELECTORS
JTAG SIGNAL BUFFERS
L2 MESH AND EDGE CONNECTORS
JTAG SIGNAL SWITCHES
GLOBAL 25MHz CLK GENERATION
Power test points
Removed NC7WZ17 had ref U131
Double clock buffer to support such a large fanout.
Boot speed set
1 = 20x = 500MHz
0 = 8.33x = 208MHz
Mechanicals
Swallow V2
Design by: Simon Hollis (simon@cs.bris.ac.uk) University of Bristol, Sept. 2012.
Based on XMP16-03 design by University of Bristol and XMOS Ltd 2011.

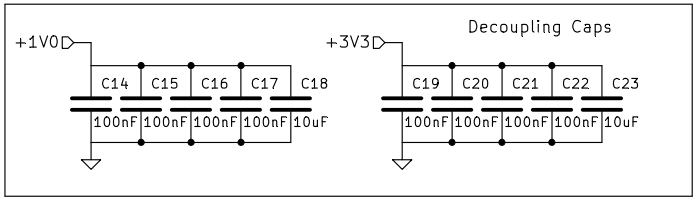



| | | |
|---|---|---|
| File: l2_pair-BL.sch | | |
| Sheet: /L2_PAIR_Q4/ | | |
| **Title:** | | |
| Size: A4 | Date: 26 sep 2012 | **Rev:** |
| KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable | | Id: 2/13 |




Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0

L2

U40A
XS1_L2-QFN124

MODE_0 B33 MODE0
+3V3 B34 MODE1
B35 MODE2
MSEL B36 MODE3
+3.3V A35 MODE4
DEBUG_N B37 DEBUG
RST_N B8 RST_N
CLK B7 CLK
CONFIG
TDO B9 TDO
TDI B12 TDI
TMS B11 TMS
TCK B10 TCK
RST_N B13 TRST_N

U40B
XS1_L2-QFN124

+3V3 A2 VDDIO_A2
A17 VDDIO_A17
A36 VDDIO_A36
A51 VDDIO_51
B1 VDDIO_B1
B14 VDDIO_B14
B29 VDDIO_B29
B42 VDDIO_B42
+1V0 A19 VDD_A19
A34 VDD_A34
A53 VDD_A53
A68 VDD_A68
B15 VDD_B15
B28 VDD_B28
B43 VDD_B43
B56 VDD_B56
POWER
OTP_VDDIO B32
PCU_VDDIO B4
PCU_VDD B5
PCU_GATE B3
PCU_WAKE B2
PCU_CLK B6
PLL_AVDD A38
PLL_AVGND A37
GND_A1 A1
GND_A18 A18
GND_A52 A52
GND_PAD GND
+3V3
+1V0
2R2 R48
CLK
C13 0.1uF

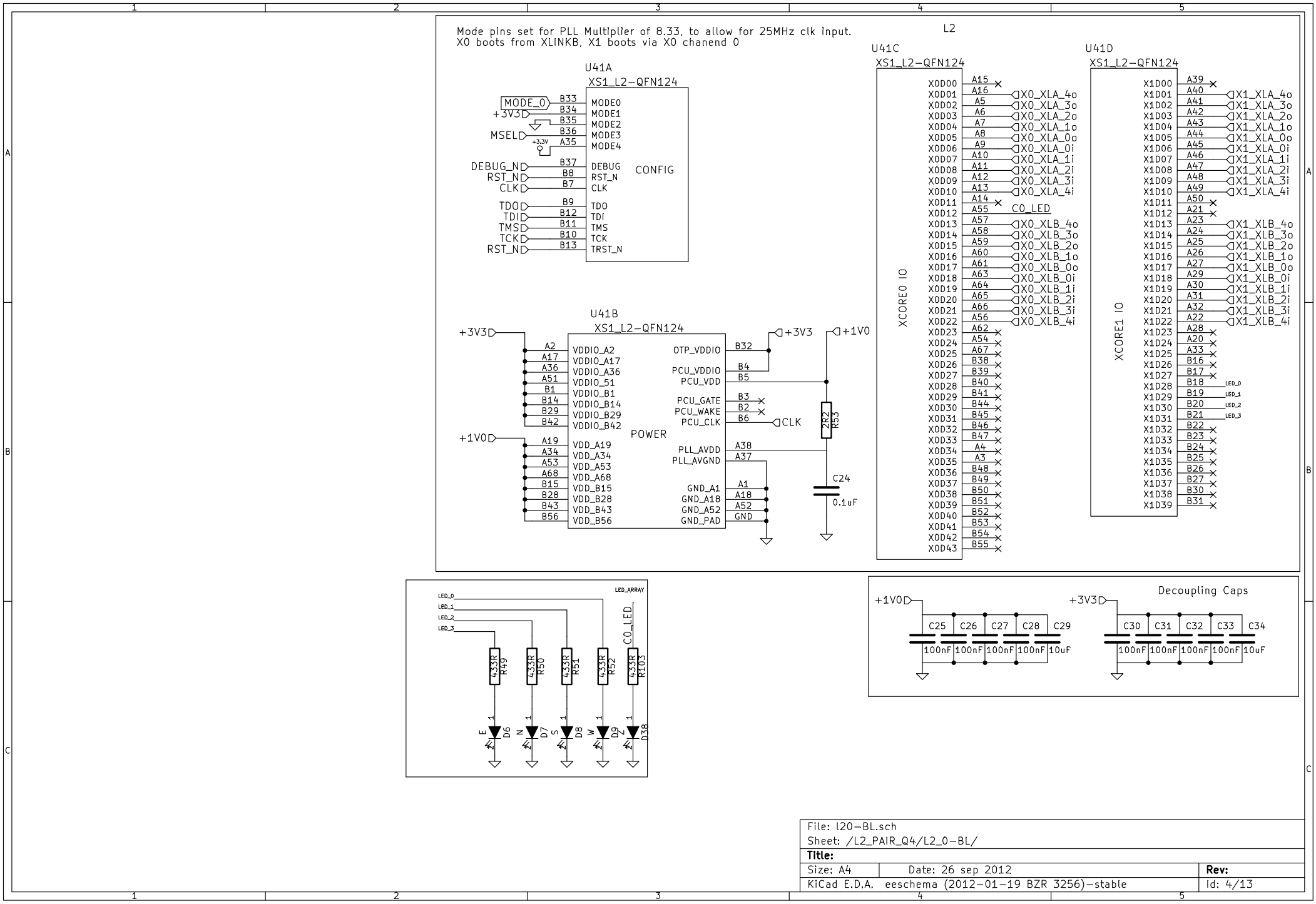
U40C
XS1_L2-QFN124

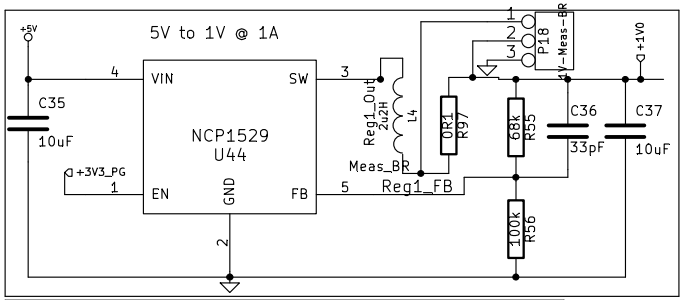
XCORE0 IO
X0D00 A15
X0D01 A16 X0_XLA_4o
X0D02 A5 X0_XLA_3o
X0D03 A6 X0_XLA_2o
X0D04 A7 X0_XLA_1o
X0D05 A8 X0_XLA_0o
X0D06 A9 X0_XLA_0i
X0D07 A10 X0_XLA_1i
X0D08 A11 X0_XLA_2i
X0D09 A12 X0_XLA_3i
X0D10 A13 X0_XLA_4i
X0D11 A14
X0D12 A55
X0D13 A57 X0_XLB_4o
X0D14 A58 X0_XLB_3o
X0D15 A59 X0_XLB_2o
X0D16 A60 X0_XLB_1o
X0D17 A61 X0_XLB_0o
X0D18 A63 X0_XLB_0i
X0D19 A64 X0_XLB_1i
X0D20 A65 X0_XLB_2i
X0D21 A66 X0_XLB_3i
X0D22 A56 X0_XLB_4i
X0D23 A62
X0D24 A54
X0D25 A67 C0_LED
X0D26 B38
X0D27 B39
X0D28 B40
X0D29 B41
X0D30 B44
X0D31 B45
X0D32 B46
X0D33 B47
X0D34 A4
X0D35 A3
X0D36 B48
X0D37 B49
X0D38 B50
X0D39 B51
X0D40 B52
X0D41 B53
X0D42 B54
X0D43 B55

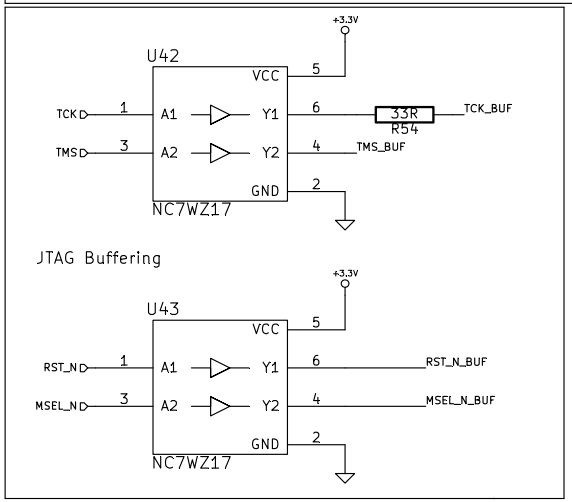
U40D
XS1_L2-QFN124

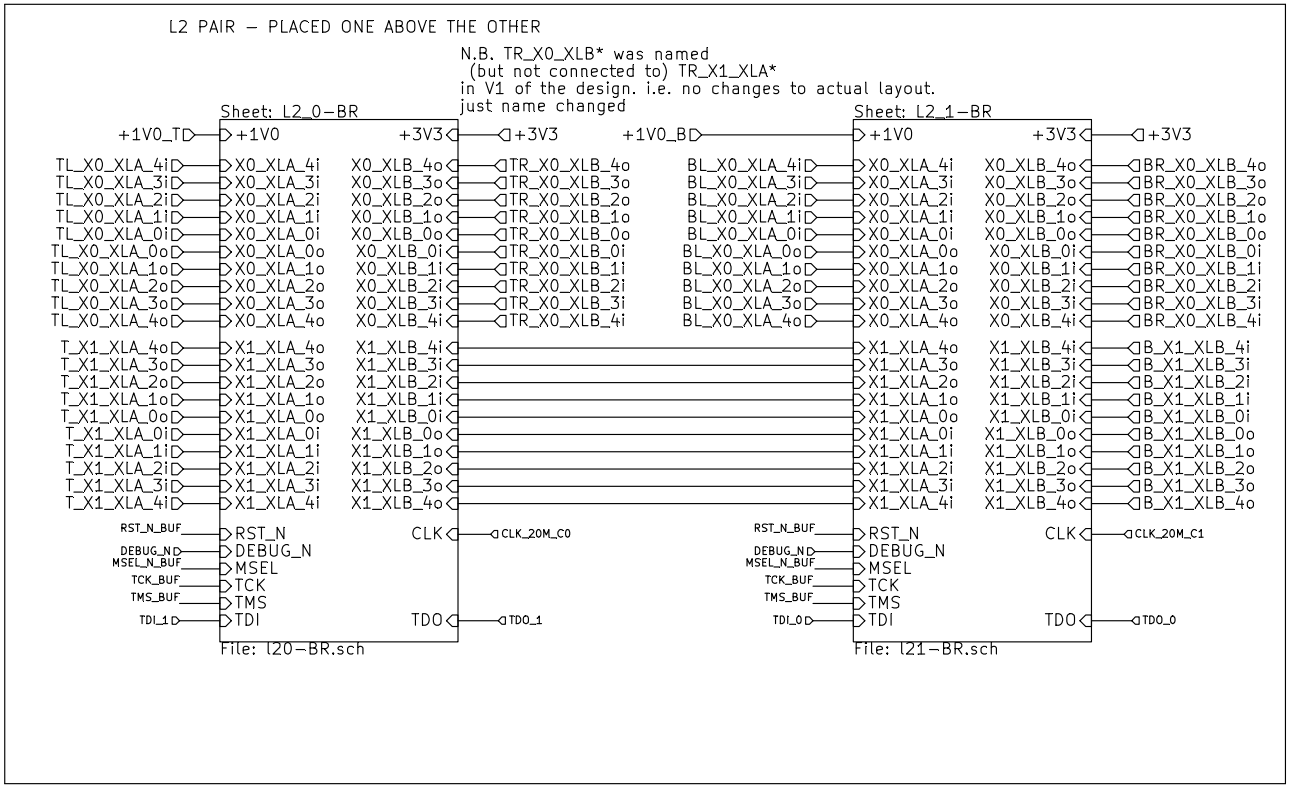
XCORE1 IO
X1D00 A39
X1D01 A40 X1_XLA_4o
X1D02 A41 X1_XLA_3o
X1D03 A42 X1_XLA_2o
X1D04 A43 X1_XLA_1o
X1D05 A44 X1_XLA_0o
X1D06 A45 X1_XLA_0i
X1D07 A46 X1_XLA_1i
X1D08 A47 X1_XLA_2i
X1D09 A48 X1_XLA_3i
X1D10 A49 X1_XLA_4i
X1D11 A50 BL_P1D
X1D12 A21 BL_P1E
X1D13 A23 X1_XLB_4o
X1D14 A24 X1_XLB_3o
X1D15 A25 X1_XLB_2o
X1D16 A26 X1_XLB_1o
X1D17 A27 X1_XLB_0o
X1D18 A29 X1_XLB_0i
X1D19 A30 X1_XLB_1i
X1D20 A31 X1_XLB_2i
X1D21 A32 X1_XLB_3i
X1D22 A22 X1_XLB_4i
X1D23 A28 BL_P1H
X1D24 A20 BL_P1I
X1D25 A33 BL_P1J
X1D26 B16
X1D27 B17
X1D28 B18 LED_0
X1D29 B19 LED_1
X1D30 B20 LED_2
X1D31 B21 LED_3
X1D32 B22
X1D33 B23
X1D34 B24
X1D35 B25
X1D36 B26
X1D37 B27 BL_P1N
X1D38 B30
X1D39 B31

| | | |
|---|---|---|
| File: l21-BL.sch | | |
| Sheet: /L2_PAIR_Q4/L2_1-BL/ | | |
| **Title:** | | |
| Size: A4 | Date: 26 sep 2012 | **Rev:** |
| KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable | | Id: 3/13 |

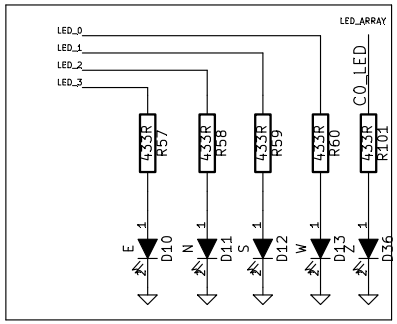

Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0
L2
U41A
XS1_L2-QFN124
MODE_0
+3V3
MSEL
DEBUG_N
RST_N
CLK
TDO
TDI
TMS
TCK
RST_N
MODE0
MODE1
MODE2
MODE3
MODE4
DEBUG
RST_N
CLK
TDO
TDI
TMS
TCK
TRST_N
CONFIG
U41B
XS1_L2-QFN124
+3V3
+1V0
VDDIO_A2
VDDIO_A17
VDDIO_A36
VDDIO_51
VDDIO_B1
VDDIO_B14
VDDIO_B29
VDDIO_B42
VDD_A19
VDD_A34
VDD_A53
VDD_A68
VDD_B15
VDD_B28
VDD_B43
VDD_B56
OTP_VDDIO
PCU_VDDIO
PCU_VDD
PCU_GATE
PCU_WAKE
PCU_CLK
PLL_AVDD
PLL_AVGND
GND_A1
GND_A18
GND_A52
GND_PAD
POWER
CLK
2R2
R53
C24
0.1uF
U41C
XS1_L2-QFN124
XCORE0 IO
C0_LED
U41D
XS1_L2-QFN124
XCORE1 IO
LED_ARRAY
LED_0
LED_1
LED_2
LED_3
C0_LED
433R
R49
R50
R51
R52
R103
D6
D7
D8
D9
D38
E
N
S
W
Z
Decoupling Caps
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
100nF
10uF
File: l20-BL.sch
Sheet: /L2_PAIR_Q4/L2_0-BL/
Title:
Size: A4
Date: 26 sep 2012
Rev:
KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable
Id: 4/13

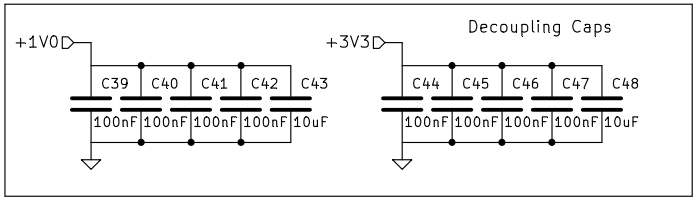



| | | |
|---|---|---|
| File: l2_pair-BR.sch | | |
| Sheet: /L2_PAIR_Q3/ | | |
| **Title:** | | |
| Size: A4 | Date: 26 sep 2012 | **Rev:** |
| KiCad E.D.A. | eeschema (2012-01-19 BZR 3256)-stable | Id: 5/13 |




Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0

L2

U45A
XS1_L2-QFN124

MODE_0 B33 MODE0
+3V3 B34 MODE1
B35 MODE2
MSEL B36 MODE3
+3.3V A35 MODE4
DEBUG_N B37 DEBUG
RST_N B8 RST_N
CLK B7 CLK
CONFIG
TDO B9 TDO
TDI B12 TDI
TMS B11 TMS
TCK B10 TCK
RST_N B13 TRST_N

U45B
XS1_L2-QFN124

+3V3 A2 VDDIO_A2
A17 VDDIO_A17
A36 VDDIO_A36
A51 VDDIO_51
B1 VDDIO_B1
B14 VDDIO_B14
B29 VDDIO_B29
B42 VDDIO_B42
+1V0 A19 VDD_A19
A34 VDD_A34
A53 VDD_A53
A68 VDD_A68
B15 VDD_B15
B28 VDD_B28
B43 VDD_B43
B56 VDD_B56
POWER
OTP_VDDIO B32
PCU_VDDIO B4
PCU_VDD B5
PCU_GATE B3
PCU_WAKE B2
PCU_CLK B6
PLL_AVDD A38
PLL_AVGND A37
GND_A1 A1
GND_A18 A18
GND_A52 A52
GND_PAD GND
+3V3
+1V0
CLK
2R2 R61
C38 0.1uF

U45C
XS1_L2-QFN124

XCORE0 IO
X0D00 A15
X0D01 A16 X0_XLA_4o
X0D02 A5 X0_XLA_3o
X0D03 A6 X0_XLA_2o
X0D04 A7 X0_XLA_1o
X0D05 A8 X0_XLA_0o
X0D06 A9 X0_XLA_0i
X0D07 A10 X0_XLA_1i
X0D08 A11 X0_XLA_2i
X0D09 A12 X0_XLA_3i
X0D10 A13 X0_XLA_4i
X0D11 A14
X0D12 A55
X0D13 A57 X0_XLB_4o
X0D14 A58 X0_XLB_3o
X0D15 A59 X0_XLB_2o
X0D16 A60 X0_XLB_1o
X0D17 A61 X0_XLB_0o
X0D18 A63 X0_XLB_0i
X0D19 A64 X0_XLB_1i
X0D20 A65 X0_XLB_2i
X0D21 A66 X0_XLB_3i
X0D22 A56 X0_XLB_4i
X0D23 A62
X0D24 A54
X0D25 A67 C0_LED
X0D26 B38
X0D27 B39
X0D28 B40
X0D29 B41
X0D30 B44
X0D31 B45
X0D32 B46
X0D33 B47
X0D34 A4
X0D35 A3
X0D36 B48
X0D37 B49
X0D38 B50
X0D39 B51
X0D40 B52
X0D41 B53
X0D42 B54
X0D43 B55

U45D
XS1_L2-QFN124

XCORE1 IO
X1D00 A39
X1D01 A40 X1_XLA_4o
X1D02 A41 X1_XLA_3o
X1D03 A42 X1_XLA_2o
X1D04 A43 X1_XLA_1o
X1D05 A44 X1_XLA_0o
X1D06 A45 X1_XLA_0i
X1D07 A46 X1_XLA_1i
X1D08 A47 X1_XLA_2i
X1D09 A48 X1_XLA_3i
X1D10 A49 X1_XLA_4i
X1D11 A50 BR_P1D
X1D12 A21 BR_P1E
X1D13 A23 X1_XLB_4o
X1D14 A24 X1_XLB_3o
X1D15 A25 X1_XLB_2o
X1D16 A26 X1_XLB_1o
X1D17 A27 X1_XLB_0o
X1D18 A29 X1_XLB_0i
X1D19 A30 X1_XLB_1i
X1D20 A31 X1_XLB_2i
X1D21 A32 X1_XLB_3i
X1D22 A22 X1_XLB_4i
X1D23 A28 BR_P1H
X1D24 A20 BR_P1I
X1D25 A33 BR_P1J
X1D26 B16
X1D27 B17
X1D28 B18 LED_0
X1D29 B19 LED_1
X1D30 B20 LED_2
X1D31 B21 LED_3
X1D32 B22
X1D33 B23
X1D34 B24
X1D35 B25
X1D36 B26
X1D37 B27 BR_P1N
X1D38 B30
X1D39 B31

| | | |
|---|---|---|
| File: l21-BR.sch | | |
| Sheet: /L2_PAIR_Q3/L2_1-BR/ | | |
| **Title:** | | |
| Size: A4 | Date: 26 sep 2012 | **Rev:** |
| KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable | | Id: 6/13 |

Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0

L2

U46A
XS1_L2-QFN124

MODE_0 B33 MODE0
+3V3 B34 MODE1
B35 MODE2
MSEL B36 MODE3
+3.3V A35 MODE4
DEBUG_N B37 DEBUG
RST_N B8 RST_N
CLK B7 CLK
CONFIG
TDO B9 TDO
TDI B12 TDI
TMS B11 TMS
TCK B10 TCK
RST_N B13 TRST_N

U46B
XS1_L2-QFN124

+3V3 A2 VDDIO_A2
A17 VDDIO_A17
A36 VDDIO_A36
A51 VDDIO_51
B1 VDDIO_B1
B14 VDDIO_B14
B29 VDDIO_B29
B42 VDDIO_B42
+1V0 A19 VDD_A19
A34 VDD_A34
A53 VDD_A53
A68 VDD_A68
B15 VDD_B15
B28 VDD_B28
B43 VDD_B43
B56 VDD_B56
POWER
OTP_VDDIO B32
PCU_VDDIO B4
PCU_VDD B5
PCU_GATE B3
PCU_WAKE B2
PCU_CLK B6
PLL_AVDD A38
PLL_AVGND A37
GND_A1 A1
GND_A18 A18
GND_A52 A52
GND_PAD GND
+3V3
+1V0
CLK
2R2 R66
C49 0.1uF

U46C
XS1_L2-QFN124

XCORE0 IO
X0D00 A15
X0D01 A16 X0_XLA_4o
X0D02 A5 X0_XLA_3o
X0D03 A6 X0_XLA_2o
X0D04 A7 X0_XLA_1o
X0D05 A8 X0_XLA_0o
X0D06 A9 X0_XLA_0i
X0D07 A10 X0_XLA_1i
X0D08 A11 X0_XLA_2i
X0D09 A12 X0_XLA_3i
X0D10 A13 X0_XLA_4i
X0D11 A14
X0D12 A55
X0D13 A57 X0_XLB_4o
X0D14 A58 X0_XLB_3o
X0D15 A59 X0_XLB_2o
X0D16 A60 X0_XLB_1o
X0D17 A61 X0_XLB_0o
X0D18 A63 X0_XLB_0i
X0D19 A64 X0_XLB_1i
X0D20 A65 X0_XLB_2i
X0D21 A66 X0_XLB_3i
X0D22 A56 X0_XLB_4i
X0D23 A62
X0D24 A54
X0D25 A67 C0_LED
X0D26 B38
X0D27 B39
X0D28 B40
X0D29 B41
X0D30 B44
X0D31 B45
X0D32 B46
X0D33 B47
X0D34 A4
X0D35 A3
X0D36 B48
X0D37 B49
X0D38 B50
X0D39 B51
X0D40 B52
X0D41 B53
X0D42 B54
X0D43 B55
P14 I2C_B
P13 I2C_A

U46D
XS1_L2-QFN124

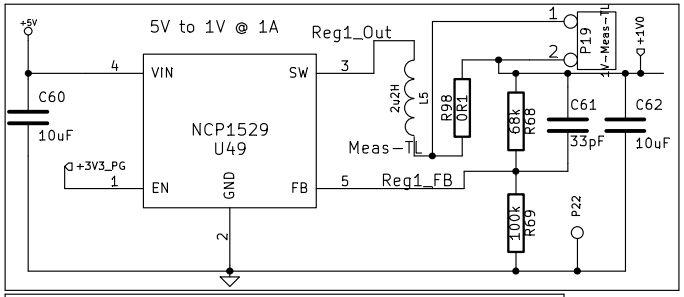
XCORE1 IO
X1D00 A39
X1D01 A40 X1_XLA_4o
X1D02 A41 X1_XLA_3o
X1D03 A42 X1_XLA_2o
X1D04 A43 X1_XLA_1o
X1D05 A44 X1_XLA_0o
X1D06 A45 X1_XLA_0i
X1D07 A46 X1_XLA_1i
X1D08 A47 X1_XLA_2i
X1D09 A48 X1_XLA_3i
X1D10 A49 X1_XLA_4i
X1D11 A50
X1D12 A21
X1D13 A23 X1_XLB_4o
X1D14 A24 X1_XLB_3o
X1D15 A25 X1_XLB_2o
X1D16 A26 X1_XLB_1o
X1D17 A27 X1_XLB_0o
X1D18 A29 X1_XLB_0i
X1D19 A30 X1_XLB_1i
X1D20 A31 X1_XLB_2i
X1D21 A32 X1_XLB_3i
X1D22 A22 X1_XLB_4i
X1D23 A28
X1D24 A20
X1D25 A33
X1D26 B16
X1D27 B17
X1D28 B18 LED_0
X1D29 B19 LED_1
X1D30 B20 LED_2
X1D31 B21 LED_3
X1D32 B22
X1D33 B23
X1D34 B24
X1D35 B25
X1D36 B26
X1D37 B27
X1D38 B30
X1D39 B31

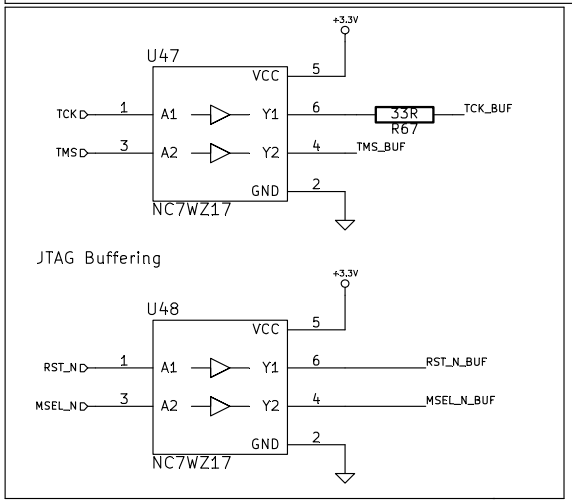
Two I2C interfaces which are just 2x(2x(1-bit)) ports. Intended for use with power monitoring board.

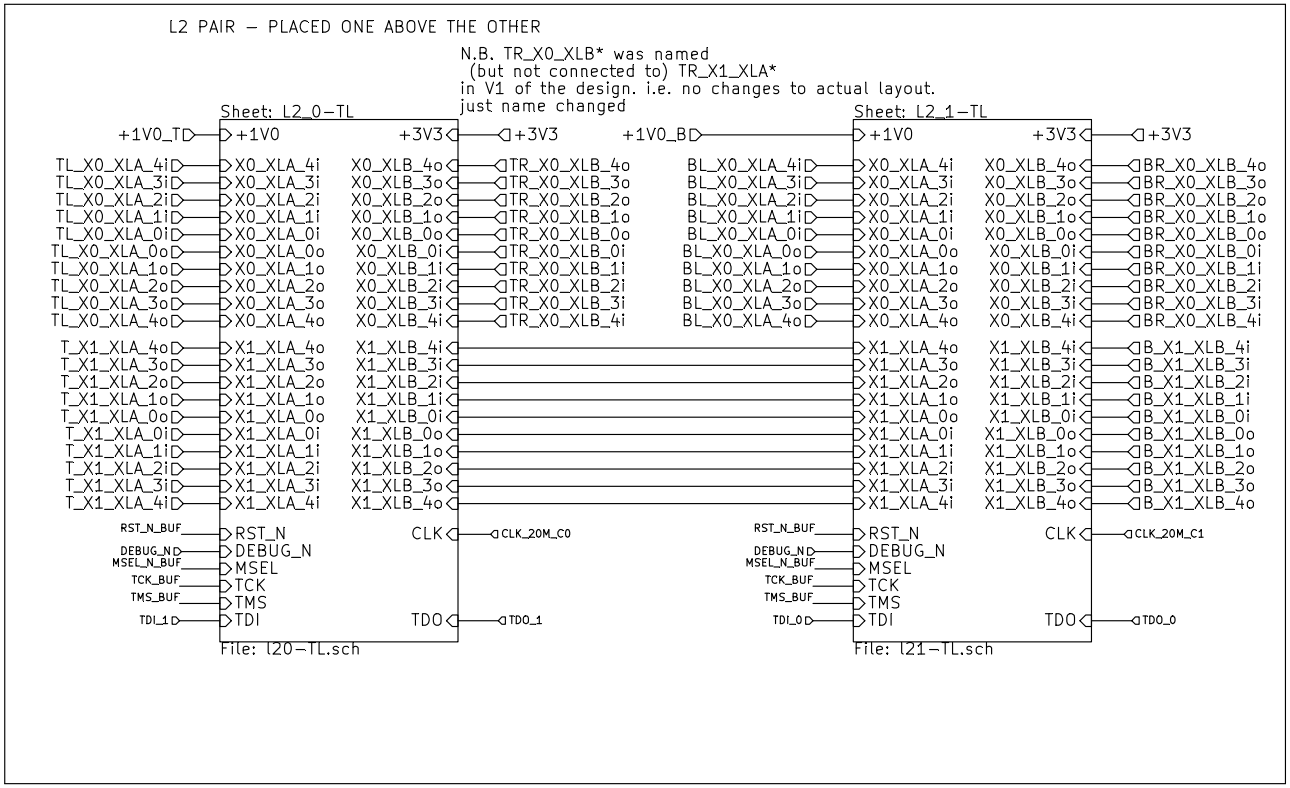
LED_ARRAY
LED_0
LED_1
LED_2
LED_3
C0_LED
433R R62 R63 R64 R65 R104
E D14
N D15
S D16
W D17
Z D39

Decoupling Caps
+1V0
C50 C51 C52 C53 C54
100nF 100nF 100nF 100nF 10uF
+3V3
C55 C56 C57 C58 C59
100nF 100nF 100nF 100nF 10uF

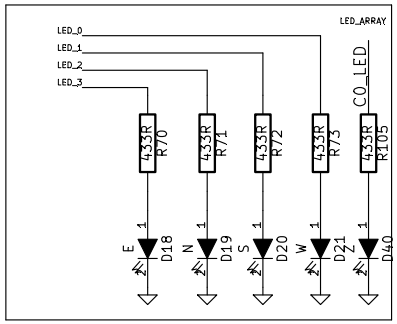
| | | |
|---|---|---|
| File: l20-BR.sch | | |
| Sheet: /L2_PAIR_Q3/L2_0-BR/ | | |
| **Title:** | | |
| Size: A4 | Date: 26 sep 2012 | **Rev:** |
| KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable | | Id: 7/13 |

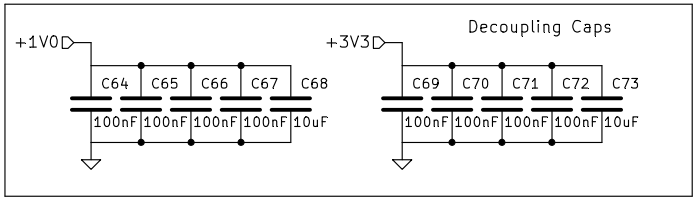



| | | |
|---|---|---|
| File: l2_pair-TL.sch | | |
| Sheet: /L2_PAIR_Q1/ | | |
| **Title:** | | |
| Size: A4 | Date: 26 sep 2012 | **Rev:** |
| KiCad E.D.A. | eeschema (2012-01-19 BZR 3256)-stable | Id: 8/13 |




Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0

L2

U50A
XS1_L2-QFN124

MODE_0 B33 MODE0
+3V3 B34 MODE1
B35 MODE2
MSEL B36 MODE3
+3.3V A35 MODE4
DEBUG_N B37 DEBUG
RST_N B8 RST_N
CLK B7 CLK
CONFIG
TDO B9 TDO
TDI B12 TDI
TMS B11 TMS
TCK B10 TCK
RST_N B13 TRST_N

U50B
XS1_L2-QFN124

+3V3 A2 VDDIO_A2
A17 VDDIO_A17
A36 VDDIO_A36
A51 VDDIO_51
B1 VDDIO_B1
B14 VDDIO_B14
B29 VDDIO_B29
B42 VDDIO_B42
+1V0 A19 VDD_A19
A34 VDD_A34
A53 VDD_A53
A68 VDD_A68
B15 VDD_B15
B28 VDD_B28
B43 VDD_B43
B56 VDD_B56
POWER
OTP_VDDIO B32
PCU_VDDIO B4
PCU_VDD B5
PCU_GATE B3
PCU_WAKE B2
PCU_CLK B6 CLK
PLL_AVDD A38
PLL_AVGND A37
GND_A1 A1
GND_A18 A18
GND_A52 A52
GND_PAD GND
+3V3
+1V0
2R2 R74
C63 0.1uF

U50C
XS1_L2-QFN124

XCORE0 IO
X0D00 A15
X0D01 A16 X0_XLA_4o
X0D02 A5 X0_XLA_3o
X0D03 A6 X0_XLA_2o
X0D04 A7 X0_XLA_1o
X0D05 A8 X0_XLA_0o
X0D06 A9 X0_XLA_0i
X0D07 A10 X0_XLA_1i
X0D08 A11 X0_XLA_2i
X0D09 A12 X0_XLA_3i
X0D10 A13 X0_XLA_4i
X0D11 A14
X0D12 A55
X0D13 A57 X0_XLB_4o
X0D14 A58 X0_XLB_3o
X0D15 A59 X0_XLB_2o
X0D16 A60 X0_XLB_1o
X0D17 A61 X0_XLB_0o
X0D18 A63 X0_XLB_0i
X0D19 A64 X0_XLB_1i
X0D20 A65 X0_XLB_2i
X0D21 A66 X0_XLB_3i
X0D22 A56 X0_XLB_4i
X0D23 A62
X0D24 A54
X0D25 A67 C0_LED
X0D26 B38
X0D27 B39
X0D28 B40
X0D29 B41
X0D30 B44
X0D31 B45
X0D32 B46
X0D33 B47
X0D34 A4
X0D35 A3
X0D36 B48
X0D37 B49
X0D38 B50
X0D39 B51
X0D40 B52
X0D41 B53
X0D42 B54
X0D43 B55

U50D
XS1_L2-QFN124

XCORE1 IO
X1D00 A39
X1D01 A40 X1_XLA_4o
X1D02 A41 X1_XLA_3o
X1D03 A42 X1_XLA_2o
X1D04 A43 X1_XLA_1o
X1D05 A44 X1_XLA_0o
X1D06 A45 X1_XLA_0i
X1D07 A46 X1_XLA_1i
X1D08 A47 X1_XLA_2i
X1D09 A48 X1_XLA_3i
X1D10 A49 X1_XLA_4i
X1D11 A50
X1D12 A21
X1D13 A23 X1_XLB_4o
X1D14 A24 X1_XLB_3o
X1D15 A25 X1_XLB_2o
X1D16 A26 X1_XLB_1o
X1D17 A27 X1_XLB_0o
X1D18 A29 X1_XLB_0i
X1D19 A30 X1_XLB_1i
X1D20 A31 X1_XLB_2i
X1D21 A32 X1_XLB_3i
X1D22 A22 X1_XLB_4i
X1D23 A28
X1D24 A20
X1D25 A33
X1D26 B16
X1D27 B17
X1D28 B18 LED_0
X1D29 B19 LED_1
X1D30 B20 LED_2
X1D31 B21 LED_3
X1D32 B22
X1D33 B23
X1D34 B24
X1D35 B25
X1D36 B26
X1D37 B27
X1D38 B30
X1D39 B31

| | | |
|---|---|---|
| File: l21-TL.sch | | |
| Sheet: /L2_PAIR_Q1/L2_1-TL/ | | |
| **Title:** | | |
| Size: A4 | Date: 26 sep 2012 | **Rev:** |
| KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable | | Id: 9/13 |

Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.

Undocumented 'reserved' 110 boot functionality used:
X0 boots from XLINKB or internal links, X1 boots via internal links or via XLINK B (i.e. identical options)

L2

U51A
XS1_L2-QFN124

Mode_0 B33 MODE0
+3V3 B34 MODE1
B35 MODE2
MSEL B36 MODE3
+3.3V A35 MODE4
B37 DEBUG
DEBUG_N B8 RST_N
RST_N B7 CLK
CLK
B9 TDO
TDO B12 TDI
TDI B11 TMS
TMS B10 TCK
TCK B13 TRST_N
RST_N
CONFIG

U51B
XS1_L2-QFN124

+3V3 A2 VDDIO_A2
A17 VDDIO_A17
A36 VDDIO_A36
A51 VDDIO_51
B1 VDDIO_B1
B14 VDDIO_B14
B29 VDDIO_B29
B42 VDDIO_B42
+1V0 A19 VDD_A19
A34 VDD_A34
A53 VDD_A53
A68 VDD_A68
B15 VDD_B15
B28 VDD_B28
B43 VDD_B43
B56 VDD_B56
POWER
OTP_VDDIO B32 +3V3
PCU_VDDIO B4
PCU_VDD B5 +1V0
PCU_GATE B3
PCU_WAKE B2
PCU_CLK B6 CLK
PLL_AVDD A38
PLL_AVGND A37
GND_A1 A1
GND_A18 A18
GND_A52 A52
GND_PAD GND
2R2 R79
C74 0.1uF

U51C
XS1_L2-QFN124
XCORE0 IO

X0D00 A15 P1A
X0D01 A16 X0_XLA_4o
X0D02 A5 X0_XLA_3o
X0D03 A6 X0_XLA_2o
X0D04 A7 X0_XLA_1o
X0D05 A8 X0_XLA_0o
X0D06 A9 X0_XLA_0i
X0D07 A10 X0_XLA_1i
X0D08 A11 X0_XLA_2i
X0D09 A12 X0_XLA_3i
X0D10 A13 X0_XLA_4i
X0D11 A14
X0D12 A55 P1E P1D
X0D13 A57 X0_XLB_4o
X0D14 A58 X0_XLB_3o
X0D15 A59 X0_XLB_2o
X0D16 A60 X0_XLB_1o
X0D17 A61 X0_XLB_0o
X0D18 A63 X0_XLB_0i
X0D19 A64 X0_XLB_1i
X0D20 A65 X0_XLB_2i
X0D21 A66 X0_XLB_3i
X0D22 A56 X0_XLB_4i
X0D23 A62
X0D24 A54 P1H
X0D25 A67 P1J C0_LED
X0D26 B38 P4E0
X0D27 B39 P4E1
X0D28 B40 P4F0
X0D29 B41 P4F1
X0D30 B44 P4F2
X0D31 B45 P4F3
X0D32 B46 P4E2
X0D33 B47 P4E3
X0D34 A4
X0D35 A3 P1J
X0D36 B48 P1H
X0D37 B49 P1E
X0D38 B50 P1K
X0D39 B51
X0D40 B52
X0D41 B53
X0D42 B54
X0D43 B55

U51D
XS1_L2-QFN124
XCORE1 IO

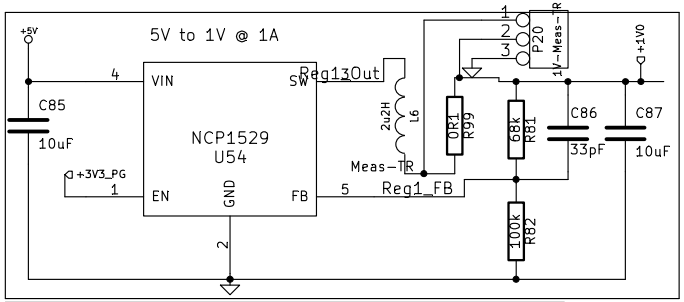
X1D00 A39
X1D01 A40 X1_XLA_4o
X1D02 A41 X1_XLA_3o
X1D03 A42 X1_XLA_2o
X1D04 A43 X1_XLA_1o
X1D05 A44 X1_XLA_0o
X1D06 A45 X1_XLA_0i
X1D07 A46 X1_XLA_1i
X1D08 A47 X1_XLA_2i
X1D09 A48 X1_XLA_3i
X1D10 A49 X1_XLA_4i
X1D11 A50
X1D12 A21
X1D13 A23 X1_XLB_4o
X1D14 A24 X1_XLB_3o
X1D15 A25 X1_XLB_2o
X1D16 A26 X1_XLB_1o
X1D17 A27 X1_XLB_0o
X1D18 A29 X1_XLB_0i
X1D19 A30 X1_XLB_1i
X1D20 A31 X1_XLB_2i
X1D21 A32 X1_XLB_3i
X1D22 A22 X1_XLB_4i
X1D23 A28
X1D24 A20
X1D25 A33
X1D26 B16
X1D27 B17
X1D28 B18 LED_0
X1D29 B19 LED_1
X1D30 B20 LED_2
X1D31 B21 LED_3
X1D32 B22
X1D33 B23
X1D34 B24
X1D35 B25
X1D36 B26
X1D37 B27
X1D38 B30
X1D39 B31

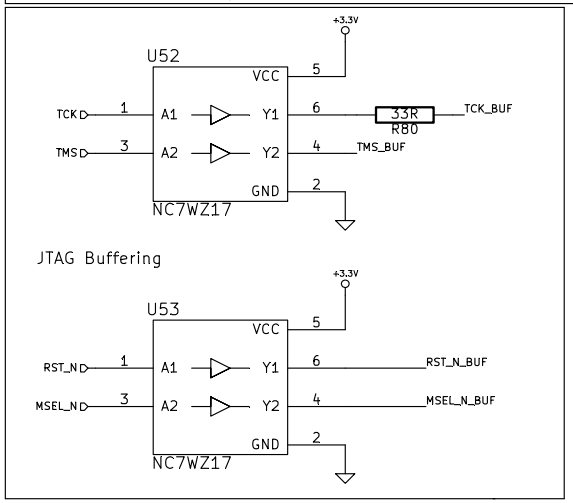
LED_ARRAY
LED_0
LED_1
LED_2
LED_3
C0_LED
433R R75 E D22
433R R76 N D23
433R R77 S D24
433R R78 W D25
433R R106 Z D41

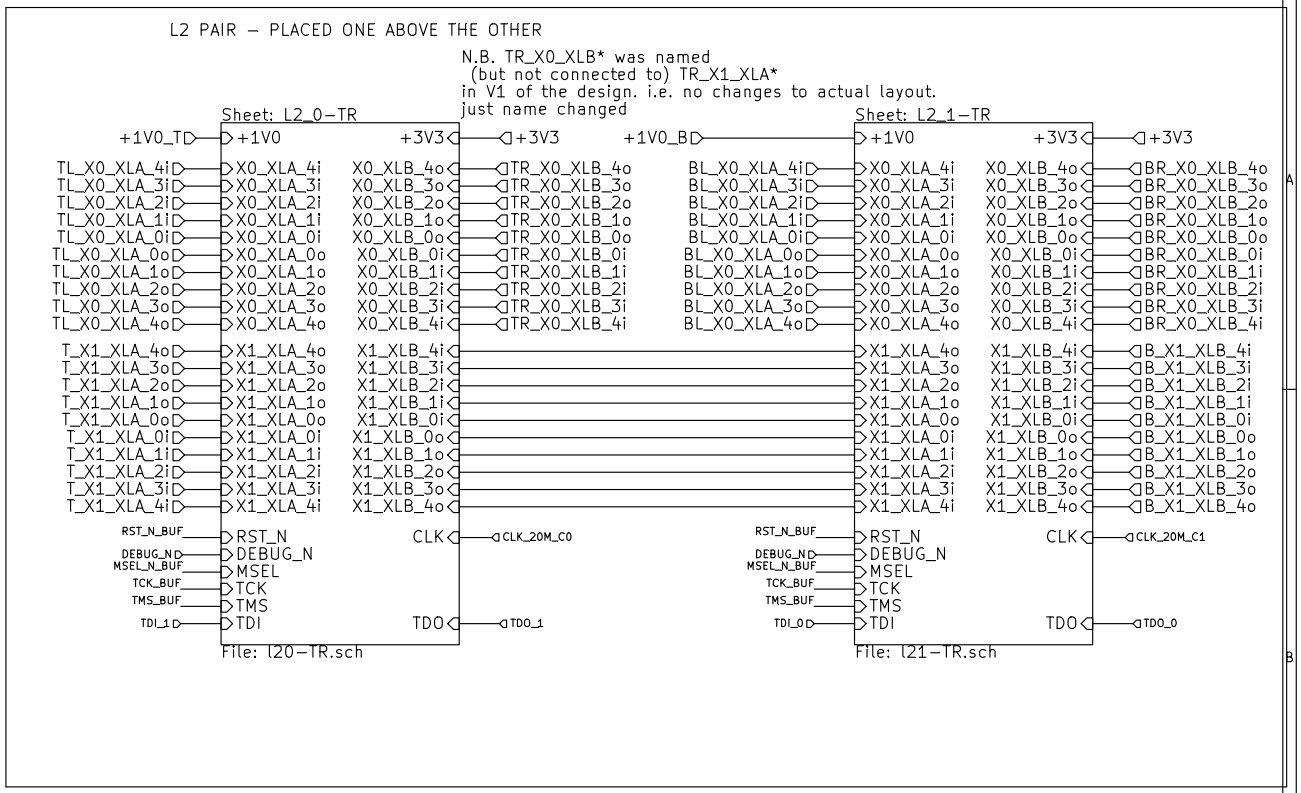
P4F0 1
P4E0 2
P4F1 3
P4E1 4
P4F2 5
P4E2 6
P4F3 7
P4E3 8
P1H 9
P1J 10
P1K 11
P1E 12
P1D 13
P1A 14
+3.3V 15
16
P15 Core2 I/O
RST_N_G P28

Decoupling Caps
+1V0 C75 C76 C77 C78 C79 100nF 100nF 100nF 100nF 10uF
+3V3 C80 C81 C82 C83 C84 100nF 100nF 100nF 100nF 10uF

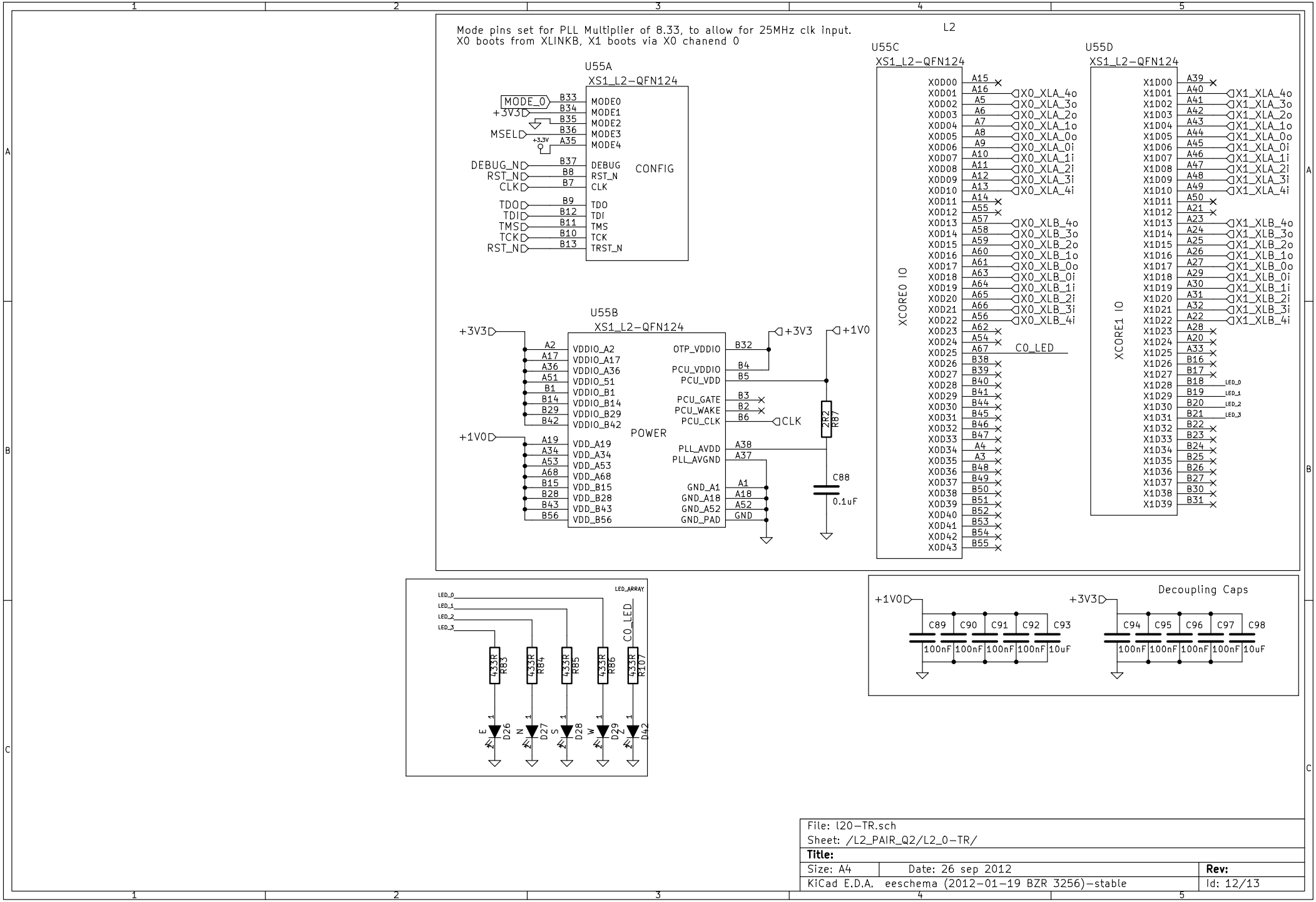
| | | |
|---|---|---|
| File: l20-TL.sch | | |
| Sheet: /L2_PAIR_Q1/L2_0-TL/ | | |
| **Title:** | | |
| Size: A4 | Date: 26 sep 2012 | **Rev:** |
| KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable | | Id: 10/13 |

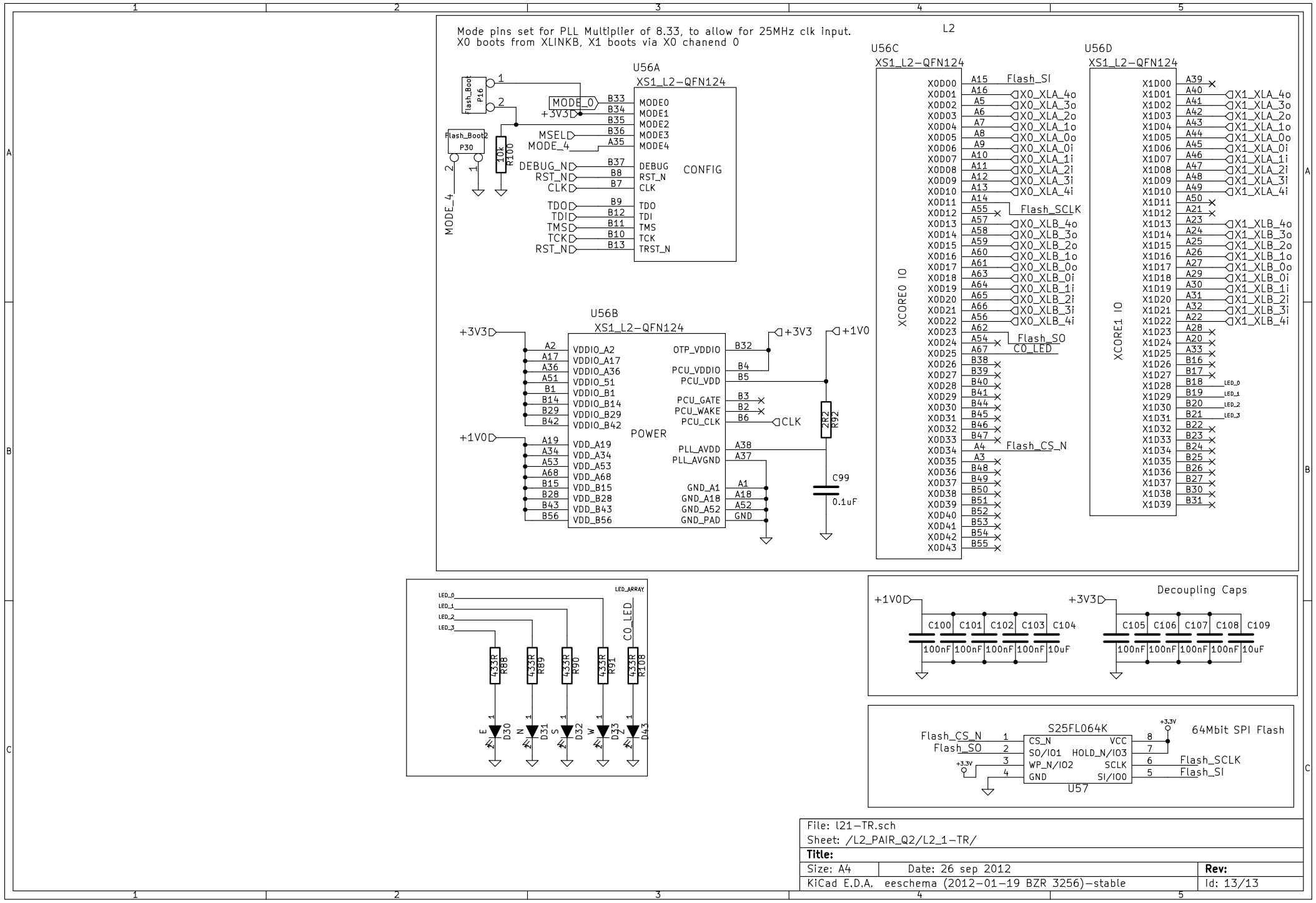



| | | |
|---|---|---|
| File: l2_pair-TR.sch | | |
| Sheet: /L2_PAIR_Q2/ | | |
| **Title:** | | |
| Size: A4 | Date: 26 sep 2012 | **Rev:** |
| KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable | | Id: 11/13 |


Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0
L2
U55A
XS1_L2-QFN124
MODE_0
+3V3
MSEL
DEBUG_N
RST_N
CLK
TDO
TDI
TMS
TCK
RST_N
MODE0
MODE1
MODE2
MODE3
MODE4
DEBUG
RST_N
CLK
TDO
TDI
TMS
TCK
TRST_N
CONFIG
U55B
XS1_L2-QFN124
+3V3
+1V0
VDDIO_A2
VDDIO_A17
VDDIO_A36
VDDIO_51
VDDIO_B1
VDDIO_B14
VDDIO_B29
VDDIO_B42
VDD_A19
VDD_A34
VDD_A53
VDD_A68
VDD_B15
VDD_B28
VDD_B43
VDD_B56
POWER
OTP_VDDIO
PCU_VDDIO
PCU_VDD
PCU_GATE
PCU_WAKE
PCU_CLK
PLL_AVDD
PLL_AVGND
GND_A1
GND_A18
GND_A52
GND
CLK
2R2
R87
C88
0.1uF
U55C
XS1_L2-QFN124
XCORE0 IO
X0D00
X0D01
X0D02
X0D03
X0D04
X0D05
X0D06
X0D07
X0D08
X0D09
X0D10
X0D11
X0D12
X0D13
X0D14
X0D15
X0D16
X0D17
X0D18
X0D19
X0D20
X0D21
X0D22
X0D23
X0D24
X0D25
X0D26
X0D27
X0D28
X0D29
X0D30
X0D31
X0D32
X0D33
X0D34
X0D35
X0D36
X0D37
X0D38
X0D39
X0D40
X0D41
X0D42
X0D43
X0_XLA_4o
X0_XLA_3o
X0_XLA_2o
X0_XLA_1o
X0_XLA_0o
X0_XLA_0i
X0_XLA_1i
X0_XLA_2i
X0_XLA_3i
X0_XLA_4i
X0_XLB_4o
X0_XLB_3o
X0_XLB_2o
X0_XLB_1o
X0_XLB_0o
X0_XLB_0i
X0_XLB_1i
X0_XLB_2i
X0_XLB_3i
X0_XLB_4i
C0_LED
U55D
XS1_L2-QFN124
XCORE1 IO
X1D00
X1D01
X1D02
X1D03
X1D04
X1D05
X1D06
X1D07
X1D08
X1D09
X1D10
X1D11
X1D12
X1D13
X1D14
X1D15
X1D16
X1D17
X1D18
X1D19
X1D20
X1D21
X1D22
X1D23
X1D24
X1D25
X1D26
X1D27
X1D28
X1D29
X1D30
X1D31
X1D32
X1D33
X1D34
X1D35
X1D36
X1D37
X1D38
X1D39
X1_XLA_4o
X1_XLA_3o
X1_XLA_2o
X1_XLA_1o
X1_XLA_0o
X1_XLA_0i
X1_XLA_1i
X1_XLA_2i
X1_XLA_3i
X1_XLA_4i
X1_XLB_4o
X1_XLB_3o
X1_XLB_2o
X1_XLB_1o
X1_XLB_0o
X1_XLB_0i
X1_XLB_1i
X1_XLB_2i
X1_XLB_3i
X1_XLB_4i
LED_0
LED_1
LED_2
LED_3
LED_ARRAY
C0_LED
433R
R83
R84
R85
R86
R107
D26
D27
D28
D29
D42
E
N
S
W
Z
Decoupling Caps
+1V0
+3V3
C89
C90
C91
C92
C93
C94
C95
C96
C97
C98
100nF
10uF
File: l20-TR.sch
Sheet: /L2_PAIR_Q2/L2_0-TR/
Title:
Size: A4
Date: 26 sep 2012
Rev:
KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable
Id: 12/13


Mode pins set for PLL Multiplier of 8.33, to allow for 25MHz clk input.
X0 boots from XLINKB, X1 boots via X0 chanend 0
L2
U56A
XS1_L2-QFN124
Flash_Boot
P16
Flash_Boot2
P30
MODE_4
10K
R100
MODE_0
+3V3
MSEL
DEBUG_N
RST_N
CLK
TDO
TDI
TMS
TCK
TRST_N
MODE0
MODE1
MODE2
MODE3
MODE4
DEBUG
CONFIG
U56B
POWER
VDDIO_A2
VDDIO_A17
VDDIO_A36
VDDIO_51
VDDIO_B1
VDDIO_B14
VDDIO_B29
VDDIO_B42
VDD_A19
VDD_A34
VDD_A53
VDD_A68
VDD_B15
VDD_B28
VDD_B43
VDD_B56
OTP_VDDIO
PCU_VDDIO
PCU_VDD
PCU_GATE
PCU_WAKE
PCU_CLK
PLL_AVDD
PLL_AVGND
GND_A1
GND_A18
GND_A52
GND_PAD
+1V0
2R2
R92
C99
0.1uF
U56C
XCORE0 IO
Flash_SI
Flash_SCLK
Flash_SO
C0_LED
Flash_CS_N
U56D
XCORE1 IO
LED_ARRAY
LED_0
LED_1
LED_2
LED_3
C0_LED
433R
R88
R89
R90
R91
R108
D30
D31
D32
D33
D43
Decoupling Caps
C100
C101
C102
C103
C104
C105
C106
C107
C108
C109
100nF
10uF
S25FL064K
64Mbit SPI Flash
U57
+3.3V
File: l21-TR.sch
Sheet: /L2_PAIR_Q2/L2_1-TR/
Title:
Size: A4
Date: 26 sep 2012
Rev:
KiCad E.D.A. eeschema (2012-01-19 BZR 3256)-stable
Id: 13/13