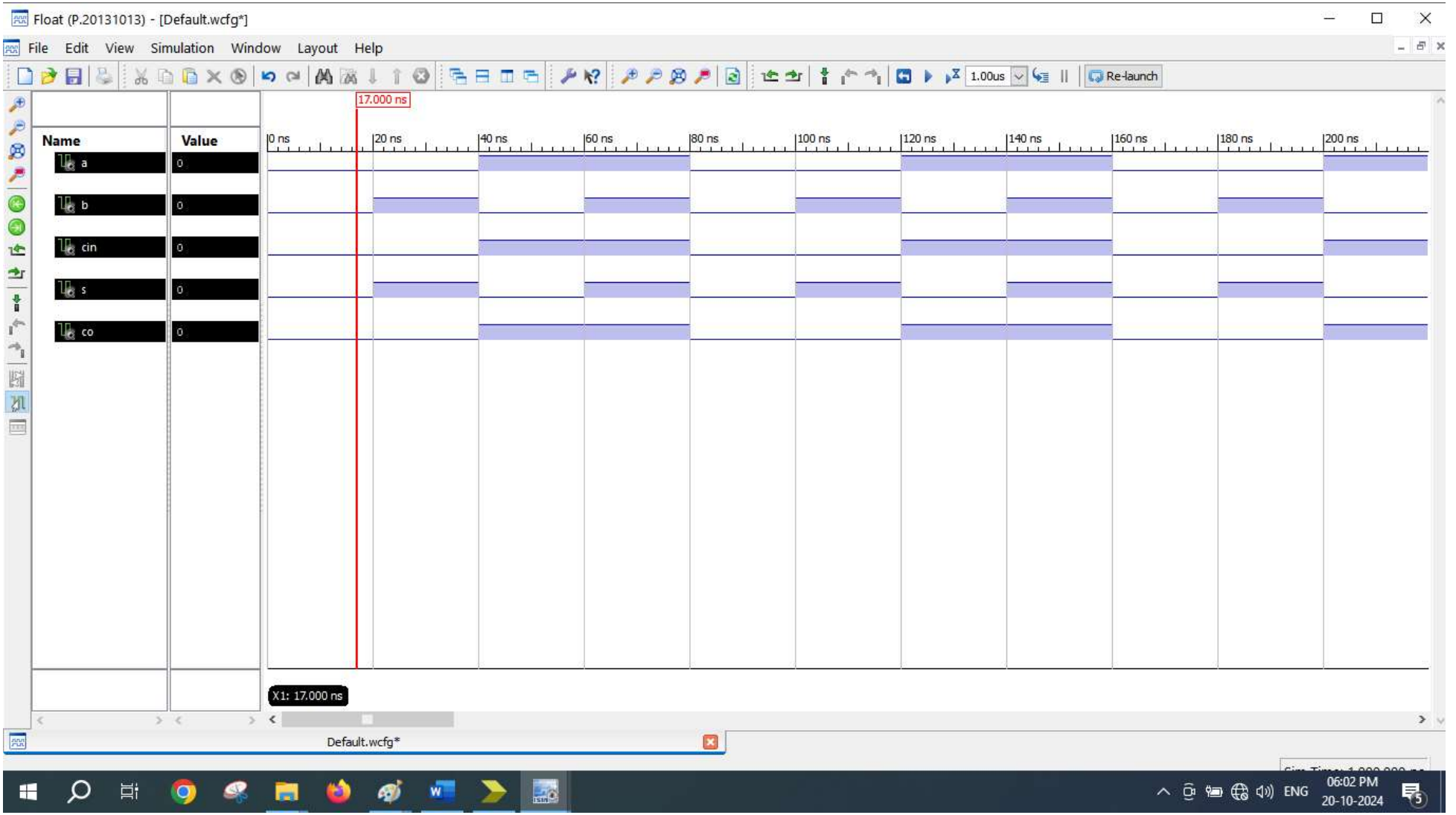
# Expt. 1

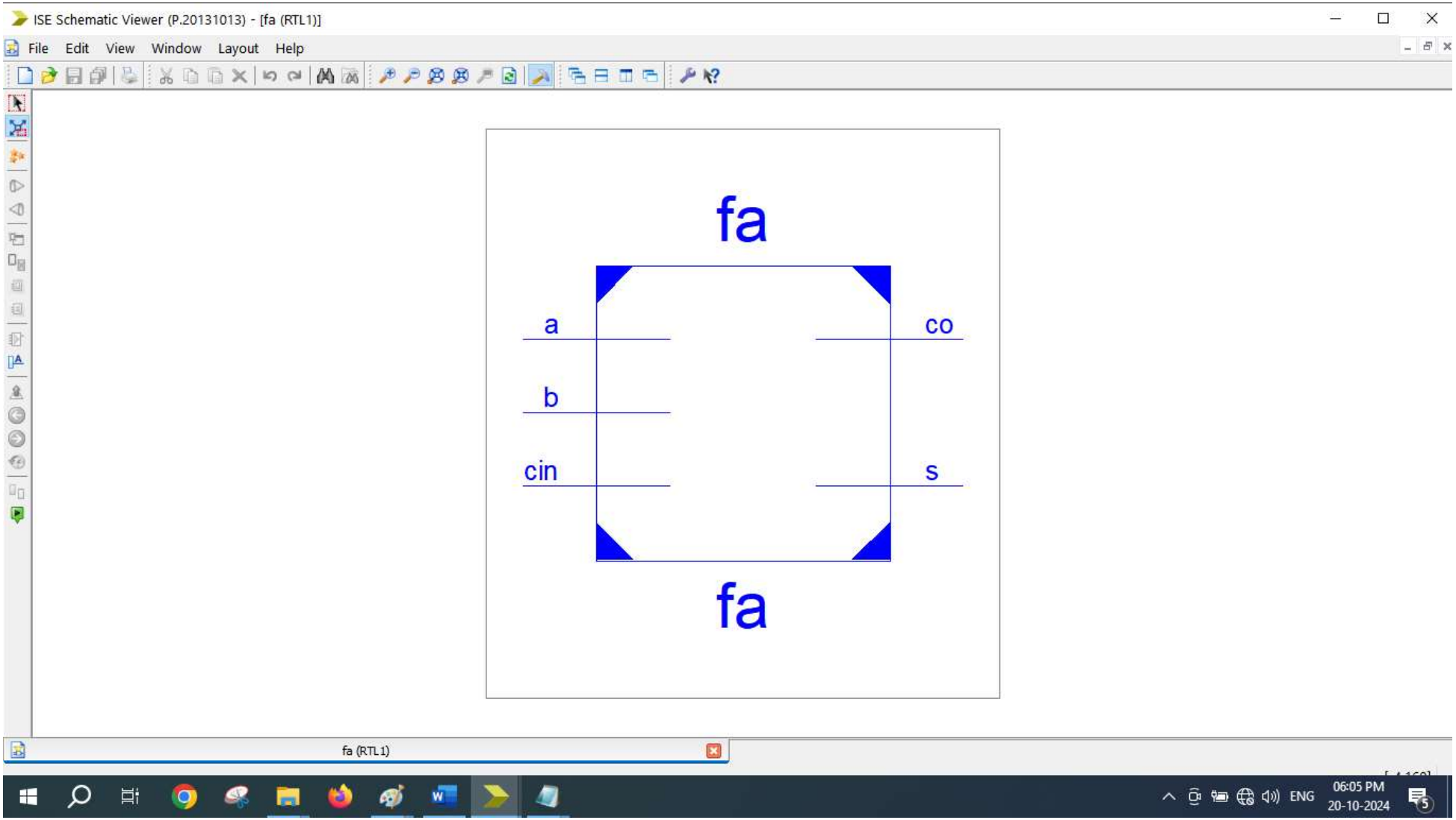
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity fa is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           cin : in  STD_LOGIC;
           s : out  STD_LOGIC;
           co : out  STD_LOGIC);
end fa;

architecture Behavioral of fa is

begin
s <= a xor b xor cin;
co <= (a and b) or (b and cin) or (a and cin);

end Behavioral;
```

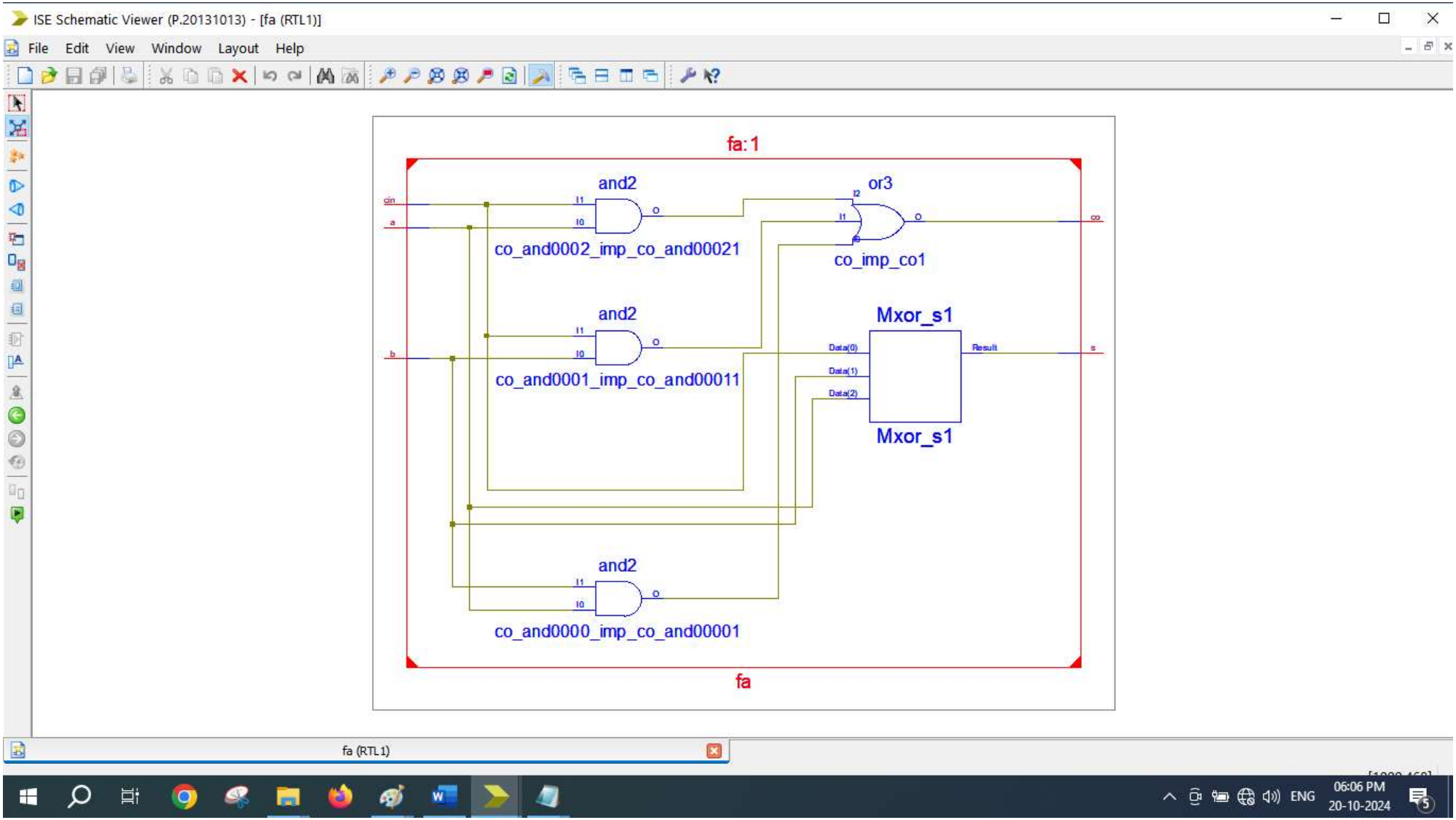
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY fa_tb IS
END fa_tb;

ARCHITECTURE behavior OF fa_tb IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT fa
    PORT(
         a : IN  std_logic;
         b : IN  std_logic;
         cin : IN  std_logic;
         s : OUT  std_logic;
         co : OUT  std_logic
        );
    END COMPONENT;


   --Inputs
   signal a : std_logic := '0';
   signal b : std_logic := '0';
   signal cin : std_logic := '0';

        --Outputs
   signal s : std_logic;
   signal co : std_logic;
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

BEGIN

        -- Instantiate the Unit Under Test (UUT)
   uut: fa PORT MAP (
          a => a,
          b => b,
          cin => cin,
          s => s,
          co => co
        );
   -- Stimulus process
   stim_proc: process
   begin
      a <= '0';
                b <= '0';
                cin <= '0';
      wait for 20 ns;
      a <= '0';
```

```
                b <= '1';
                cin <= '0';
      wait for 20 ns;
      a <= '1';
                b <= '0';
                cin <= '1';
      wait for 20 ns;
      a <= '1';
                b <= '1';
                cin <= '1';
      wait for 20 ns;
   end process;

END;
```


Float (P.20131013) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
1.00us
Re-launch
17.000 ns
Name
Value
a
b
cin
s
co
0
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
200 ns
X1: 17.000 ns
Default.wcfg*
ENG
06:02 PM
20-10-2024

```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : fa.ngr
Top Level Output File Name         : fa
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 5

Cell Usage :
# BELS                             : 2
#      LUT3                        : 2
# IO Buffers                       : 5
#      IBUF                        : 3
#      OBUF                        : 2
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                        1  out of   2448     0%
 Number of 4 input LUTs:                  2  out of   4896     0%
 Number of IOs:                           5
 Number of bonded IOBs:                   5  out of    158     3%

---------------------------
```


ISE Schematic Viewer (P.20131013) - [fa (RTL1)]
File Edit View Window Layout Help
fa
a
b
cin
co
s
fa
fa (RTL1)
ENG
06:05 PM
20-10-2024

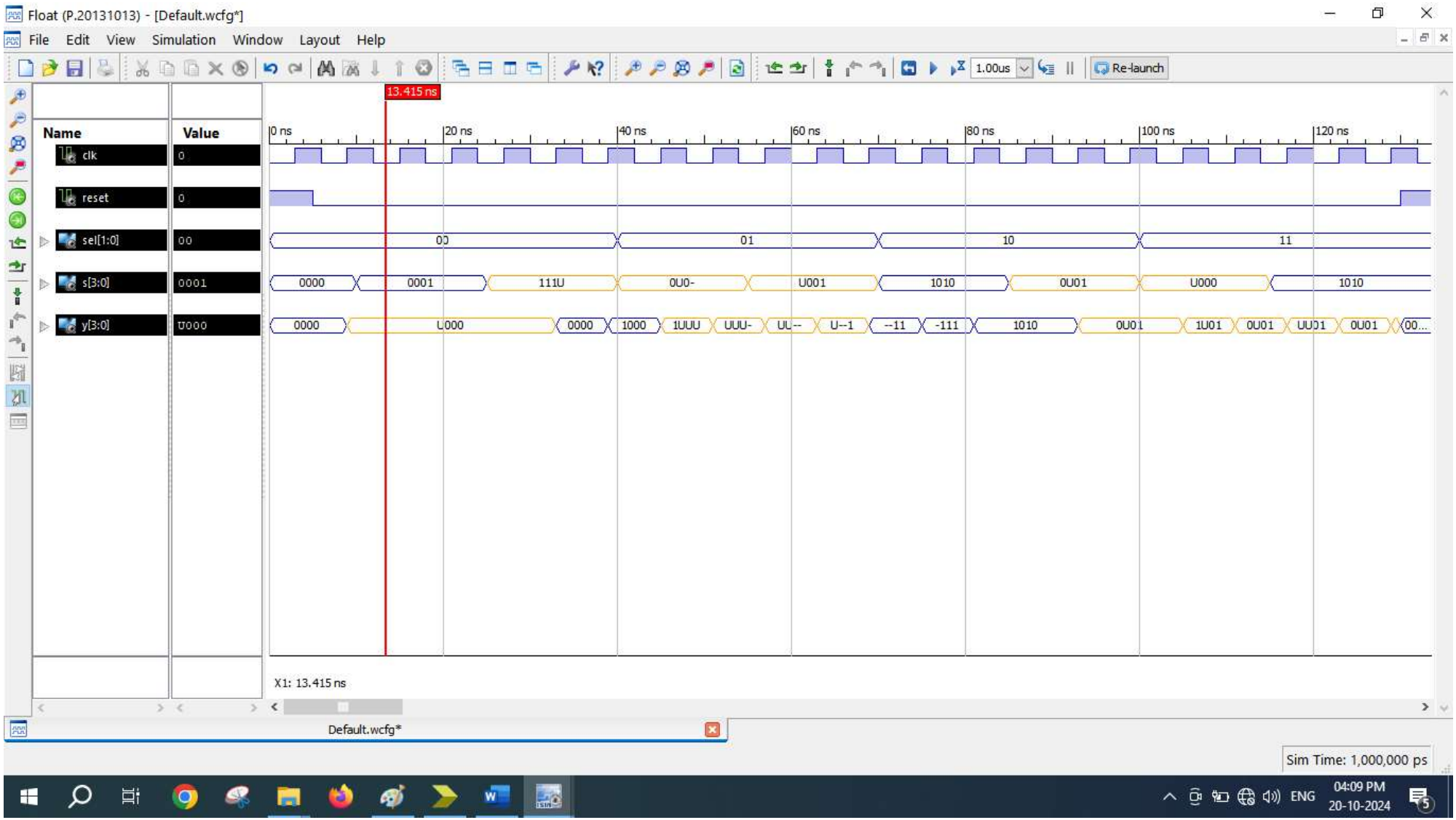

ISE Schematic Viewer (P.20131013) - [fa (RTL1)]
File Edit View Window Layout Help
fa:1
and2
co_and0002_imp_co_and00021
or3
co_imp_co1
and2
co_and0001_imp_co_and00011
Mxor_s1
Mxor_s1
and2
co_and0000_imp_co_and00001
cin
a
b
I1
I0
O
I2
Data(0)
Data(1)
Data(2)
Result
co
s
fa
fa (RTL1)
ENG
06:06 PM
20-10-2024

# Expt. 2

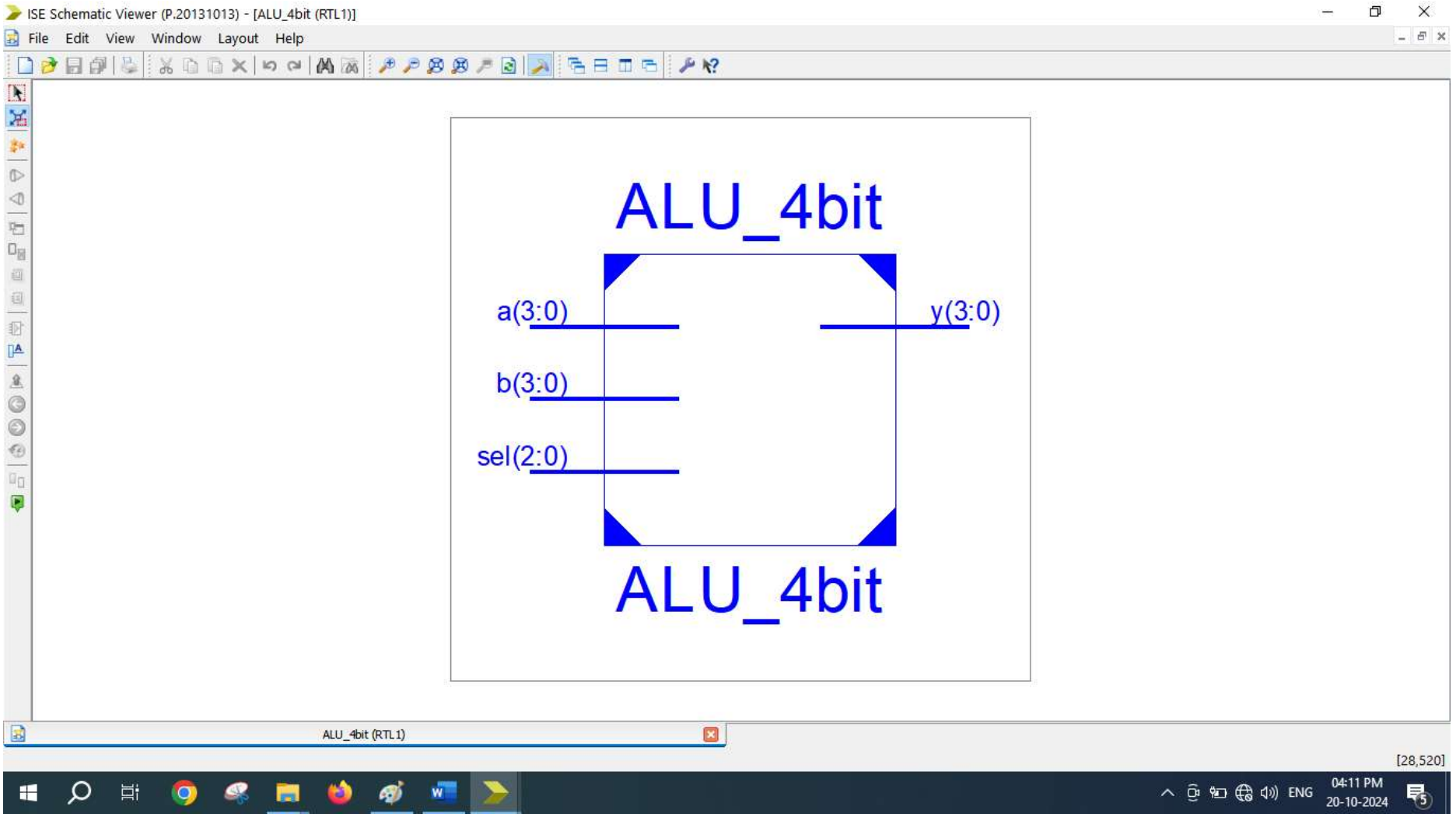
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;


entity ALU_4bit is
    Port ( a : in  STD_LOGIC_VECTOR (3 downto 0);
           b : in  STD_LOGIC_VECTOR (3 downto 0);
           sel : in  STD_LOGIC_VECTOR (2 downto 0);
           y : out  STD_LOGIC_VECTOR (3 downto 0));
end ALU_4bit;

architecture Behavioral of ALU_4bit is

begin
process (a, b, sel)
begin
case sel is
        when "000" => y <= a + b;
        when "001" => y <= a - b;
        when "010" => y <= b - a;
        when "011" => y <= a and b;
        when "100" => y <= a or b;
        when "101" => y <= a nand b;
        when "110" => y <= a xor b;
        when "111" => y <= a nor b;
        when others => null;
end case;
end process;
end Behavioral;
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY ALU_TB IS
END ALU_TB;

ARCHITECTURE behavior OF ALU_TB IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT ALU_4bit
    PORT(
         a : IN  std_logic_vector(3 downto 0);
         b : IN  std_logic_vector(3 downto 0);
         sel : IN  std_logic_vector(2 downto 0);
         y : OUT  std_logic_vector(3 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal a : std_logic_vector(3 downto 0) := (others => '0');
   signal b : std_logic_vector(3 downto 0) := (others => '0');
   signal sel : std_logic_vector(2 downto 0) := (others => '0');

        --Outputs
   signal y : std_logic_vector(3 downto 0);
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

 BEGIN

        -- Instantiate the Unit Under Test (UUT)
   uut: ALU_4bit PORT MAP (
          a => a,
          b => b,
          sel => sel,
          y => y
        );

    -- Stimulus process
   stim_proc: process
   begin
      a <= "1010";
                b <= "0101";
                sel <= "000";
                wait for 10 ns;
                sel <= "001";
                wait for 10 ns;
                sel <= "010";
```

```
                wait for 10 ns;
                sel <= "011";
                wait for 10 ns;
                sel <= "100";
                wait for 10 ns;
                sel <= "101";
                wait for 10 ns;
                sel <= "110";
                wait for 10 ns;
                sel <= "111";
                wait for 10 ns;

   end process;

END;
```


Float (P.20131013) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
13.415 ns
Name
Value
clk
0
reset
0
sel[1:0]
00
s[3:0]
0001
y[3:0]
U000
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
00
01
10
11
0000
0001
111U
0U0-
U001
1010
0U01
U000
1010
0000
U000
0000
1000
1UUU
UUU-
UU--
U--1
--11
-111
1010
0U01
1U01
0U01
UU01
0U01
X1: 13.415 ns
Default.wcfg*
Sim Time: 1,000,000 ps
ENG
04:09 PM
20-10-2024

```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : ALU_4bit.ngr
Top Level Output File Name         : ALU_4bit
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 15

Cell Usage :
# BELS                             : 30
#      INV                         : 1
#      LUT2                        : 2
#      LUT3                        : 2
#      LUT4                        : 18
#      MUXF5                       : 7
# IO Buffers                       : 15
#      IBUF                        : 11
#      OBUF                        : 4
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                       13  out of   2448     0%
 Number of 4 input LUTs:                 23  out of   4896     0%
 Number of IOs:                          15
 Number of bonded IOBs:                  15  out of    158     9%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
```


ISE Schematic Viewer (P.20131013) - [ALU_4bit (RTL1)]
File Edit View Window Layout Help
ALU_4bit
a(3:0)
b(3:0)
sel(2:0)
y(3:0)
ALU_4bit
ALU_4bit (RTL1)
[28,520]
ENG
04:11 PM
20-10-2024

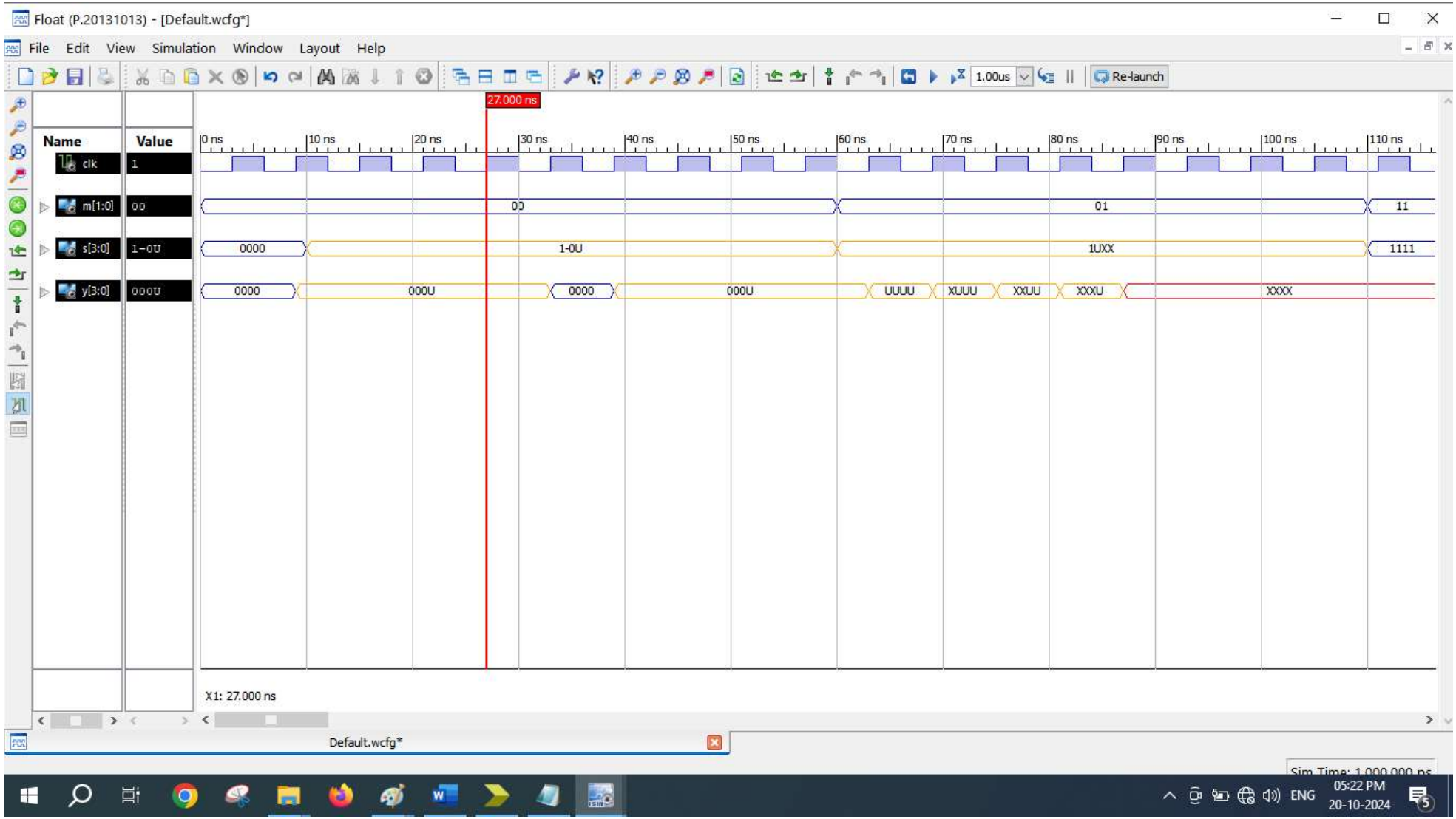
# Expt. 3

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity shiftregister is
        Port( clk,rst : in std_logic;
              s : in std_logic_vector(3 downto 0);
                        m : in std_logic_vector(1 downto 0); -- mode
                        y : out std_logic_vector(3 downto 0) );
end shiftregister;

architecture Behavioral of shiftregister is
        signal t : std_logic_vector(3 downto 0);
begin
        process(clk, rst)
        begin
                if rst = '1' then
                        y <= "0000";
                elsif clk'event and clk = '1' then
                        case m is
                                when "00" =>  -- SISO
                                        t(3) <= s(0); -- LSB as input S(0)
                                        t(2) <= t(3);
                                        t(1) <= t(2);
                                        t(0) <= t(1);
                                        y(0) <= t(0); -- LSB as output Y(0)

                                when "01" =>  -- SIPO
                                        t(3) <= s(0); -- LSB as input S(0)
                                        t(2) <= t(3);
                                        t(1) <= t(2);
                                        t(0) <= t(1);
                                        y <= t;  -- parallel output

                                when "10" =>  -- PIPO
                                        t <= s;
                                        y <= t;

                                when "11" =>  -- PISO
                                        t <= s; -- 4 bit input S  &  t <= s
                                        t(2) <= t(3); --  MSB input as t(3) <= S(3)

                                        t(1) <= t(2);
                                        t(0) <= t(1);
                                        y(3) <= t(0); -- MSB as output  Y(3) <=
S(3)
                                when others => NULL;
                        end case;
                end if;
        end process;
end Behavioral;
```

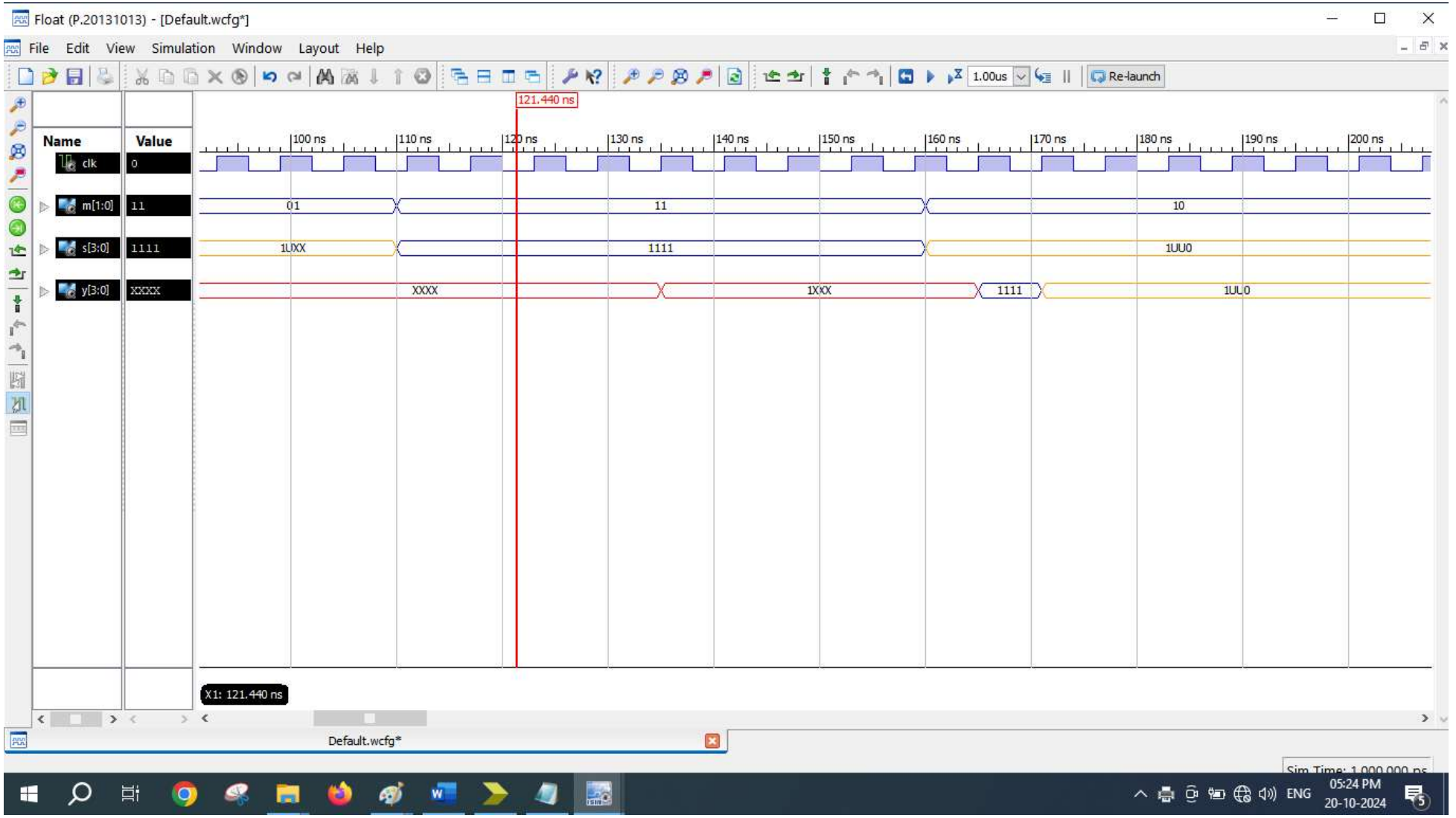
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY usr2_tb IS
END usr2_tb;

ARCHITECTURE behavior OF usr2_tb IS

    COMPONENT shiftregister
    PORT(
         clk : IN  std_logic;
         rst : IN  std_logic;
         s : IN  std_logic_vector(3 downto 0);
         m : IN  std_logic_vector(1 downto 0);
         y : OUT  std_logic_vector(3 downto 0)
        );
    END COMPONENT;

   -- Inputs
   signal clk : std_logic := '0';
   signal rst : std_logic := '0';
   signal s : std_logic_vector(3 downto 0) := (others => '0');
   signal m : std_logic_vector(1 downto 0) := (others => '0');

   -- Outputs
   signal y : std_logic_vector(3 downto 0);

 BEGIN

   -- Instantiate the Unit Under Test (UUT)
   uut: shiftregister PORT MAP (
          clk => clk,
          rst => rst,
          s => s,
          m => m,
          y => y
        );

   -- Clock process definitions
   clk_process : process
   begin
                clk <= '0';
                wait for 3 ns;
                clk <= '1';
                wait for 3 ns;
   end process;

   -- Stimulus process
   stim_proc: process
   begin
```

```
      rst <= '1';
      wait for 5 ns;
          rst <= '0';
      wait for 5 ns;

          -- Test SISO Mode
          m <= "00";
          s <= "1-0U";
          wait for 50 ns;

          -- Test SIPO Mode
          m <= "01";
          s <= "1UXX";
          wait for 50 ns;

          -- Test PISO Mode
          m <= "11";
          s <= "1111";
          wait for 50 ns;

          -- Test PIPO Mode
          m <= "10";
          s <= "1UU0";
          wait for 50 ns;
   end process;
END;
```

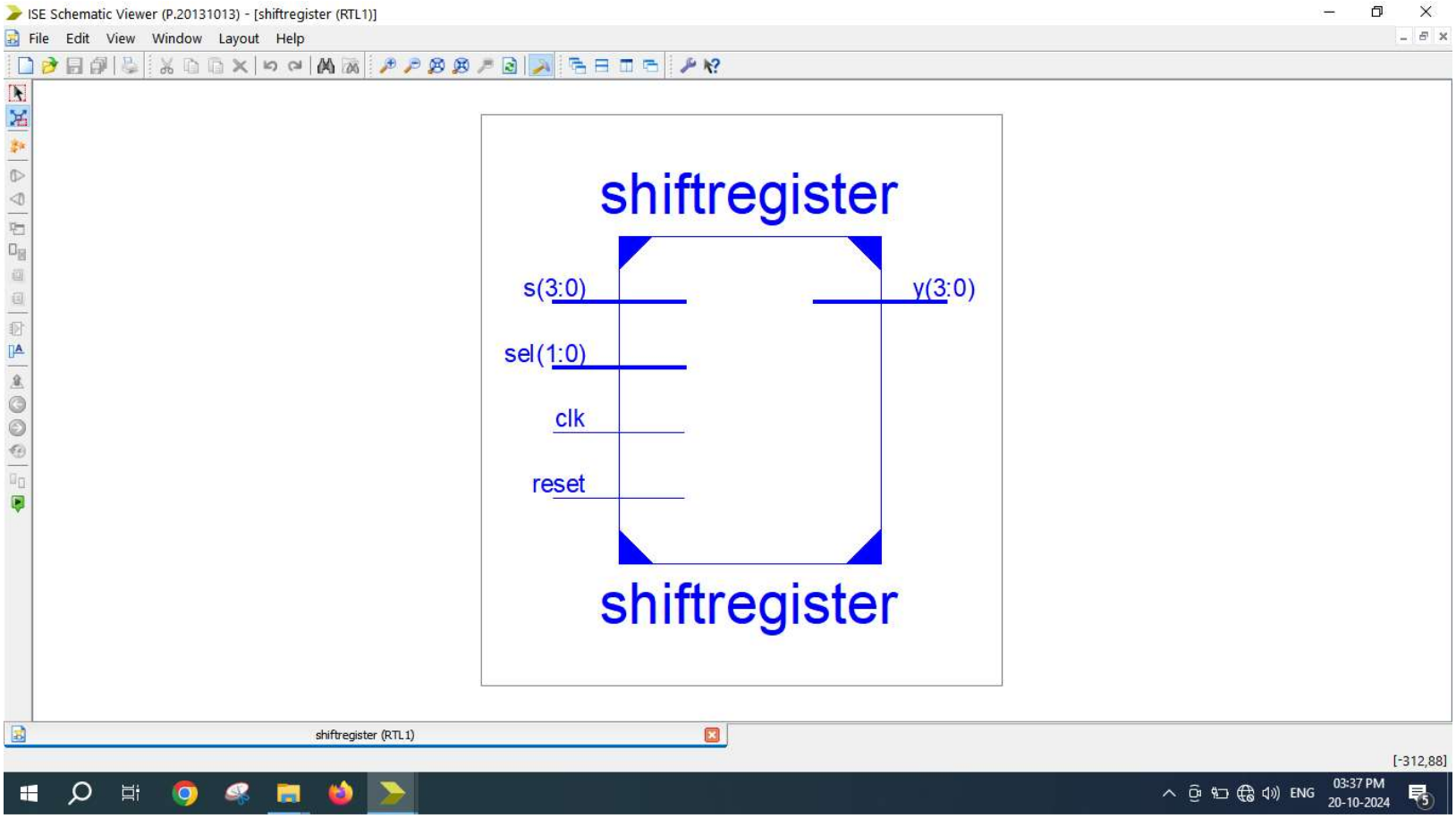
# Output for SISO and SIPO

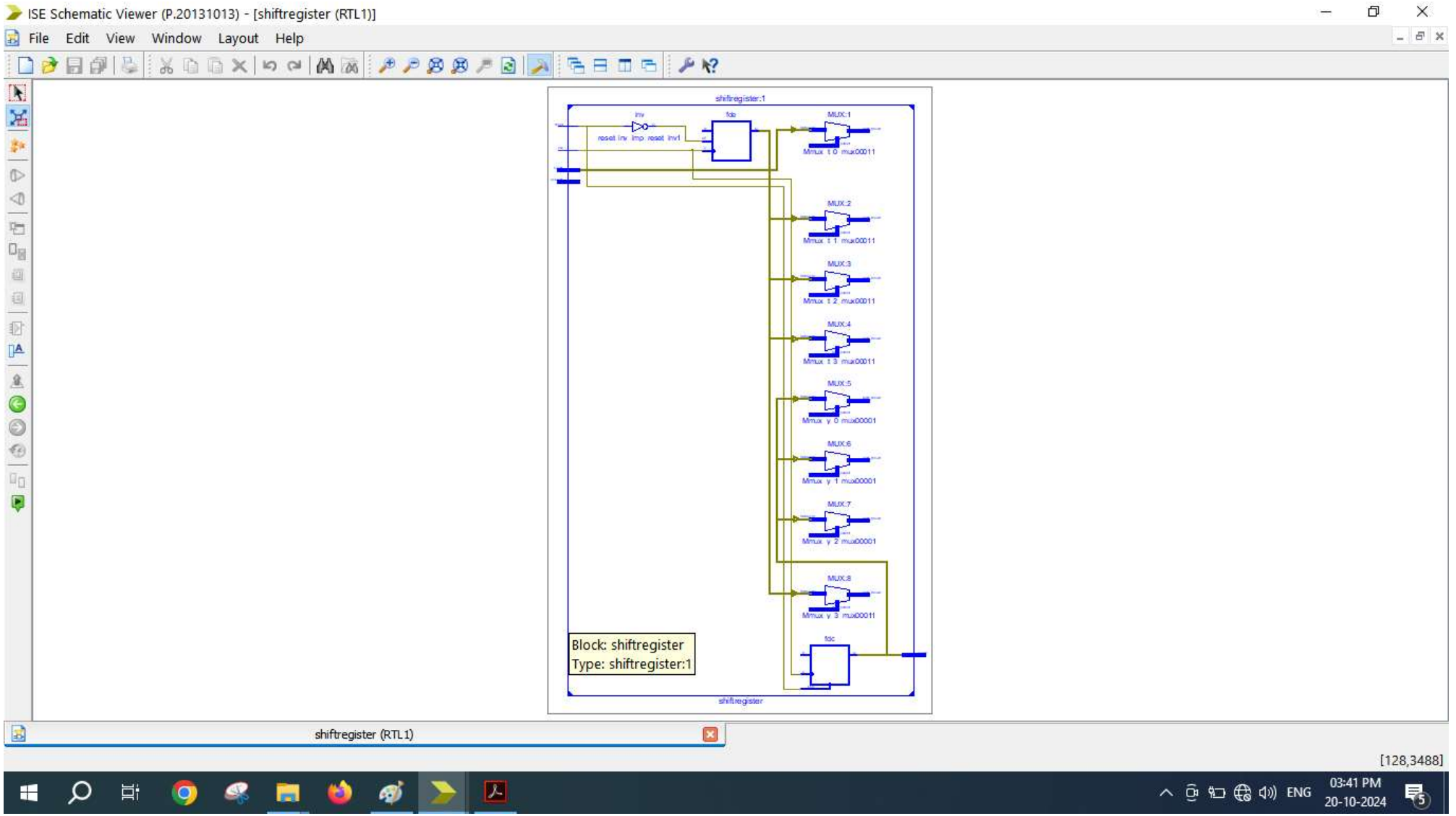


# Output for PISO and PIPO



```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : shiftregister.ngr
Top Level Output File Name         : shiftregister
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 12

Cell Usage :
# BELS                             : 11
#      INV                         : 1
#      LUT3                        : 3
#      LUT3_L                      : 2
#      LUT4                        : 5
# FlipFlops/Latches                : 8
#      FDC                         : 4
#      FDE                         : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 11
#      IBUF                        : 7
#      OBUF                        : 4
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                        5  out of   2448     0%
 Number of Slice Flip Flops:              8  out of   4896     0%
 Number of 4 input LUTs:                 11  out of   4896     0%
 Number of IOs:                          12
 Number of bonded IOBs:                  12  out of    158     7%
 Number of GCLKs:                         1  out of     24     4%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```


ISE Schematic Viewer (P.20131013) - [shiftregister (RTL1)]
File Edit View Window Layout Help
shiftregister
s(3:0)
sel(1:0)
clk
reset
y(3:0)
shiftregister
shiftregister (RTL1)
[-312,88]
ENG
03:37 PM
20-10-2024

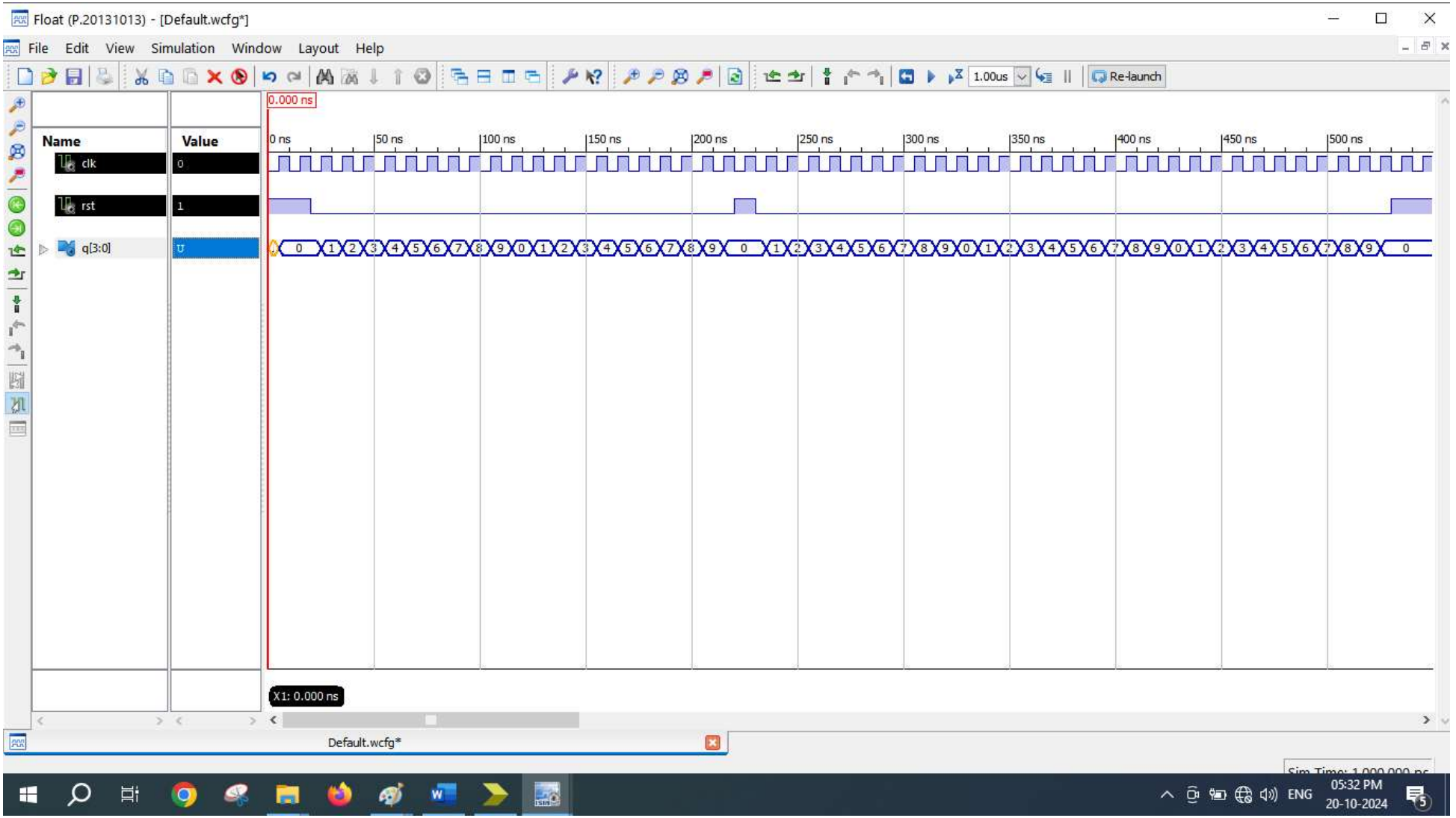

ISE Schematic Viewer (P.20131013) - [shiftregister (RTL1)]
File Edit View Window Layout Help
shiftregister:1
inv
fdc
MUX:1
MUX:2
MUX:3
MUX:4
MUX:5
MUX:6
MUX:7
MUX:8
fdc
Block: shiftregister
Type: shiftregister:1
shiftregister
shiftregister (RTL1)
[128,3488]
ENG
03:41 PM
20-10-2024

# Expt. 4

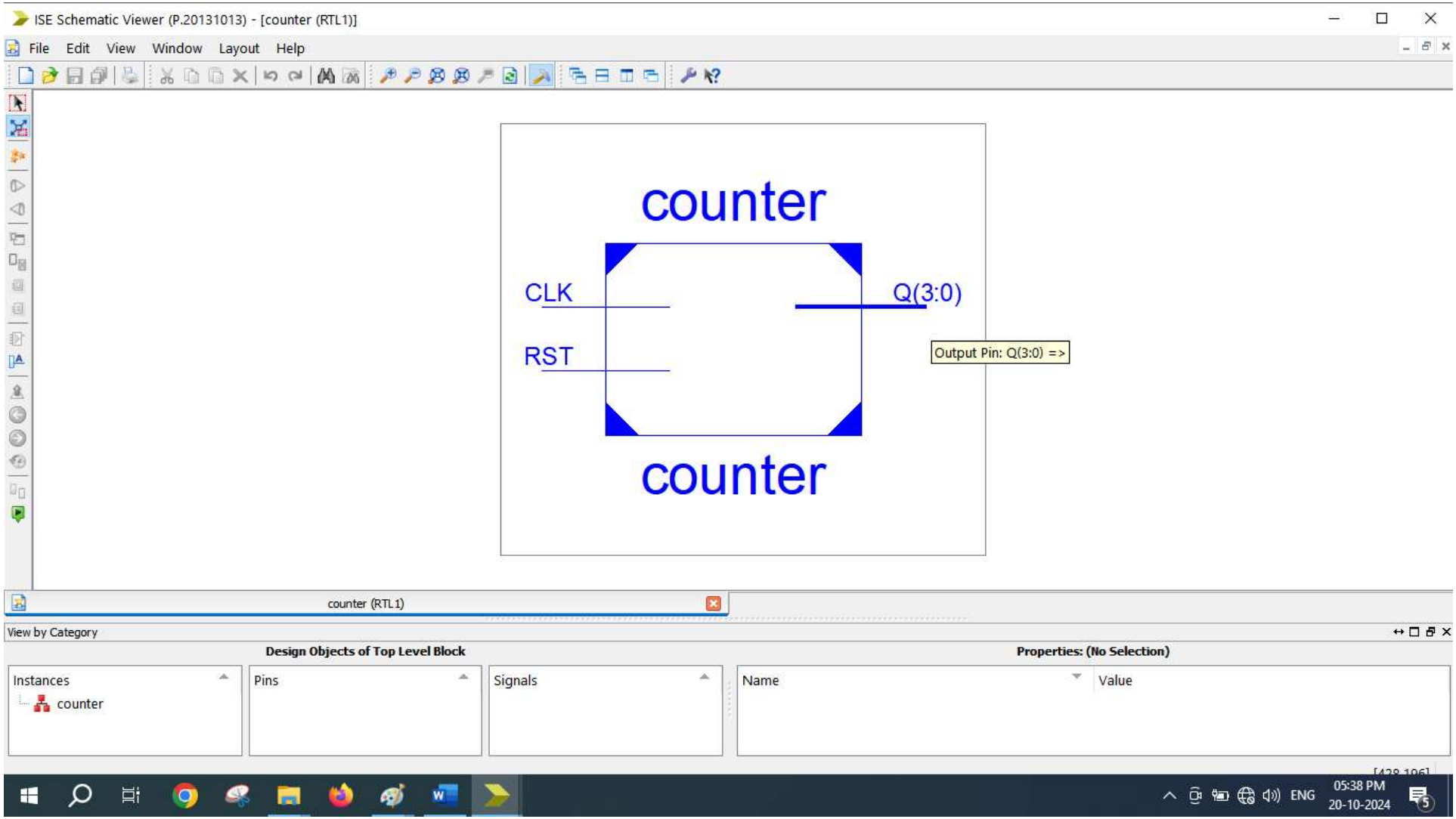
```
-- Modulo-10 Counter with Synchronous Reset : 0 to 9 (0000 to 1001)
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity counter is
        port ( CLK : in std_logic;
                        RST : in std_logic; -- Synchronous reset input RST active
high
                        Q : out std_logic_vector(3 downto 0));
end counter;

architecture counter_arch of counter is
signal TEMP_Q : std_logic_vector(3 downto 0);
begin
        process(CLK)
          begin
           if rising_edge(CLK) then  -- if clk'event and clk = '1' then
              if RST = '1' then  -- active high and it is inside clock therfore its
synchronous reset
                TEMP_Q <= (others => '0'); -- TEMP_Q <= "0000"
              else
                if (TEMP_Q = "1001") then
                  TEMP_Q <= (others => '0'); -- TEMP_Q <= "0000"
                else
                  TEMP_Q <= TEMP_Q + 1;  -- up counting
                end if ;
               end if ;
              end if;
        end process;
        Q <= TEMP_Q;
end counter_arch;
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY counter_tb IS
END counter_tb;

ARCHITECTURE behavior OF counter_tb IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT counter
    PORT(
         CLK : IN  std_logic;
         RST : IN  std_logic;
         Q : OUT  std_logic_vector(3 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal CLK : std_logic := '0';
   signal RST : std_logic := '0';

        --Outputs
   signal Q : std_logic_vector(3 downto 0);

   -- Clock period definitions
BEGIN

        -- Instantiate the Unit Under Test (UUT)
   uut: counter PORT MAP (
          CLK => CLK,
          RST => RST,
          Q => Q
        );

   -- Clock process definitions
   CLK_process :process
   begin
                CLK <= '0';
                wait for 5 ns;
                CLK <= '1';
                wait for 5 ns;
   end process;


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
```

```
      RST <= '1';
                wait for 20 ns;
      RST <= '0';
                wait for 200 ns;
      RST <= '1';
                wait for 10 ns;
      RST <= '0';
                wait for 300 ns;
   end process;

END;
```

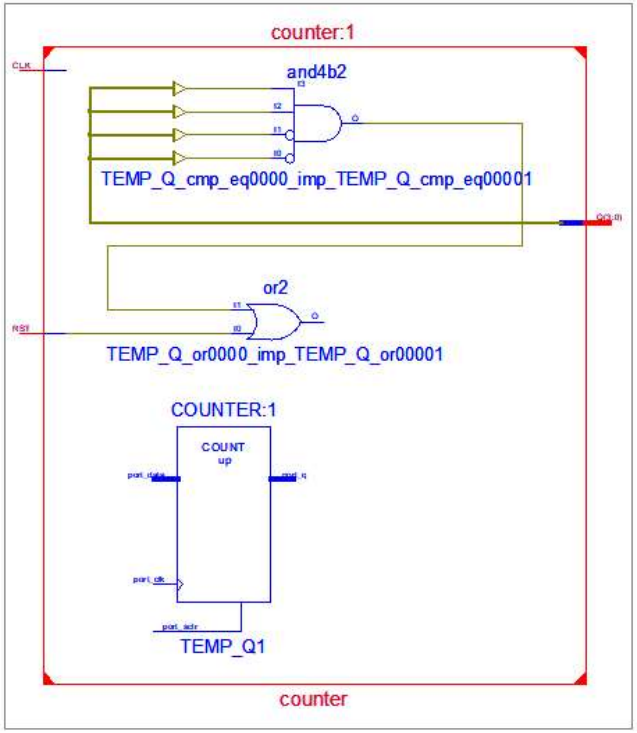

Float (P.20131013) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
1.00us
Re-launch
0.000 ns
Name
Value
clk
0
rst
1
q[3:0]
U
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
350 ns
400 ns
450 ns
500 ns
X1: 0.000 ns
Default.wcfg*
ENG
05:32 PM
20-10-2024

```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : counter.ngr
Top Level Output File Name         : counter
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 6

Cell Usage :
# BELS                             : 6
#      INV                         : 1
#      LUT2                        : 1
#      LUT2_L                      : 1
#      LUT3                        : 1
#      LUT4                        : 2
# FlipFlops/Latches                : 4
#      FDR                         : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 5
#      IBUF                        : 1
#      OBUF                        : 4
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                        3  out of   2448     0%
 Number of Slice Flip Flops:              4  out of   4896     0%
 Number of 4 input LUTs:                  6  out of   4896     0%
 Number of IOs:                           6
 Number of bonded IOBs:                   6  out of    158     3%
 Number of GCLKs:                         1  out of     24     4%

---------------------------
```


ISE Schematic Viewer (P.20131013) - [counter (RTL1)]
File Edit View Window Layout Help
counter
CLK
RST
Q(3:0)
Output Pin: Q(3:0) =>
counter
counter (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
Pins
Signals
Name
Value
counter
ENG
05:38 PM
20-10-2024

ISE Schematic Viewer (P.20131013) - [counter (RTL1)]

File Edit View Window Layout Help




counter (RTL1)



ENG 05:39 PM 20-10-2024

# Expt. 5

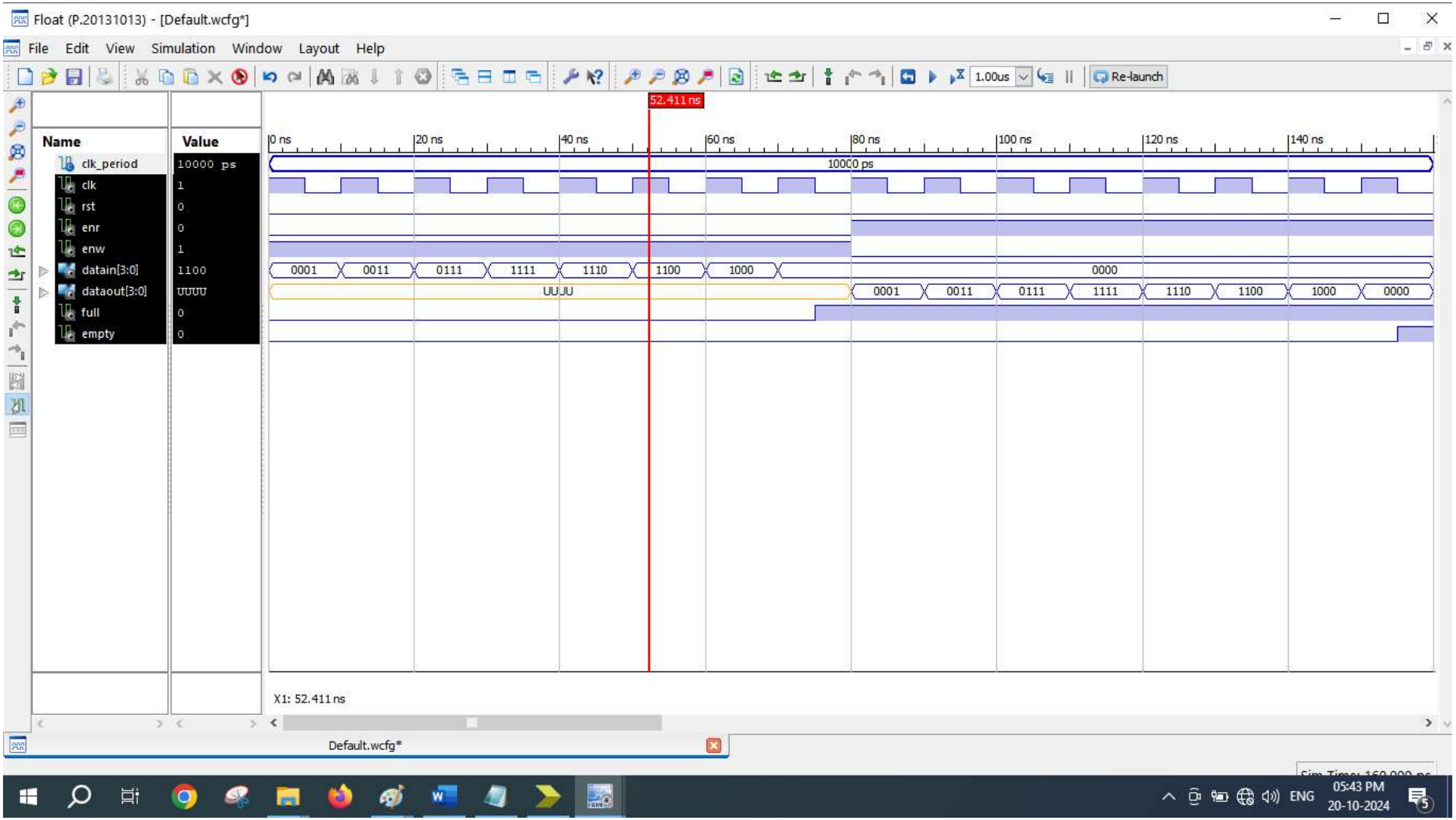
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
use IEEE.STD_LOGIC_arith.ALL;



-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity FIFO_4bit is
    Port ( clk,rst : in  STD_LOGIC;
           enr,enw : in  STD_LOGIC;
           datain : in  STD_LOGIC_VECTOR (3 downto 0);
           dataout : out  STD_LOGIC_VECTOR (3 downto 0);
           full,empty : out  STD_LOGIC);
end FIFO_4bit;

architecture Behavioral of FIFO_4bit is

type memory_type is array (0 to 7) of std_logic_vector(3 downto 0);

                signal memory : memory_type;

                signal readptr,writeptr : std_logic_vector(3 downto 0):="0000";

                --signal cnt:std_logic_vector(24 downto 0);

                --signal clk1:std_logic;
begin

        FIFO_Process: process(clk)

                begin

                if(clk'event and clk='1' and enw ='1' and enr='0') then --WRITE
OPERATION

                                        memory(conv_integer(writeptr)) <= datain;

                                        writeptr <= writeptr + '1';

                end if;
```

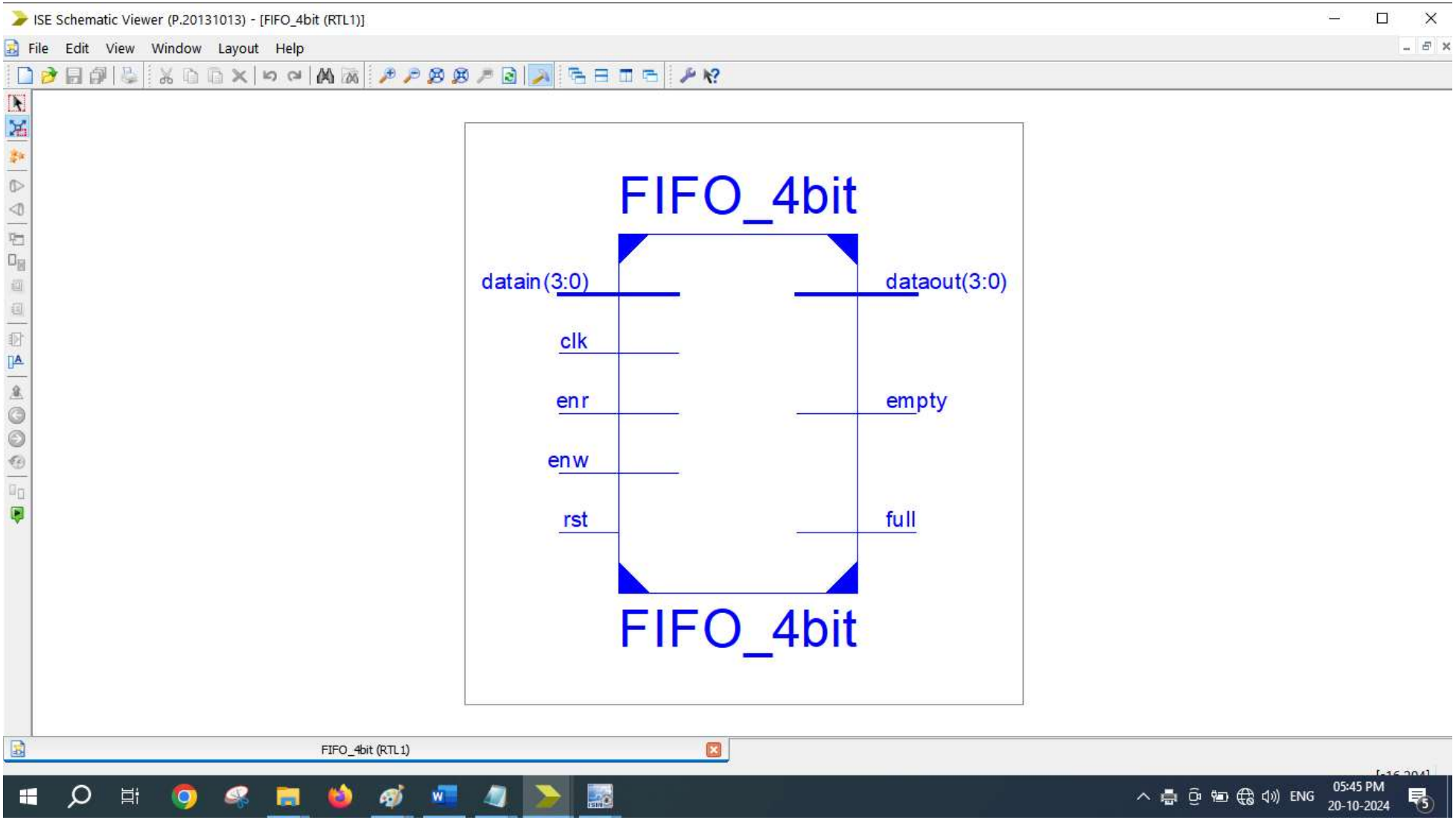
```
                if(clk'event and clk='1' and enr ='1' and enw='0') then  --READ
OPERATION
                                        dataout <= memory(conv_integer(readptr));
                                        readptr <= readptr + '1';
                end if;
                if(readptr = "1000") then
                                empty<='1';
                else
                                empty<='0';
                end if;
                if(writeptr = "1000") then
                                full <='1';
                else
                                full <='0';
                end if;
        end process;
end Behavioral;
```

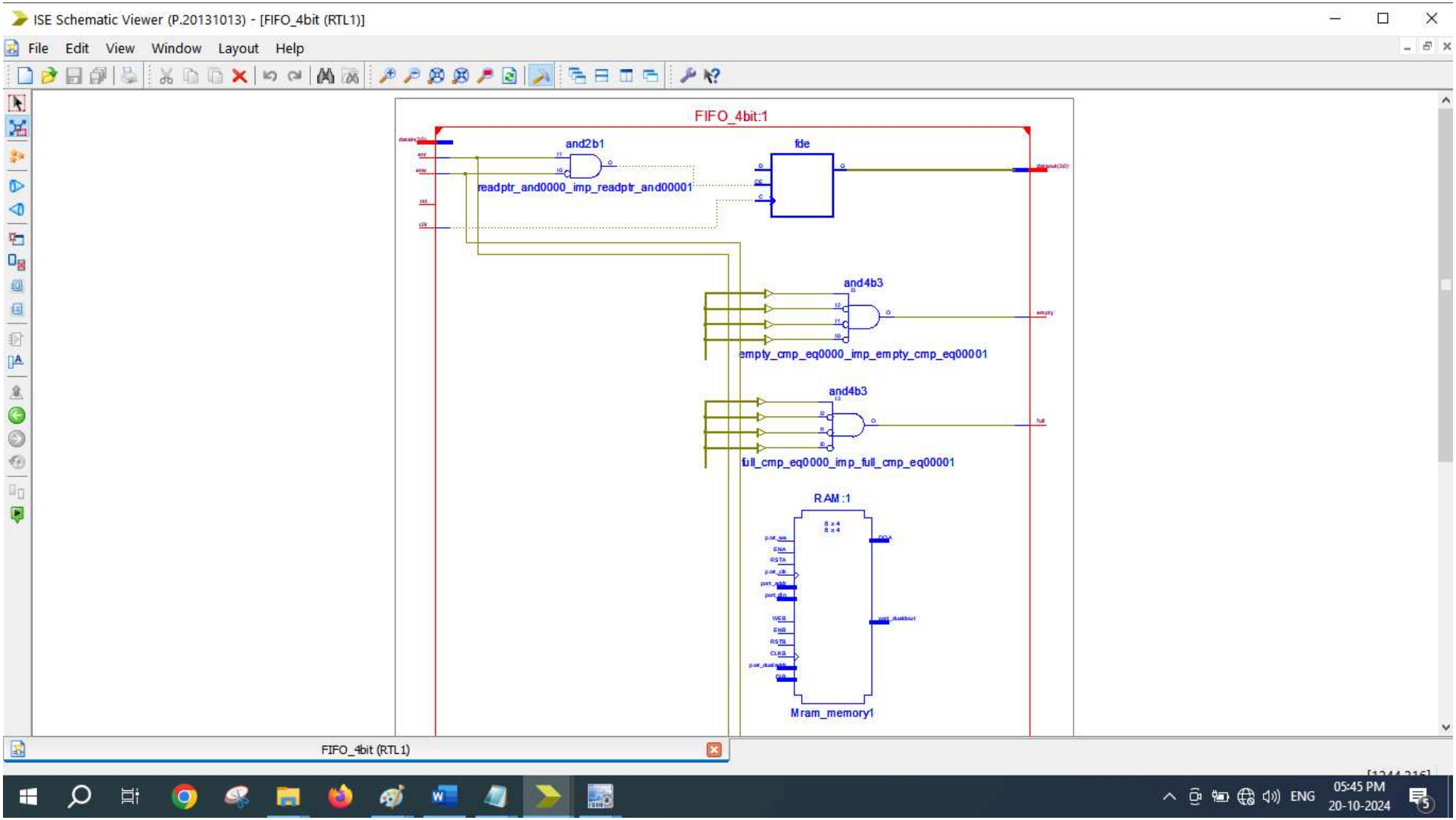
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY test1 IS
END test1;

ARCHITECTURE behavior OF test1 IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT FIFO_4bit
    PORT(
         clk : IN  std_logic;
         rst : IN  std_logic;
         enr : IN  std_logic;
         enw : IN  std_logic;
         datain : IN  std_logic_vector(3 downto 0);
         dataout : OUT  std_logic_vector(3 downto 0);
         full : OUT  std_logic;
         empty : OUT  std_logic
        );
    END COMPONENT;


   --Inputs
   signal clk : std_logic := '0';
   signal rst : std_logic := '0';
   signal enr : std_logic := '0';
   signal enw : std_logic := '0';
   signal datain : std_logic_vector(3 downto 0) := (others => '0');

        --Outputs
   signal dataout : std_logic_vector(3 downto 0);
   signal full : std_logic;
   signal empty : std_logic;

   -- Clock period definitions
   constant clk_period : time := 10 ns;

BEGIN

        -- Instantiate the Unit Under Test (UUT)
   uut: FIFO_4bit PORT MAP (
          clk => clk,
          rst => rst,
          enr => enr,
```

```
       enw => enw,
       datain => datain,
       dataout => dataout,
       full => full,
       empty => empty
     );

-- Clock process definitions
clk_process :process
begin
             clk <= '1';
             wait for 5 ns;
             clk <= '0';
             wait for 5 ns;
end process;


-- Stimulus process
stim_proc: process
begin
                              enw<='1';
                              enr<='0';
                              datain<="0001";
                              wait for 10ns;

                              datain<="0011";
                              wait for 10ns;

                              datain<="0111";
                              wait for 10ns;

                              datain<="1111";
                              wait for 10ns;

                              datain<="1110";
                              wait for 10ns;

                              datain<="1100";
                              wait for 10ns;

                              datain<="1000";
                              wait for 10ns;

                              datain<="0000";
                              wait for 10ns;
```

```
                                    enw<='0';
                                    enr<='1';
                                    wait for 80ns;


  end process;

END;
```


Float (P.20131013) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
Re-launch
52.411 ns
Name
Value
clk_period
10000 ps
clk
1
rst
0
enr
0
enw
1
datain[3:0]
1100
dataout[3:0]
UUUU
full
0
empty
0
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
10000 ps
0001
0011
0111
1111
1110
1100
1000
0000
UUUU
X1: 52.411 ns
Default.wcfg*
ENG
05:43 PM
20-10-2024


ISE Schematic Viewer (P.20131013) - [FIFO_4bit (RTL1)]
File Edit View Window Layout Help
FIFO_4bit
datain(3:0)
clk
enr
enw
rst
dataout(3:0)
empty
full
FIFO_4bit
FIFO_4bit (RTL1)
ENG
05:45 PM
20-10-2024


ISE Schematic Viewer (P.20131013) - [FIFO_4bit (RTL1)]
File Edit View Window Layout Help
FIFO_4bit:1
and2b1
readptr_and0000_imp_readptr_and00001
fde
and4b3
empty_cmp_eq0000_imp_empty_cmp_eq00001
and4b3
full_cmp_eq0000_imp_full_cmp_eq00001
RAM:1
Mram_memory1
FIFO_4bit (RTL1)
ENG
05:45 PM
20-10-2024

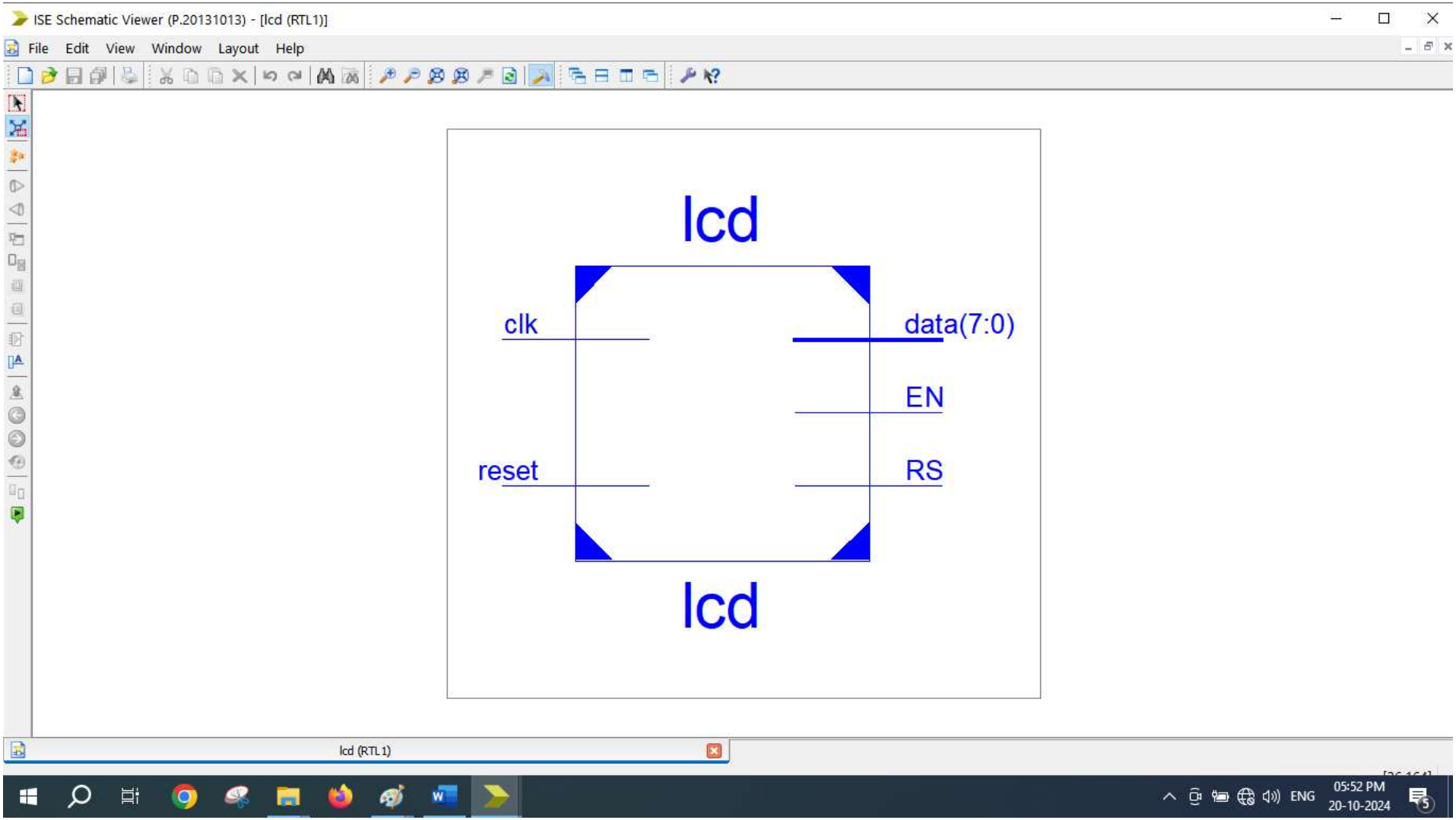
```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : FIFO_4bit.ngr
Top Level Output File Name         : FIFO_4bit
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 14

Cell Usage :
# BELS                             : 13
#      GND                         : 1
#      INV                         : 2
#      LUT2                        : 4
#      LUT3                        : 2
#      LUT4                        : 4
# FlipFlops/Latches                : 12
#      FDE                         : 12
# RAMS                             : 4
#      RAM16X1D                    : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 12
#      IBUF                        : 6
#      OBUF                        : 6
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                       10  out of   2448     0%
 Number of Slice Flip Flops:             12  out of   4896     0%
 Number of 4 input LUTs:                 20  out of   4896     0%
    Number used as logic:                12
    Number used as RAMs:                  8
 Number of IOs:                          14
 Number of bonded IOBs:                  13  out of    158     8%
 Number of GCLKs:                         1  out of     24     4%

---------------------------
```

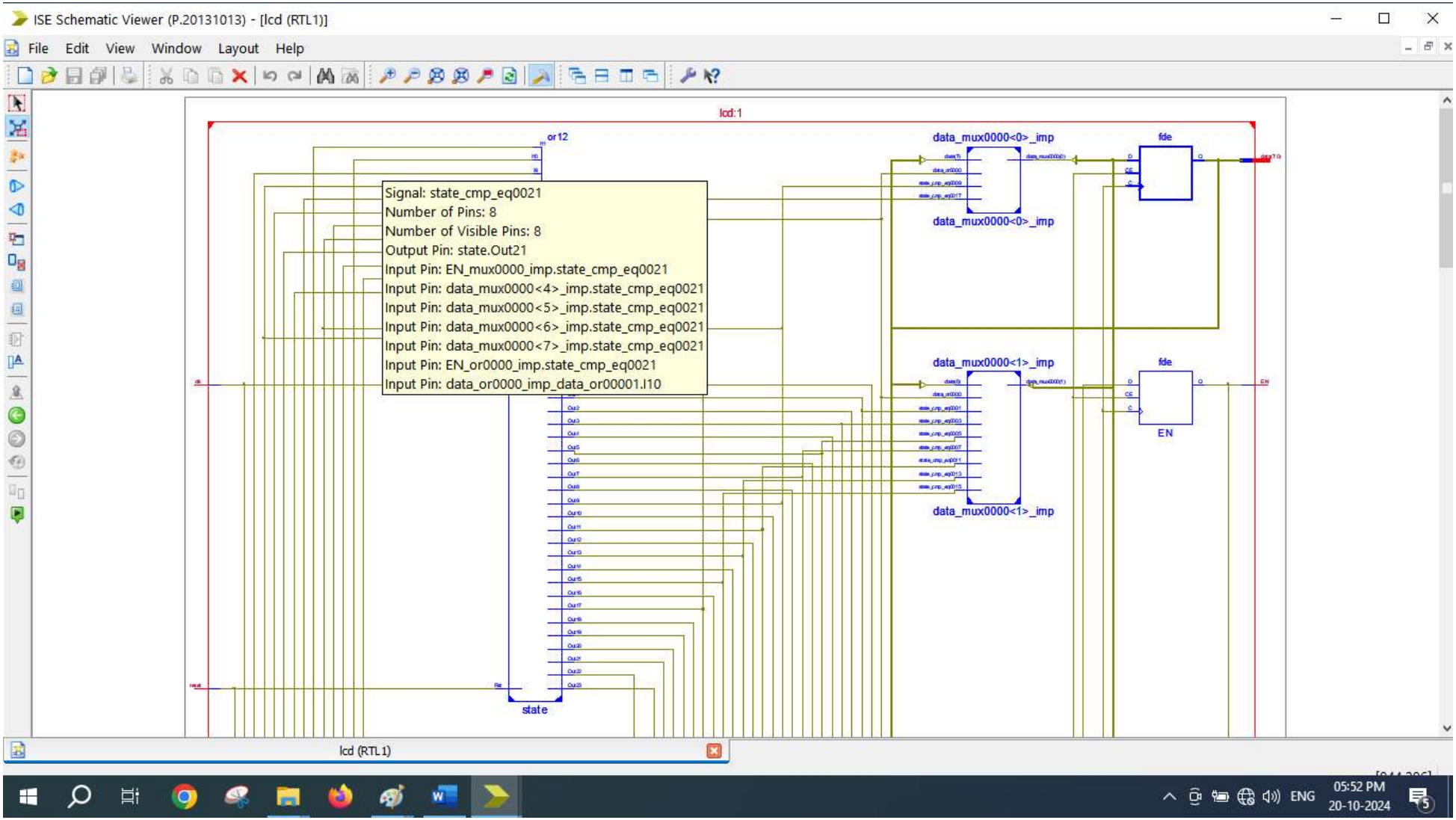
# Expt. 6

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity lcd is
    Port ( clk,reset : in std_logic;
           RS,EN : out std_logic;
           data : out std_logic_vector(7 downto 0));
end lcd;
architecture Behavioral of lcd is
    type state_type is (s0,s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s11,
    s12,s13,s14,s15,s16,s17,s18,s19,s20,s21,s22,s23);
    signal state:state_type;
begin
        process(clk, reset, state)
        begin
           if reset = '1' then
                        state <= s0;
                elsif rising_edge(clk) then
                        if state = s0 then
                                state <= s1;
                                RS<='0'; -- Write commands to LCD.
                                EN <= '1';
                                data <= "00110000"; -- Function set for 8 bit
interface, 1 line mode and 5x7 dot matrix.
                        end if;
                        if state = s1 then
                                state <= s2;
                                EN <= '0';
                        end if;
                        if state = s2 then
                                state <= s3;
                                EN <= '1';
                                data <= "00001111"; -- Display cursor and blinking
ON.
                        end if;
                        if state = s3 then
                                state <= s4;
                                EN <= '0';
                        end if;
                        if state = s4 then
                                state <= s5;
                                EN <= '1';
                                data <= "00000001";     -- Clear display.
                        end if;
                        if state = s5 then
                                state <= s6;
                                EN <= '0';
                        end if;
                        if state = s6 then
```

```
            state <= s7;
            EN <= '1';
            data <= "10000100"; -- Display address.
   end if;
   if state = s7 then
            state <= s8;
            EN <= '0';
   end if;
   if state = s8 then
            RS <= '1';  -- Write data to LCD.
            state <= s9;
            EN <= '1';
            data <= "01010111"; --W
   end if;
   if state = s9 then
            state <= s10;
            EN <= '0';
   end if;
if state = s10 then
            state <= s11;
            EN <= '1';
            data <= "01000101"; --E
   end if;
   if state = s11 then
            state <= s12;
            EN <= '0';
   end if;
   if state = s12 then
            state <= s13;
            EN <= '1';
            data <= "01001100"; --L
   end if;
   if state = s13 then
            state <= s14;
            EN <= '0';
   end if;
   if state = s14 then
            state <= s15;
            EN <= '1';
            data <= "10110000"; --(-)
   end if;
   if state = s15 then
            state <= s16;
            EN <= '0';
   end if;
   if state = s16 then
            state <= s17;
            EN <= '1';
            data <= "01000011"; --C
   end if;
```

```
                        if state = s17 then
                                state <= s18;
                                EN <= '0';
                        end if;
                         if state = s18 then
                                state <= s19;
                                EN <= '1';
                                data <= "01001111"; --O
                        end if;
                        if state = s19 then
                                state <= s20;
                                EN <= '0';
                        end if;
                        if state = s20 then
                                state <= s21;
                                EN <= '1';
                                data <= "01001101"; --M
                        end if;
                        if state = s21 then
                                state <= s22;
                                EN <= '0';
                        end if;
                        if state = s22 then
                                state <= s23;
                                EN <= '1';
                                data <= "01000101"; --E
                        end if;
                        if state = s23 then
                                EN <= '0';
                        end if;
                end if;
        end process;
end Behavioral;
```


ISE Schematic Viewer (P.20131013) - [lcd (RTL1)]
File Edit View Window Layout Help
lcd
clk
reset
data(7:0)
EN
RS
lcd
lcd (RTL1)
ENG
05:52 PM
20-10-2024


ISE Schematic Viewer (P.20131013) - [lcd (RTL1)]
File Edit View Window Layout Help
lcd:1
or12
Signal: state_cmp_eq0021
Number of Pins: 8
Number of Visible Pins: 8
Output Pin: state.Out21
Input Pin: EN_mux0000_imp.state_cmp_eq0021
Input Pin: data_mux0000<4>_imp.state_cmp_eq0021
Input Pin: data_mux0000<5>_imp.state_cmp_eq0021
Input Pin: data_mux0000<6>_imp.state_cmp_eq0021
Input Pin: data_mux0000<7>_imp.state_cmp_eq0021
Input Pin: EN_or0000_imp.state_cmp_eq0021
Input Pin: data_or0000_imp_data_or00001.I10
data_mux0000<0>_imp
fde
data_mux0000<0>_imp
data_mux0000<1>_imp
fde
EN
data_mux0000<1>_imp
state
lcd (RTL1)
ENG
05:52 PM
20-10-2024

```
=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : lcd.ngr
Top Level Output File Name         : lcd
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 12

Cell Usage :
# BELS                             : 30
#      GND                         : 1
#      INV                         : 1
#      LUT2_L                      : 2
#      LUT3                        : 1
#      LUT3_D                      : 1
#      LUT3_L                      : 3
#      LUT4                        : 17
#      LUT4_L                      : 3
#      VCC                         : 1
# FlipFlops/Latches                : 34
#      FDC                         : 22
#      FDCE                        : 1
#      FDE                         : 10
#      FDP                         : 1
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 11
#      IBUF                        : 1
#      OBUF                        : 10
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s250epq208-5

 Number of Slices:                       24  out of   2448     0%
 Number of Slice Flip Flops:             34  out of   4896     0%
 Number of 4 input LUTs:                 28  out of   4896     0%
 Number of IOs:                          12
 Number of bonded IOBs:                  12  out of    158     7%
 Number of GCLKs:                         1  out of     24     4%

---------------------------
```