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Career Objective

A highly motivated B.Tech graduate in Electronics and Communication Engineering with a strong foundation in VLSI Physical Design. Proficient in ASIC design flow including synthesis, floorplanning, placement, CTS, routing, and STA. Hands-on experience with industry-standard EDA tools. Committed to delivering high-quality semiconductor designs and growing as a skilled Physical Design Engineer.

Education

sree vidyanikethan engineering college,Tirupati, Andhra Pradesh	2025
Bachelor of Technology (B.Tech) | Electronics and Communication Engineering |Tirupati |Andhra Pradesh	C.G.P.A: 8.93
Government Polytechnic Kalyanadurg, kalyandure, Andhra Pradesh	2022
Polytechnic| ECE | State Board of Technical Education and Training Andhra Pradesh	Percentage:82.5
Karanam Chikappa Government High School, Kalyandurg, Andhra Pradesh	2019
SSC | State Board of Secondary Education|Andhra Pradesh	C.G.P.A: 8.7

Professional Training

- Completed Physical Design Course from February 2025 to August 2025 in Takshila Institute of VLSI technologies.
- Good Understanding of block level Physical design and verification concepts like **Floor planning, PLACEMENT, ROUTING, CTS, STA, DRC/LVS etc.**
- Practical exposure to Physical Design tools from **IC Compiler** tools.

Technical Skills

- Strong understanding in the RTL to GDSII flow or design implementation.
- Good in concepts related to synthesis, place and route, CTS .
- Good knowledge and experience in Block-level Floor-planning and Physical verification.
- Working experience with tools like ICC.
- Strong knowledge in standard place and route flows ICC/Synopsys flows preferred.
- Well versed with timing constraints and STA.
- Good knowledge of Windows and Linux
- TCL, Python
- Synthesis: Design compiler
- PNR: ICC1
- **Extra Tools & Platforms**: OpenLane, Yosys, Openroad, Xilinx, EDA Playground, GitHub, MATLAB, P-spice, LabVIEW

PROJECT WORKED ON:

Title		I.ORCA_TOP,	II.ORCA_TOP_IO
Tool used	IC Compiler		
Description	• Technology: • No. of macros: • Layer: • Std. cell count: • No. of Clocks: • frequency:	32nm 40 9 56013 7 416 Mgh	28nm 30 9 50000 7 400 Mgh
Responsibilities	Iterative Floorplan, IO ports placement, Power planning, Placement and CTS reviews, Routing and DRC checks, Timing Closure and ECO		

Certifications

- **Takshila Institute of VLSI Technologies**
- **Title:** Professional Training on Physical Design.

Internships

Integrated VLSI Internship | **SURE TRUST (**Remote**) |** **Oct 2024 – Aug 2025**

- RTL to GDSII.
- DFT: Scan chains, fault models.
- **Physical Design**: Floorplan, Placement, CTS**,** routing, timing closure and DRC, LVS.
- **STA:** Setup/hold checks, slack analysis.

PROJECT WORKED ON:

Title	RISC-V Core Physical Design (picorv32)
Tool Used	OpenLane
Technology	130nm (Sky130)
Clocks	1
Frequency	208 MHz
Std. Cells	~17,000
Responsibilities	RTL to GDS flow: Synthesis, Floorplan, Power Plan, Placement, CTS, Routing, DRC/LVS, STA

Academic Project

AES Encryption & Decryption | Verilog HDL |Jan 2025 – May 2025

- Implemented AES algorithm for secure data transmission.
- Designed pipelined architecture to improve speed and efficiency.
- Verified functionality using testbenches and waveform analysis.
- Optimized RTL for better area, timing, and synthesis results.
- Prepared design for backend physical implementation.

Interpersonal Skills

- Leadership, Positive Attitude, Teamwork, Self- Management, Good Time Management

Awards and Achivments

- **National** Player in Softball and Baseball, two-time **national medalist.**
- **NMMS** Scholar for academic excellence.
- **ECET Rank: 428**

Declaration

- I declare that the information given above is true to the best of my knowledge.

Date:18/08/2025

Place: Bengaluru Boya yerriswamy