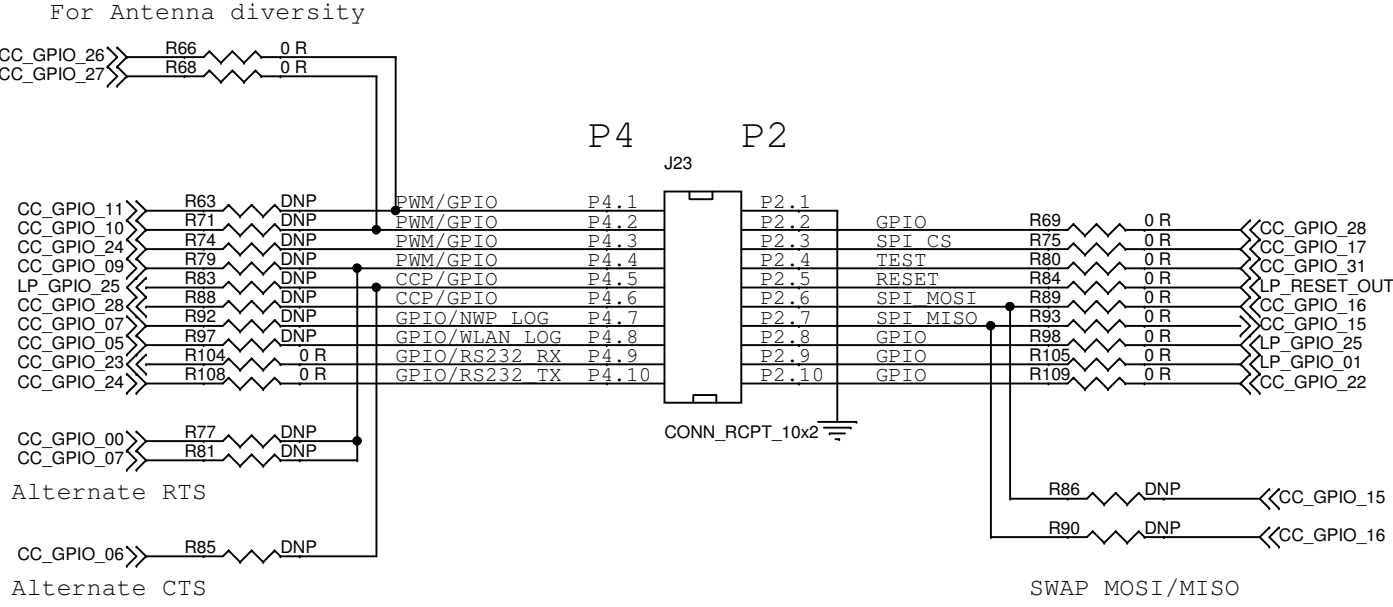
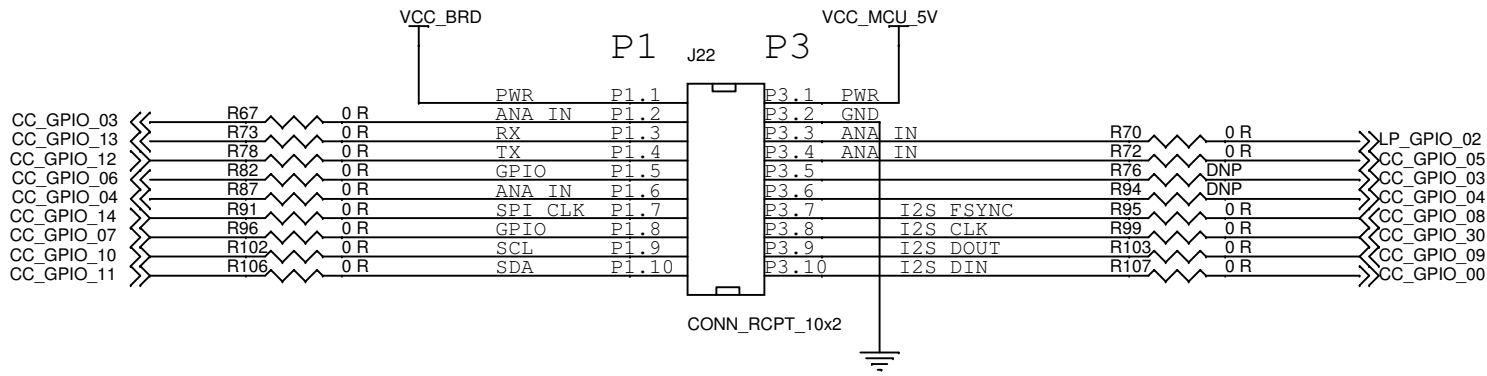
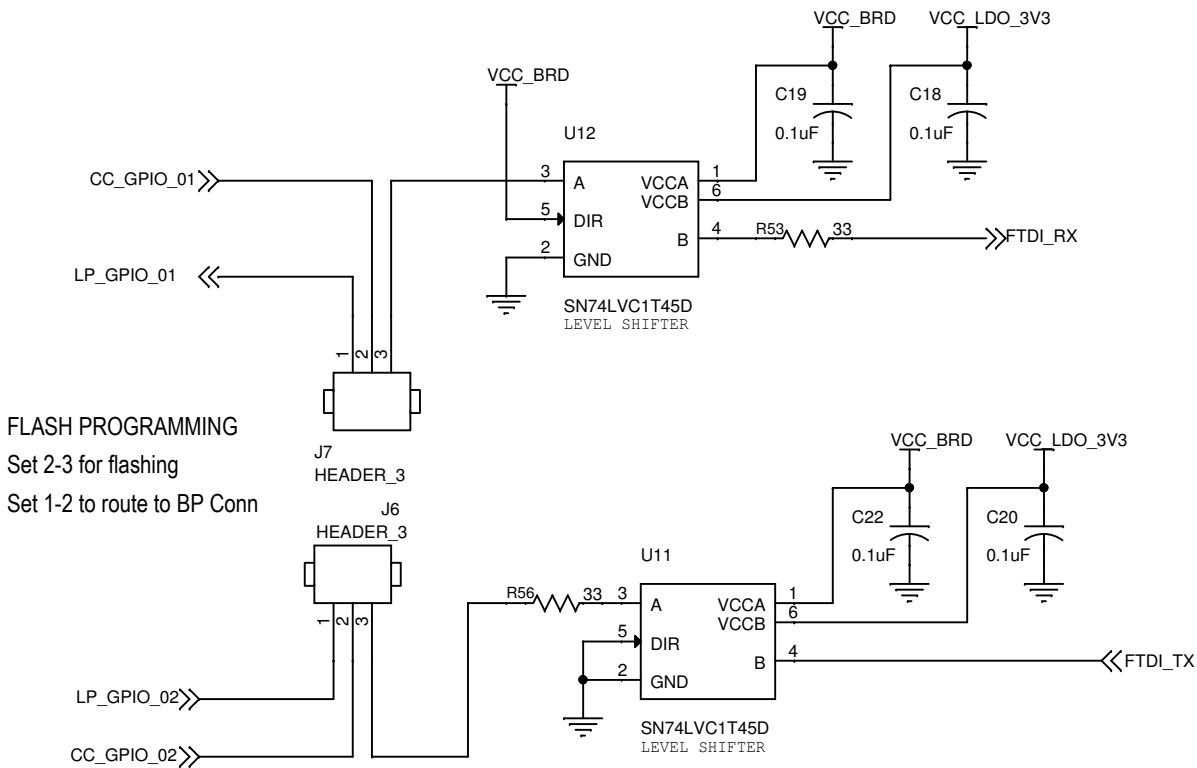


BOOSTER PACK INTERFACE

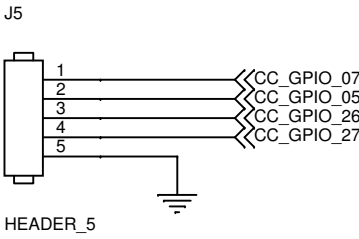


UART MUXING



TEST POINTS

OBSERVE NWP & MAC LOG



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The schematic diagram illustrates the interface circuit for the BRD_JTAG_TCK, BRD_JTAG_TDI, BRD_JTAG_TMS, and BRD_JTAG_TDO signals. The circuit is powered by VCC_LDO_3V3 and includes various resistors (R11, R16, R19, R25, R29, R49) and a capacitor (C3).

Inputs and Signals:

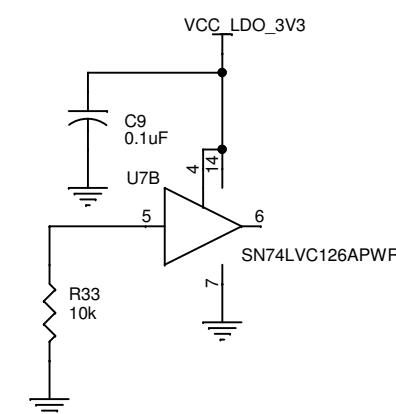
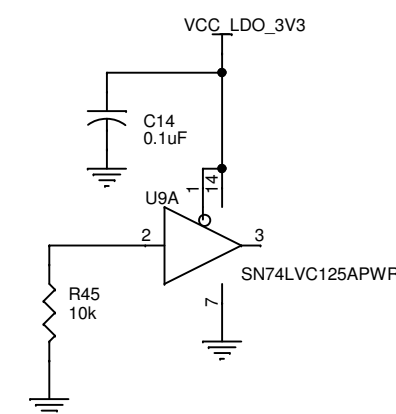
- FT_SK
- FT_DO
- DBGMOD
- DBGEn
- FT_CS
- FT_DI


Components and Connections:

- SN74LVC125APWR (U4A, U4B, U4C, U4D):** Monostable multivibrators used for signal conditioning.
 - U4A: Input 2 (DBGMOD), Output 3 (FT_SK).
 - U4B: Input 5 (DBGEn), Output 6 (FT_DO).
 - U4C: Input 9 (FT_SK), Output 8 (BRD_JTAG_TDI).
 - U4D: Input 12 (FT_SK), Output 11 (BRD_JTAG_TCK).
- SN74LVC126APWR (U7A, U7B, U7C, U7D):** Buffer/drivers used for signal conditioning.
 - U7A: Input 2 (FT_DI), Output 3 (FT_DI).
 - U7B: Input 11 (FT_DI), Output 12 (FT_DI).
 - U7C: Input 9 (FT_CS), Output 8 (BRD_JTAG_TMS).
 - U7D: Input 11 (FT_CS), Output 12 (BRD_JTAG_TDO).

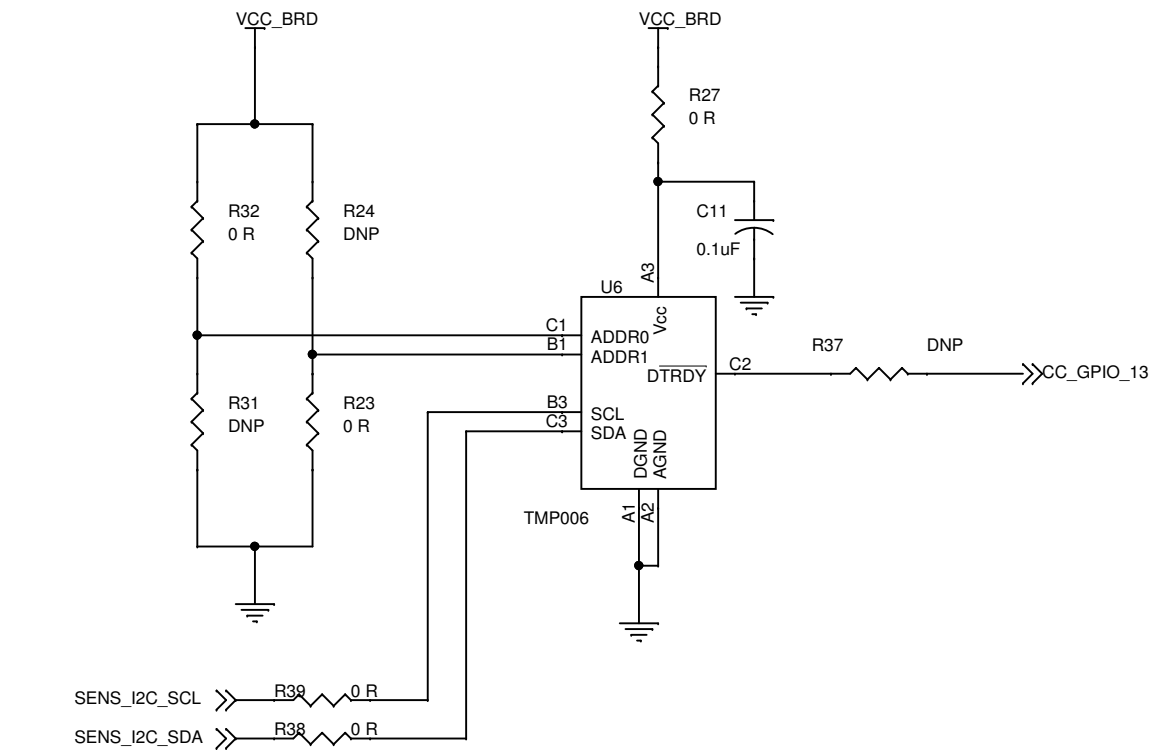
Resistors and Capacitors:

- R11: 10k, connected to VCC_LDO_3V3 and FT_DO.
- R16: 10k, connected to VCC_LDO_3V3 and FT_DO.
- R19: 33, connected to VCC_LDO_3V3 and BRD_JTAG_TDI.
- R25: 33, connected to VCC_LDO_3V3 and BRD_JTAG_TDO.
- R29: 33, connected to VCC_LDO_3V3 and BRD_JTAG_TMS.
- R49: 10k, connected to VCC_LDO_3V3 and FT_DI.
- C3: 0.1uF, connected to VCC_LDO_3V3 and FT_DO.

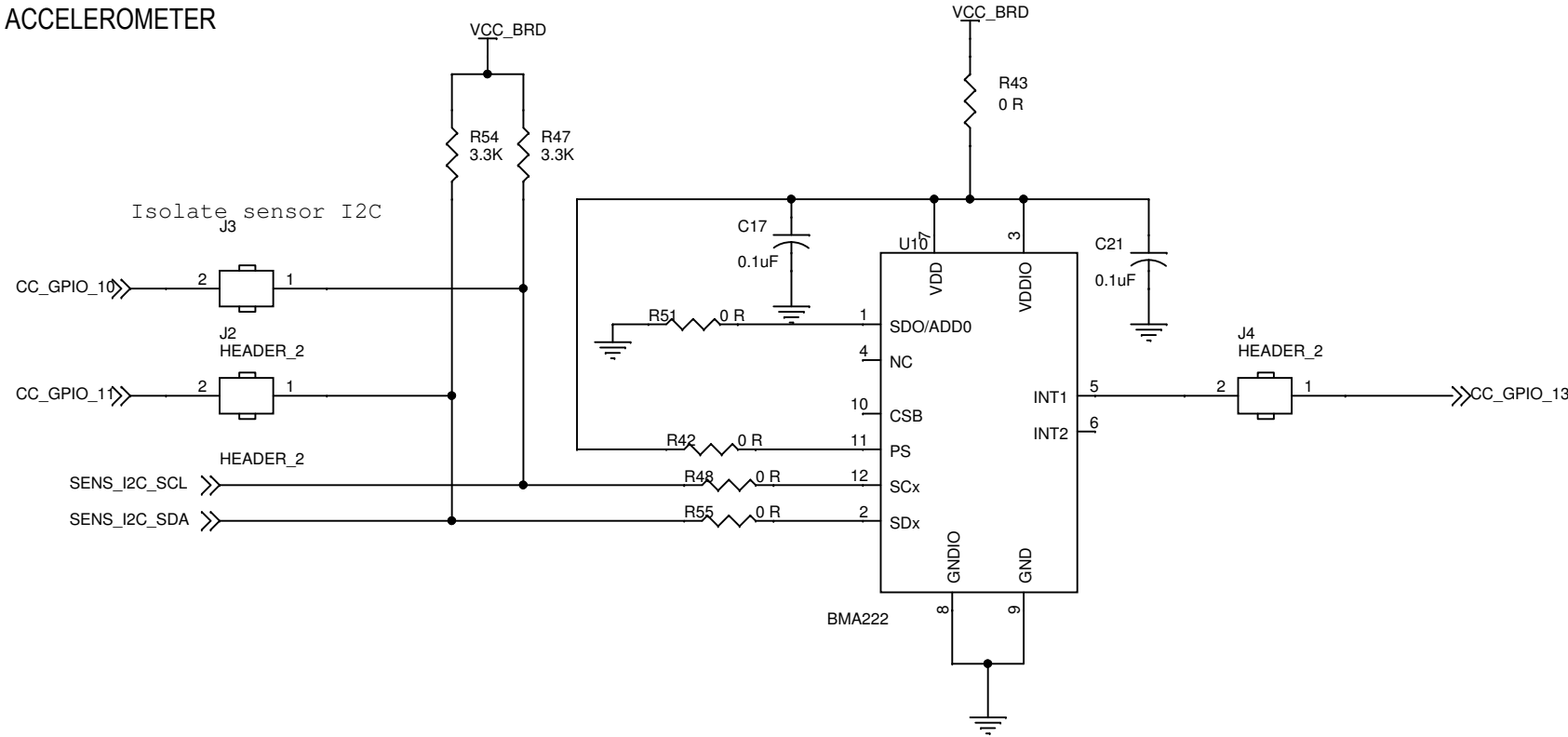


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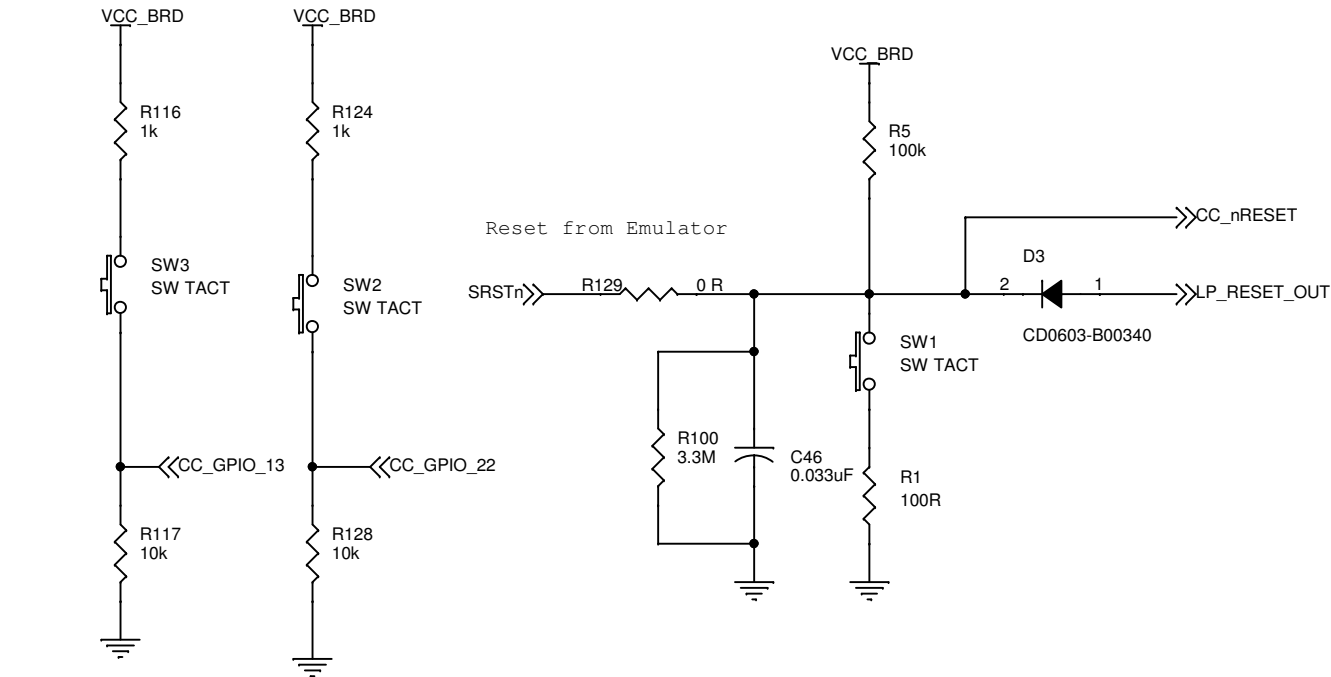
TEMP SENSOR



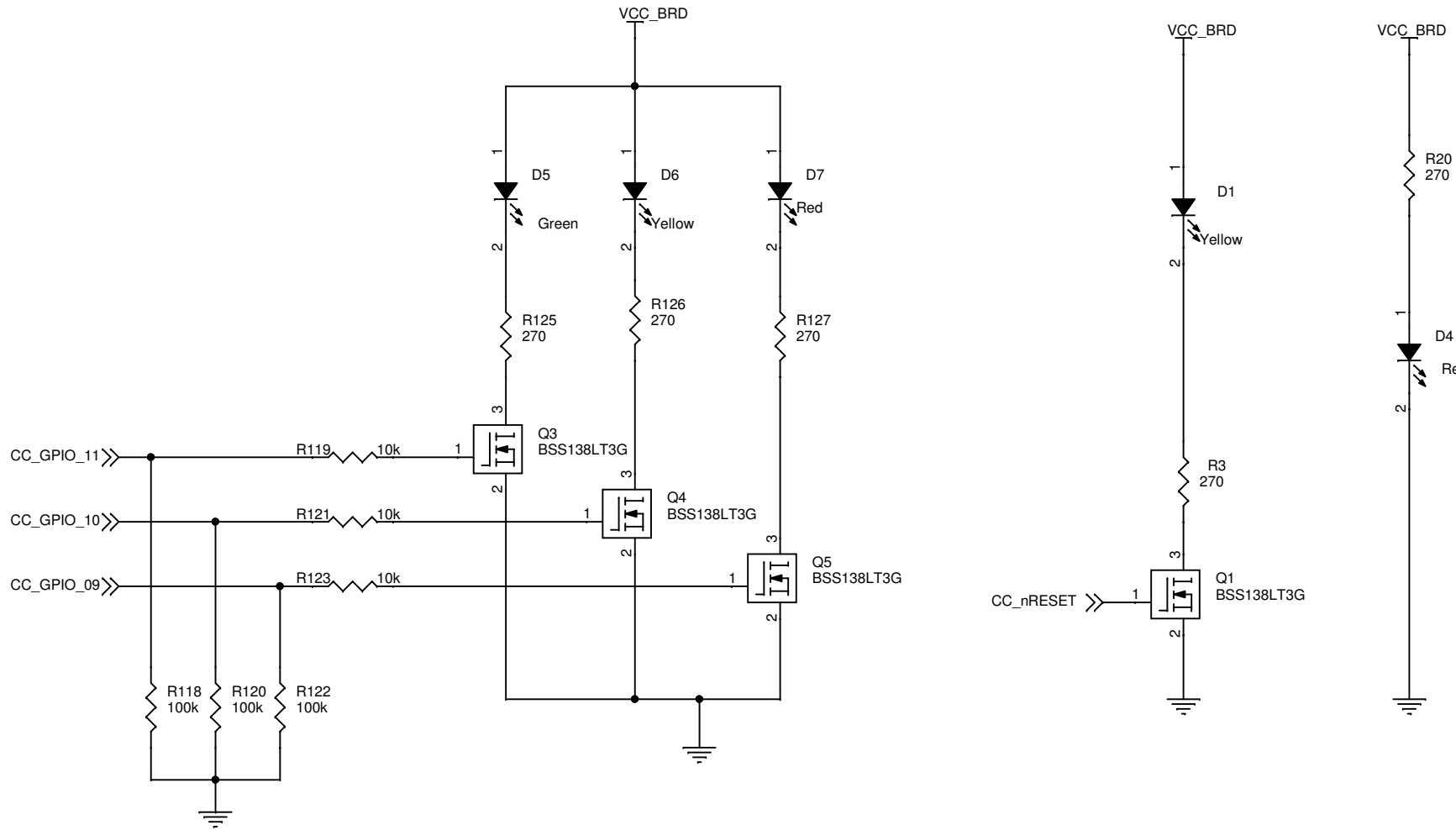
ACCELEROMETER



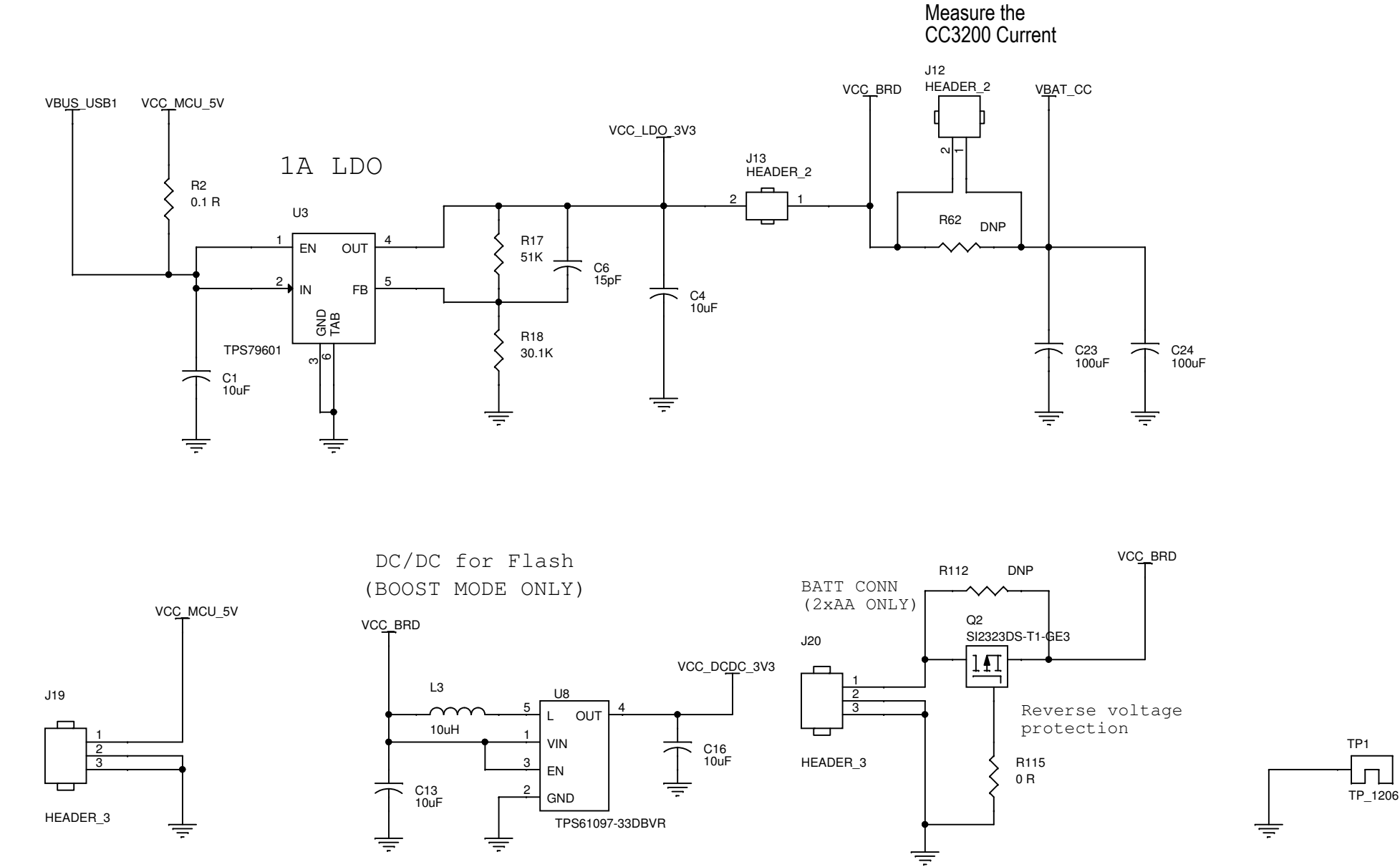
SWITCHES & RESET



LED INDICATORS



POWER MANAGEMENT



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