Applying Verified Z3 Proof Checking to Ladder Logic Verification of Railway Interlockings

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Abstract. Railway systems are safety critical and demand the highest levels of assurance for their control software. Formal verification tools, used alongside conventional testing, are essential for ensuring compliance with stringent safety and regulatory standards. In this article, we present a solution with the goal to be part of a future verification toolchain involving Z3 SAT/SMT solving and to be certified at Safety Integrity Level 4 (SIL4). We demonstrate this via a verified and formally extracted SAT proof checker in the context of Ladder Logic verification. Our approach is tailored to the needs of our industrial partner, adaptable, and also extendable to include further SMT theories. Our proof checker currently works for Z3's full propositional proof output, including Tseitin transformations. A checker for Z3 proofs of CNF formulas has been formalised and verified in Rocq, with a certified OCaml implementation extracted from the proof, whilst the full extendable framework including RUP inferences and Tseitin transformation has been fully verified in Agda. Our approach enables formal reasoning about Z3 outputs in both theorem provers. Finally, we demonstrate the entire approach with a small case study, and provide results on the scalability on an industrial level.

Keywords: Railway Verification · Verification · Proof Checking · Coq · Rocq · Ladder Logic · Interlocking Systems · Z3 · SAT solving · SMT solving · RUP · Tseitin transformation.

1 Introduction

Railway systems are among the most safety-critical infrastructures, where software failures can have severe consequences. To ensure safety and regulatory compliance, railway control systems, particularly interlockings, must be validated against formalised safety requirements, such as those defined by Network Rail in the UK [1]. These are based on operational procedures, historical incidents, and formal design rules. Validation typically involves weeks of testing, and any failure requires costly redesign and retesting. To mitigate this, formal verification tools (see e.g. [2]–[4]) are increasingly used early in development. These tools automatically check interlocking designs against formal safety properties, helping to catch issues before physical testing. One such tool is the Ladder Logic

Verifier [5], which targets interlockings written in ladder logic [6], a graphical language defined by the IEC 61131 standard [7]. The approach proves the unreachability of unsafe states by demonstrating the unsatisfiability of the negated safety property. Many verification tools use Z3 [8], a leading SMT solver, but its internal complexity makes independent validation challenging. To support Safety Integrity Level 4 (SIL4) certification, we adopt a proof-checking approach (e.g. [9]) that verifies Z3's unsatisfiability proofs rather than the solver itself. This ensures interlockings proceed to industrial testing only after both verification and proof validation are complete (Fig. 1).

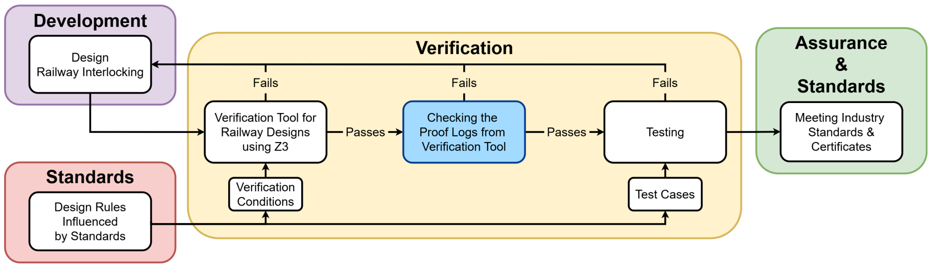

Development
Design Railway Interlocking
Verification
Fails
Fails
Fails
Verification Tool for Railway Designs using Z3
Passes
Checking the Proof Logs from Verification Tool
Passes
Testing
Assurance & Standards
Meeting Industry Standards & Certificates
Standards
Design Rules Influenced by Standards
Verification Conditions
Test Cases

Fig. 1: Proposed railway interlocking design methodology: The interlocking and the safety properties are translated into SMTLIB [10] for analysis with Z3. If successful, then our proof checker validates the proof log of unsatisfiability. Only if both are successful, then industrial testing takes place.

We present a formally verified proof checker for Z3's RUP (Reverse Unit Propagation) proof format, introduced in 2022 [11]. The RUP checker, developed entirely in the Rocq proof assistant [12] and extracted to OCaml [13]–[15], validates full propositional proofs, including Tseitin transformations[3]. However, here only the RUP steps are fully verified. We also introduce a prototype full checker for verifying both Tseitin and RUP steps as part of a broader, extensible toolchain in Agda. This enables independent validation of solver outputs and provides a certifiable link between SMT solving and formal proof checking. Our approach integrates with Rocq/Agda, verifying the actual program rather than just the algorithm. It is designed to be extensible and adaptable to future changes in Z3's proof format, ensuring long-term maintainability. Currently, it deals with general propositional formulas, not just CNFs [17]. Developed in collaboration with our industrial partner, who required the use of Z3 due to its certification status, the checker has been evaluated on industrial-scale interlocking systems. While our current focus is on discrete interlockings written in ladder logic, the methodology is generalisable to modern railway systems such as ERTMS and the verification of scheme plan data [4]. By independently validating solver outputs, our approach eliminates a key point of failure in automated verification pipelines. It contributes directly to certification efforts and strengthens safety assurance in railway software engineering.

[3] The Agda implementation of the RUP checker has been presented in [16], the formalisation in Rocq and the treatment of Tseitin is new.

Related Work. SAT/SMT competitions nowadays require not just answers but also independently checkable unsatisfiability proofs. This has driven extensive research into proof checking and reconstruction across using different proof formats and tools (see e.g. [18]–[29]).[4] The currently fastest verified SAT Checker is presented in [30] using LRAT, a modification of the DRAT format.

Recent work using cvc5 [31]–[33] provides a good framework for SMT proof checking and also introduces a modular proof architecture intended to support integration with in SMTCoq, Isabelle and Lean. Feng et al. [34] provide and approach to SMT proof checking SAT Modulo Monotonic Theories using MONOSAT. Finally, the Lambdapi proof checker project [35] aims at providing a platform to exchange proofs between different interactive proof assistants. While Z3 (RUP) outputs could be converted to other formats for checking[5], this adds overhead and reduces clarity - undesirable in industrial settings where simplicity and transparency are critical. This motivated our development of a checker tailored to Z3's native format.

Earlier work aimed at directly verifying SAT solvers (see, for instance, [36], [37] for formalisations in Rocq and Isabelle).Versat [38] is verified solver that includes CDCL, though their C implementation was only manually derived. In [39], a provably correct DPLL prover has been automatically extracted from a formal proof, and the extracted solver has been applied in Railway verification case studies.

Contributions. The main contribution of this article is a verified proof checker that supports SIL certification in railway verification (Fig. 1). It is extracted and applied to discrete interlocking systems, with support for full propositional logic via Tseitin transformation. This also serves as a proof-of-concept for extending the approach to additional Z3 theories.[6] The main results are:

1. Demonstration of an extensible proof checker for validating Z3's unsatisfiability proofs, supporting SIL compliance in railway verification. We present a tailored solution to fit the requirements[7] of our industrial partner.
2. Checker works for full Z3 propositional proofs, and is not restricted to formulas in CNF (e.g. DIMACS format); i.e., the checker can process Z3 proofs which include Tseitin steps for translating propositional formulas into CNF.
3. The checker itself is fully verified in Agda, and the RUP checker is verified in Rocq. We provide a tool chain from SMT solver to Agda/Rocq, i.e. a proof of correctness of our SMT proof checker, which also allows to integrate theorems in Z3 into Agda and Z3 theorems in CNF into Rocq.

[4] Interestingly we could not find an off the shelf solution to fit the format of our industrial needs. Therefore we decided for own development to meet the requirements by our partner, and be able to further extend it with the Z3 theories we need.

[5] We are aware that there is an internal RUP checker in Z3, and also the option to produce a (longer) resolution proof (Z3's old proof format).

[6] Z3 theories are essential for verifying advanced railway systems such as ERTMS and geographic data [4].

[7] Formats/tools used form part of an overarching certification framework, involving Z3.

4. Small case study[8] to demonstrate the entire tool qualification process.
5. A GitHub repository [40] containing the SAT checker code in Rocq, Agda, and OCaml, as well as our case study.

2 Z3 Proofs of Unsatisfiability

The Z3 SMT solver [8] is widely used to verify whether an interlocking satisfies a propositional safety property. It checks the satisfiability of the negated property $\neg\varphi$ combined with the interlocking model (see James et al. [41]). If unsatisfiable, the original property φ holds, and Z3 can generate a proof log [42] for independent checking. Otherwise, a counterexample is returned [43]–[46]. The Ladder Logic Verifier uses Z3 first in inductive verification [41], [47], and falls back to bounded model checking [48], [49] if needed. To illustrate, we model a simple interlocking with a passing loop (Fig. 2) [50], where a signal turns green only if the point is correctly set and the opposing signal is red. The safety property ensures that opposing signals are never green at the same time. We assert its negation, $(s0 \wedge s1) \vee (s2 \wedge s3)$, and Z3 returns `unsat`, confirming the design is safe. Z3's proof log [42] shows the logical steps leading to unsatisfiability (Fig. 3). The proof includes nine assumption steps, 18 Tseitin steps, and seven RUP steps. Assumption introduces disjunctions, Tseitin encodes formulas into CNF [17], [51]–[53], and RUP derives new clauses.

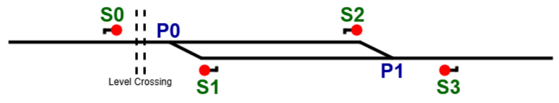


Fig. 2: Simple railway interlocking with a passing loop

```
tseitin(Not(And(Not(s1), p0)), Not(s1)) [] [Not(s1), Not(And(Not(s1), p0))]
tseitin(Not(And(Not(s1), p0)), p0) [] [p0, Not(And(Not(s1), p0))]
tseitin(s1, Not(p0), And(Not(s1), p0)) [] [s1, Not(p0), And(Not(s1), p0)]
assumption [] [Not(s0), And(Not(s1), p0)]
-- intermediate steps omitted --
rup [] [Not(And(Not(s2), Not(p1)))]
rup [] []
```

Fig. 3: Snippet of Z3 proof log of unsatisfiability of the railway interlocking

The Tseitin transformation introduces fresh variables to represent subformulas, preserving equisatisfiability while enabling efficient SAT solving. In Z3, however, these fresh variables are replaced directly by the original formulas, resulting in tautological clauses. Our prototype checker validates Tseitin steps by matching them against known tautological patterns including:

[8] Due to an NDA agreement in place we cannot demonstrate the process using a real world interlocking, but we will report on the scalability of the approach.

- `And`:
  - `tseitin(Not(And(`$a_1, ..., a_n$`)), `a_i`) [] [`a_i`, Not(And(`$a_1, ..., a_n$`))]`
  - `tseitin(Neg(`a_1`),..., Neg(`a_n`), And(`$a_1, ..., a_n$`)) []`
    `[Neg(`a_1`),..., Neg(`a_n`), And(`$a_1, ..., a_n$`)]`
- `Not`:
  - `tseitin(b, Not(b)) [] [b, Not(Not(Neg(b)))]`
- `Or`:
  - `tseitin(Neg(`a_i`), Or(`$a_1, ..., a_n$`)) [] [Neg(`a_i`), Or(`$a_1, ..., a_n$`)]`
  - `tseitin(`$a_1, ..., a_n$`, Not(Or(`$a_1, ..., a_n$`))) []`
    `[`$a_1, ..., a_n$`, Not(Or(`$a_1, ..., a_n$`))]`

We implemented a prototype checker for these Tseitin steps in Agda [54], a dependently typed language and proof assistant. The checker verifies that each Tseitin clause matches a valid tautological pattern. Correctness is formally proven by showing that all such clauses are tautologies, ensuring that the transformation preserves equisatisfiability [55]. Together with our formally verified RUP checker, these components form a complete SMT proof checker for propositional formulas. Future work will focus on translating the Tseitin checker to Rocq and integrating it with the RUP checker for industrial deployment. Using the correctness proofs of both the Tseitin and RUP checkers, we establish the following key result: if the proof checker returns true, then the assumptions of the Z3 proof entail its conclusions (Fig. 4). Furthermore, if in addition the assumptions contain the empty clause, the proof confirms unsatisfiability (Fig. 5).

```
    correctnessZ3ProofCheck : (p : ZProof)
                            → atom (ZProofCheck p)
                            → EntailsListZCl (ZProof2Assumption p
                              (ZProof2ConclusionOpt p)
```

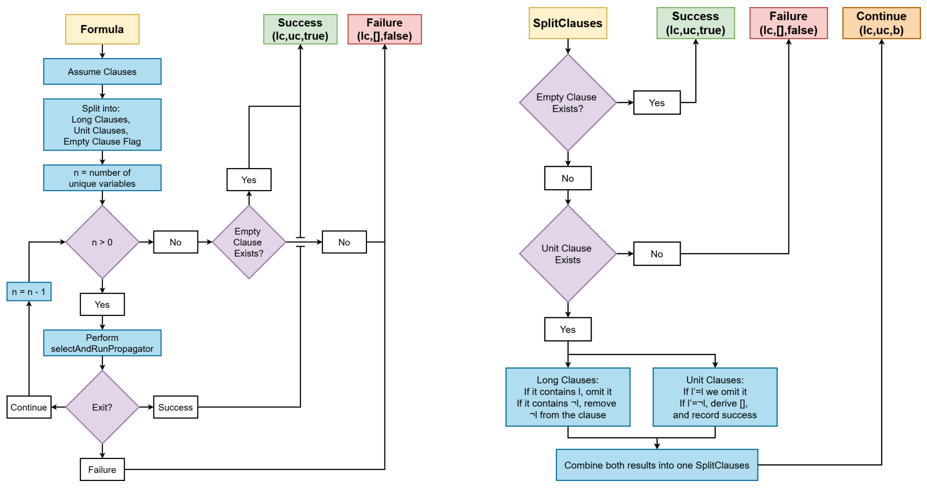
Fig. 4: If the checker is true, then the proof's assumptions entail its conclusions

```
correctenessZ3ProofCheckUnsat : (p : ZProof)
                                → atom (ZProofCheckUnsat p)
                                → UnSat (ZProof2Assumption p)
```

Fig. 5: Proof of checker returning [] confirms the assumptions are unsatisfiable

3 Three Level Approach for a Verified RUP Checker

The basis of the new Z3 proof log format is Reverse Unit Propagation (RUP) [56]–[58]. In a RUP proof each inference, of the form `rup [a]`, indicates that the clause `a` has been derived and validated by showing that its negation and a formula `f` leads to a contradiction via unit propagation. Ultimately, the proof concludes with `rup []`, signifying that falsity has been reached directly, without needing to derive any further clauses (success) or no further steps are possible (failure). Clauses can be of length ≥ 2, which we call *long clauses*, unit clauses, which are clauses of length 1, or the empty clause. In RUP, a formula is a conjunction of clauses written in CNF.


Formula
Assume Clauses
Split into: Long Clauses, Unit Clauses, Empty Clause Flag
n = number of unique variables
n > 0
No
Empty Clause Exists?
Yes
No
Success (lc,uc,true)
Failure (lc,[],false)
n = n - 1
Yes
Perform selectAndRunPropagator
Exit?
Continue
Success
Failure
SplitClauses
Success (lc,uc,true)
Failure (lc,[],false)
Continue (lc,uc,b)
Empty Clause Exists?
Yes
No
Unit Clause Exists
No
Yes
Long Clauses: If it contains l, omit it If it contains ¬l, remove ¬l from the clause
Unit Clauses: If l'=l we omit it If l'=¬l, derive [], and record success
Combine both results into one SplitClauses

(a) Unit Propagation Checker Process (b) selectAndRunPropagator Process

Fig. 6: Overview of the RUP checker processes

Termination is guaranteed by structurally reducing variables at each step, satisfying Rocq's requirements. The implementation follows a loop that applies one-step unit propagation (Fig. 6a): clauses containing l are removed, and those with $\neg l$ are reduced to $c' := c \setminus \neg l$. Unit clauses are handled similarly - if $l' = l$, it is omitted; if $l' = \neg l$, the empty clause is derived; otherwise, it is retained (Fig. 6b). The checker and its formal correctness proofs were developed in Rocq and are available on GitHub [40]. We extracted the implementation to OCaml using Rocq's built-in mechanism [13]–[15], and built a parser for Z3 proof logs. To prove correctness, we formalised the `TreeProof` datatype in Rocq, representing unit resolution proofs.[9]

```
Inductive TreeProof : Type := | ass : nat → TreeProof
                              | ures : TreeProof → TreeProof → TreeProof.
```

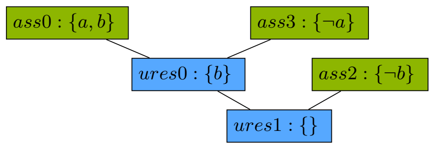


Fig. 7: Example of Tree proof deriving a contradiction.

RUP is proven via unit propagation, which employs a series of unit resolution steps. Here `(ass n)` denotes the assumption rule, deriving the `n`th assumption. The assumptions are the original set of clauses prior to unit propagation. For each unit resolution cut, we create `(ures t1 t2)` which denotes a `TreeProof` of unit resolution from `TreeProofs` `t1` and `t2`. For example, we derive that the formula $\{a, b\}$, $\{\neg a, b\}$ and $\{\neg b\}$ is unsatisfiable. The RUP format first derives $\{a\}$, by adding $\{\neg a\}$ to the assumptions and deriving falsity using unit resolution

[9] The term "tree proof" distinguishes this format from SMT and Rocq proofs.

(Fig. 7). An extended version of our Rocq code generates Tree Proofs, offering additional confidence in the checker by providing a trace of the resolution cuts.

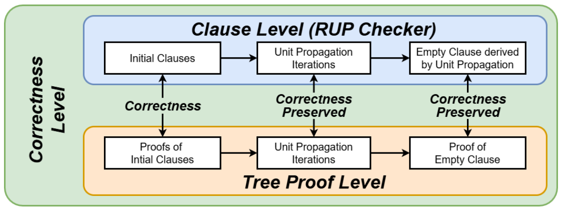


Fig. 8: The three level architecture of the RUP proof checker

To prove soundness, we show that if the RUP checker returns `true`, then there exists a valid `TreeProof` of the empty clause from a RUP step `c'`. We implemented a unit resolution checker operating on long clauses and unit clauses. Each clause-level operation is mirrored at the `TreeProof` level to produce a matching resolution trace. We proved these operations preserve correctness with respect to the original clauses (Fig. 8). A `TreeProof t` is correct if it derives a clause `c`, from assumptions `al`, that matches the result on the clause level:

```
Definition CorrectProof (al : Assumption)(c : Clause)(t : TreeProof) : Prop :=
  correctConclusion al t = Some c.
```

A `TreeProof` is valid if every use of `(ass n)` refers to a valid assumption `(n < length al)`, and each subproof of the form `(ures t1 t2)` where `t2` is a unit clause. This ensures that `c'` entails falsity in all models. Since `c'` is defined as `negate_clause c ++ a`, its unsatisfiability implies the original assumptions `a` entail the RUP clause `c`. Therefore, if `[]` can be derived from `a`, then `a` is unsatisfiable. By the definition of entailment [59], any model satisfying the assumptions must also satisfy the conclusion. If the assumptions are true in a `model`, so is the clause. As in the Agda prototype, we proved that if the RUP checker returns true, the empty clause was derived, and the assumptions entail it. This implies the correctness of RUP proofs and therefore of Z3 proofs of formulas in CNF:

```
Lemma RUP_Checker_correct : forall (a : Assumption) (c : Clause),
  RUP_Checker a c = true → entails a c.

Lemma RupProofcheckerUnSat : forall (pl : RupProof),
  rupProofCheckerUnsat pl = true → UnSatFor (rupProof2Assumptions pl).
```

4 Applying the Z3 SAT Proof Checker

The checker consists of two components. The first is the reverse unit propagation procedure extracted from Rocq, extended to support `assumption` and `Tseitin` steps for SAT proof logs. Full checking of `Tseitin` steps will be added in future work. The second is a parser that reads Z3 proof logs line by line, converting each entry into the datatypes written in Rocq. The checker processes the proof sequentially, confirming validity if all steps succeed, or reporting the first invalid step encountered. The proof log from the example interlocking (Fig. 3) was successfully validated. To evaluate scalability, we tested the checker on an industrial interlocking with 75,000 propositional variables and 12,000 ladder logic rungs.

Two proof logs were generated using Inductive Verification (IV) and Bounded Model Checking (BMC). The IV logs contained around 29,000 steps, while BMC logs exceeded 500,000, reflecting BMC's higher computational cost. All logs were successfully validated (Table 1), with IV completing significantly quicker[10].

Approach	Proof Logs	Validity	Average Runtime
BMC	13	All Valid	7 hours, 49 minutes, 54 seconds
IV	6	All Valid	2 minutes, 50 seconds

Table 1: RUP proof checker runtimes on the proof logs from running the Ladder Logic Verifier on industrial interlockings

5 Conclusion

This work introduces a verified Z3 SAT proof checker to strengthen trust in railway verification tools such as the Ladder Logic Verifier. A key component is a formally verified Tseitin transformation, implemented in Agda, which converts arbitrary formulas into CNF. Each transformation step is proven to be a tautology, ensuring logical equivalence with the original formula. This framework is designed for extensibility, allowing additional SMT proof rules to be incorporated and verified within the same formal setting. The RUP checker, developed in Rocq, is an extracted verified program that validates Z3-generated RUP proofs. A key strength of our approach is that the checker operates directly on proof logs, avoiding inefficient translations into formats like resolution proofs. While such conversions are possible (e.g., using legacy Z3 formats), they are impractical for large-scale systems. Our method eliminates this overhead by using unit resolution trees as a formal foundation. Though not required during checking, these trees are useful for small examples and debugging. The extracted OCaml implementation supports full Z3 SAT traces and is designed for extensibility, enabling future support for theory-specific rules [42]. Developed with our industrial partner, the checker integrates into safety-critical toolchains and supports real-world SIL certification efforts. Our long-term goal is to automate and to verify the encoding of interlocking system designs into SMT-LIB [10], enabling broad safety property verification through a formally verified, extensible infrastructure.

Further steps will include: (1) Translating the Tseitin checker written in Agda into Rocq and integrating it with the current extracted checker. (2) Extracting the checker to C using CertiCoq [60], followed by performance testing and scalability improvements. (3) Formalising the proof in Rocq's safe core, leveraging its infrastructure to ensure the core logic is verified within a minimal, trusted kernel. (4) Exploring certified program extraction, evaluating existing frameworks for full certification and identifying limitations. (5) Extending the checker to full SMT by integrating provably correct rules like Farkas, and adding support for more complex railway verification tasks. (6) Applying the checker in our toolchain for verifying geographic scheme data [4], and developing larger case studies to evaluate scalability and robustness.

[10] Tests were run on a machine with 128 64-core processors at 2194.443 MHz.

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