Registers

- Control: dictates current state of the machine
- Status: indicates status of operation (error, overflow, etc.)
- MAR: Memory Address Register (holds address of memory location currently referenced)
- MDR: Memory Data Register: holds data being sent to or retrieved from the memory address in the MAR
- IP: Instruction Pointer (holds memory address of next instruction)
- IR: Instruction Register (holds current machine instruction)
- Operand_1, Operand_2, Result: ALU registers (for calculations and comparisons)
- General: fast temporary storage eax,ebx,ecx,edx

Instruction Execution Cycle

- 1. **Fetch** next instruction (at address in IP) into IR.
- 2. **Increment** IP to point to next instruction.
- 3. **Decode** instruction in IR
- 4. If instruction requires memory access,
 - A. Determine memory address.
 - B. **Fetch operand** from memory into a CPU register, or send operand from a CPU register to memory.
- 5. **Execute** micro-program for instruction
- 6. Go to step 1 (unless the "halt" instruction has been executed)

$$Ki = 2^{10}$$
, $Mi = 2^{20}$, $Gi = 2^{30}$

- **ReadString** Reads a string from keyboard, terminated by the Enter key.
- Preconditions: **OFFSET** of memory destination in **EDX**, **Size** of memory destination in **ECX**
- Postconditions: String entered is in memory
- Return : **Length** of string entered is in **EAX**
- •ReadDec, unsigned int EAX, ReadInt signed int EAX

push	decrements esp then copies
pop	copies and then <u>increments</u> esp
ESP	always points to a value not an empty spo

- The **CALL** instruction calls a procedure
- **Pushes** the offset of the next instruction onto the stack
- **copies** the address of the called procedure into EIP

LOOP first decrements ECX then Jumps if !=0 [n-1]

CMP dest, source JE d=s JNE d!=s

Give dest, source sind a sind a v			
UNSIGNED	SIGNED		
JA, JNBE dest > source	JG jump if destination > source JNLE		
JAE, JNE >=	JGE jump if destination >= source JNL		
JB, JNAE <	JL jump if destination < source JNGE		
JBE, JNA <=	JLE jump if destination <= source		

<u> </u>							
0000	0001	0010	0011	0100	0101	0110	0111
0	1	2	3	4	5	6	7
F	E	D	С	В	Α	9	8
1111	1110	1101	1100	1011	1010	1001	1000

Type	Used for:
BYTE	1-byte unsigned integers [0 255], ASCII characters
SBYTE	1-byte signed integers [-128 127]
WORD	2-byte unsigned integers [0 65535], address
SWORD	2-byte signed integers [-32768 32767]
DWORD	4-byte unsigned integers [0 4294967295], address
SDWORD	4-byte signed integers [-2147483648 2147483647]
FWORD	6-byte integer
QWORD	8-byte integer
TBYTE	10-byte integer
REAL4	4-byte floating-point
REAL8	8-byte floating-point
REAL 10	10-hyte floating-noint

IMUL 1,2,3 operand Instruction Form Condition for Clearing CF and OF AL := sign-extend of AL to 16 bits r/m8 r/m16 AX := sign-extend of AX to 32 bitsr/m32 EDX:EAX := sign-extend of EAX to 32 bits r16,r/m16 Result exactly fits within r16 Result exactly fits within r32 r/32,r/m32 r16,r/m16,imm16 Result exactly fits within r16 r32.r/m32.imm32 Result exactly fits within r32 Dividend / Divisor = Quotient remainder edx:eax div reg/mem EAX **EDX** 16 SUB sets cary if a-b a<b 0100 + 0100 = 1000 (overflow flag is turned on) 8 BH AH 1000 + 1000 = 0000 (overflow flag is turned on) OF overflow flag is XORed with Carry Flag General registers Control Bus Status Register DI BI AI 0 Control Register DX S uMemory μIP (µPrograms) I n t Starting Address Generator (SAG) e Main 0.0000 0.0000 r Instruction Decoder Memory n 0.0001 0.0625 а 1 Instruction Register (IR) Arithmetic/Logic 0.1250 0.0010 Unit (ALU) В Instruction Pointer (IP) 0.1875 0.0011 u Operand 1 Adder 0.2500 0.0100 Operand 2 System Clock 0.0101 0.3125 Addressing Unit Result 0.0110 0.3750 Address Bus Memory Address Register (MAR) 0.0111 0.4375 Memory Data Register (MDR) CPU Data Bus 0.1000 0.5000 IEEE Floating-Point Binary Formats. TAble 12-1 0.1001 0.5625 0.1010 0.6250 32 bits: 1 bit for the sign, 8 bits for the exponent, and 23 bits for Single Precision the fractional part of the significand. Approximate normalized range: 2^{-126} to 2^{127} . Also called a *short real*. 0.1011 0.6875

the fractional part of the significand. Approximate normalized range: 2^{-126} to 2^{127} . Also called a *short real*.

Double Precision

64 bits: 1 bit for the sign, 11 bits for the exponent, and 52 bits for the fractional part of the significand. Approximate normalized range: 2^{-1022} to 2^{1023} . Also called a *long real*.

Double Extended Precision

80 bits: 1 bit for the sign, 16 bits for the exponent, and 63 bits for the fractional part of the significand. Approximate normalized range: 2^{-16382} to 2^{16383} . Also called an extended real.

0.1010
0.08750
0.1101
0.88750
0.1111
0.89750