Submission deadlines:

- Demonstrate completion of project 1 during evening laboratory sessions on either Tuesday March 12, or Wednesday March 13, from 6:30 pm to 8:30 pm in 302 EE West. You must sign up for a ten minute slot on either Wednesday or Thursday using SignUpGenius. You will receive an email message via your Penn State email address when the sign up sheet is available online at SignUpGenius. Slots are filled on a first-come, first-served basis.
- **Each** EE 200 student must complete both parts of this project and demonstrate their MULTISIM file and discrete-logic realization.

Part 1: (50 points)

Using Multisim, verify the operation of the finite state machine for the multicolor LED glow baton realized in Problem Set 3, problems 9 and 10. Following Figure 1, generate the signals A, B, and R using normally open (NO) push buttons. When the button SR is pressed, the system must asynchronously return to the state S0. When the input to a CMOS logic gate is allowed to float, that is, it is neither connected to V_{DD} or V_{SS}, its logic level is unpredictable. For this reason, the 27kΩ resistors are included to pull the inputs to a valid logic level when a given button is not pressed, in specific, logic low for the input signals A and B, and logic high for the input signal R. Set up the switches SA, SB, and SR so that the user may change the signals A, B, and R using the keys A, B, and R, respectively, on the keyboard.

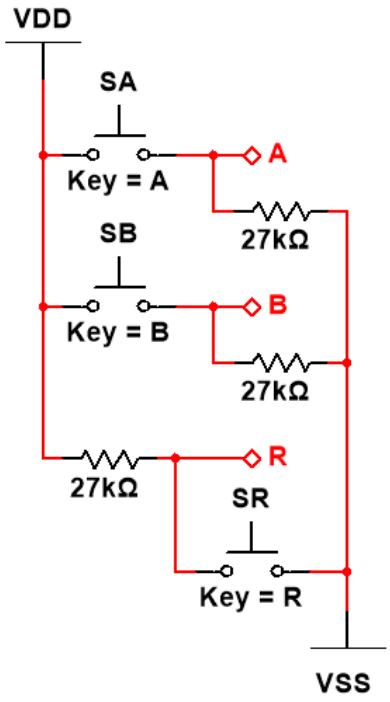

Figure 1: Realization of the signals A, B, and R in MULTISIM.

Implement the circuit using eight 4011BD_5V two-input NAND gates, six 4023BD_5V three-input NAND gates, one 4012BD_5V eight-input NAND gate, and one 40175BD_5V quad D-type flip-flop. Use a single page layout, and simplify the layout using on-page connectors, as discussed in Laboratory 3, Exercise 2. Generate a clock signal using the virtual Agilent function generator and the specifications provided on page 13 of the Laboratory 3 handout. Indicate the output signals G, Y, and R using a green, yellow, and red LED, respectively. Use a green LED to indicate the state of the clock line. Use a 330Ω resistor in series with each LED to limit current.

Part 2: (50 points)

Realize the finite state machine using the components in Table 1 that are available in the EE 200 component kit. Component specifications sheets are provided along with this project assignment.

Manufacturer Part Number	**Description**	**Quantity**
CD4012BE	Dual 4-input NAND gate	2
CD4023BE	Triple 3-input NAND gate	2
CD4068BE	Single 8-input NAND gate	1
CD40175BE	Quad D-Type flip-flop	1
CD4541BE	Programmable Timer	1
	Red LED	1
	Green LED	2
	Yellow LED	1
	330Ω 0.25 W carbon film resistor	4
	27kΩ 0.25 W carbon film resistor	1
	56kΩ 0.25 W carbon film resistor	1
	$0.01\mu F$ ceramic capacitor	1
	tactile switch	3

Table 1: Components for realizing the finite state machine.

Adhere to the following guidelines.

1. Generate a clock signal of approximately 0.6 Hz using the CD4541BE programmable timer. Start by carefully reading the attached specification sheet for this device. Set the values of R_{TC}, C_{TC}, and R_S to 27kΩ, $0.01\mu F$, and 56kΩ, respectively. In order to generate a continuous-square wave, use the recycle mode by setting the appropriate logic level on pin 10. Enable the auto reset feature and turn off the master reset by setting the appropriate logic levels on pins 5 and 6. Set the logic level of pin 9 so that the output is initially low after reset. Finally, set the appropriately logic levels for pins 12 and 13 so that the frequency of the clock signal available on pin 8 is approximately 0.6 Hz. Use a green LED in series with a 330Ω resistor to indicate the clock state.

2. Use the two tactile switches to generate the inputs A and B. Pressing a button should send the corresponding input to the logic-high state. Use a 27kΩ pull down resistor between the CMOS input and V_{SS} to make sure that the gate input sees a logic-low state when the button is not pressed.

3. As the clear input for the CD40175BE quad D-Type flip-flop is active low, pressing the tactile switch representing R must drive the clear input low on the CD40175BE. For this reason, tie the clear input to V_{DD} through a 27kΩ pull up resistor, and wire the tactile switch representing R between the clear input and V_{SS}.

4. Clearly label the tactile switches that represent the control signals A and B.

5. Use a green, yellow, and red and LED to indicate the output signals G, Y, and R, respectively, where a lit LED indicates a logic-high signal. For each LED, limit current using a 330Ω series resistor.

6. Measure the maximum current drawn by your circuit using the myDAQ as this information is need for a future problem assignment.

Each student has approximately five minutes to demonstrate their work, and points are awarded as follows:

1. (50 points) Multisim Simulation
   (a) (5 points) Pressing the keyboard keys using the keys A, B, and R changes the logic level os the signals A, B, and R,respectively.
   (b) (5 points) Appropriately label the LEDs indicating the output signals and clock state.
   (c) (5 points) The system must asynchronously returns to the state S0 when the R key is pressed.
   (d) (5 points) Appropriate use of on-page connectors to simplify the Multisim schematic
   (e) (20 points) The system must produce the desired lighting patterns in response to the push buttons SA and SB.
   (f) (10 points) The grader will ask you a question regarding the Multisim Simulation.
2. (50 points) Circuit Realization
   (a) (4 points) An appropriate label must be attached to each tactile switch and LED so that the grader can test your circuit. Use a post-it note or, alternatively, tape a piece of paper to the wiring connecting the switch or LED with the appropriate signal label.
   (b) (8 points) The programmable timer must produce the desired clock signal as indicated by the flashing green LED.
   (c) (8 points) The system must asynchronously returns to the state S0 when the tactile switch representing the input R key is pressed. Demonstrate that pressing the asynchronous reset button immediately returns the system to state S1, regardless of the clock signal state.
   (d) (20 points) Demonstrate that system responds correctly to the inputs A and B.
   (e) (10 points) The grader will ask you a question regarding the discrete-logic realization of the finite state machine.