Spring 2018 **ECE 441 – Design of Digital Systems** **Project 1**

Write separate Verilog design files for the following circuits. Simulate each in ModelSim using a testbench like the provided comb_ex2 examples at KSOL.

1. Problem 2.31(2.51) from HW1, where the function from Figure 2.31 is implemented. You do not have to simplify the function or use NAND gates. Just implement the output using Verilog assign statements. Simulate your design and view the resulting waveforms to confirm the functionality.

2. Create a design that generates parity bit for a 7-bit input. Odd parity is desired, so that the total number of 1's in the 7-bit input and the 1-bit output is an odd number. Simulate your design and view the resulting waveforms to confirm the functionality.

Produce evidence that each of your design simulates correctly using testbenches and the correct output waveforms.

DUE: 11:59 pm Friday, Feb. 2

TURN IN: (electronic submission of one pdf file that contains the following)

1) Very SHORT report on the steps you took and issues you found difficult to resolve

2) Verilog source code (commented, of course, with headings) for both your designs and their associated testbenches.

3) Output verification (typically waveforms or similar for testbench output). Just screen snapshots are ok, I don't need to see all of the waveforms for the entire simulation.

POINTS: 20