Military Institute of Science and Technology

Department of Electrical, Electronic and Communication Engineering

Assignment

VLSI II Laboratory [EECE-458]

Submitted by,

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EECE-20

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Introduction to Cadence Virtuoso

Cadence Virtuoso is an advanced Electronic Design Automation (EDA) platform for analog, digital, and mixed-signal IC design. It supports the full custom design flow, from schematic capture to physical layout and post-layout verification. Core capabilities include parameterized cell (PCell) creation, constraint-driven layout editing, and integration with simulation tools (Spectre, APS) for pre- and post-layout analysis. The Virtuoso Layout Suite enables DRC, LVS, and parasitic extraction using integrated verification engines. Designers can optimize area, performance, and power while ensuring fabrication compliance through foundry-provided PDKs. Its tight coupling between schematic, layout, and simulation accelerates design closure and minimizes costly re-spins.

Introduction to Configurable Logic Block (CLB)

A Configurable Logic Block (CLB) is a fundamental logic unit in FPGAs and reconfigurable digital ICs. It typically contains:

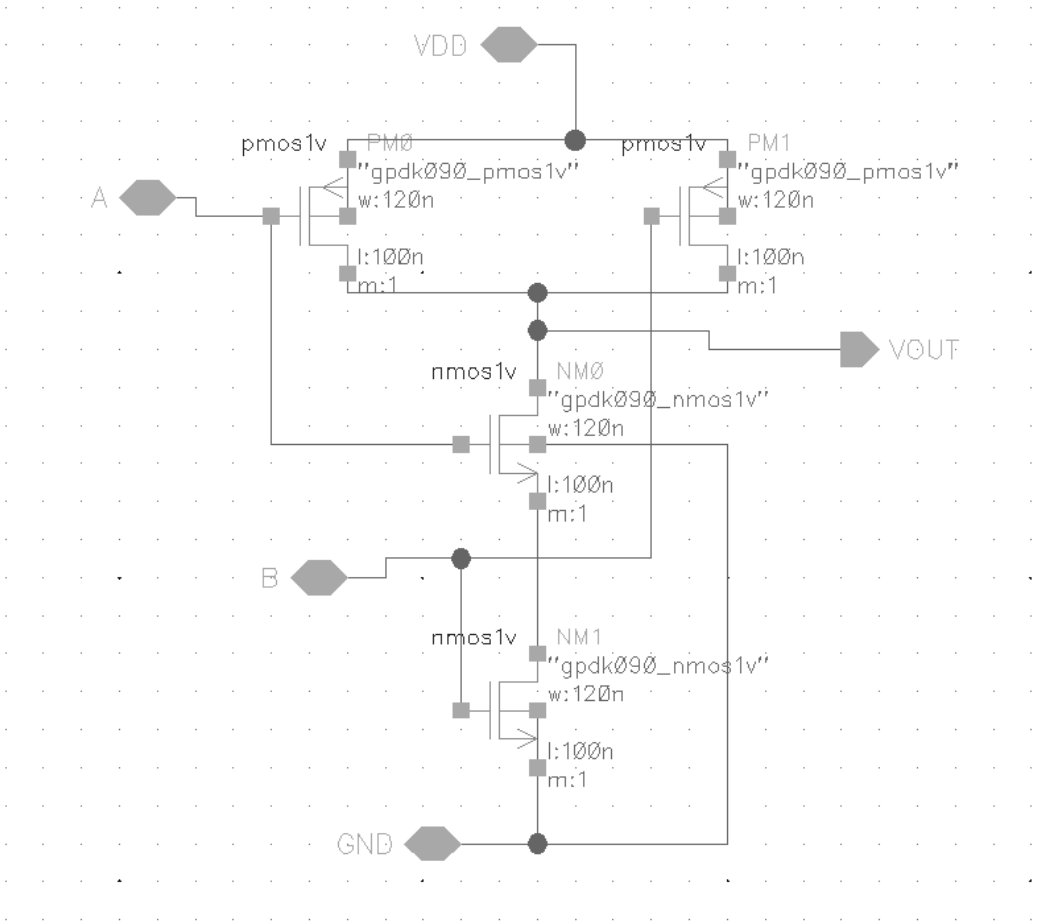
- Look-Up Tables (LUTs) – implement arbitrary combinational logic by storing truth table outputs.
- Flip-Flops/Latches – provide sequential storage for state machines and pipelining.
- Multiplexers – enable routing flexibility within the block.
- Programmable interconnects – connect CLBs to each other and to global routing.

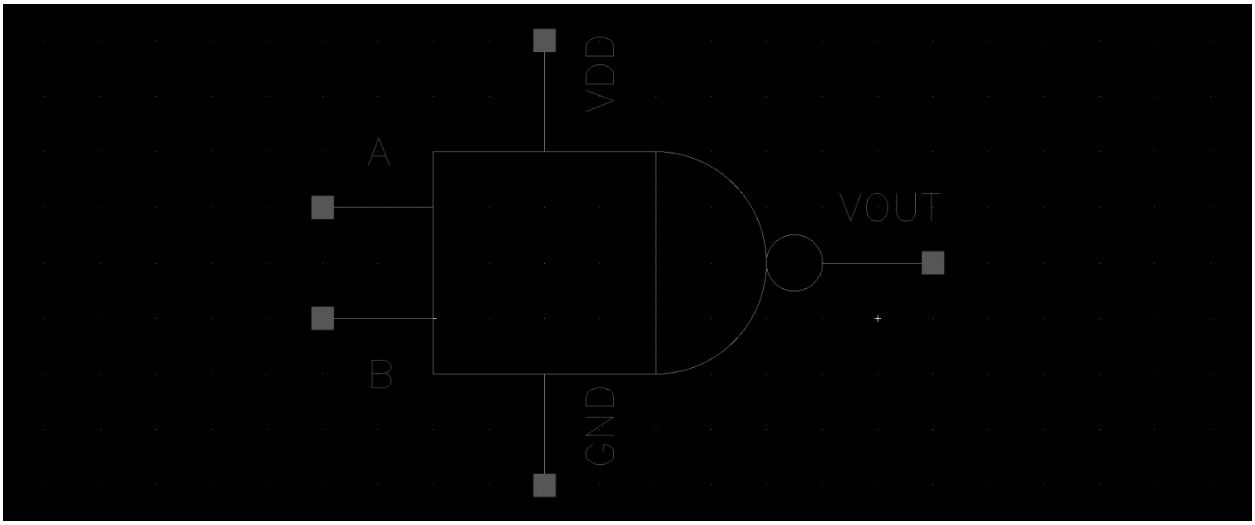
Modern CLBs support wide-input LUTs (6–8 inputs), distributed RAM, and shift-register modes. They are configured via bitstreams generated from synthesis and place-and-route tools, enabling rapid prototyping and post-deployment reprogramming. CLB architecture directly impacts FPGA density, speed, and power efficiency.

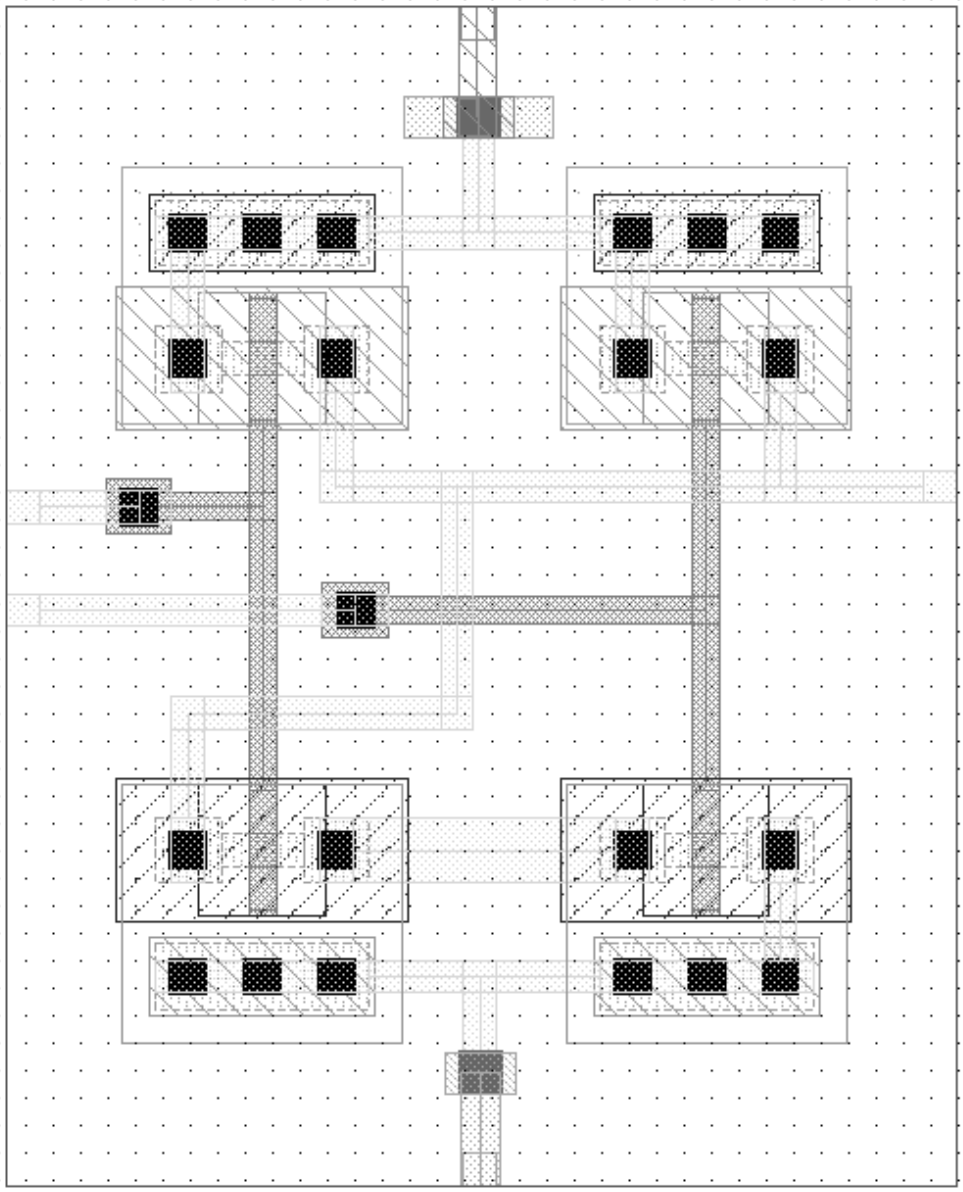
Schematic, symbol and layouts

All the necessary schematics, symbols and layouts of the used gates, logics are shown with proper graphics and values.

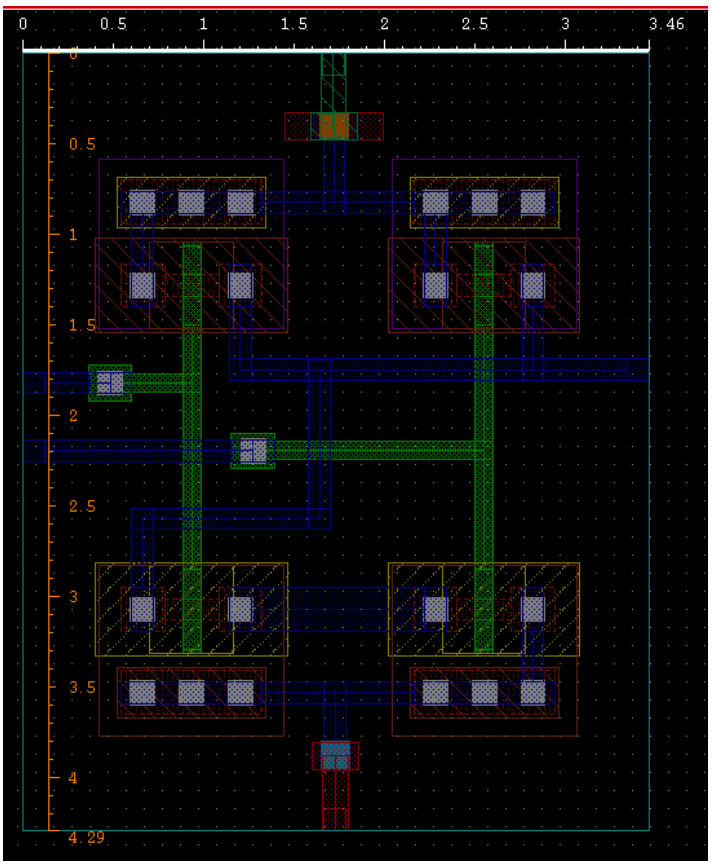
a. 2 input NAND



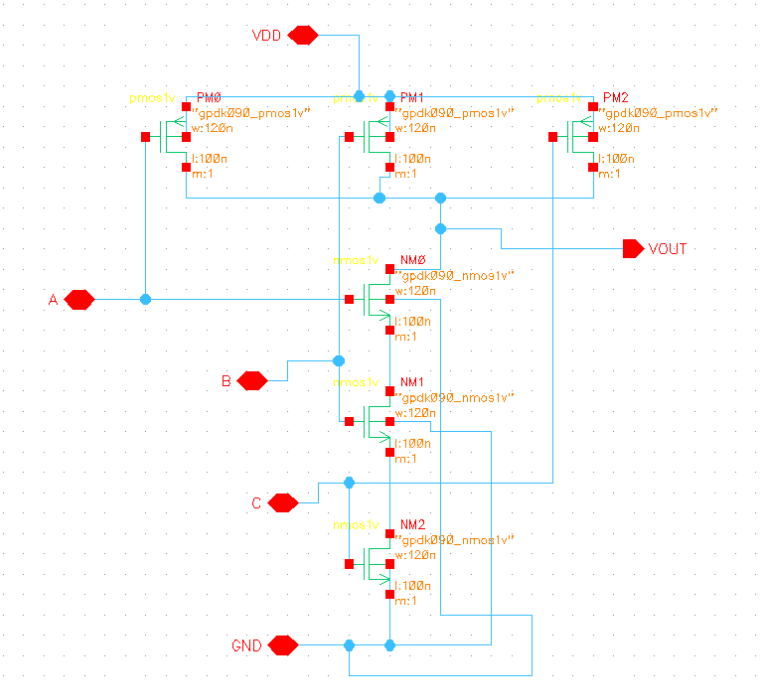


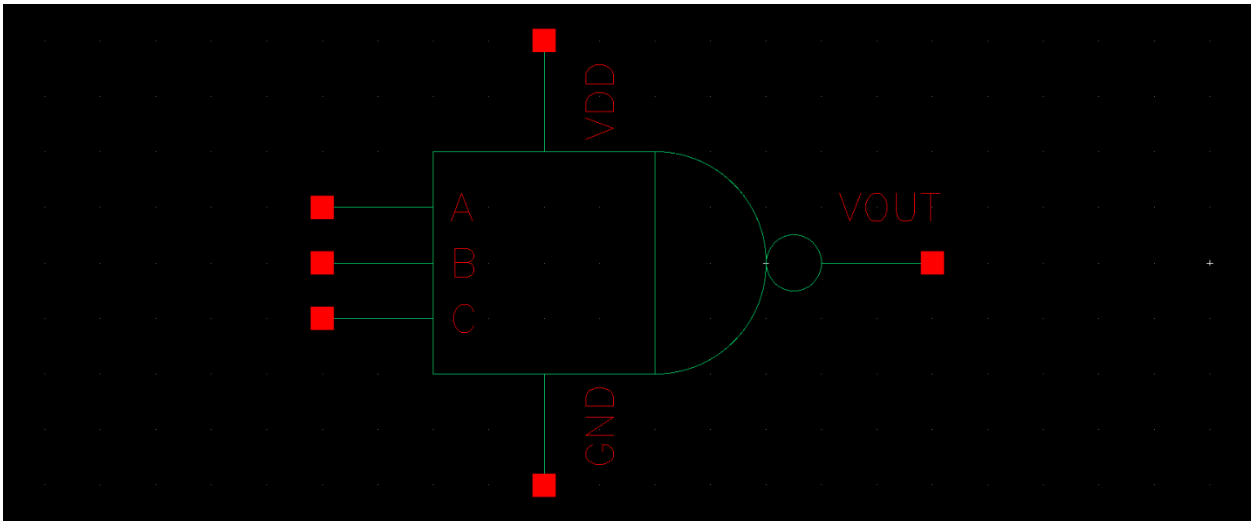


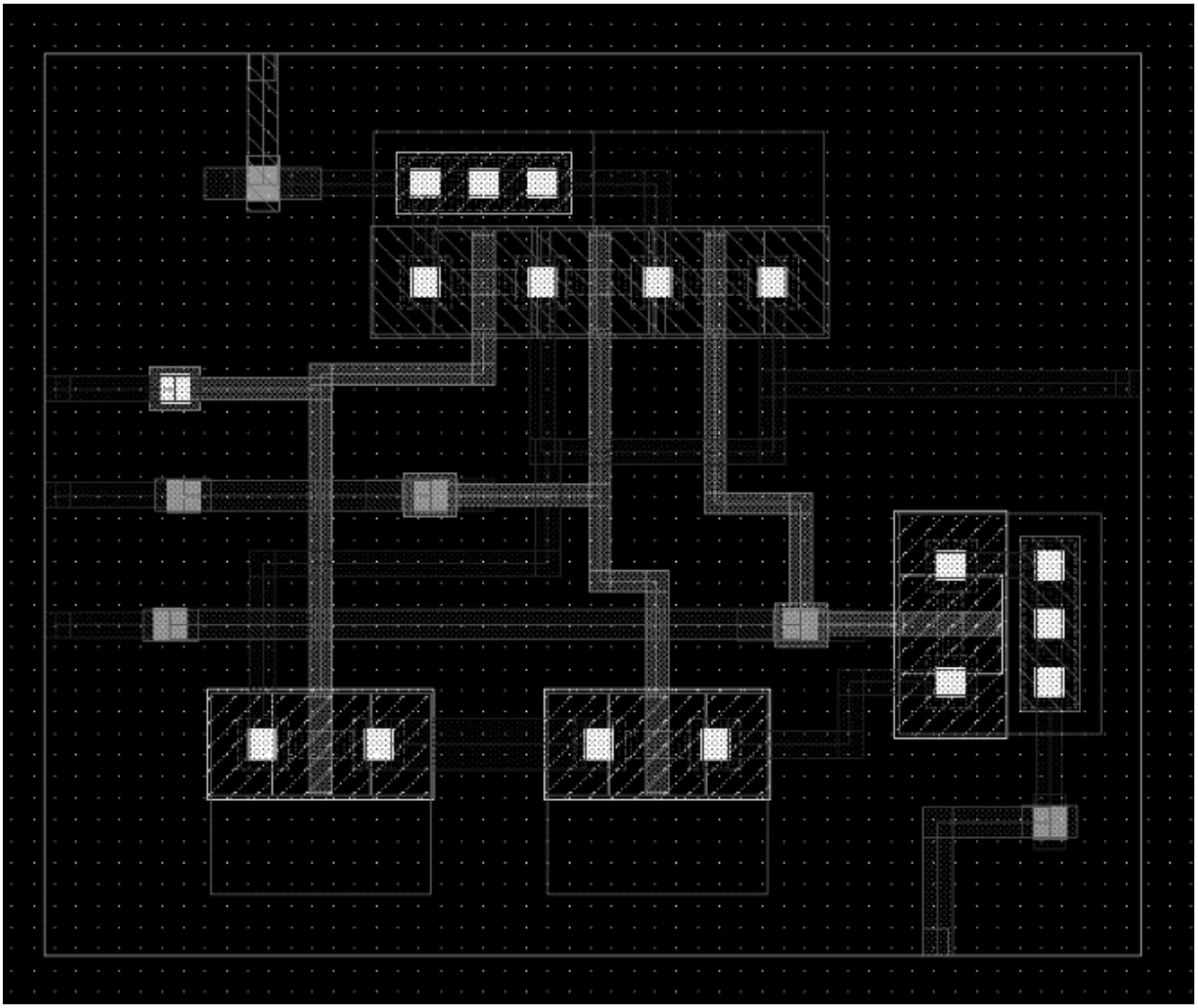
area of the layout is = 14.85 μm^2



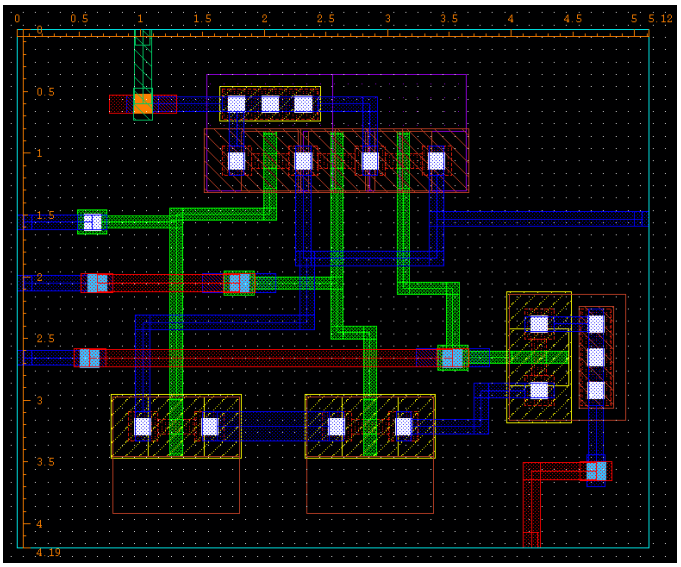
b. 3 input NAND



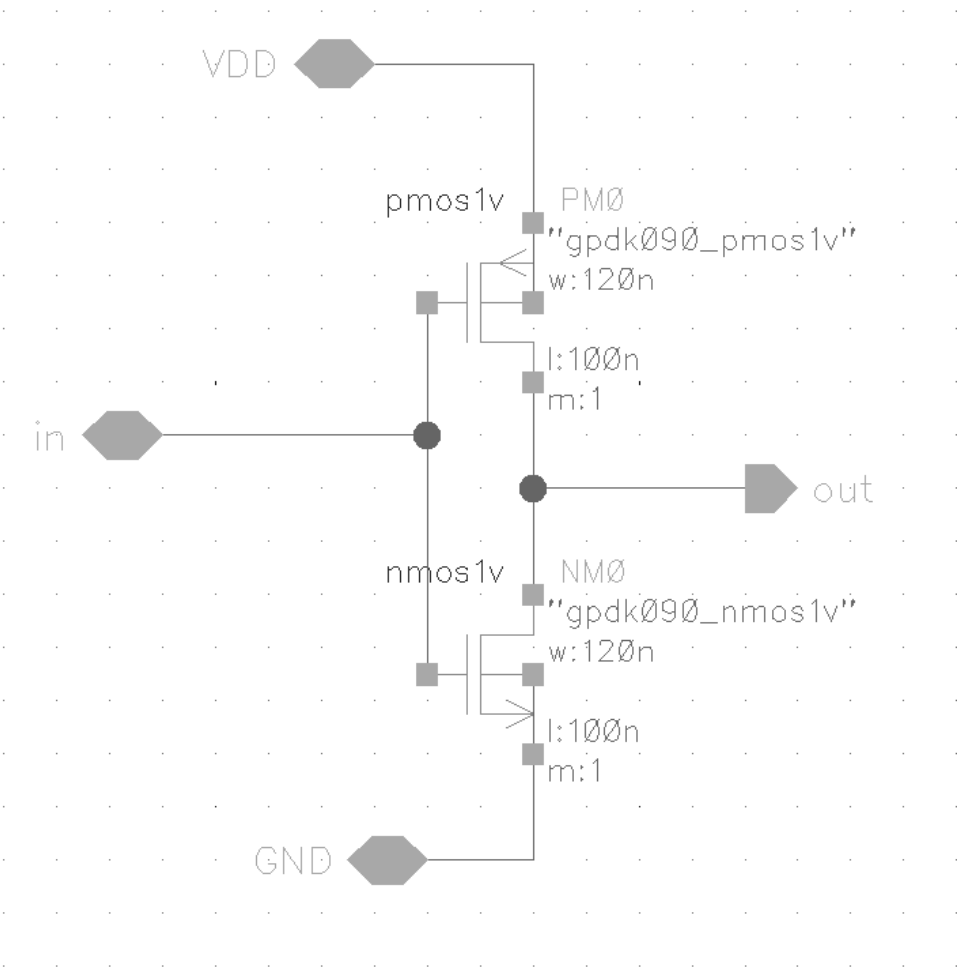

VDD
A
B
C
VOUT
GND

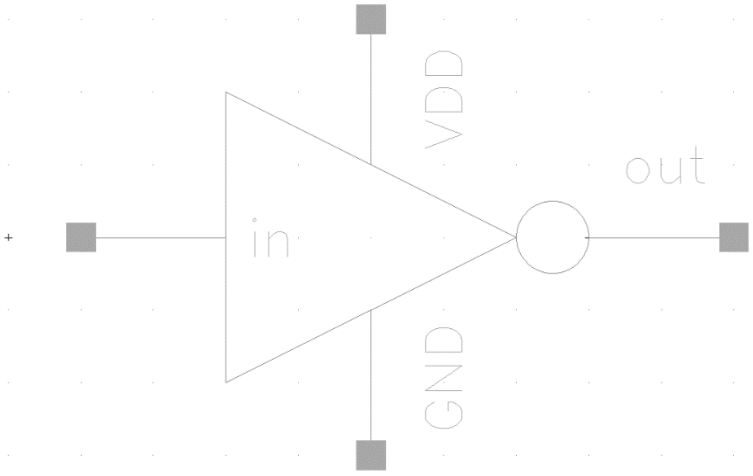


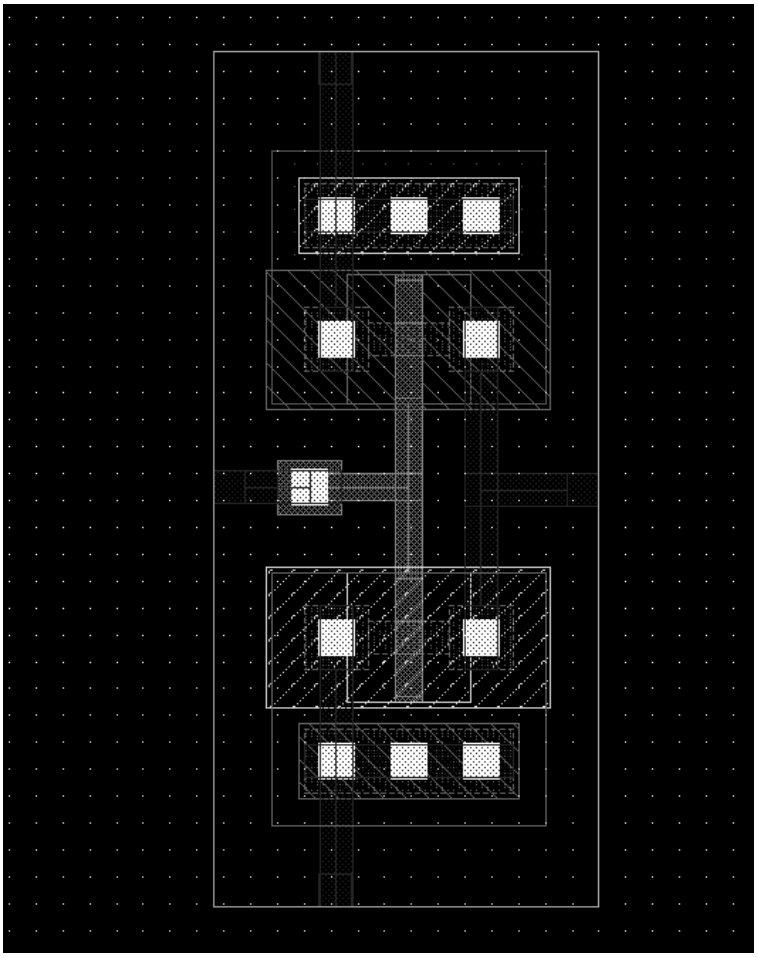
area of this layout = 21.45 μm^2



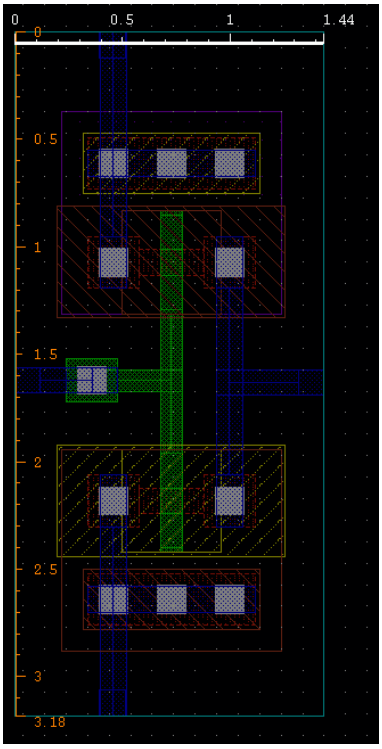
c. Inverter



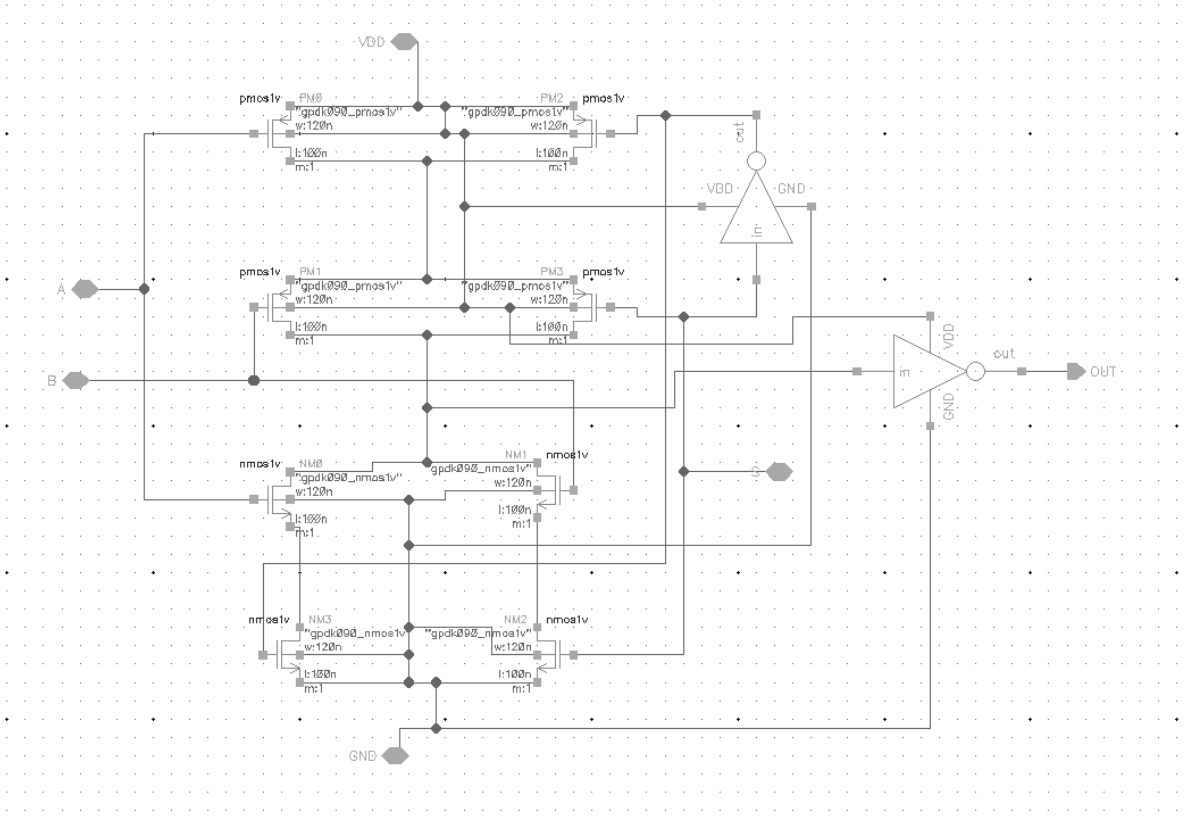

VDD
out
in
GND

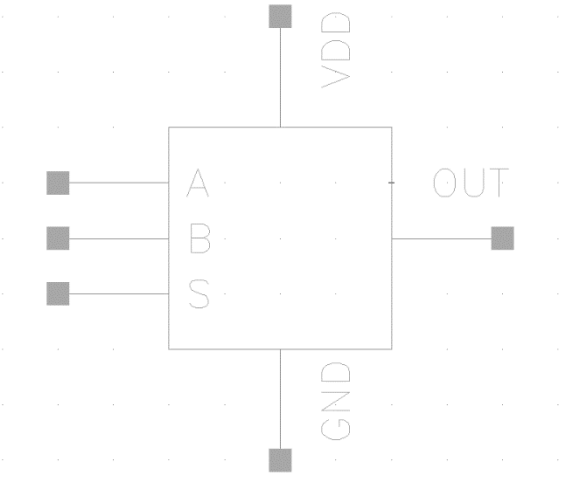


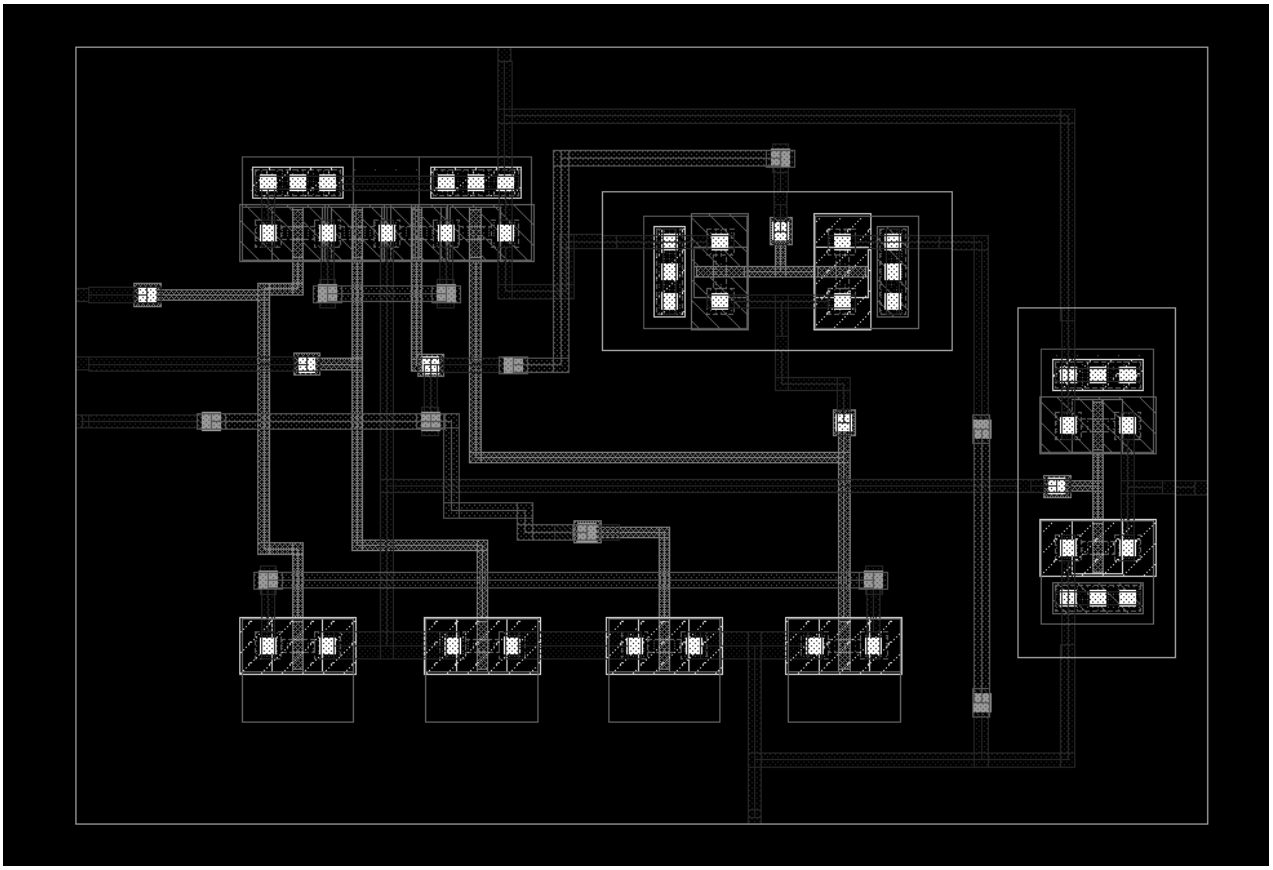
Area of the layout = 4.579 μm^2

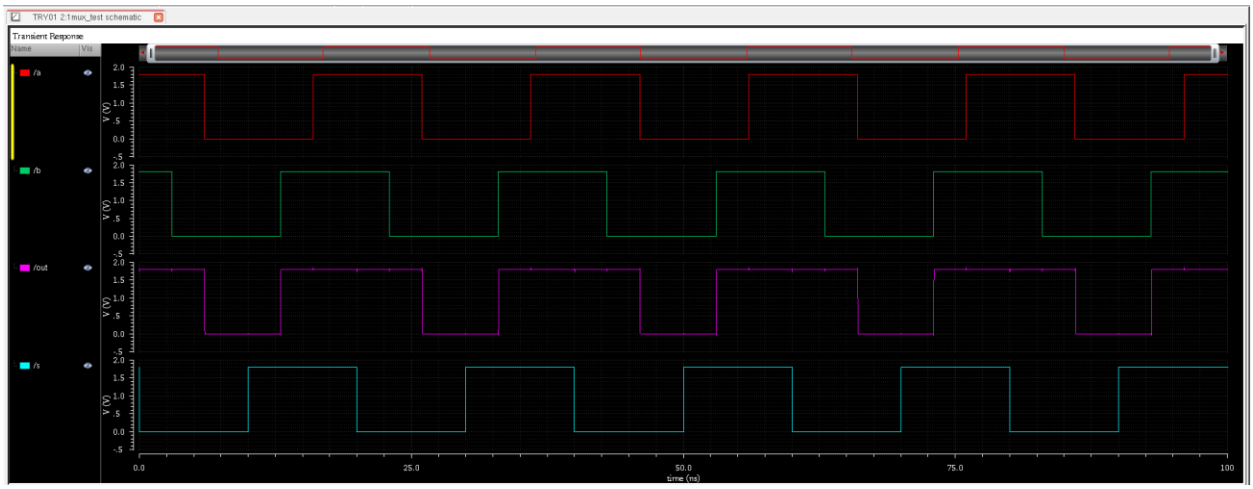


d. 2:1 MUX

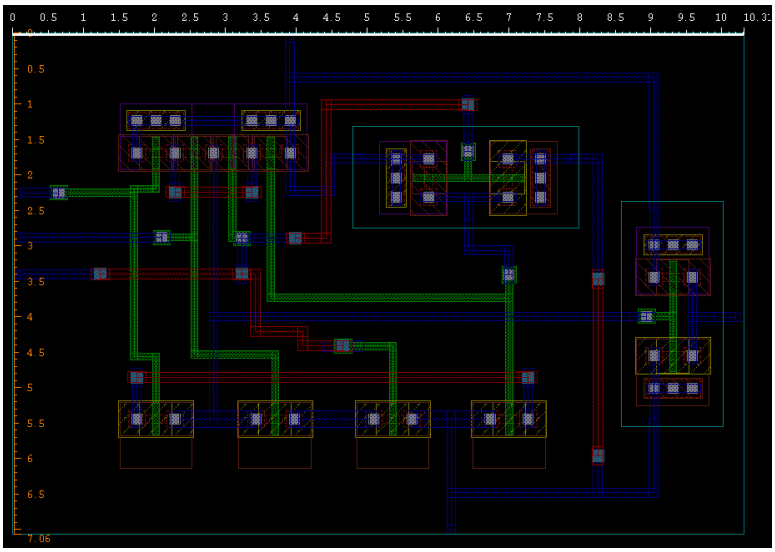



VDD
A
B
S
OUT
GND

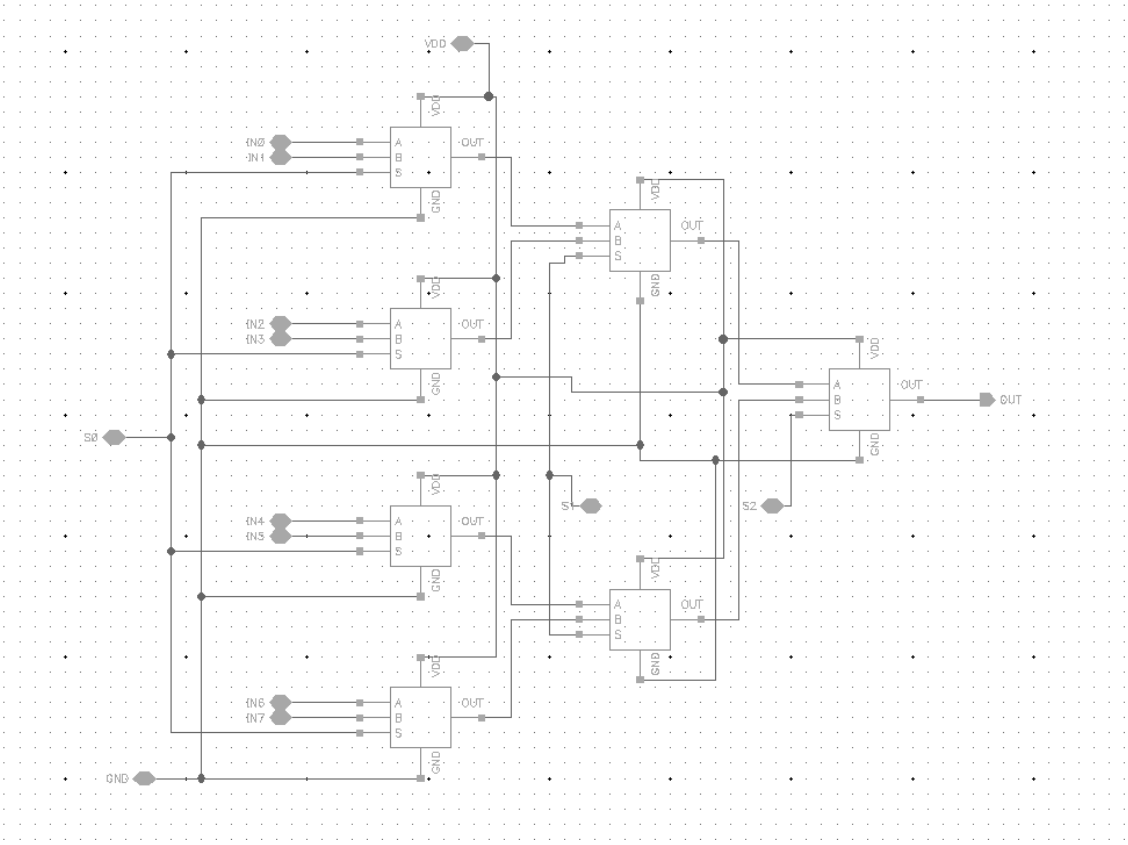


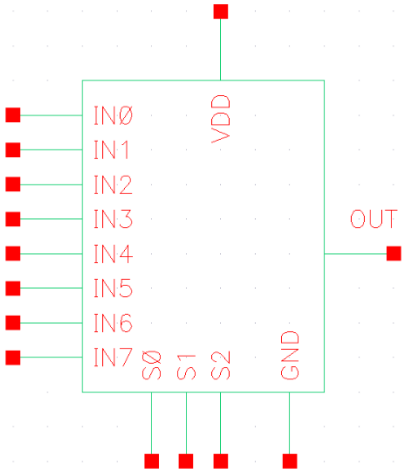


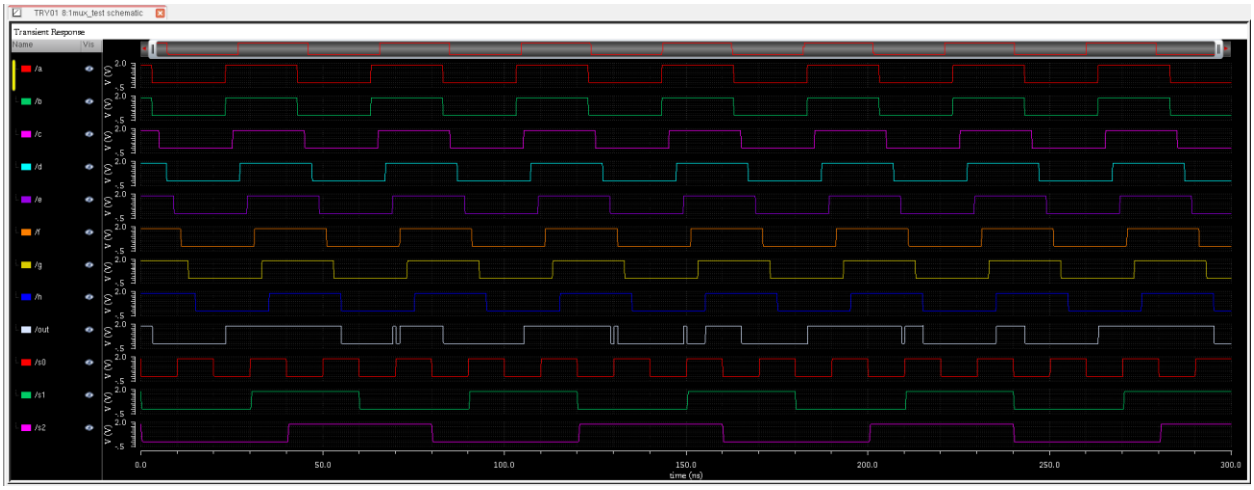
Area of the layout = 72.859 μm^2

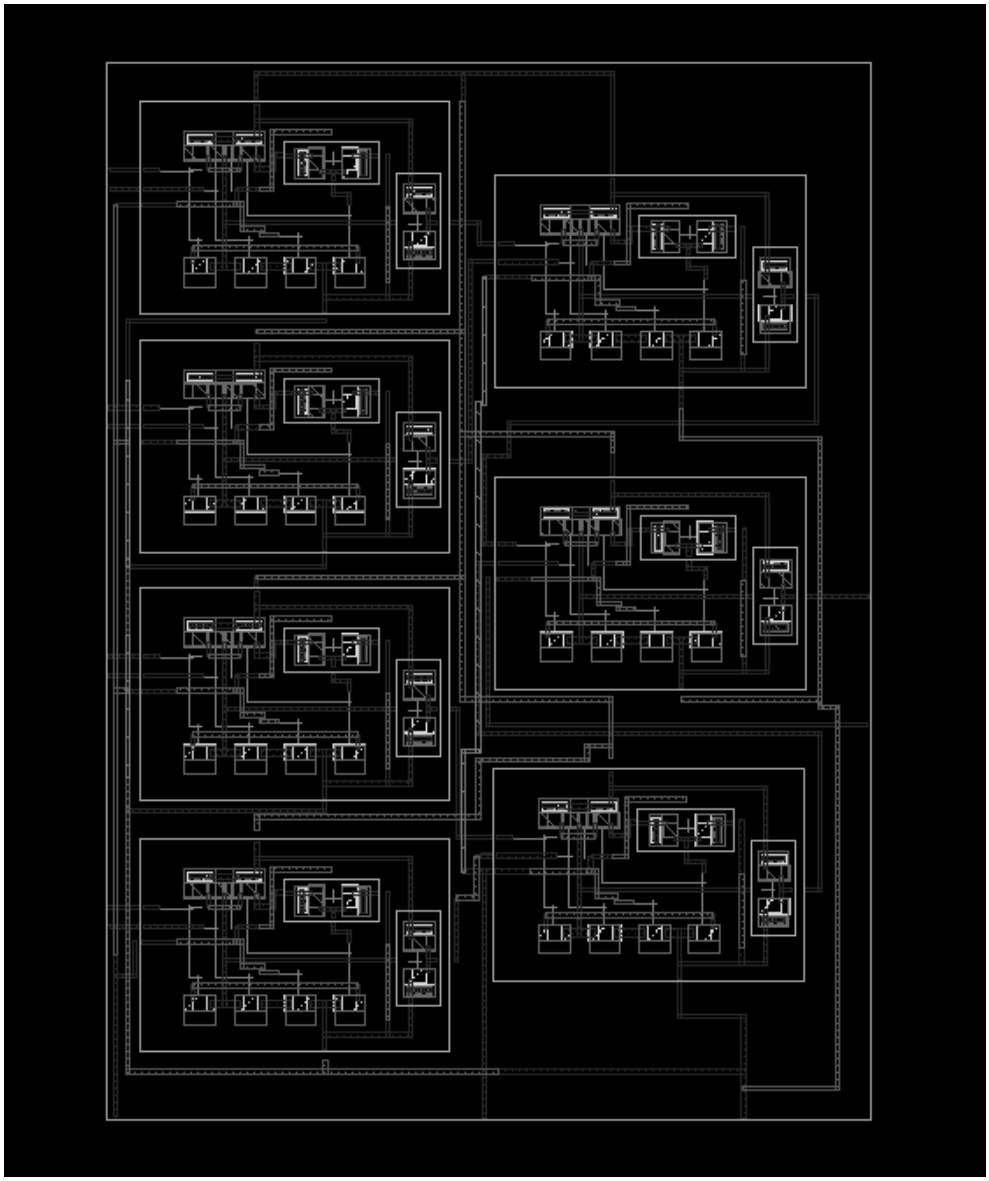


e. 8:1 MUX

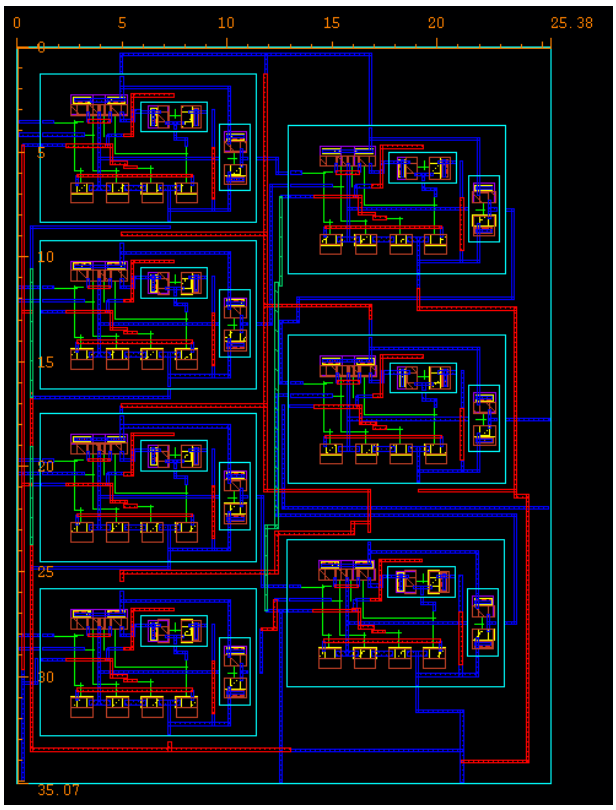

VDD
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
S0
S1
S2
GND
OUT
A
B
S


IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
VDD
OUT
S0
S1
S2
GND

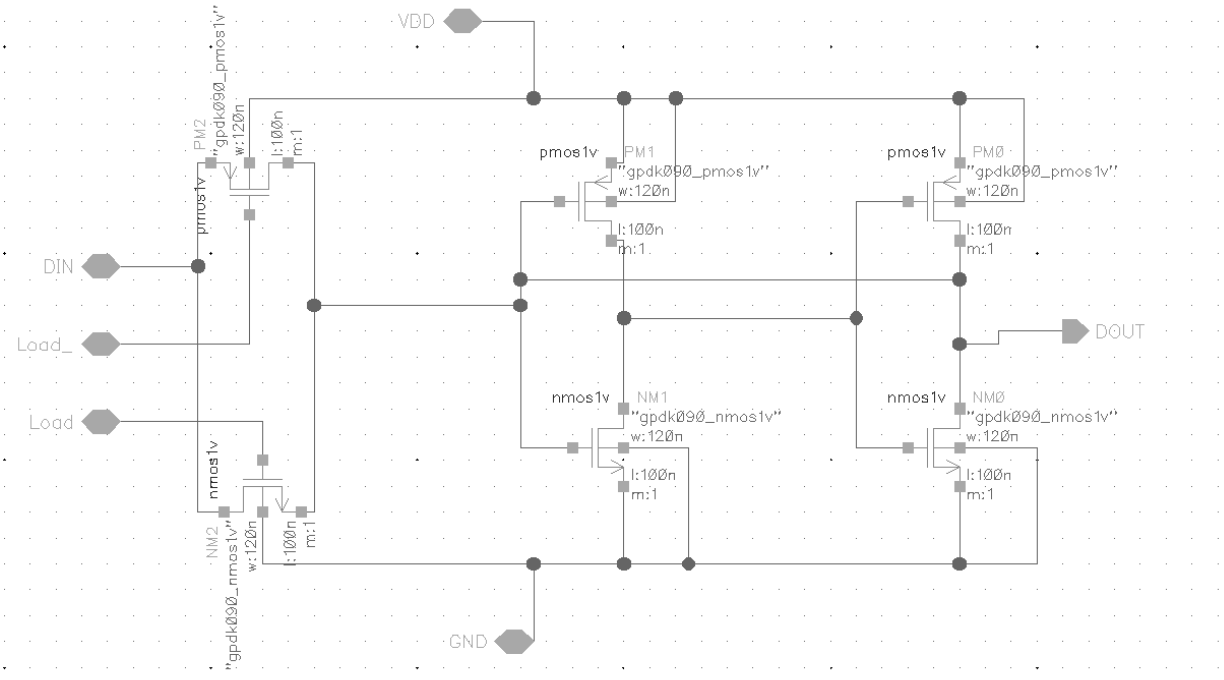

TRV01 8:1mux_test schematic
Transient Response
Name
Val
/a
/b
/c
/d
/e
/f
/g
/h
/out
/s0
/s1
/s2
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time (ns)

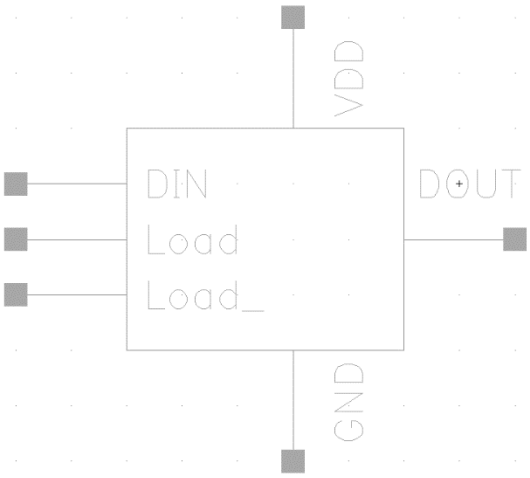


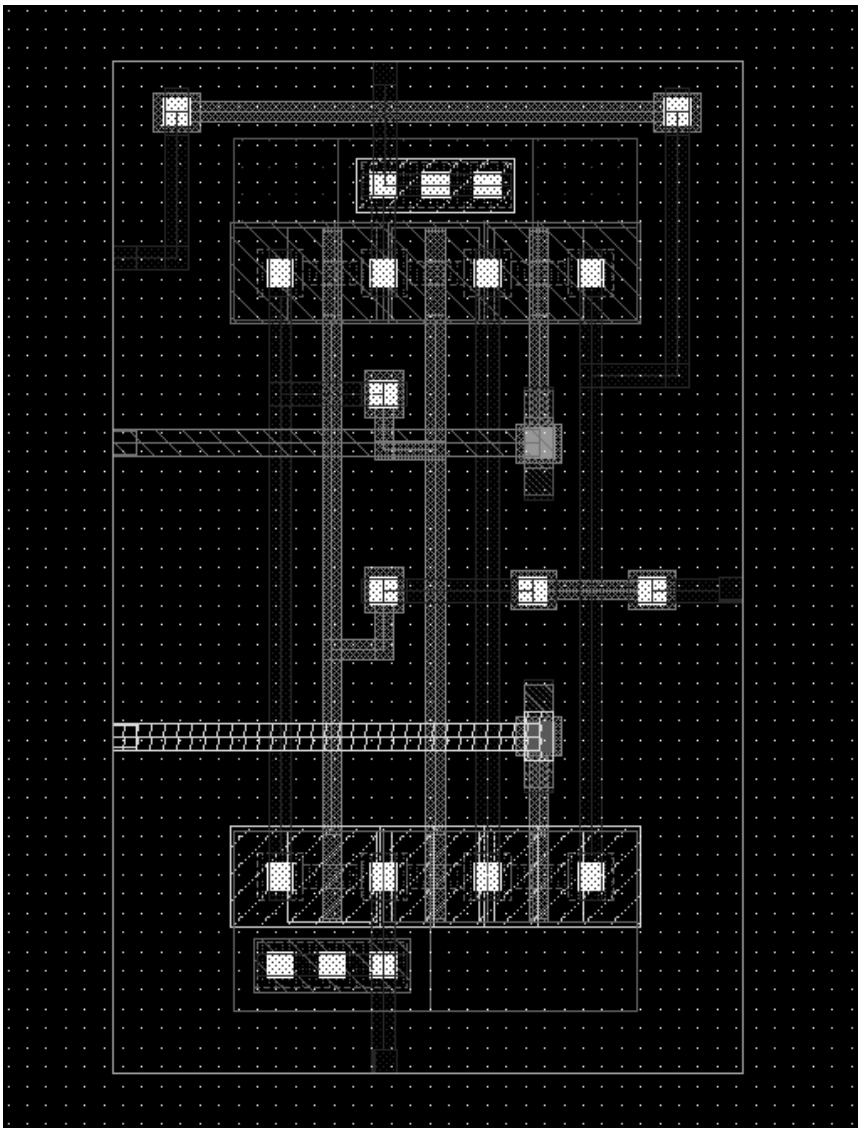
Area of the layout = 890.07 μm^2



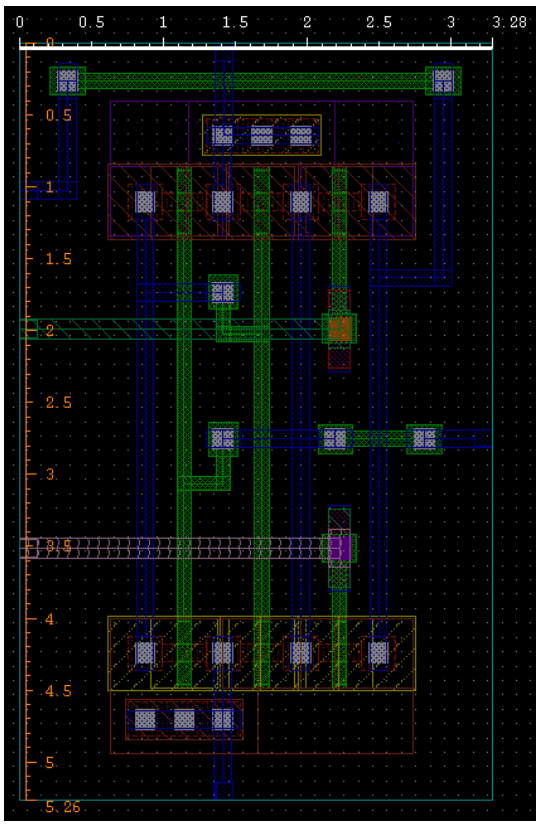
f. SRAM



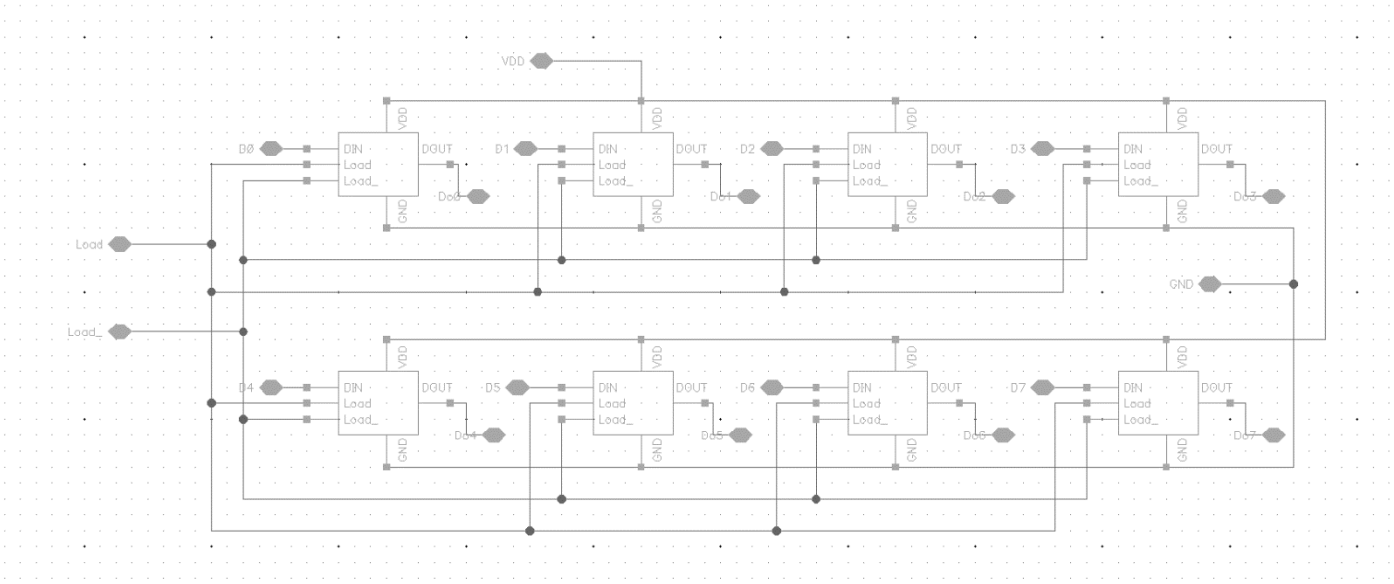

VDD
DIN
Load
Load_
DOUT
GND

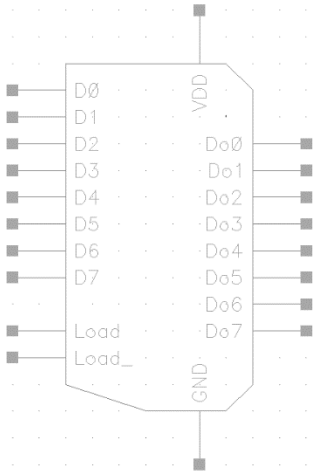


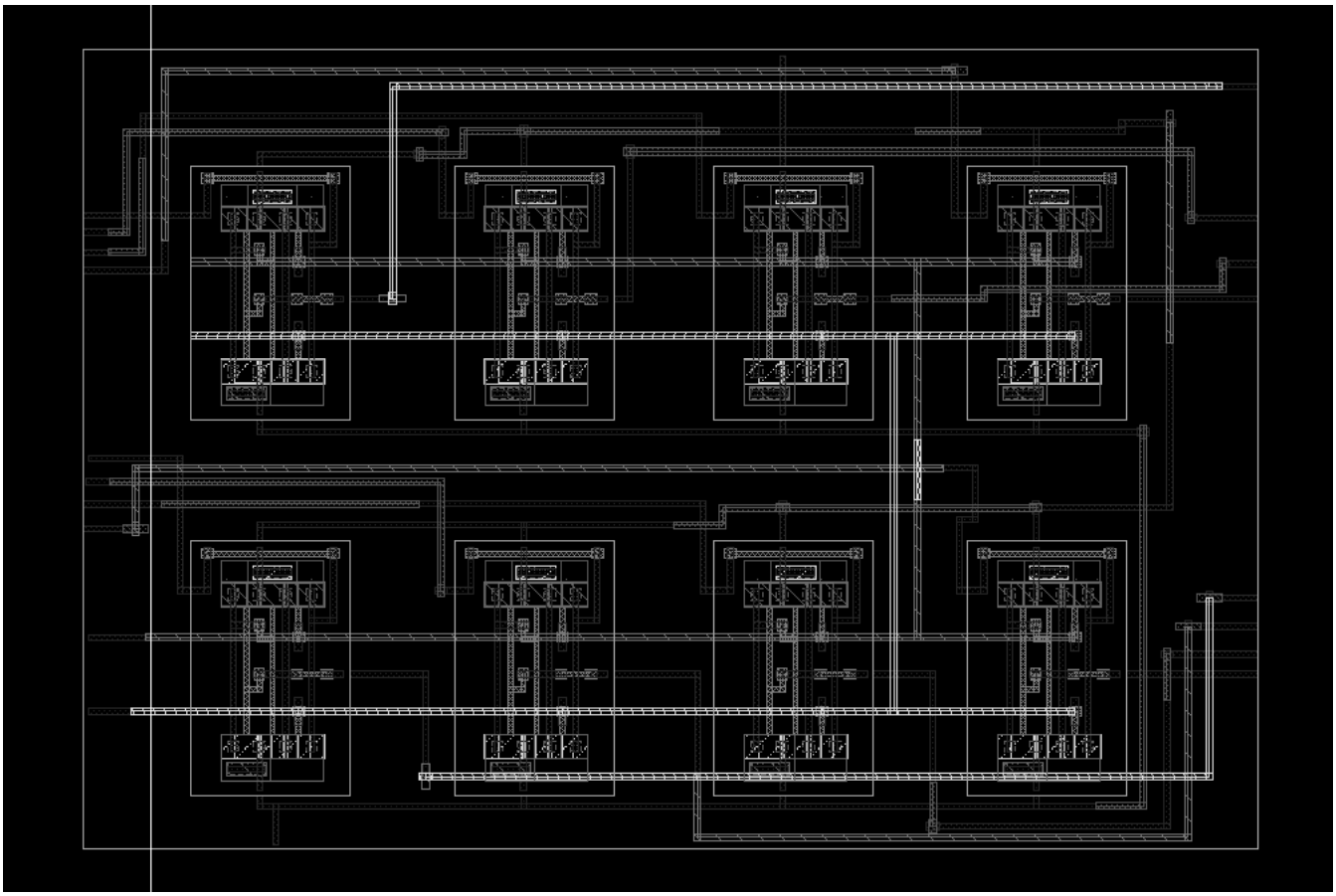
Area of the layout = 17.25 μm^2



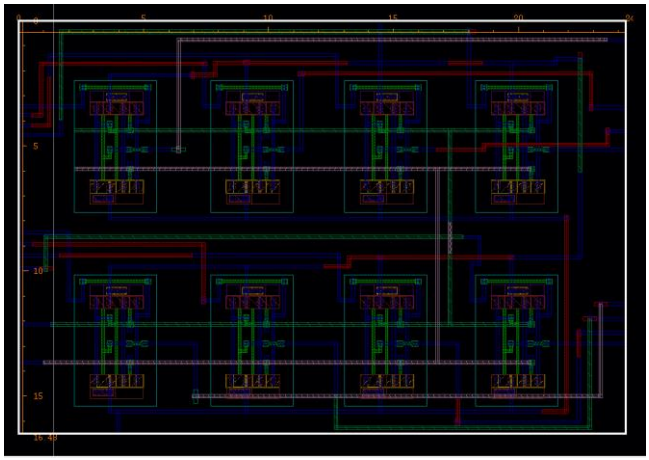
g. SRAM 8bit



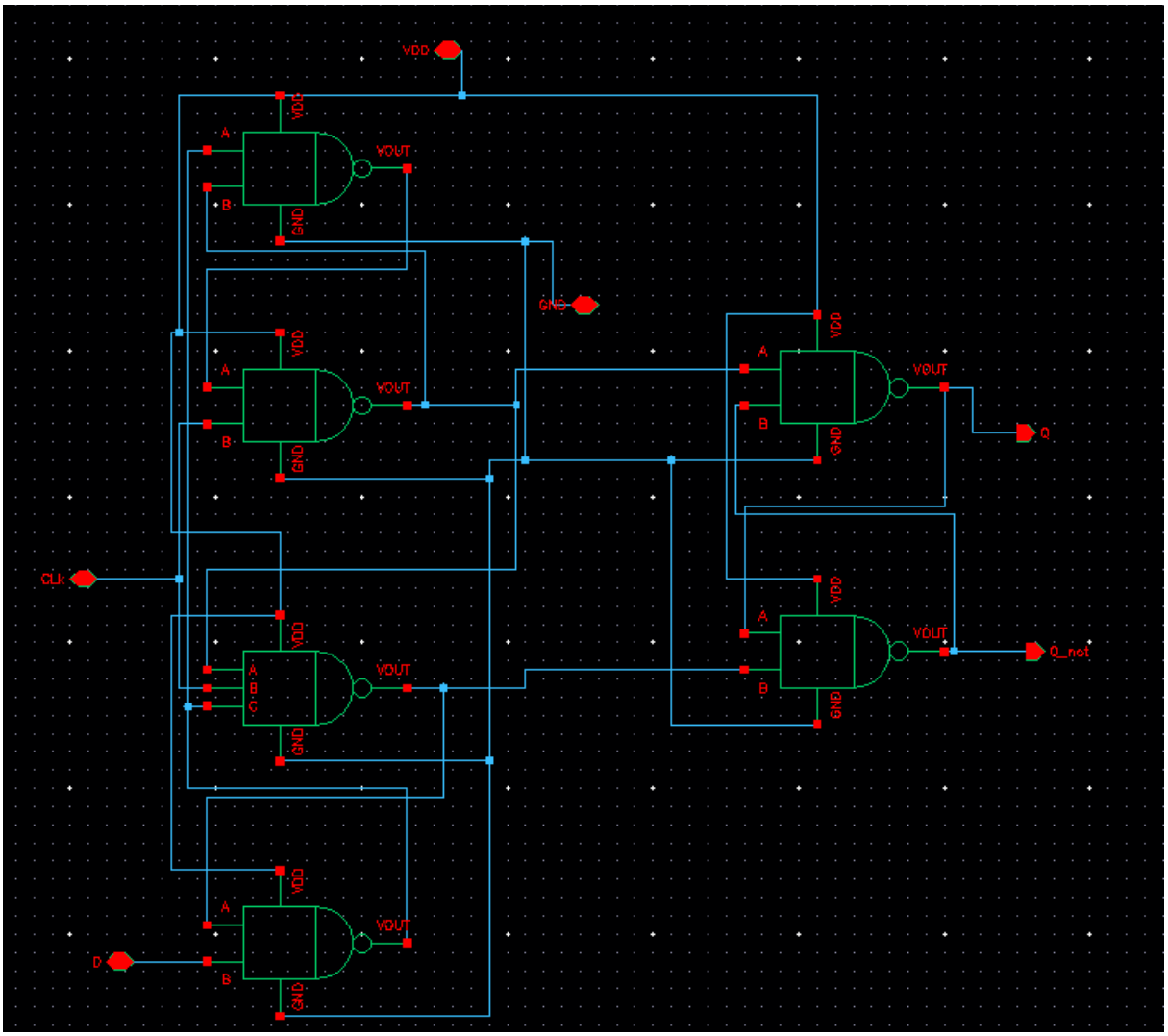

D0
D1
D2
D3
D4
D5
D6
D7
Load
Load_
VDD
GND
Do0
Do1
Do2
Do3
Do4
Do5
Do6
Do7

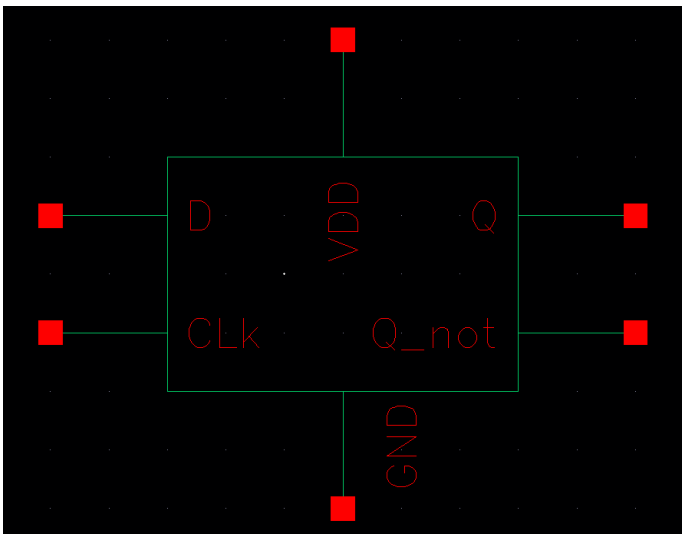


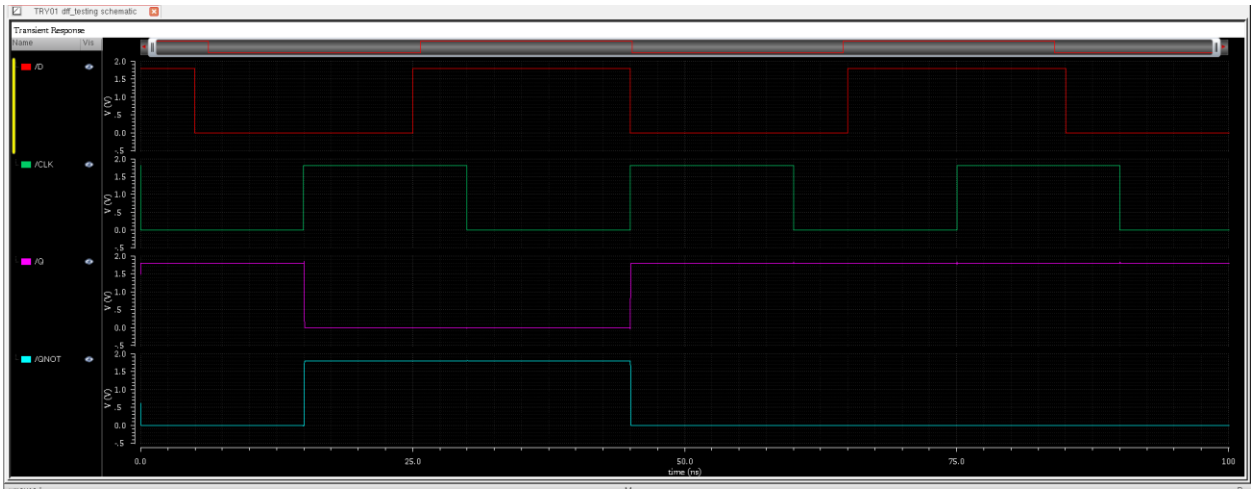
area of the layout = 395.52 μm^2



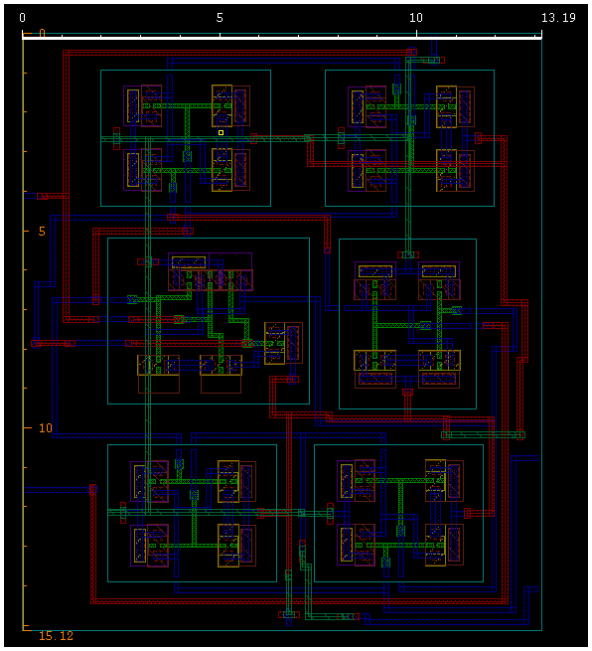
h. D positive edge flipflop



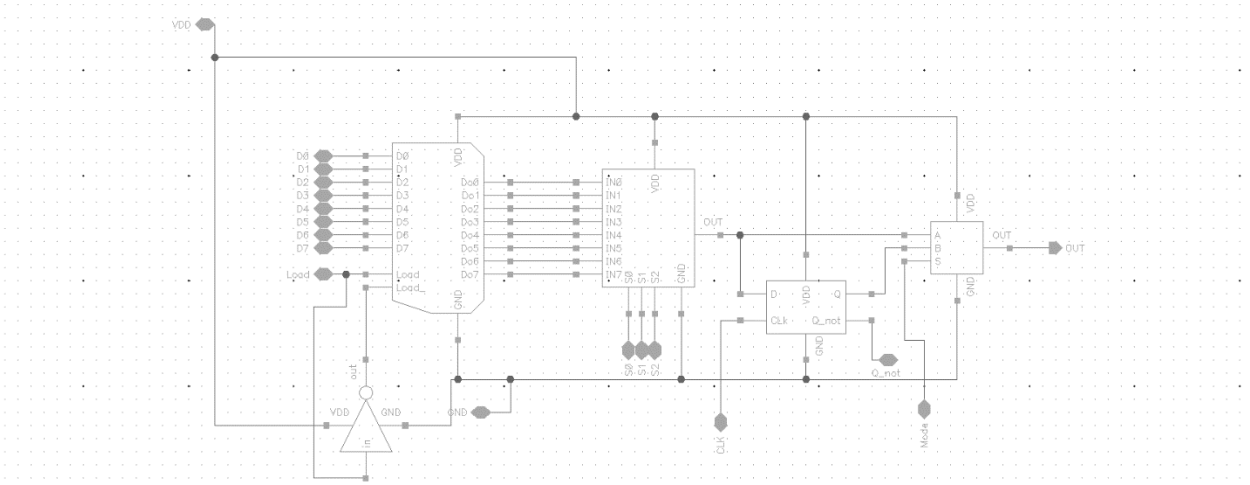


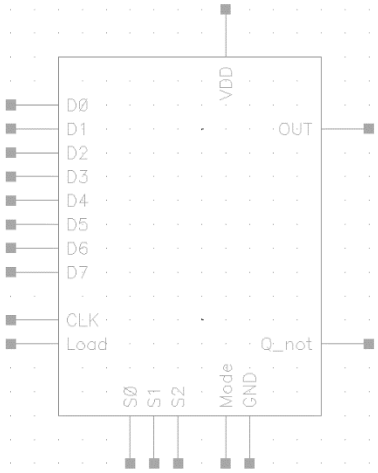


area of the layout = 200.2242 μm^2

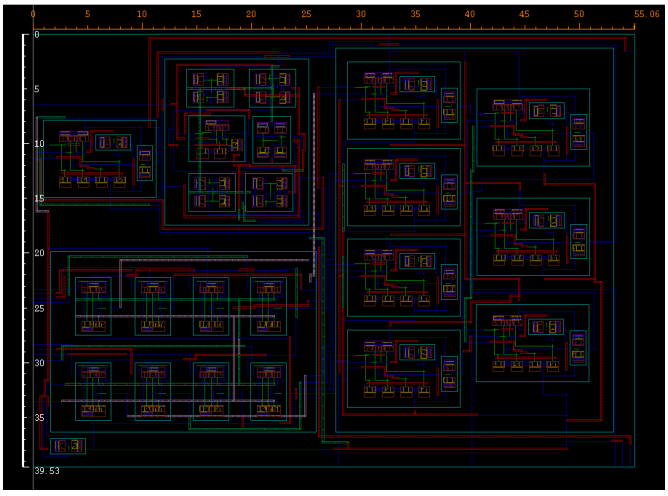


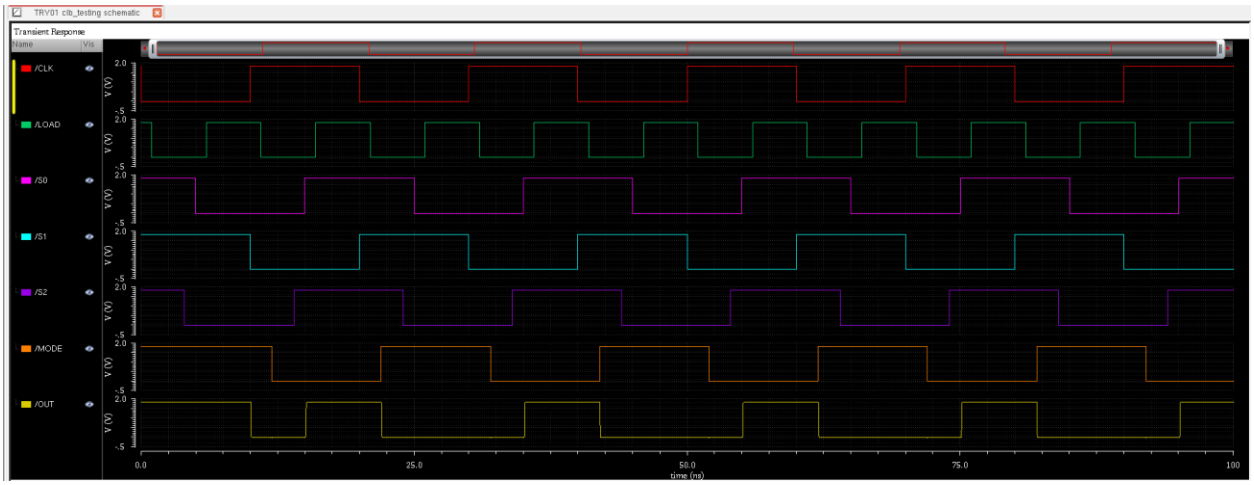
i. CLB

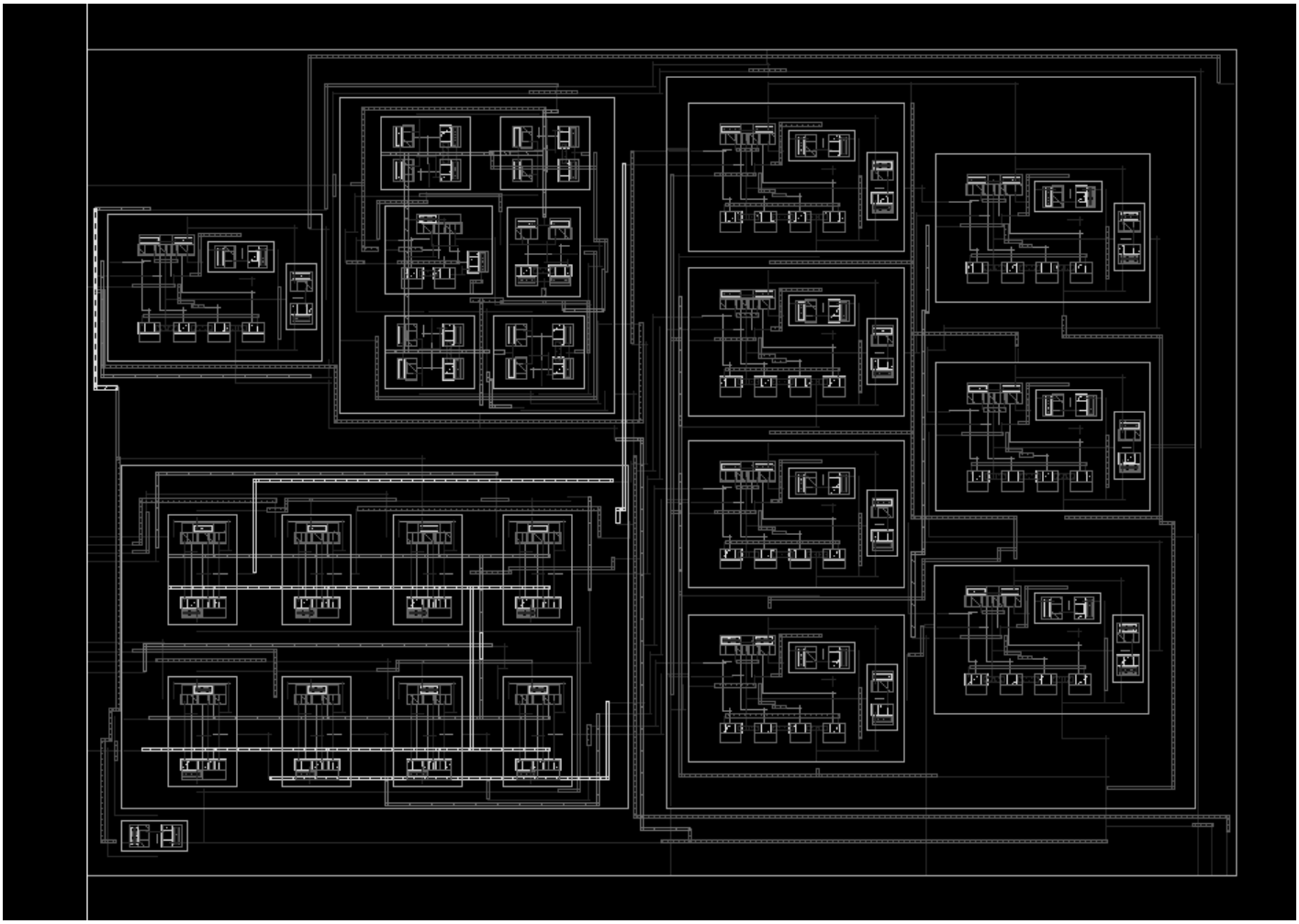




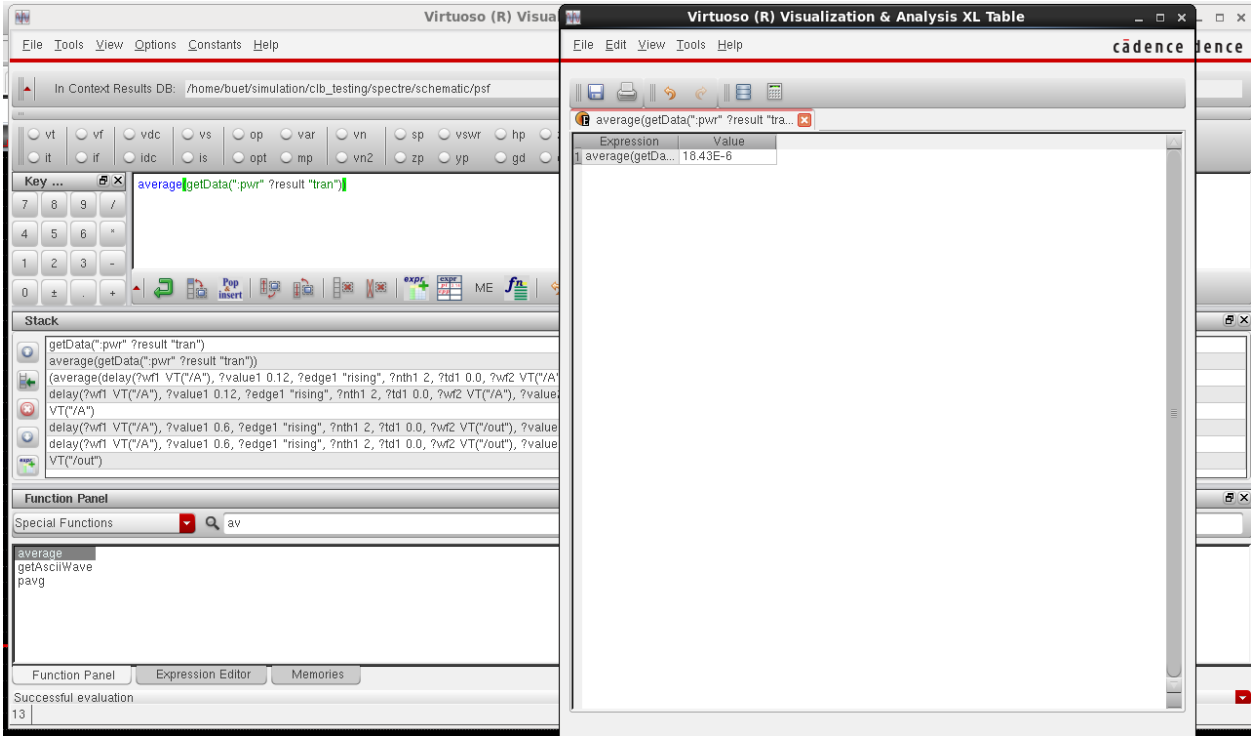
Area of the layout = 2176.52 μm^2




TRV01 clb_testing schematic
Transient Response
Name
Vis
/CLK
/LOAD
/S0
/S1
/S2
/MODE
/OUT
2.0
-.5
0.0
25.0
50.0
75.0
100
time (ns)



Average power consumed by the CLB is 16.43 µW



Average energy Is 357.8×10^{-15} J