

**Military Institute of Science and Technology**

**Department of Electrical, Electronic and Communication Engineering**

**Assignment**

**VLSI II Laboratory [EECE-458]**

**Submitted by,**

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ID: 202216058. Section – A  
EECE-20**

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# Introduction to Cadence Virtuoso

Cadence Virtuoso is an advanced Electronic Design Automation (EDA) platform for analog, digital, and mixed-signal IC design. It supports the full custom design flow, from schematic capture to physical layout and post-layout verification. Core capabilities include parameterized cell (PCell) creation, constraint-driven layout editing, and integration with simulation tools (Spectre, APS) for pre- and post-layout analysis. The Virtuoso Layout Suite enables DRC, LVS, and parasitic extraction using integrated verification engines. Designers can optimize area, performance, and power while ensuring fabrication compliance through foundry-provided PDKs. Its tight coupling between schematic, layout, and simulation accelerates design closure and minimizes costly re-spins.

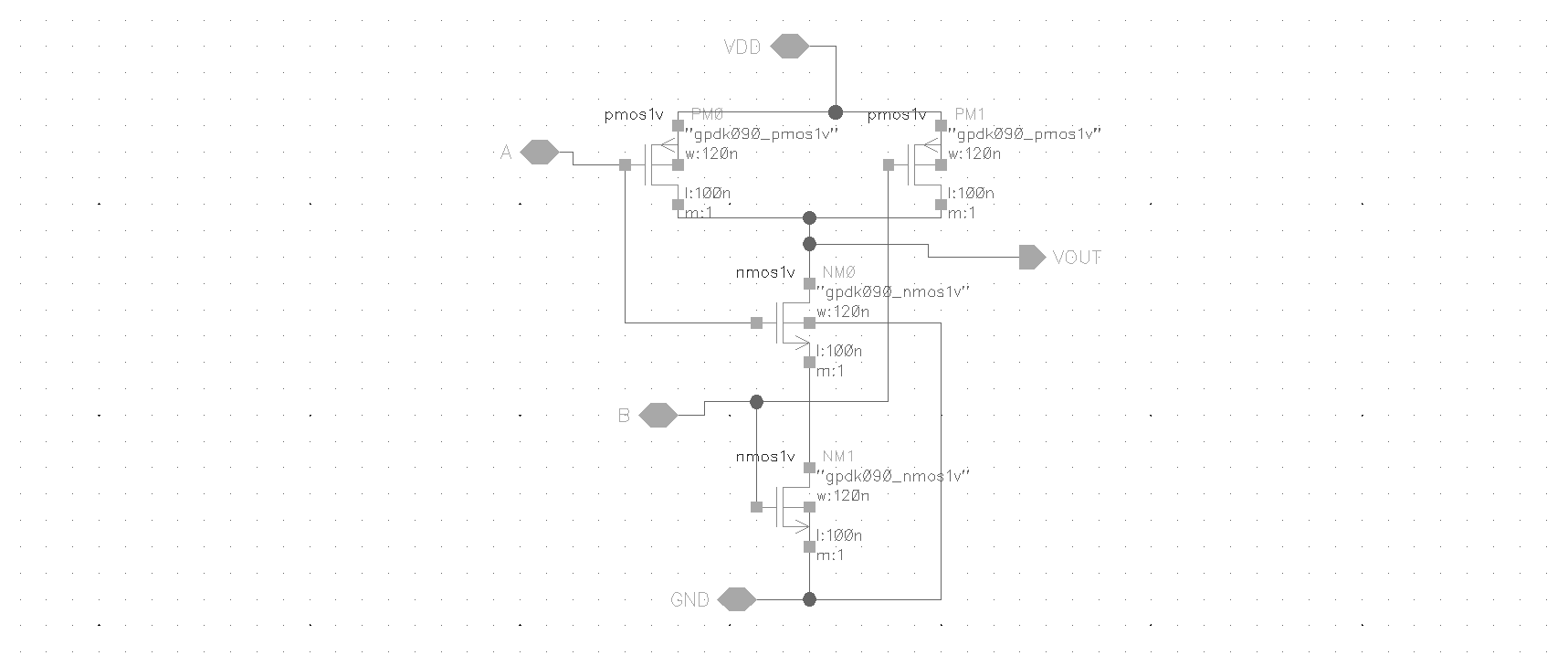
# Introduction to Configurable Logic Block (CLB)

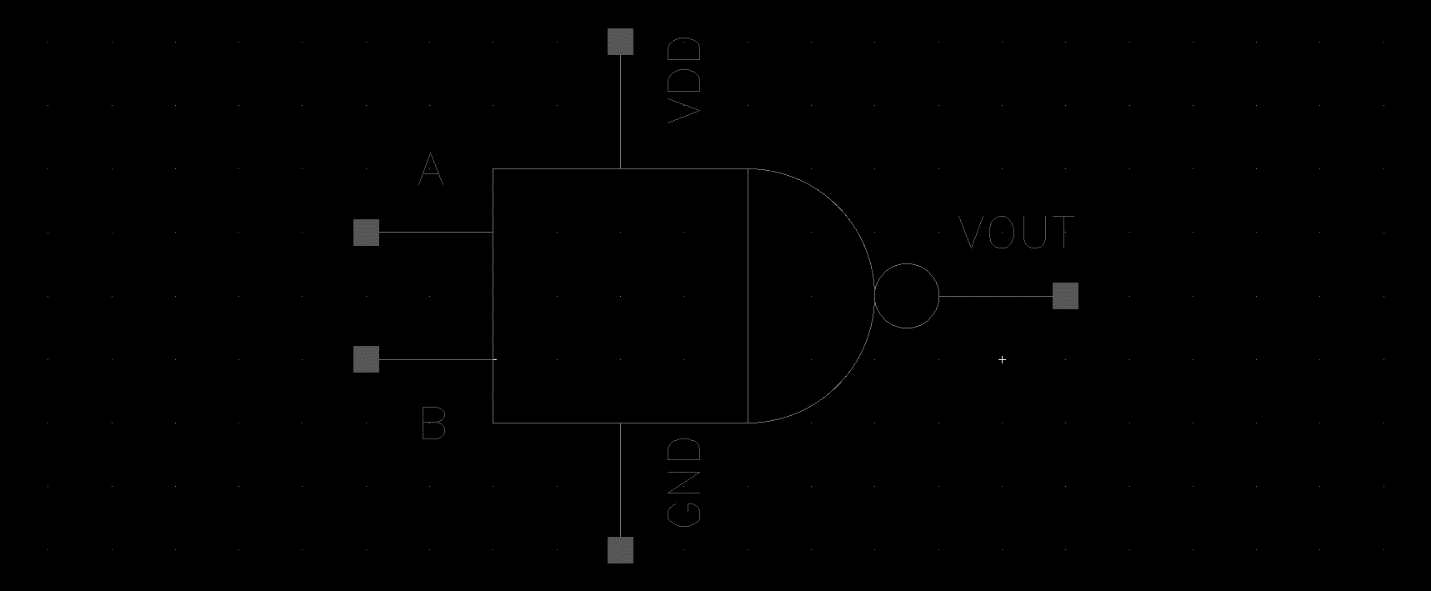
A Configurable Logic Block (CLB) is a fundamental logic unit in FPGAs and reconfigurable digital ICs. It typically contains:  
- Look-Up Tables (LUTs) – implement arbitrary combinational logic by storing truth table outputs.  
- Flip-Flops/Latches – provide sequential storage for state machines and pipelining.  
- Multiplexers – enable routing flexibility within the block.  
- Programmable interconnects – connect CLBs to each other and to global routing.  
Modern CLBs support wide-input LUTs (6–8 inputs), distributed RAM, and shift-register modes. They are configured via bitstreams generated from synthesis and place-and-route tools, enabling rapid prototyping and post-deployment reprogramming. CLB architecture directly impacts FPGA density, speed, and power efficiency.

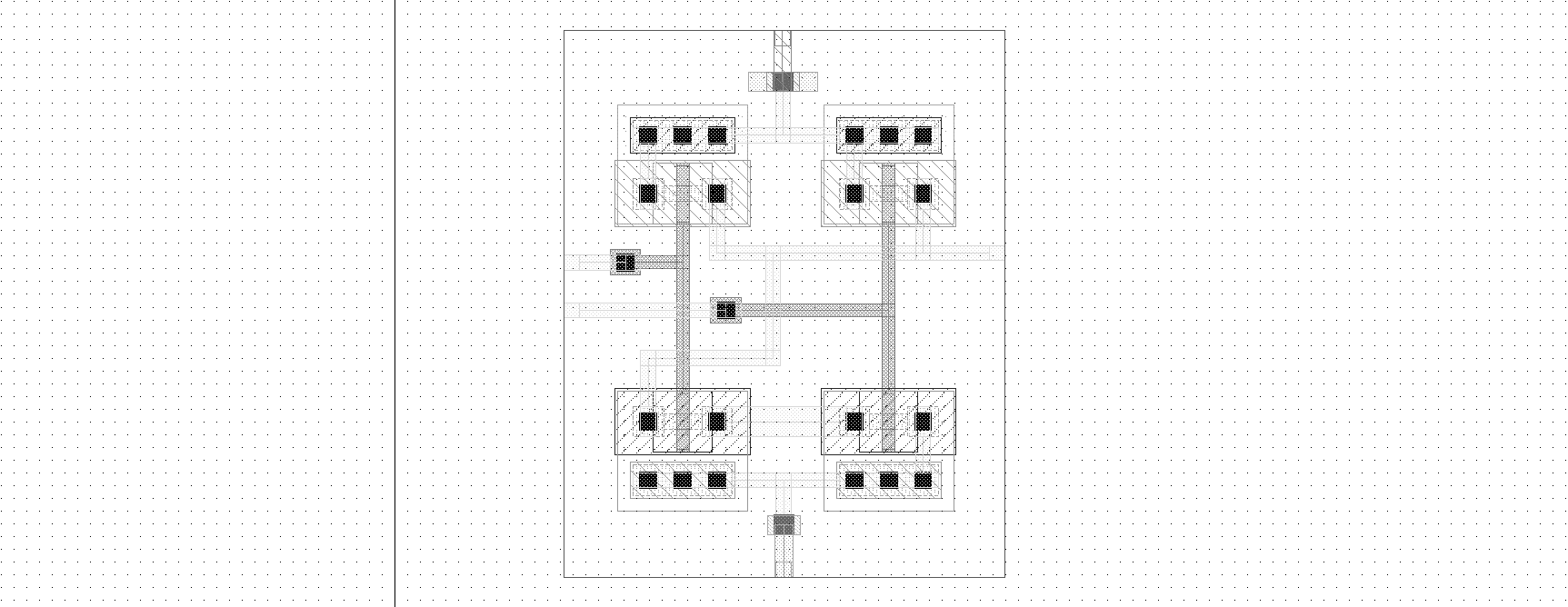
# Schematic, symbol and layouts

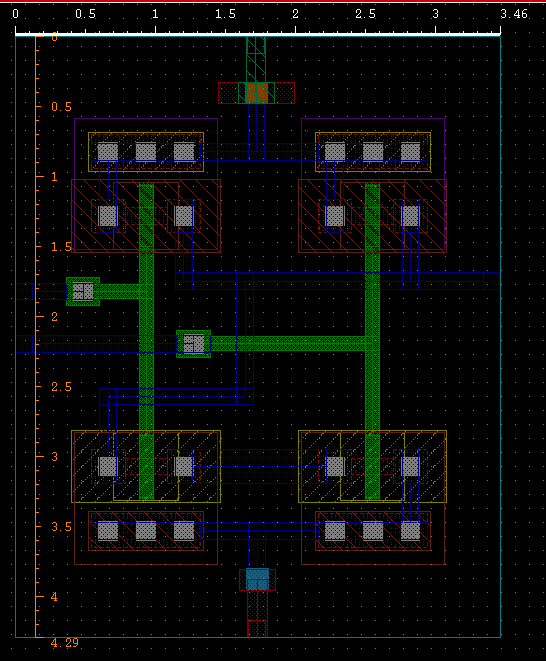
All the necessary schematics, symbols and layouts of the used gates, logics are shown with proper graphics and values.

1. 2 input NAND

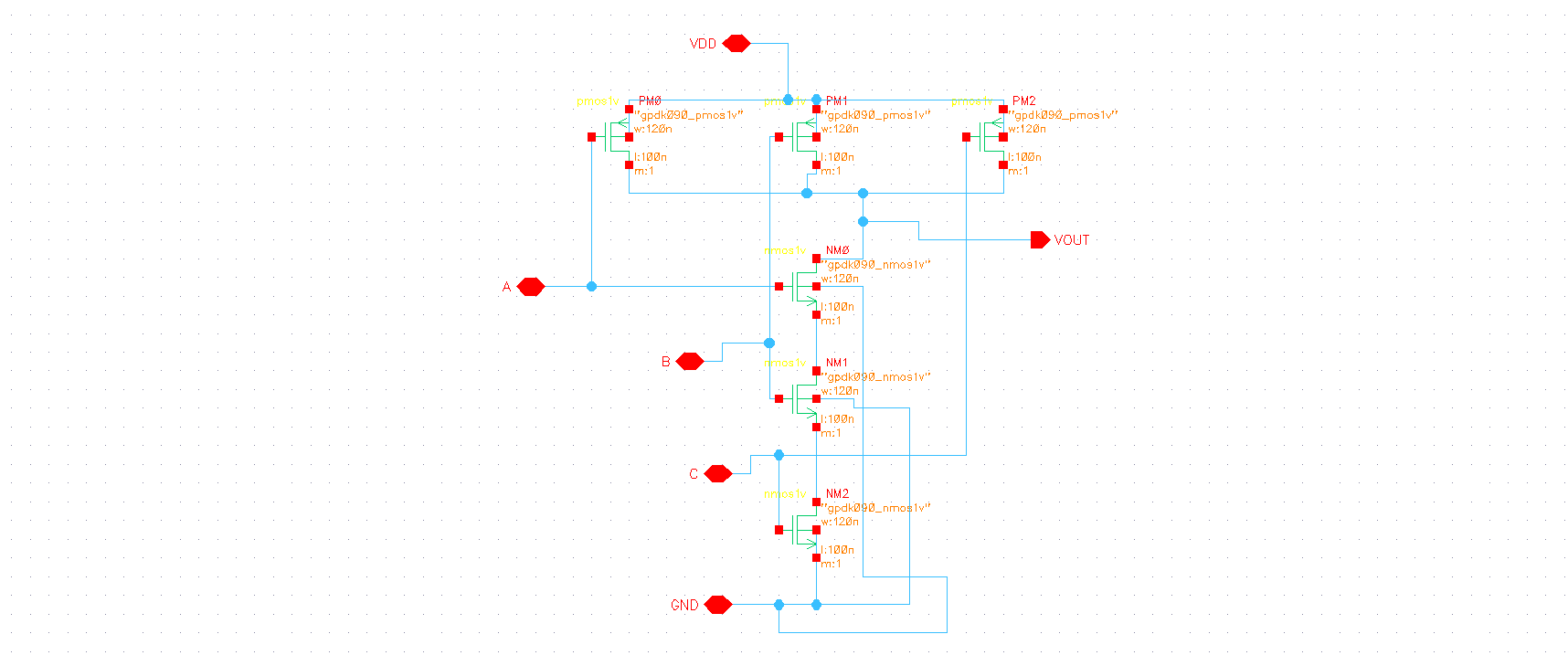


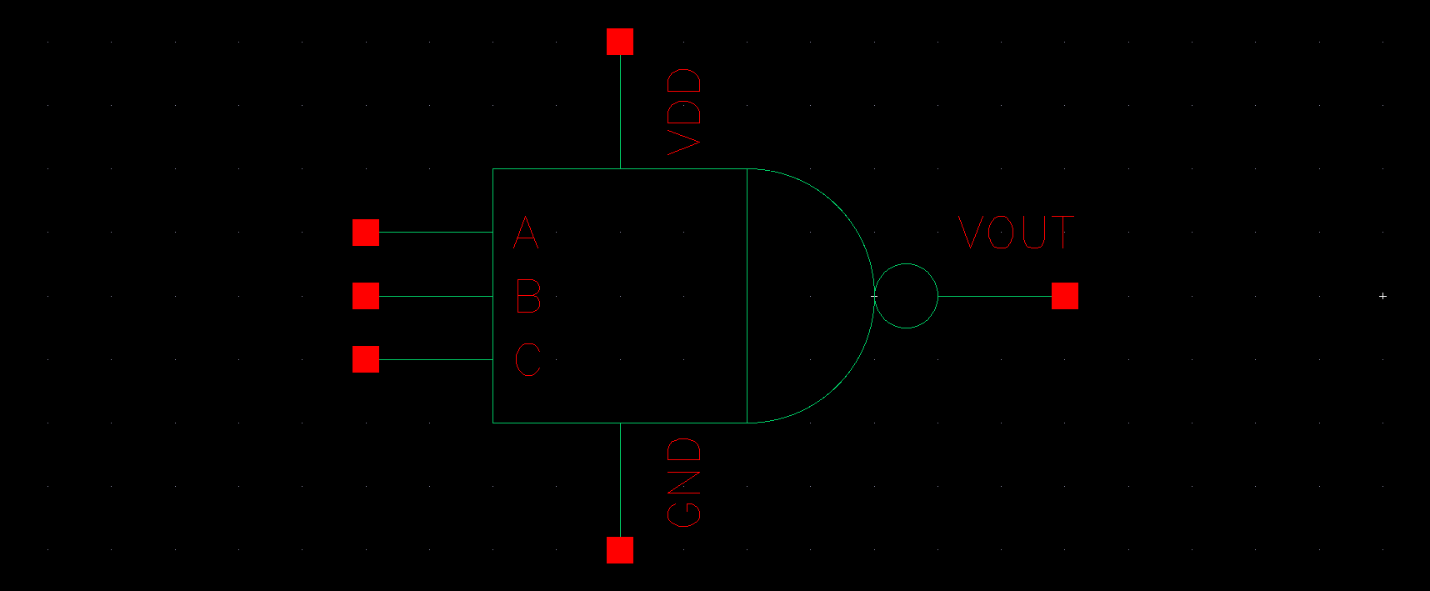


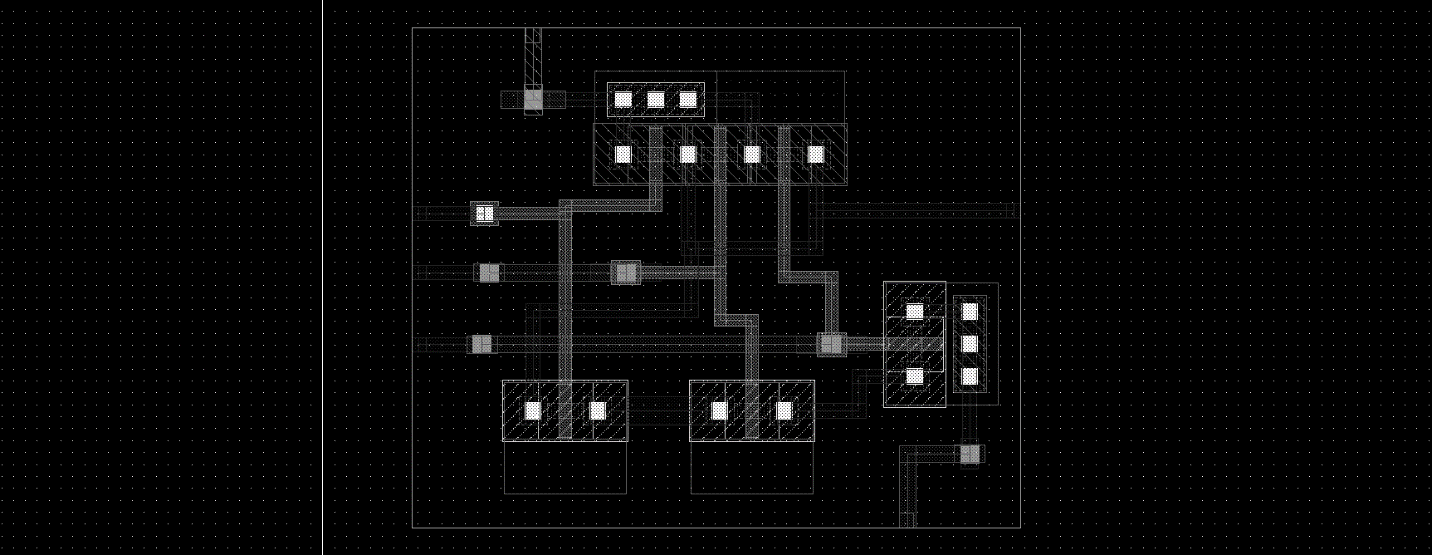


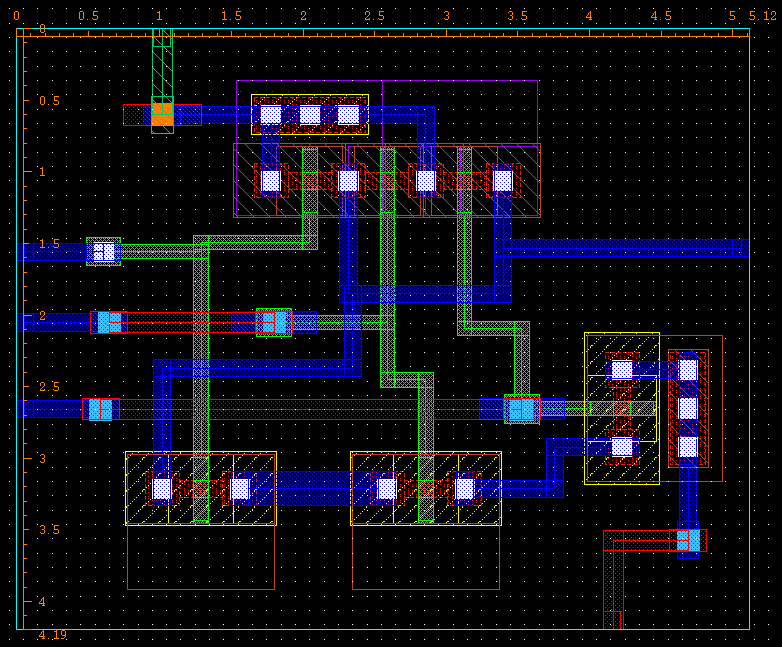
area of the layout is = 14.85 μm2

1. 3 input NAND

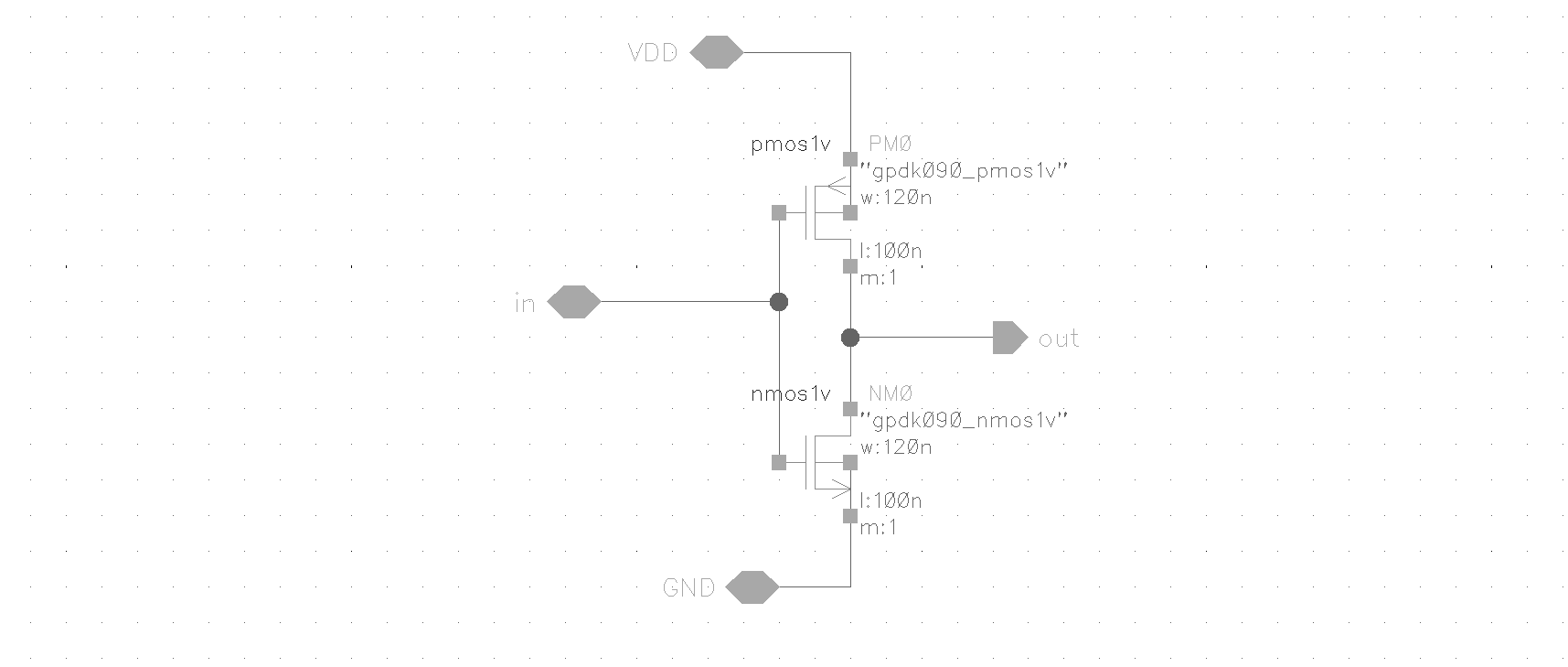


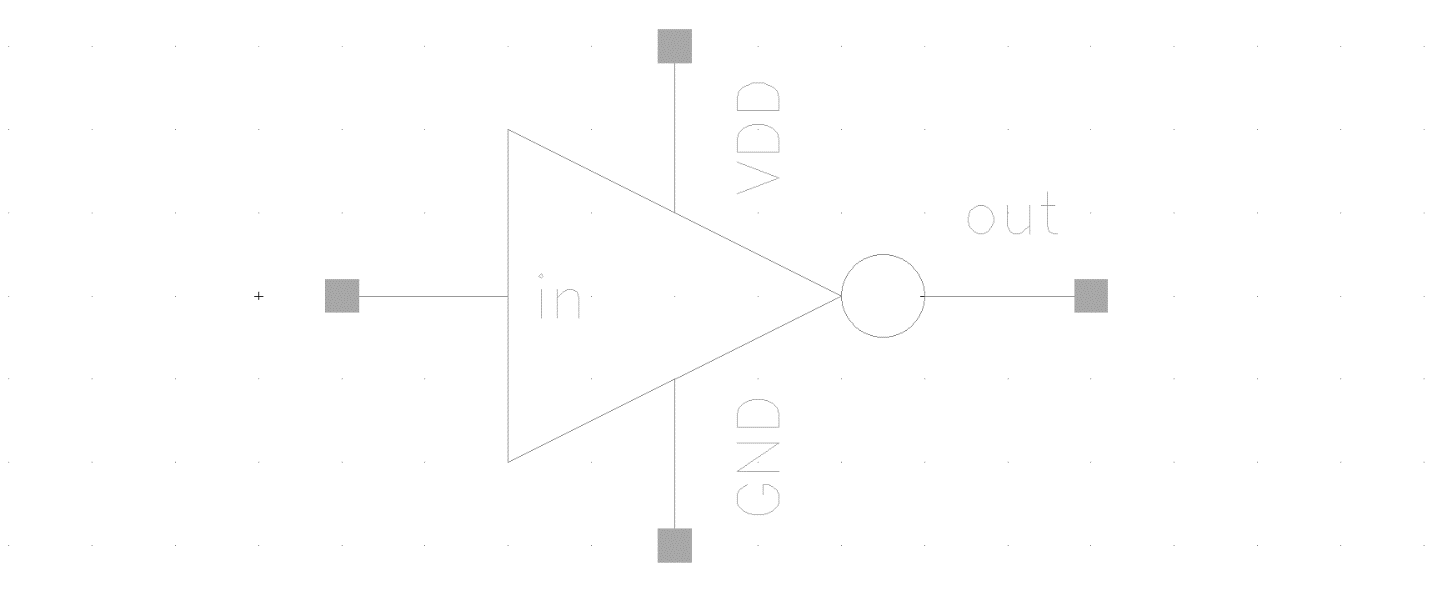


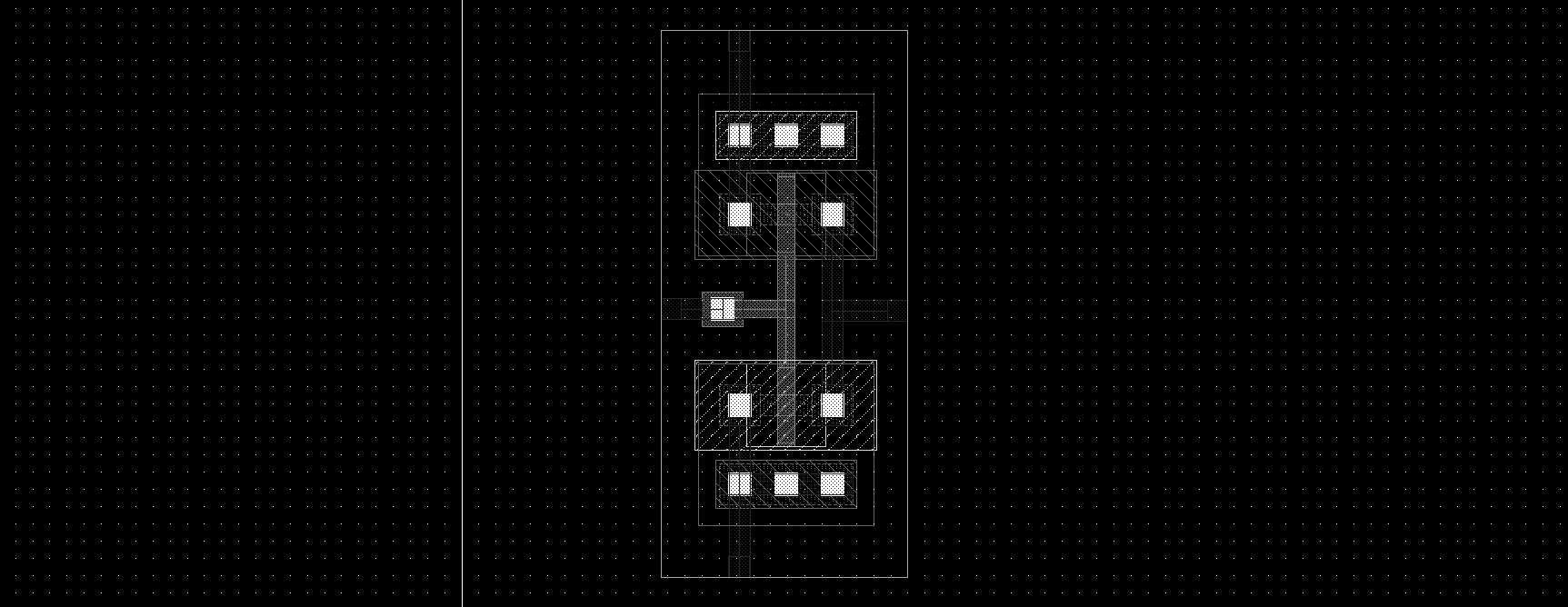


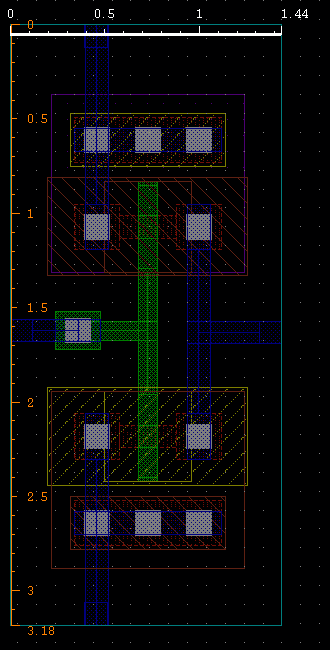
area of this layout = 21.45 μm2

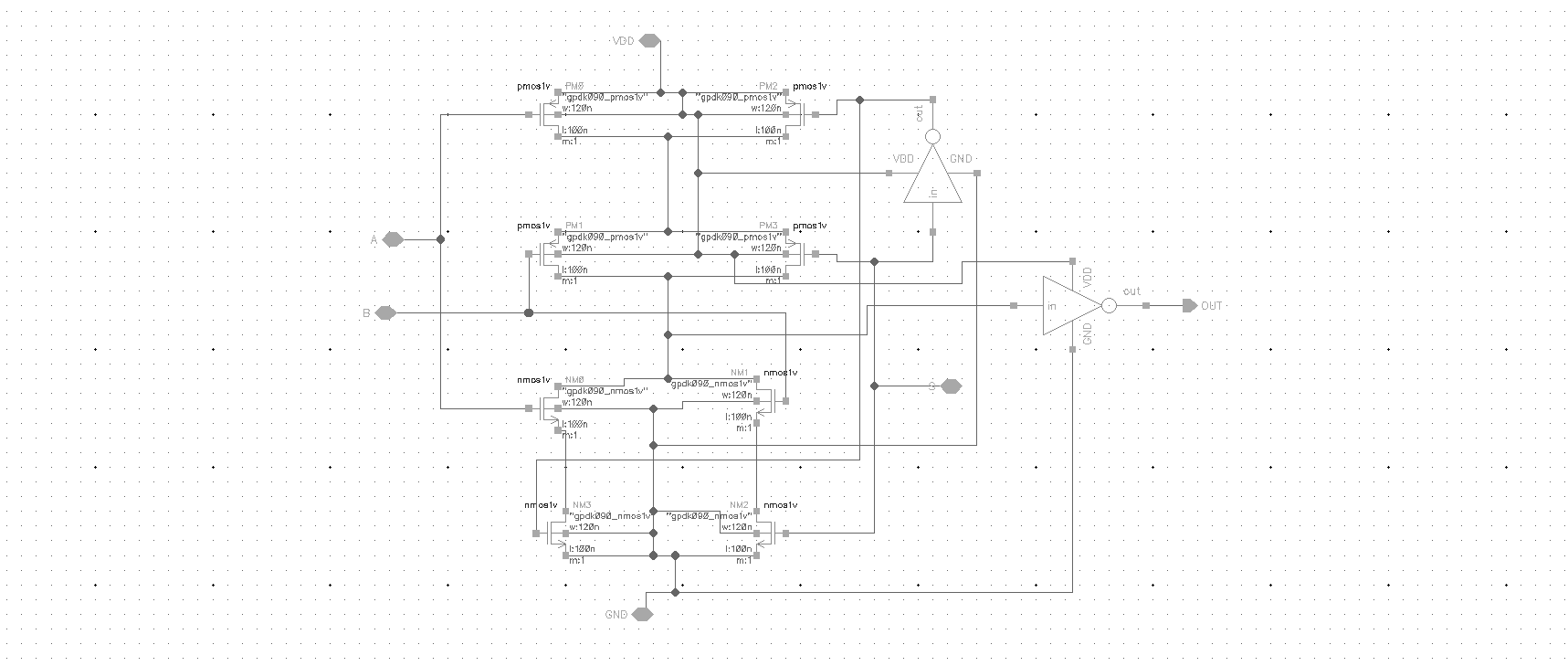
1. Inverter

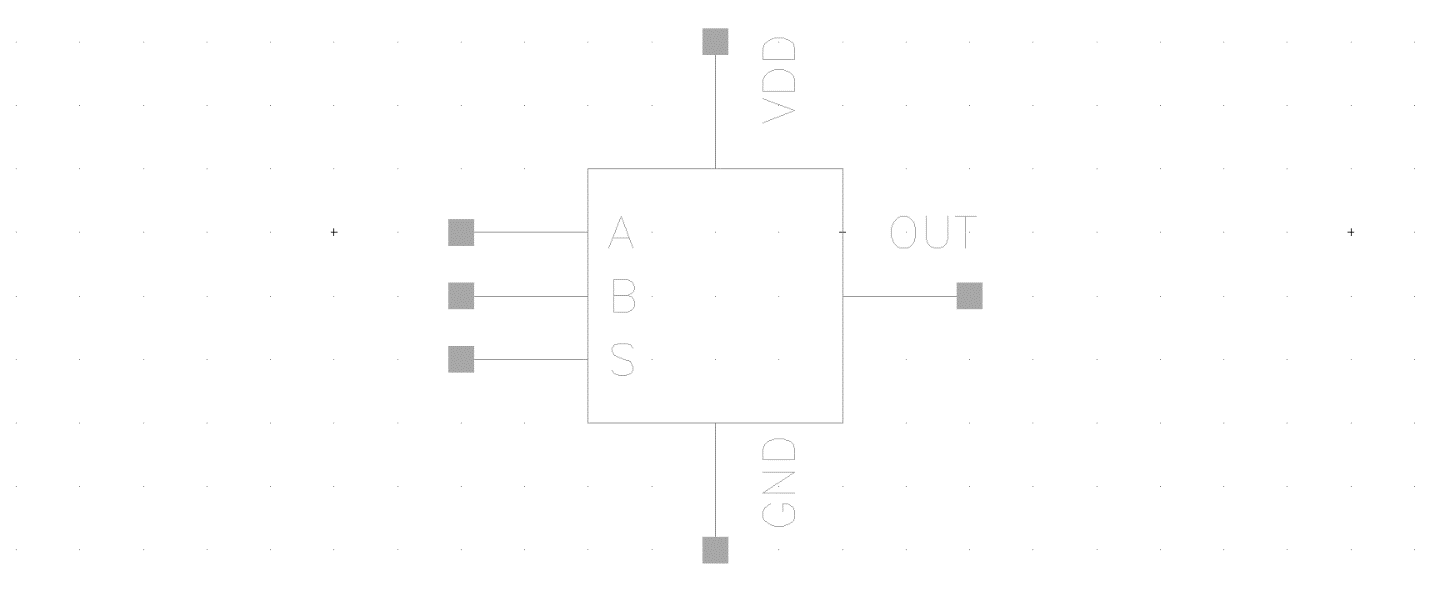


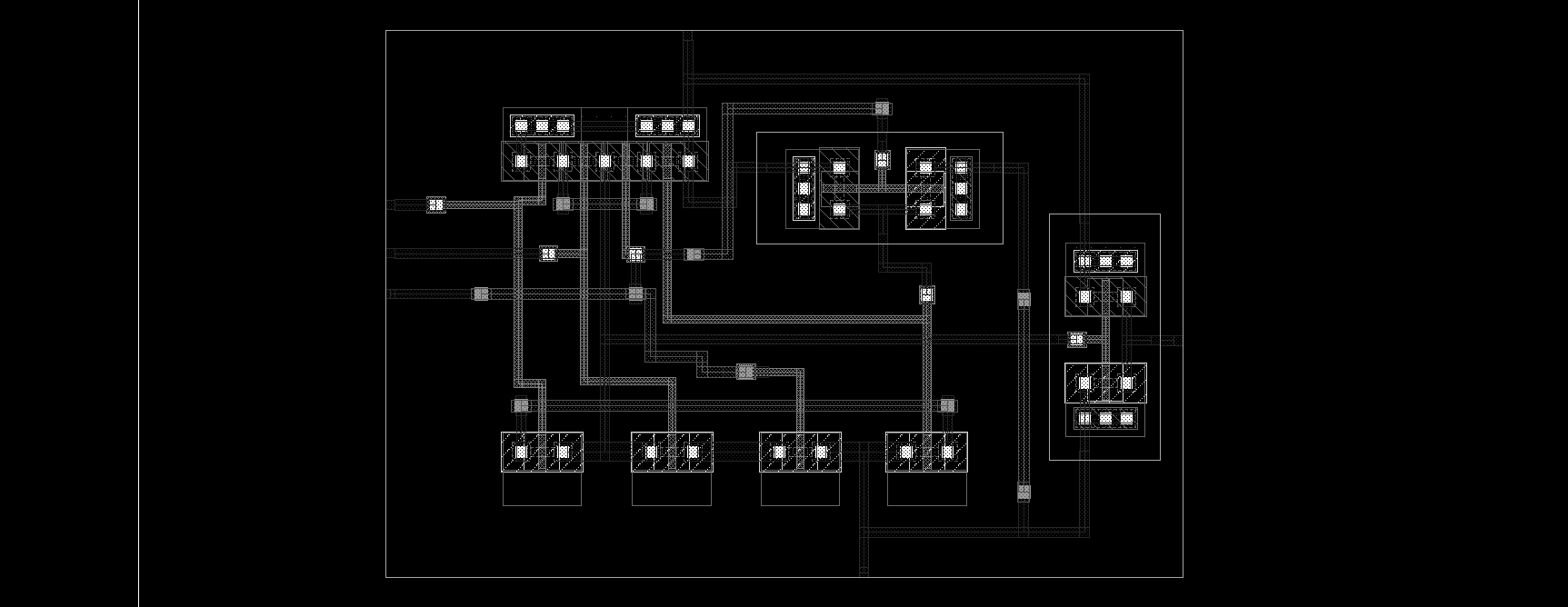


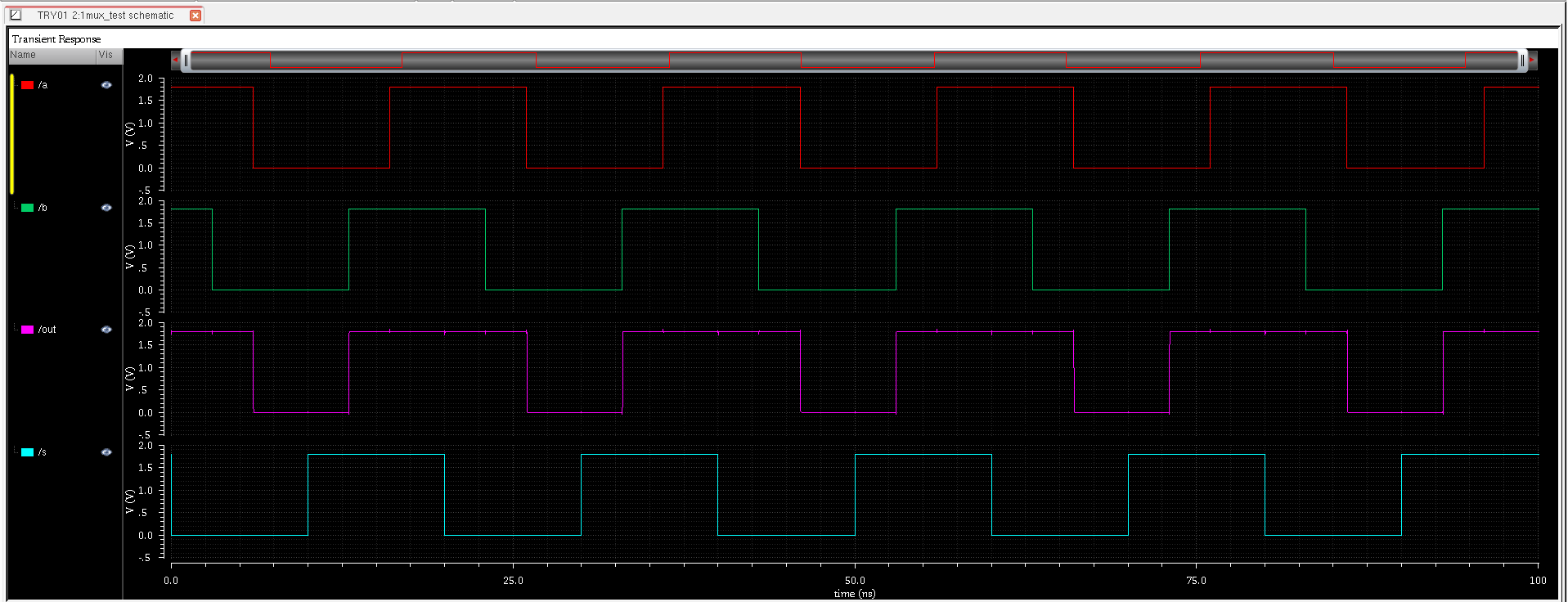


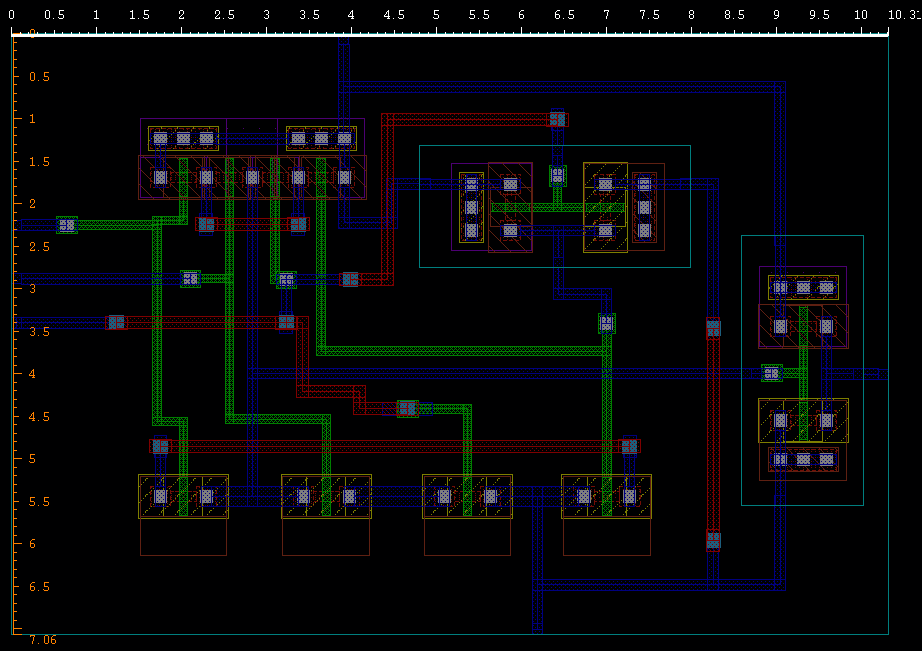
Area of the layout = 4.579 μm2

1. 2:1 MUX

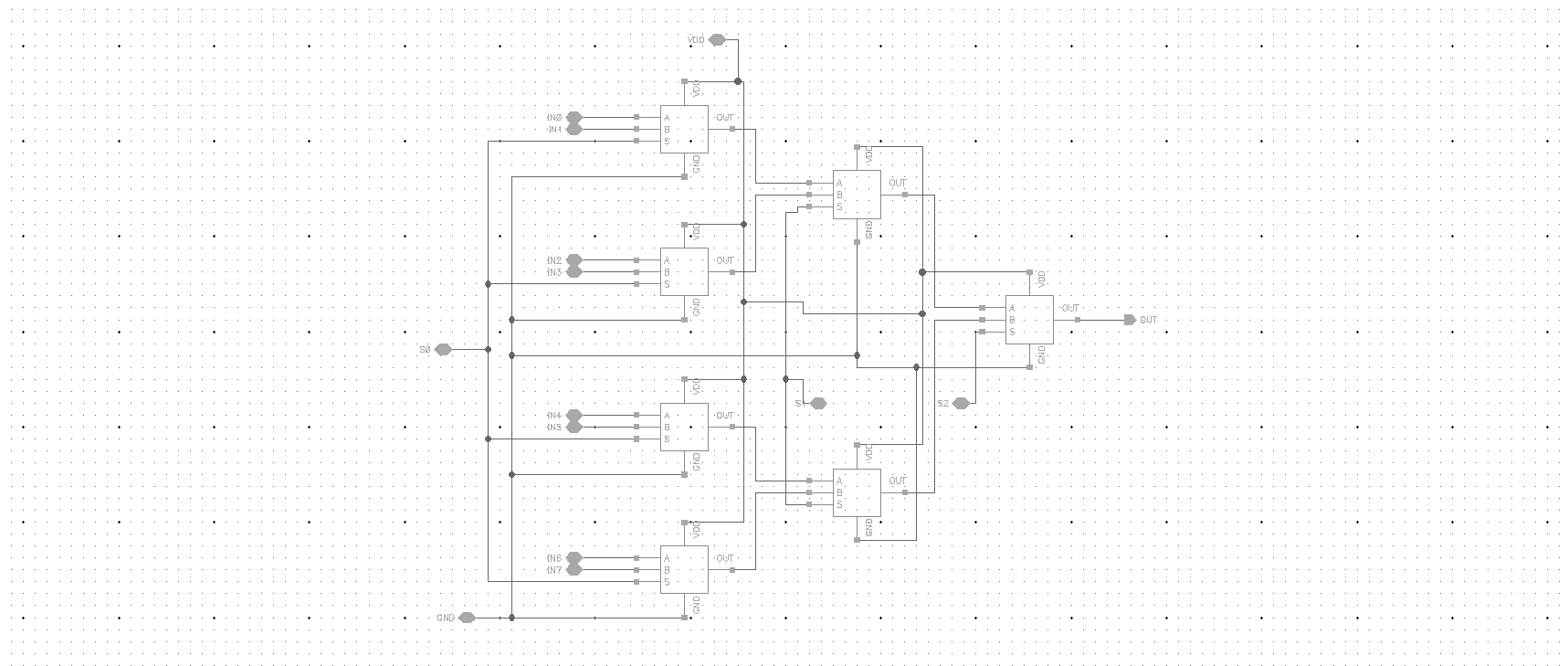


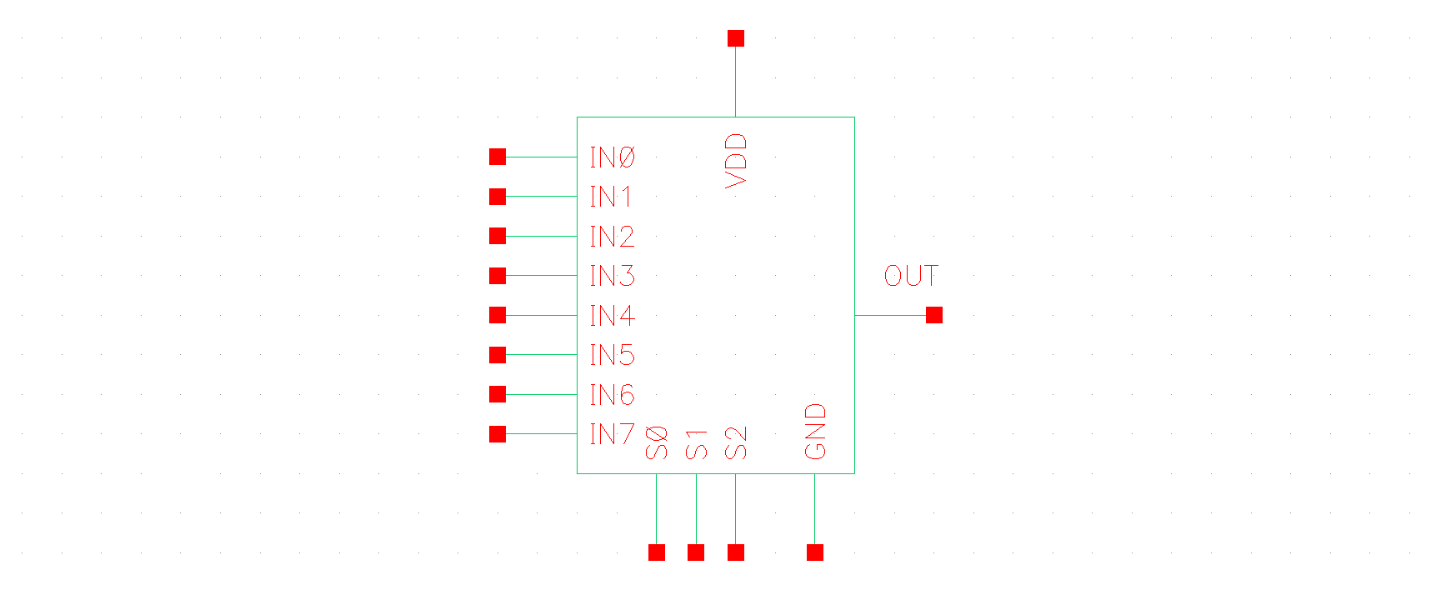


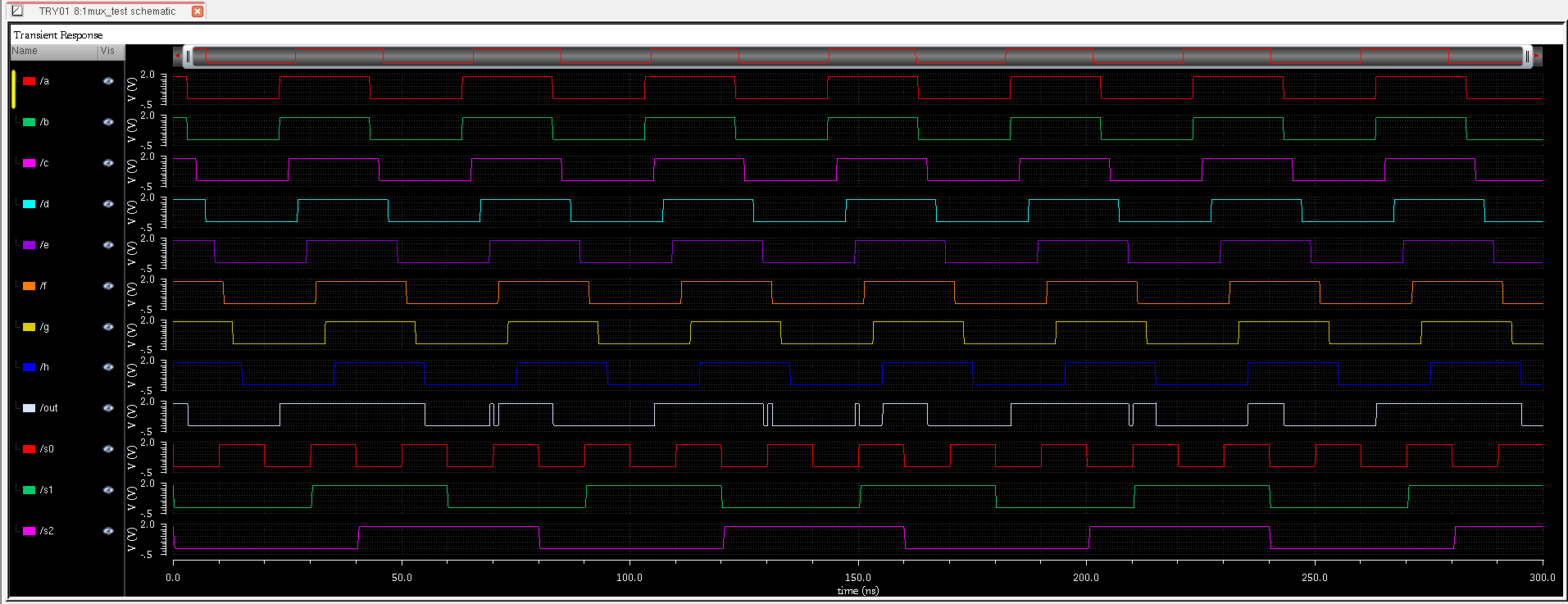


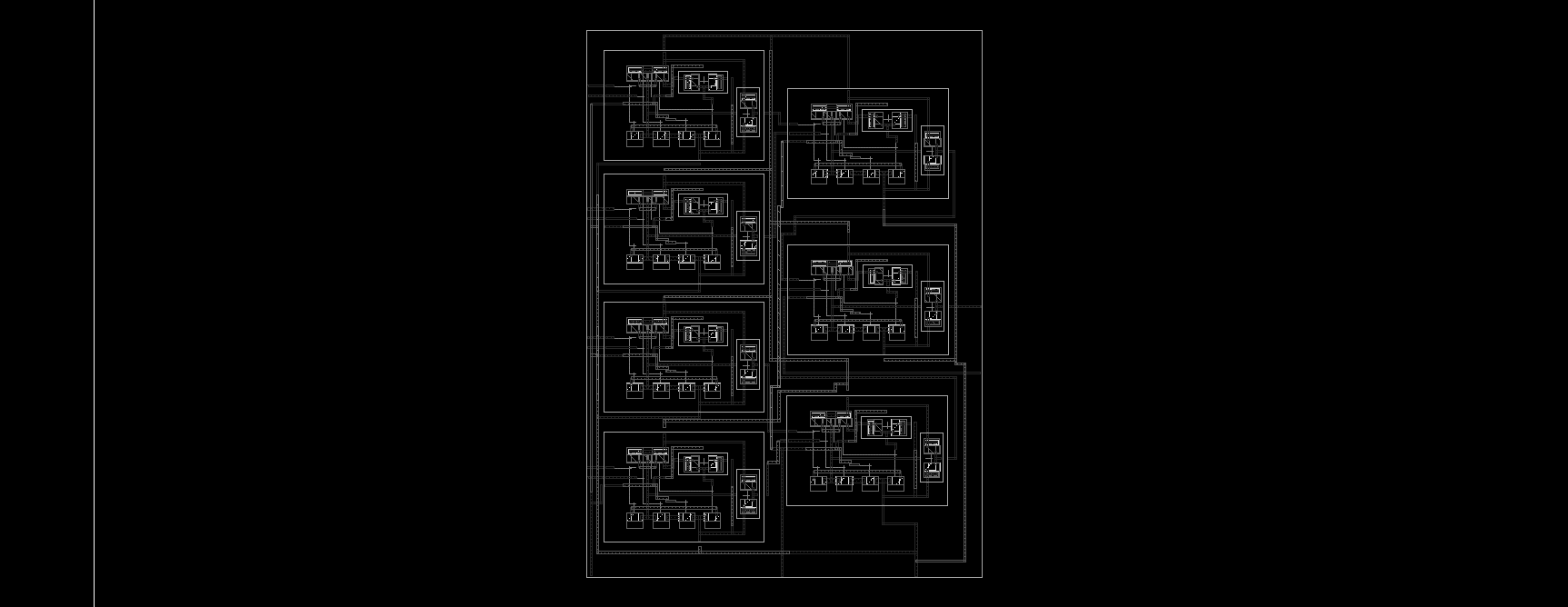
Area of the layout = 72.859 μm2

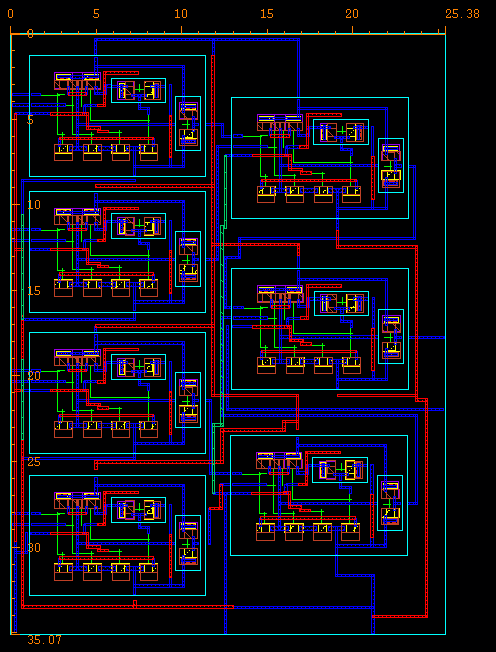
1. 8:1 MUX



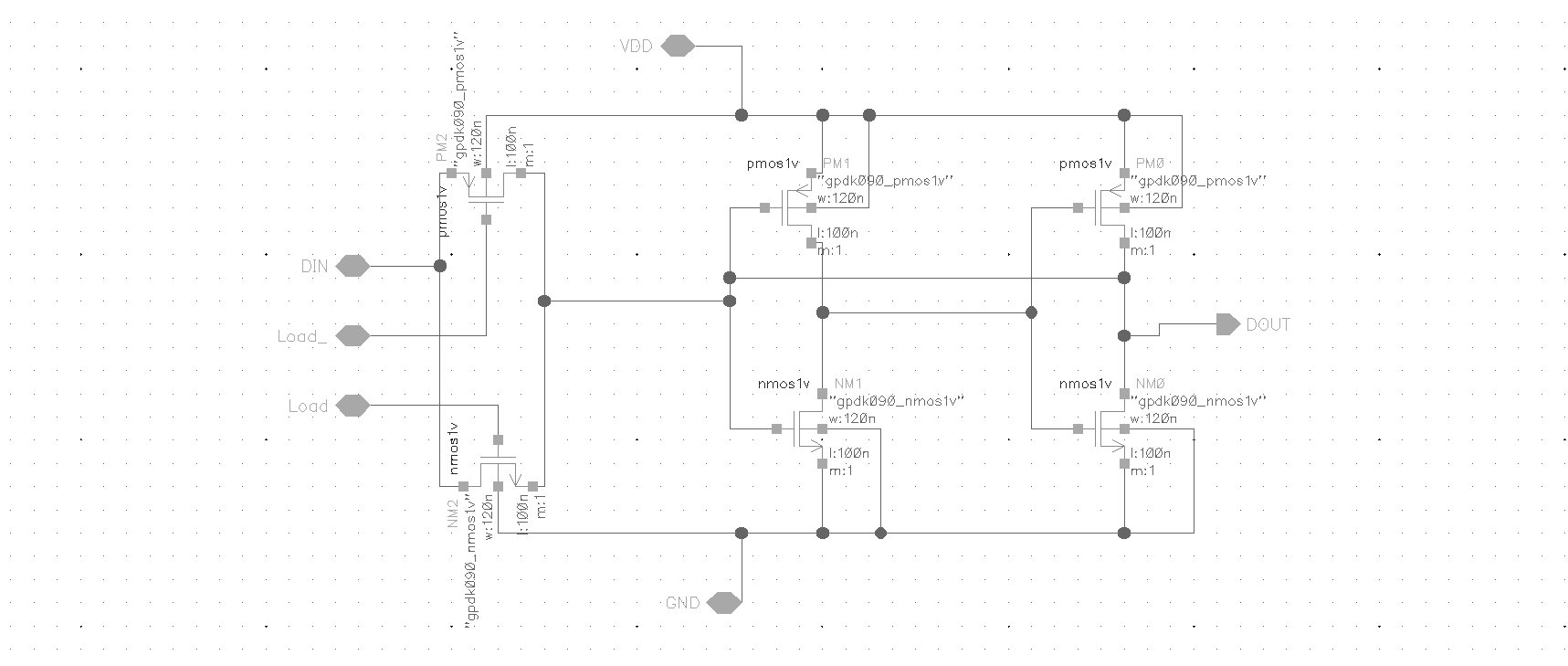


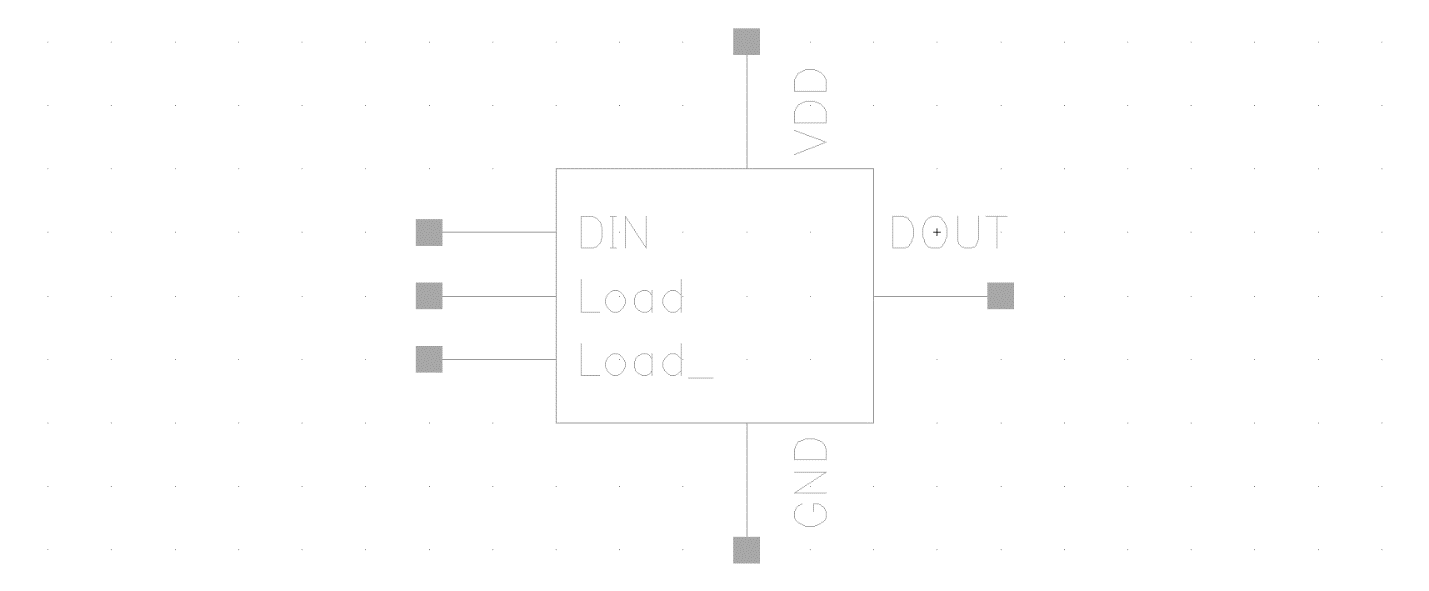


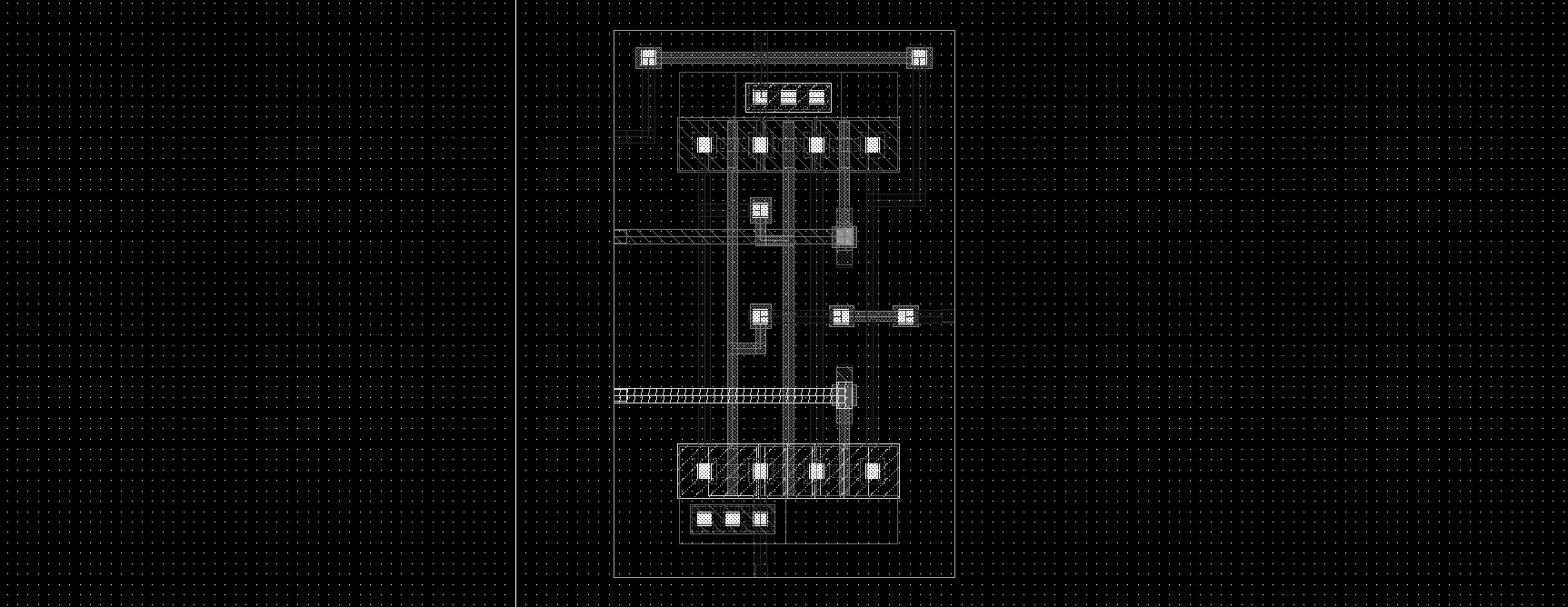


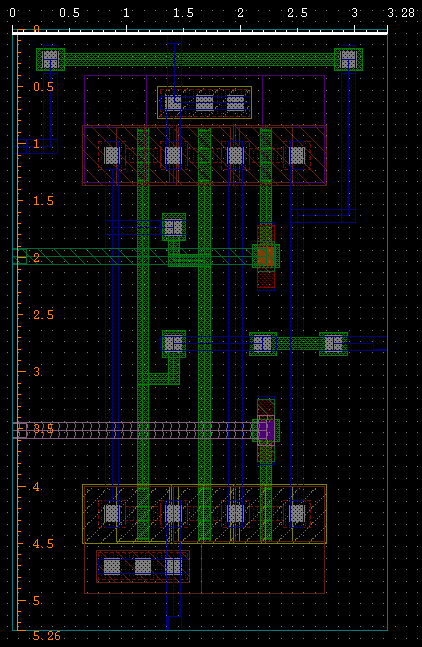
Area of the layout = 890.07 μm2

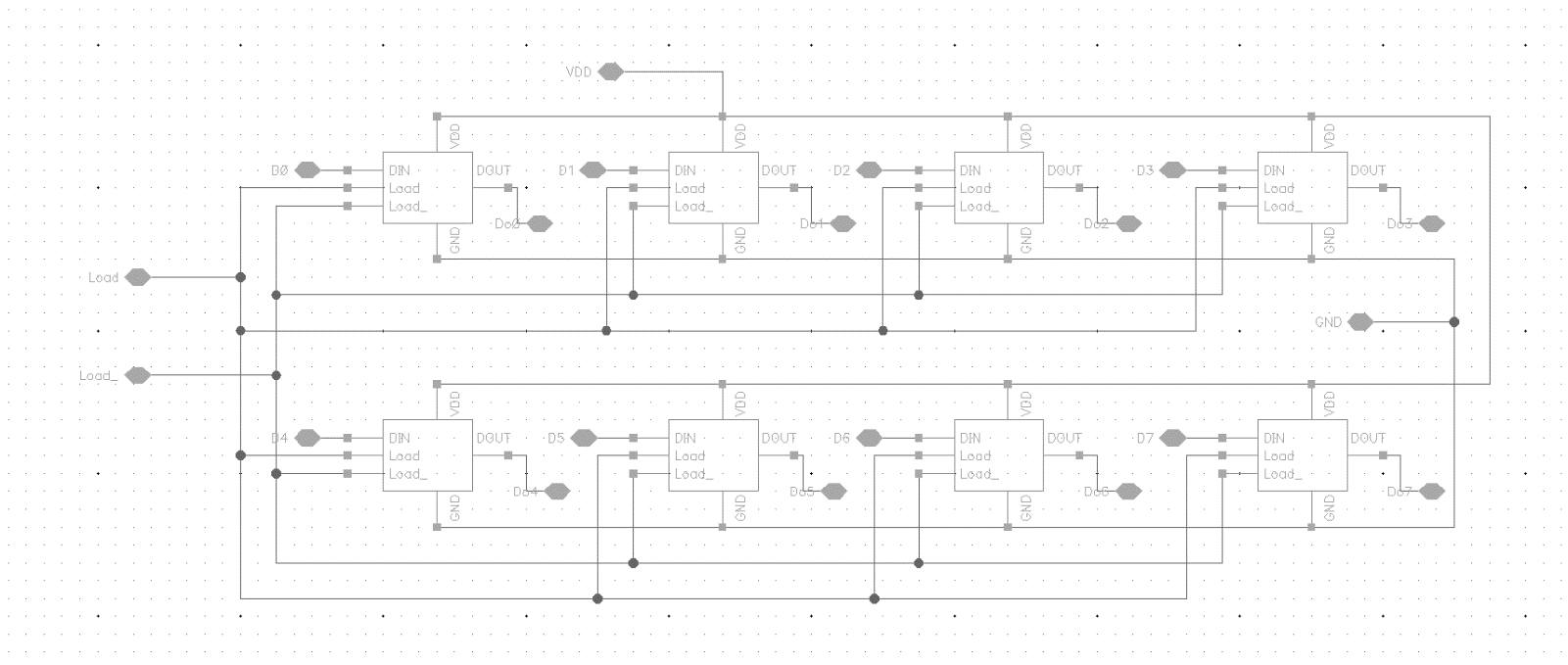
1. SRAM

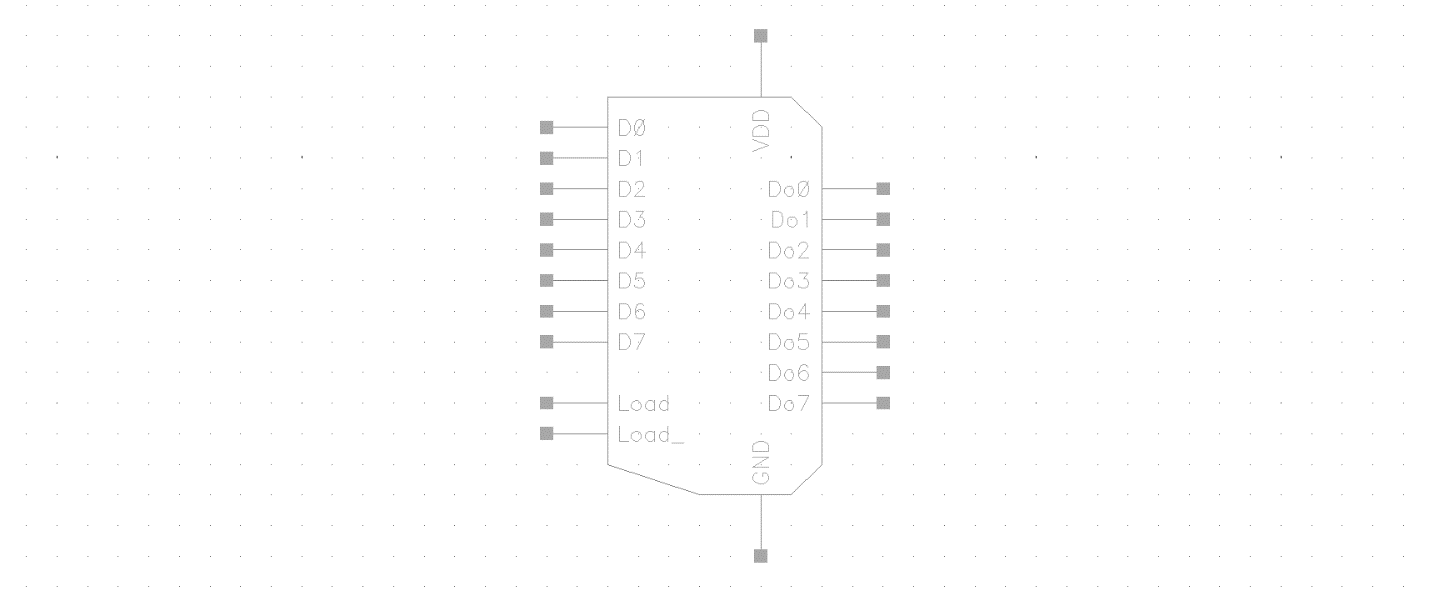


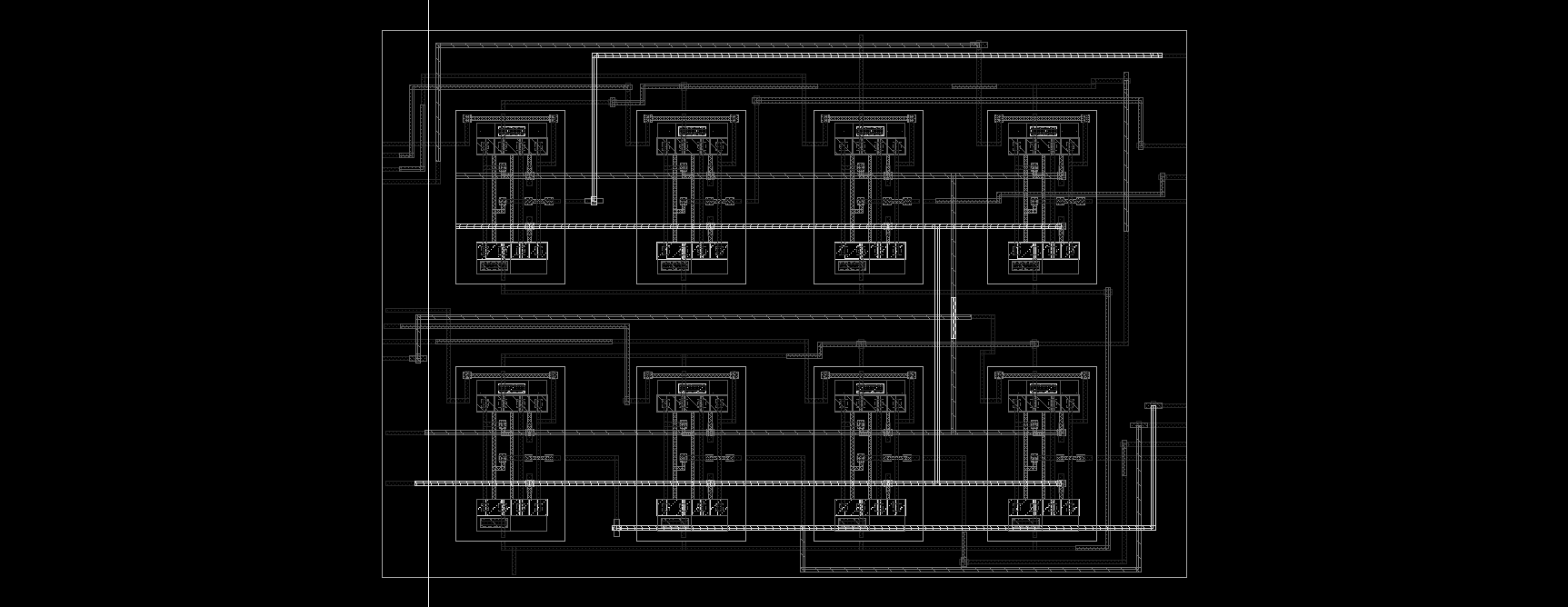


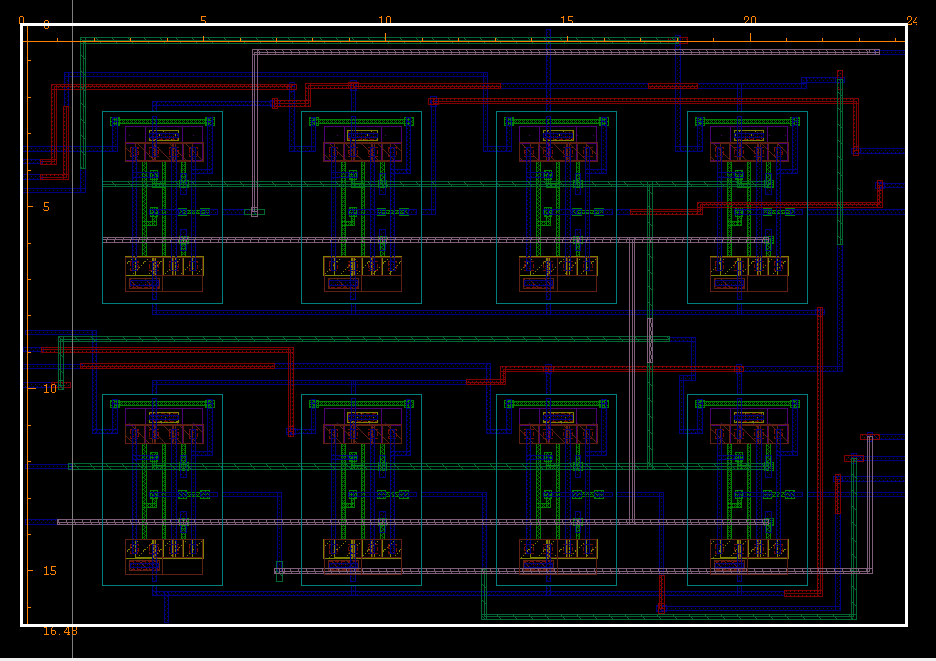


Area of the layout = 17.25 μm2

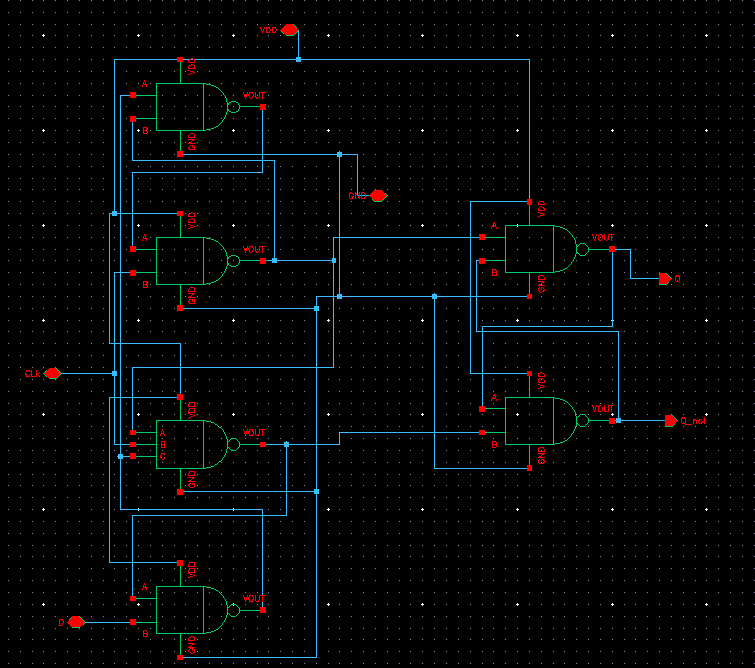
1. SRAM 8bit

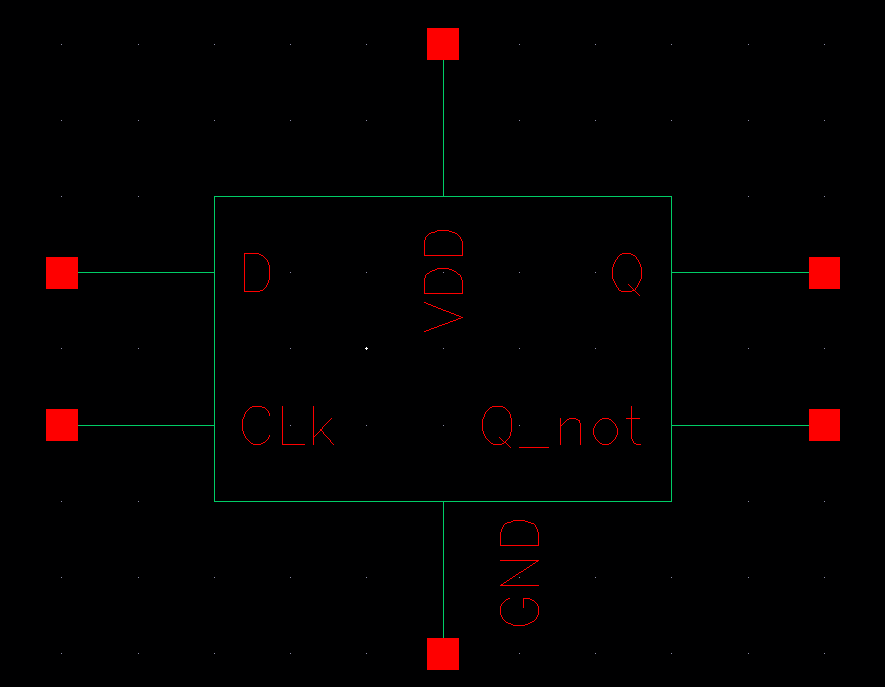


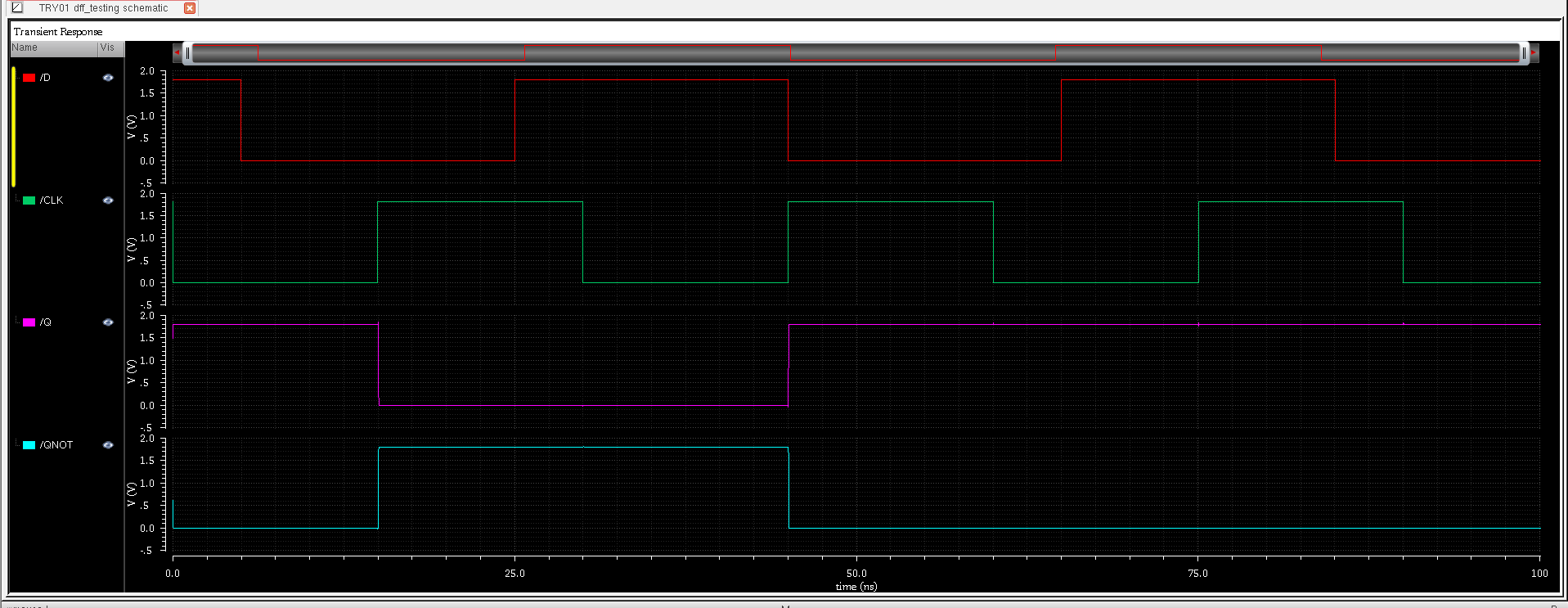


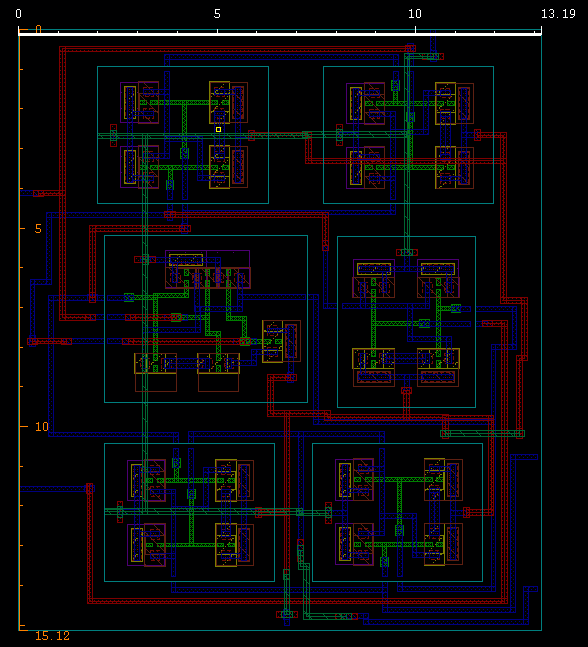
area of the layout = 395.52 μm2

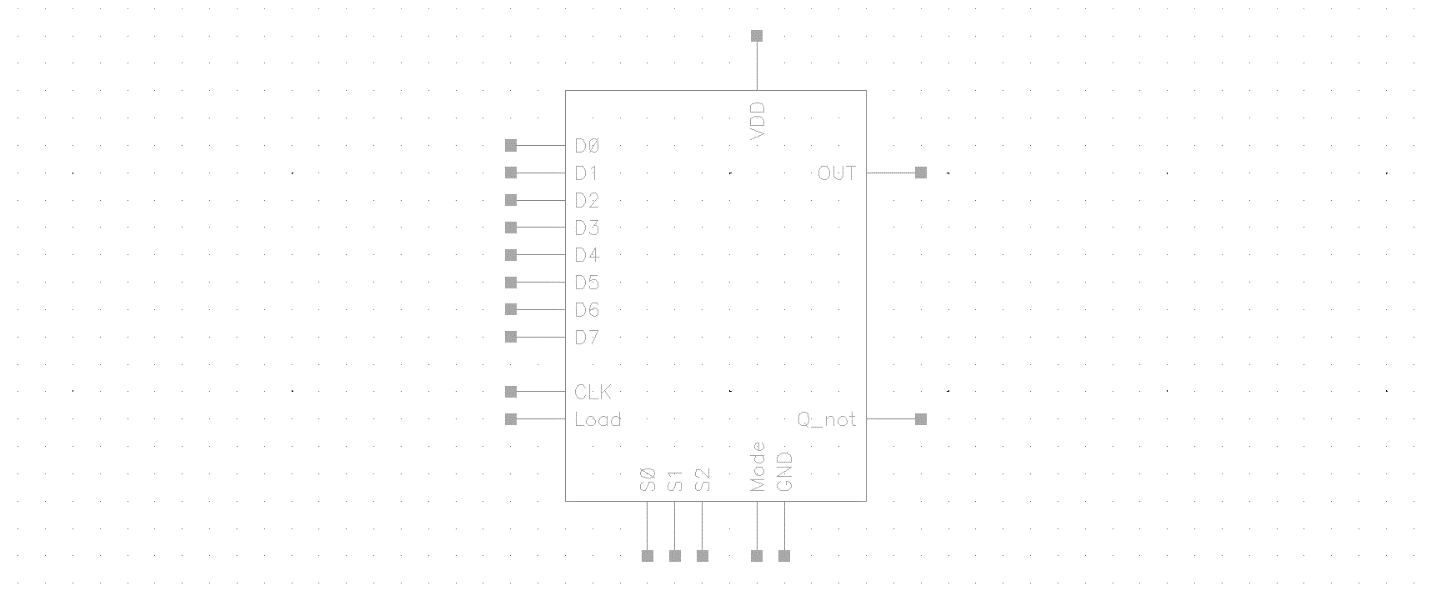
1. D positive edge flipflop

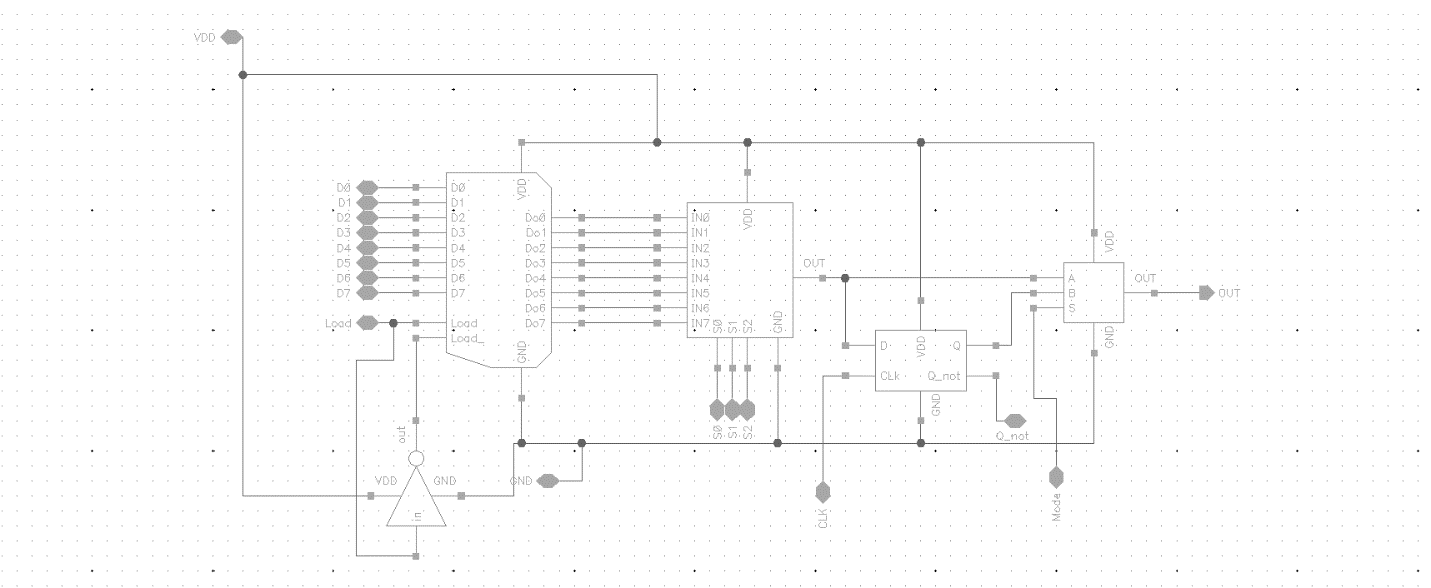


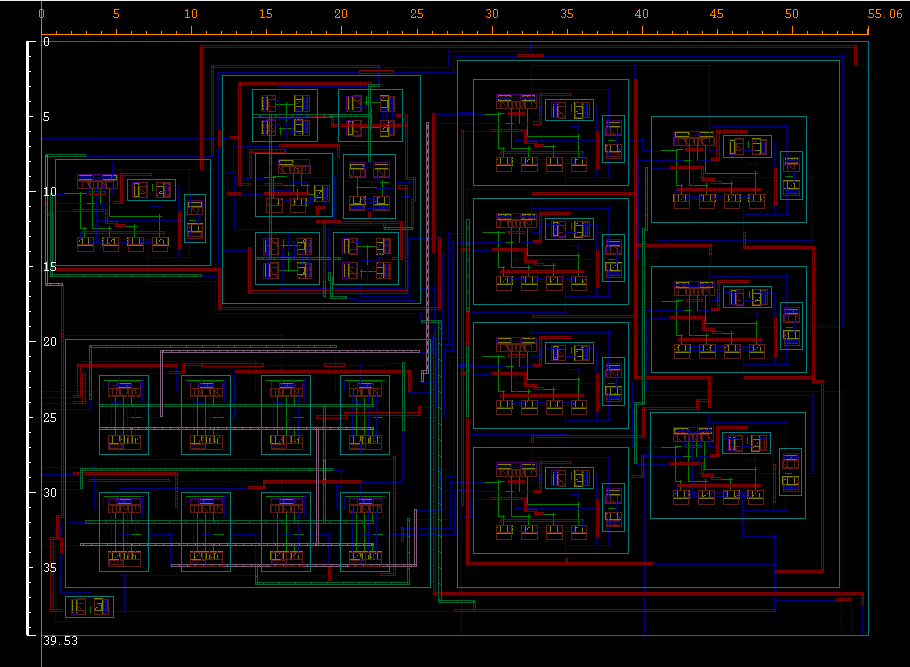




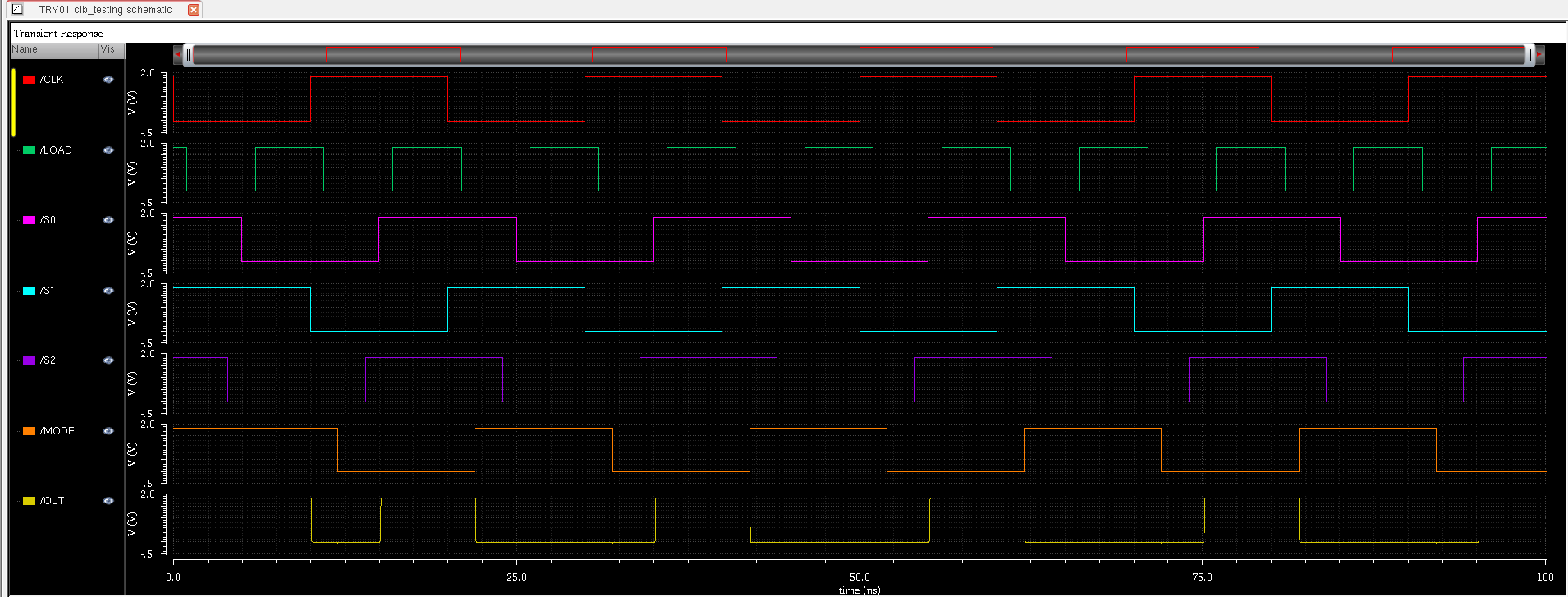
area of the layout = 200.2242 μm2

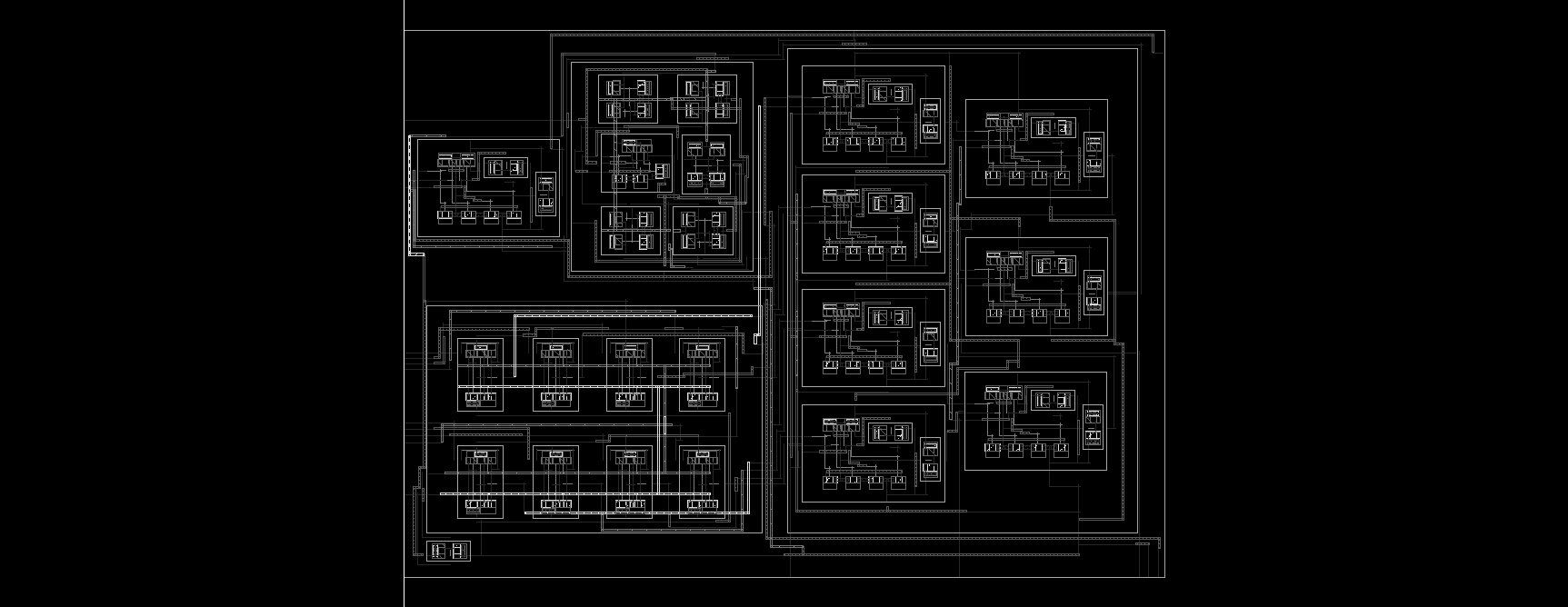
1. CLB

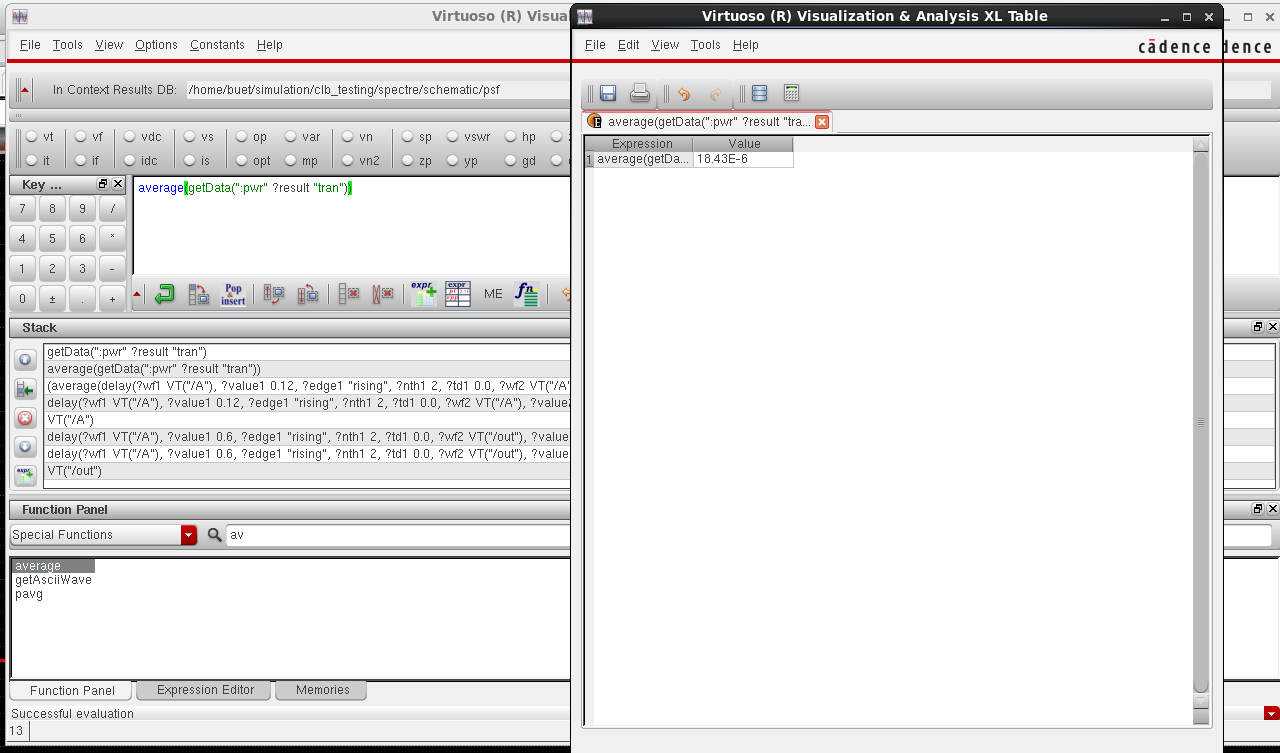




Area of the layout = 2176.52 μm2





Average power consumed by the CLB is 16.43 μW

Average energy Is 357.8x10-15 J

