

## A



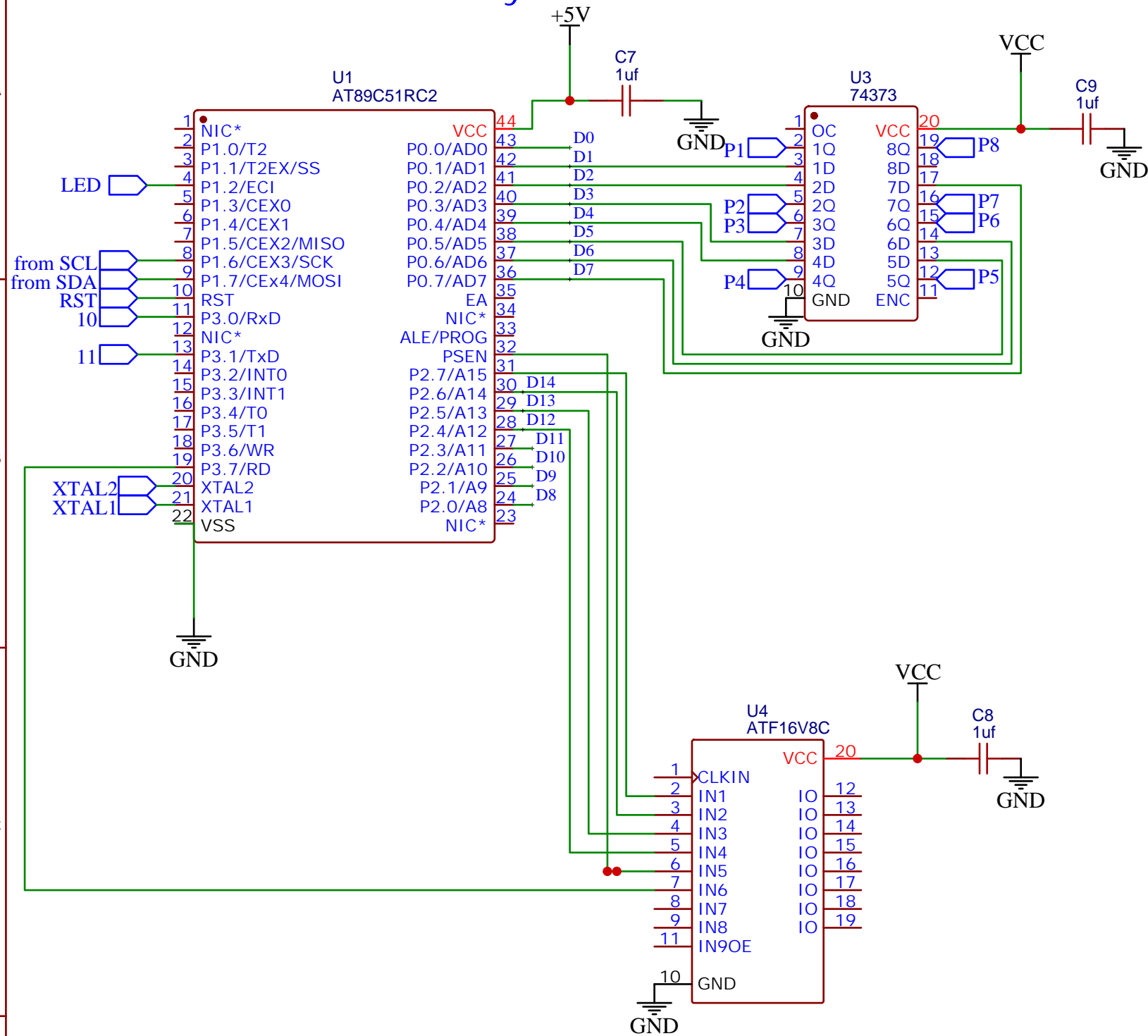
## B



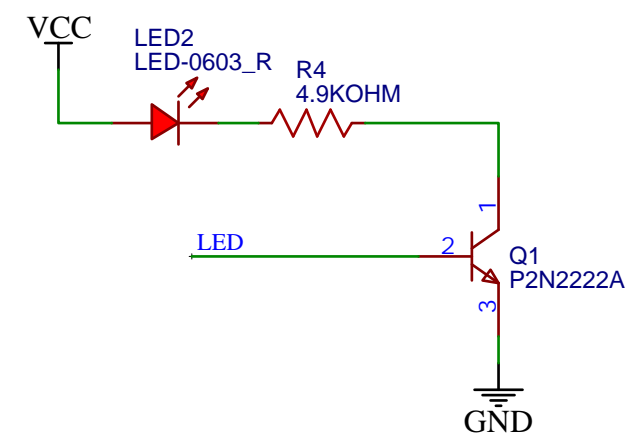
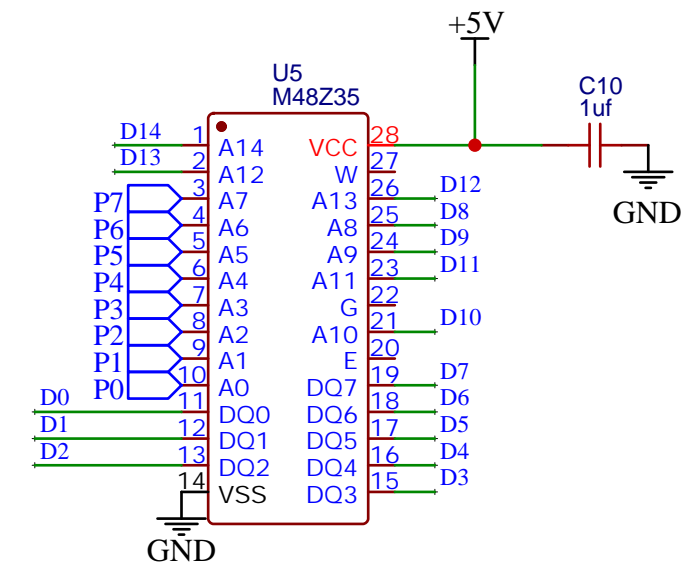
c

D

# 8051 Circuit with Memory Latch and SPLD IC

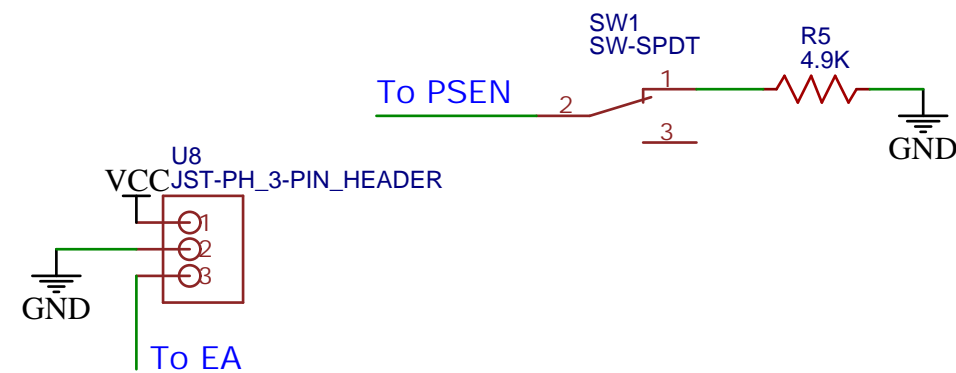
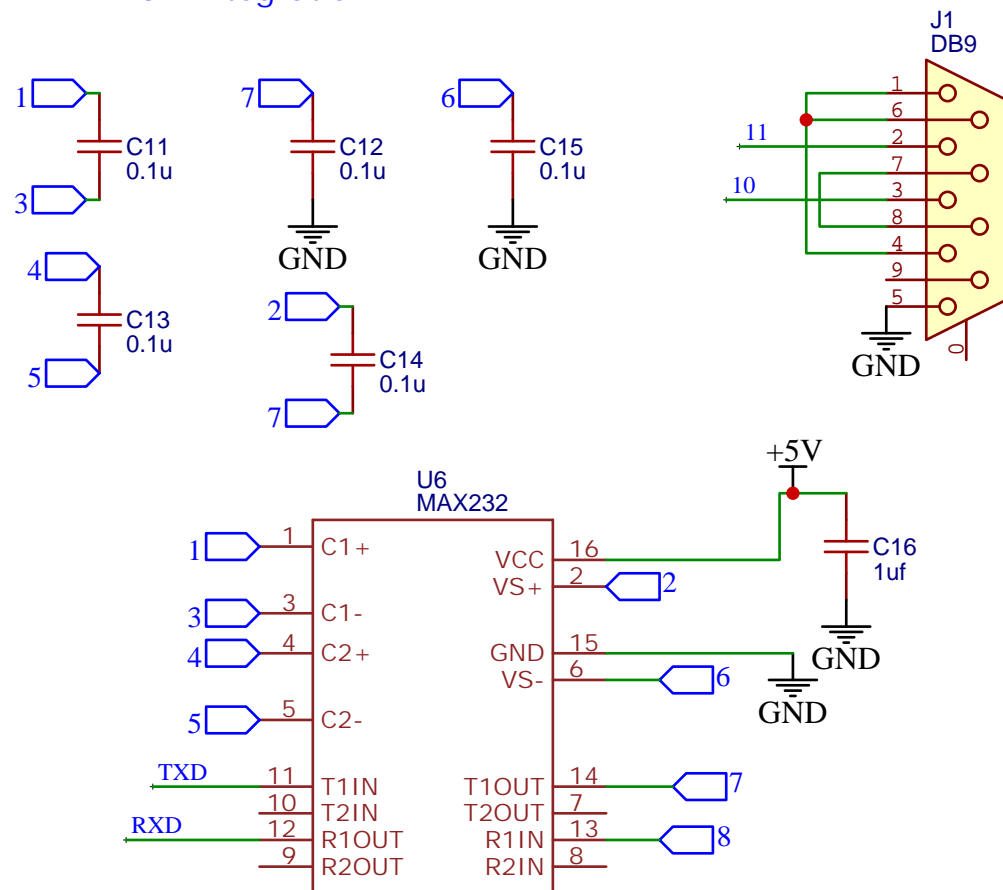


## NVRAM



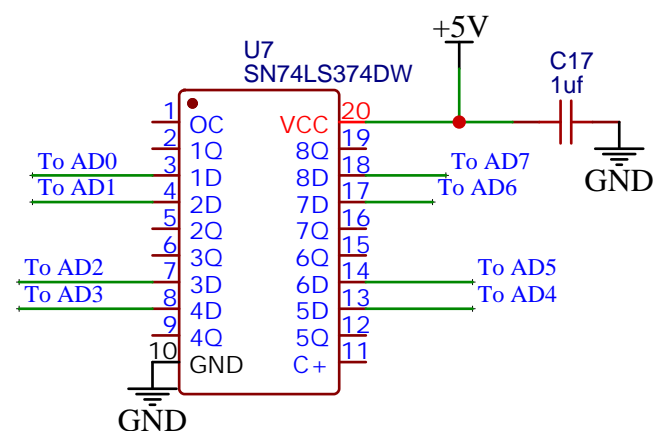
TITLE: ESD_LAB		REV: 1.0
Company: University of Colorado Boulder		Sheet: 1/1
Date: 2022-03-21		Drawn By: Swapnil Ghonge

## MAX-232 Integration

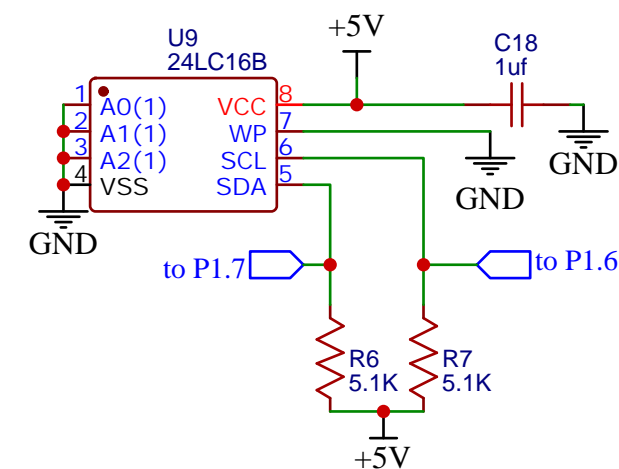


## BootLoader Circuit

## Interfacing LS374 with 8051



## I2C EEPROM Circuit



TITLE: ESD_LAB		REV: 1.0
Company: University of Colorado Boulder		Sheet: 1/1
Date: 2022-03-21		Drawn By: Swapnil Ghonge