Name: Swapnil Ghonge

Lab: ESD_LAB 2

Content: Report

Things learnt in Lab 2

Communication of microcontroller with RS-232

Learnt the interfacing for MAX-232 IC with 89C51RC2

Learnt the use of Logic analyzer with the NVRAM.

Learnt Detailed understanding of state and timing modes in Logic Port Software.

Learnt how to write interrupt program in assembly.

Learnt how to configure timer in interrupt mode..

Learnt how to use Flip software to program AT89C51RC2 using RS-232.

Toughest things to do:

Debugging the hardware for proper functioning

Interfacing LS374 with the 89C51RC2

ECEN 5613 | **Embedded System Design** | **Spring 2022**
Lab #2 Signoff Sheet

You will need to obtain the signature of your instructor or TA on the following items in order to receive credit for your lab assignment. Signatures are due by **Friday, February 11, 2022 (Part 1 Elements) and Friday, February 18, 2022 (Part 2 Elements)**.

Print your name below, sign the honor code pledge, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

Student Name: Swapnil Ghonge

Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

Student Signature: Swapnil

Signoff Checklist

Part 1 Required Elements

- ☑ Schematic of acceptable quality, correct memory map, SPLD .PLD file
- ☑ Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board
- ☑ NVRAM (as EPROM substitute), decode logic, and LED functional
- ☑ Understands device programmer.
- ☑ Demonstrated ability to use logic analyzer to capture bus cycles and view fetches from NVRAM. Shows detailed knowledge of both state and timing modes. Captures latched address lines A[15:0], data lines D[7:0], ALE, /PSEN, and NVRAM chip select signal on the logic analyzer display.
- ☑ Shows and discusses logic analyzer screen captures:
- ☑ Assembly program and timer ISR functional:

Moaaz MD 02/12/22
TA signature and date

Part 2 Required and Supplemental Elements

- ☑ AT89C51RC2, RS-232, and FLIP functional
- ☐ 74LS374 debug port functional
- ☐ Understands timing analysis, setup/hold/propagation
- ☑ ARM code build process, LED program, version control

P. Jahnavi 02/18/2022
TA signature and date

Instructor/TA Comments: ☐ ☐ ☐

FOR INSTRUCTOR USE ONLY **Part 1 Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☐	✓	☐	☐
Hardware physical implementation	☐	☐	☐	✓	☐	☐
Part 1 Required Elements functionality	☐	☐	☐	✓	☐	☐
Sign-off done without excessive retries		☐	☑			
Student understanding and skills	☐	☐	☐	✓	☐	☐
Overall Demo Quality (Part 1 Elements)	☐	☐	☐	✓	☐	☐

FOR INSTRUCTOR USE ONLY **Part 2 Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☐	✓	☐	☐
Hardware physical implementation	☐	☐	☐	✓	☐	☐
Part 2 Required Elements functionality	☐	☐	☐	✓	☐	☐
Supplemental Elements functionality	☐	☐	☐			
Sign-off done without excessive retries		☐	☐			
Student understanding and skills	☐	☐	☐	✓	☐	☐
Overall Demo Quality (Part 2 Elements)	☐	☐	☐	✓	☐	☐

NOTE: This signoff sheet should be the top/first sheet of your submission.

Lab2 Part1

(+) Assembly code functional
(+) Recommended part not implemented
(-) Wire wrapping wires are slack.
(+) Logic Analyzer demonstrated in state & Timing Mode to verify opcodes.

Lab 2 Part 1

Comments

[+] Neat schematic
[+] ARM board was completely functional
[+] Was comfortable with Flip.
[•] Would recommend completing supplemental.

22. **Part 2 Required Element**

Questions

Answer:1 I used Windows Operating System and Keil uVision5 Software to develop 8051 code development.

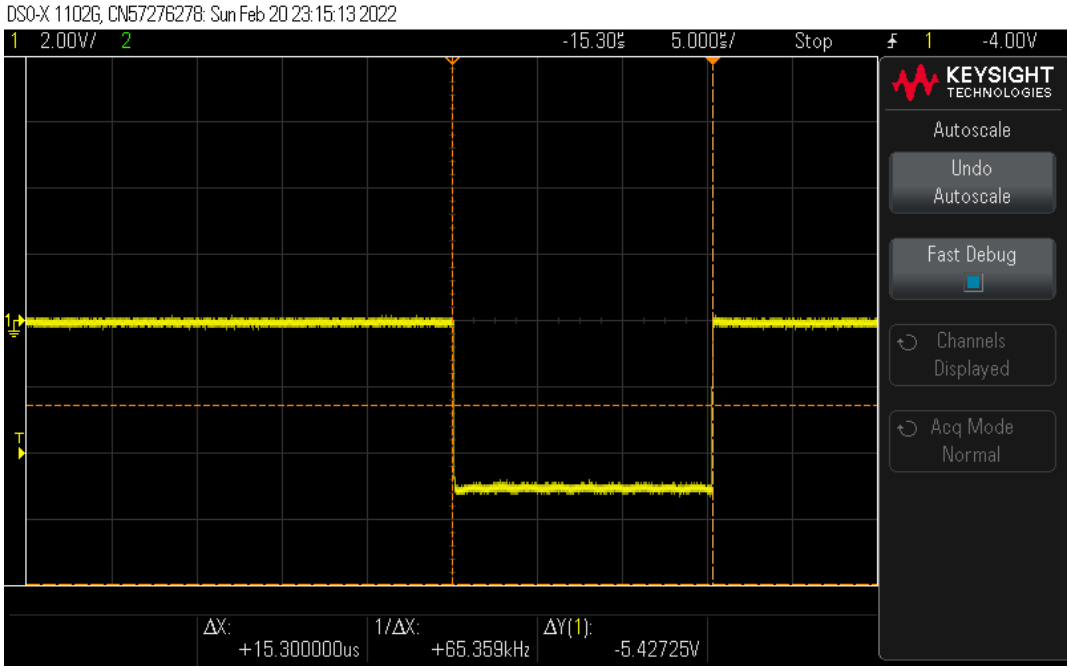
Answer:2 A51 macro Assembler.

Answer:3 I used Code Composer Studio Version 11.1.0

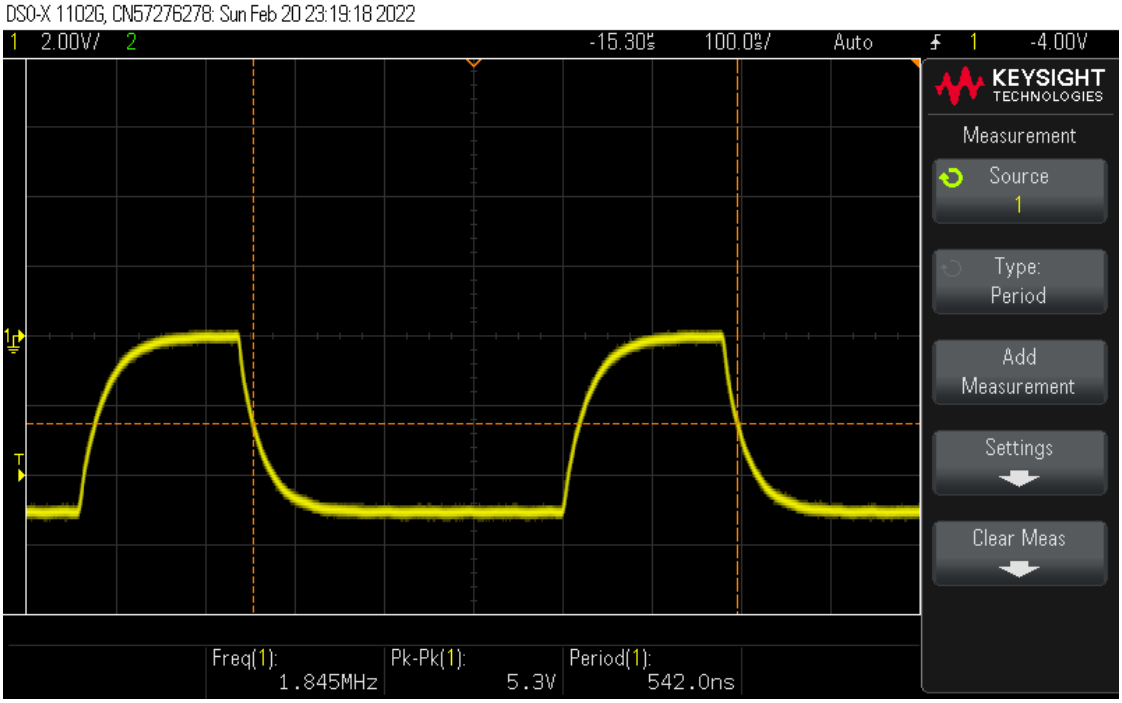
Answer: 4 I did install Logic port to view timing analysis of data and address and Flip terminal to program my AT89C51RC2 IC.

Answer:5 I did faced problems to configure the Logic port software and connection of the Logic Analyzer. The toughest part to execute was the configuring LS374 latch.

Answer: 6 I think the lab is appropriate to learn the basic stuff about RS-232 communication and memory latch.



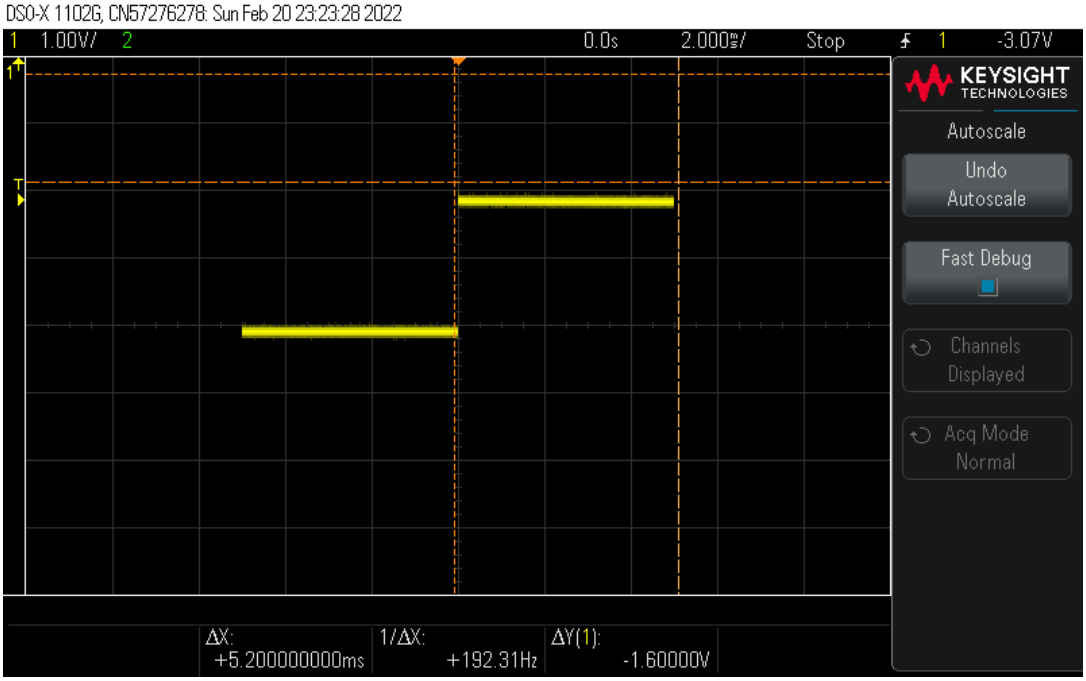
Time Period of the oscillation



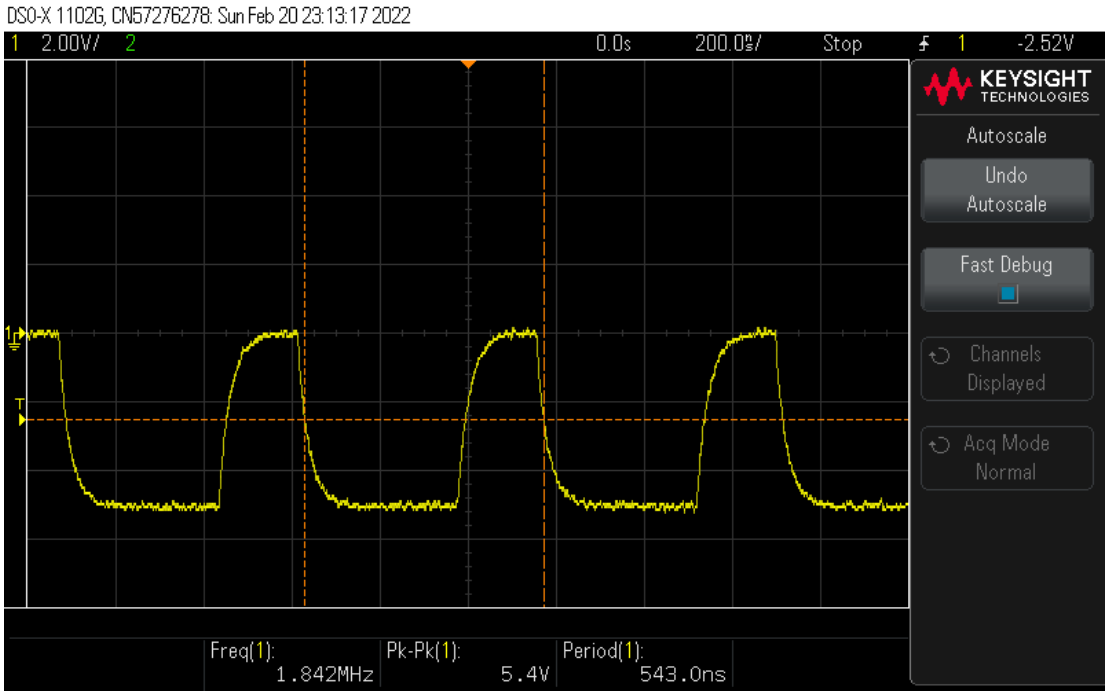
Frequency at ALE signal

ISR Routine Cycles

	Cycles	Short Interrupt	Long Interrupt
ORG 000BH	0	0	0
LJMP ISR_TIMER	1	1	1
CPL P1.2 ;	1	0	1
CJNE R1,#05H	2	2	2
CPL P1.1	1	0	1
MOV TL0,#00H	1	0	1
MOV TH0,#00H	1	0	1
MOV TCON,#10H	1	1	1
MOV R1,#00H	1	1	1
SJMP ENDLOOP	1	1	1
CPL P1.2	1	0	1
RETI	2	2	2
	Total Cycles	8	13
	Oscillation Cycles	96	156
	Execuetion Time(uS)	8.68	14.14

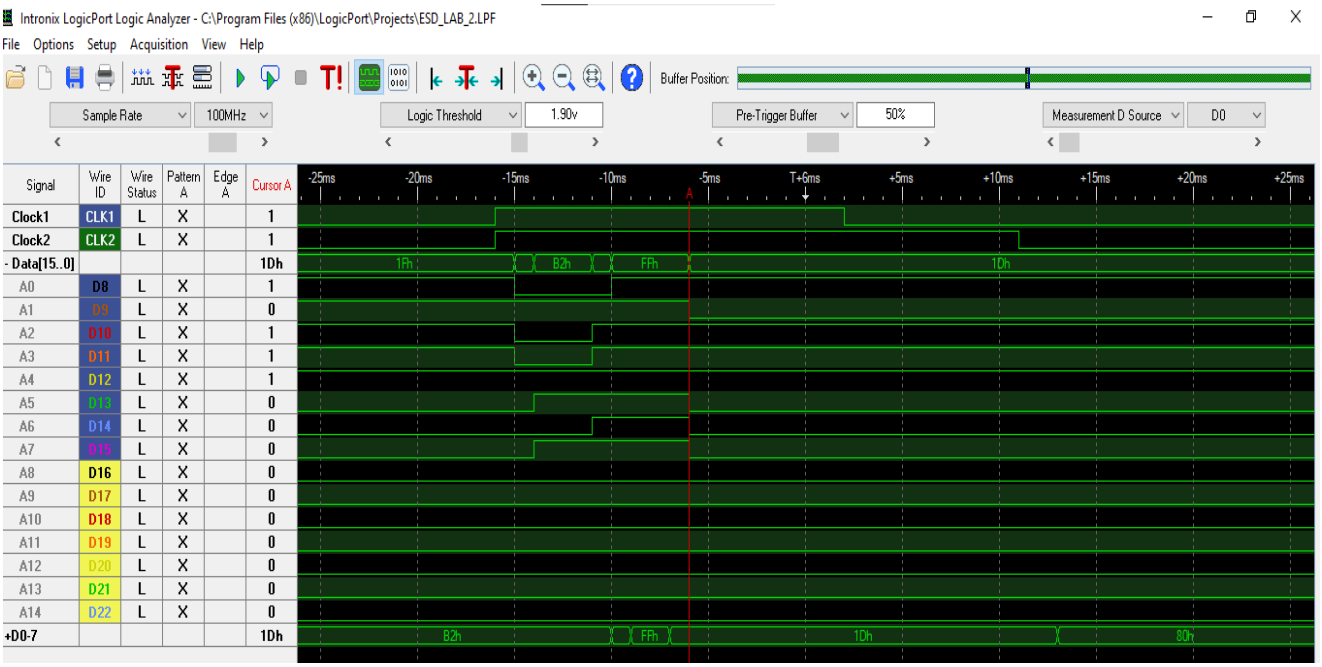


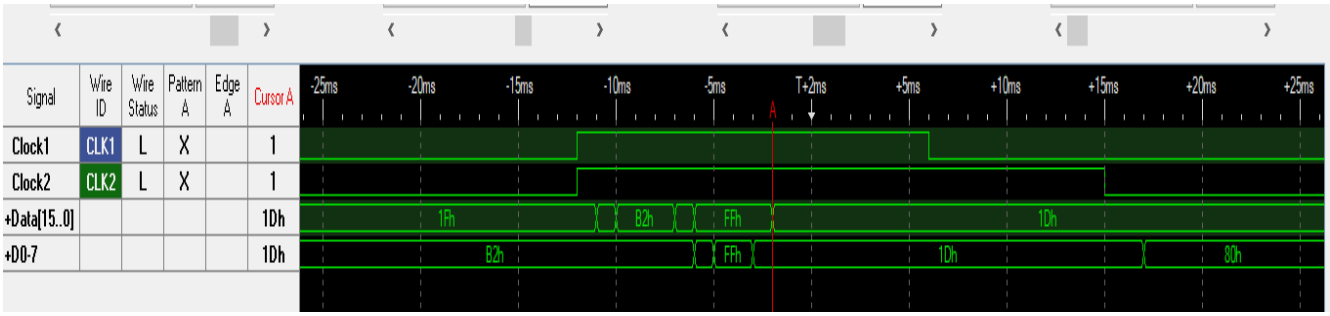
Voltage level at P1.1 of AT89C51RC2



Signal at EA of 89C51RC2

Timing Measurements on Logic Analyzer





Relative to Reference	Clock1	Clock2	Data[15..0]	D0-7
-91ms	0	0	001Eh	1Eh
-90ms	0	0	001Eh	FEh
-64ms	1	1	001Eh	FEh
-63ms	1	1	00FEh	FEh
-59ms	1	1	00FFh	FEh
-58ms	1	1	00FFh	FFh
-55ms	1	1	00FFh	1Fh
-54ms	1	1	001Fh	1Fh
-46ms	0	1	001Fh	1Fh
-37ms	0	0	001Fh	1Fh
-36ms	0	0	001Fh	B2h
-10ms	1	1	001Fh	B2h
-9ms	1	1	0012h	B2h
-8ms	1	1	00B2h	B2h
-5ms	1	1	00FEh	B2h
-4ms	1	1	00FFh	F2h
-3ms	1	1	00FFh	FFh
-1ms	1	1	00FFh	1Dh
T+0ms	1	1	001Dh	1Dh
+8ms	0	1	001Dh	1Dh
+17ms	0	0	001Dh	1Dh
+19ms	0	0	001Dh	80h
+45ms	1	1	001Dh	80h
+46ms	1	1	0080h	80h
+48ms	1	1	00A0h	80h

Time Analysis of Logic Analyzer

Clock1: ALE

Clock2: PSEN

Screenshots of MSP432 Code

Toggling of LED's and with Switch

Green LED during pop-up

Blue light is hold when switch is pressed.